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Design and Reliability Simulation of VLSI Computing Circuits

by

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Abstract

Design of very large-scale integration (VLSI) computing circuits require good means to assess circuit reliability in order to utilize the full potential of advanced submicron fabrication technologies. An integrated circuit may fail due to the degradation of some critical transistors or interconnection wires. This dissertation presents the integration of reliability modeling into the developed circuit simulator, RELY, which can predict circuit performance degradation due to progressive physical failure mechanisms. Modeling requirements and implementation of hot-carrier effects and electromigration including transistor modeling, stress monitors and degradation models for reliability simulation are addressed. Two simulation schemes for circuit reliability analysis are presented. Quick identification of weakest devices within a circuit can be achieved by the one-cycle simulation scheme. The repetitive simulation scheme provides the information on the impact of the progressive device degradation on circuit performance to account for the gradually changing stress condition in actual circuit operation. A systematic approach to include the first-order AC degradation effects in the quasi-static simulation is also described. Strategies for use in a hierarchical reliability simulation environment covering various levels of VLSI circuit design are presented. The degradation information is propagated through the design hierarchy starting from the circuit-cell level, the circuit-block level to the complete chip level. Reliability simulation using the RELY program can not only predict the degraded performance of the whole circuit, but also identify the most critical devices for improvement. Circuit topology changes can be applied to achieve high failure-tolerance in the computing circuits. Design examples of computing circuits and the associated performance degradation are presented. Example circuits including inverters, NAND gates, memory circuits, operational amplifiers and data converters have been studied using the industrial 0.8 μm and 0.5 μm CMOS technologies. By using these techniques on the design of CMOS

components, high-speed circuits can be achieved with excellent long-term long-term reliability. By adding a common-gate buffering transistor in the critical output stage of an operational amplifier, circuit lifetime is found to be improved by more than four times.

Chapter 1

Introduction

With the advent of high-performance communication networking and computer technologies, we are reaching an era of universal communications where everyone has an easy and immediate access to widely distributed information sources in multi-media including text, image, and audio. An integrated information processing system is bridged with the real world through audio and video channels. In order to support advanced integrated information system, very high speed signal processing techniques are needed. For example, in modern multimedia teleconferencing and high definition television (HDTV) applications, the required video signal processing speed has been above one billion pixel operations per second. In 1993, systems with a processing power at 100-giga operations-per-second for large-scale problems in real-time information processing are expected to emerge and the development of tera operations-per-second systems is anticipated in 1996 [1.1].

Several approaches can be applied to enhance the computational capabilities in high-speed information processing. One approach is to utilize the computational powers of computers and new developments in various fields of computer science and engineering, such as signal processing, mathematical and scientific algorithms, and graph theory. Another approach is to mimic the computations performed in the human brain, i.e. the artificial neural network fuzzy system approach. Tremendous computational power and new data routing architectures are needed in both cases. Very large scale integration (VLSI) technology can be

used to implement algorithm-specific multiprocessor chips to fully exploit the inherent computational powers of various information processing architectures. In the microprocessor domain, continuous progress on reduced instruction set computers (RISC) enables the introduction of the powerful Intel-i860 chip [1.2], and the scalable processor architecture (SPARC) chip [1.3] with the processing speed exceeding 30 million-instruction-per-second (MIPS).

Requirements in the electronic system applications have demanded the continuous reduction of device feature sizes in VLSI technologies as well as high-density packaging. CMOS technologies play a major role because of their low power dissipation, ease of scalability in the design, and high production yield. While submicron devices such as 4Mb static random access memory (SRAM) and 16Mb dynamic random access memory (DRAM) are already available, 64Mb DRAM using deep sub-micron devices are being actively developed [1.4]. The feature size has been shrunk from under 2 μm in mid-1980s to around 0.35 μm in 1991. New multi-chip module packaging techniques will give system designers a less restrictive design environment that can relax the constraint on printed-circuit board space. Innovative circuit design techniques are also mandated by high-speed information processing. Oversampling analog-to-digital data converters based on sigma-delta modulation at a sampling rate above 1.5 MHz [1.5] has been well developed for the applications of high-precision signal acquisition in voiceband communication and digital audio processing.

The development of high performance electronic computer systems has greatly increased the computing power. The functional complexity and long-term reliability of integrated circuits needed to construct such systems will continue to

increase. Although fault recovery and repair schemes are available to tolerate module failures in complex electronic systems, at some failure rate the systems will be incapable of complete recovery [1.6]. For consumer electronics such as digital watches and personal computers, a device malfunction can be remedied by simply replacing the faulty modules. For the real-time electronic system applications that require continuous and uninterrupted operation such as on-line transaction-processing and telephone exchanges, loss of function is often very costly. For system operation involving personnel safety such as flight control or electronic pacemakers in medical applications, loss of normal operation can be catastrophic. High-quality electronic system must be made of highly reliable integrated circuits. VLSI circuit reliability simulation techniques can be used in the hardware design flow to guarantee the overall circuit lifetime [1.7]-[1.10].

Integrated-circuit reliability studies were focused on the device-level in the past. Methodologies to assess circuit-level reliability need to be established. This dissertation addresses the modeling requirements and reliability simulation techniques to evaluate VLSI circuit long-term performance. An efficient approach to couple the device-level reliability studies and circuit-level reliability assessment has been developed. Chapter 2 presents an overview of the important issues on VLSI reliability for computing circuits and the needs to achieve high-accuracy circuit-level reliability assessment. Chapter 3 discusses the modeling and parameter extraction of hot-carrier effects and electromigration for reliability simulation. The computer models are used to predict the circuit reliability performance. Chapter 4 presents the methodology and algorithm developed for circuit-level reliability simulation. By using one-cycle and repetitive reliability

simulation schemes, circuit designers can not only identify the devices which have the most critical impact on the circuit, but also predict the amount of degraded circuit performance. Chapter 5 describes the detailed design flow of using the developed circuit reliability simulator, RELY [1.9], and presents measurement and reliability simulation results of several digital and analog circuits for VLSI computing circuits. Finally, Chapter 6 draws conclusions and suggestions for future studies.

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Chapter 2

Highly Reliable VLSI Circuits

To achieve high performance and high reliability for real-time signal and data processing applications, various reliability issues are reviewed is this chapter. Recent advances in VLSI technologies are described first. An overview of the key VLSI reliability concerns are summarized. The need for circuit-level reliability assessment is then discussed.

2.1 Microelectronic Technologies

Submicron CMOS technologies make possible the implementation of a whole signal processing subsystem on a single chip. As multiple millions of devices are integrated on a single die, the device feature size for the memory chips is around 0.4 μm and for the processor chips is around 0.75 μm [2.1, 2.2]. The expected device feature size for the next-generation technologies will be as small as 0.15 μm [2.3]. At present, complex microelectronic chips such as as 64-megabit DRAMs have started to appear for scientific and commercial applications [2.4]. The level of integration is expected to continue to increase up to more than one hundred million transistors per chip for ultra large-scale integrated (ULSI) circuits by 1995. A digital neural execution engine with 11 million-transistor has been developed [2.5]. In addition to high integration, speed performance of the memory chips has been pushed to be faster than 35 ns for 64-Mb DRAMs [2.4] while a data processor with a clocking speed of 100 MHz has also been introduced [2.6]. In the recent design of massively parallel signal

processors, floating-gate devices are used for long-term storage of analog values in artificial neural circuits [2.7] and offset canceling in precision amplifiers [2.8]. With the regularity and modularity in most of the multiprocessor architectures, Wafer Scale Integration (WSI) techniques have been proposed to increase the integration level [2.9].

2.2 CMOS Reliability Study

Device scaling is crucial to increase circuit packaging density, reduce power dissipation, and increase hardware performance. Scaling of device and circuit dimensions has both physical and fabrication barriers imposed by heat dissipation issue, lithographic techniques, etc. For the constant voltage scaling approach in CMOS design, the surface and vertical dimensions including channel width, channel length and oxide thickness are scaled by the same factor (1/S) with $S > 1$. Notice that drain current, power consumption, electric field are increased by S. Since gate oxide capacitance decreases by S, propagation delay per logic gate becomes $1/S^2$ and power-delay product becomes 1/S of their original values.

To retain large noise margin and compatibility in system-level design, the 5-V power supply for integrated circuits are still widely used. As a result, oxide breakdown, drain diffusion-region junction breakdown as well as punchthrough phenomena caused by high electric field pose the fundamental barriers on device scaling. Despite that a lower power supply value has been under intensive investigation [2.10], the high electric field and current density within small-geometry devices will continue to pose a major challenge to the scaling-down of device feature size. While process screening can eliminate infant mortality,

progressive degradation due to high electric field and current density can limit the effective circuit operation lifetime.

A maximum failure rate of 100 FITs (failures per 10^9 operating hours) was set as one of the key program goals by Semiconductor Research Corporation (SRC) in Research Triangle, North Carolina for 1990. At such a failure, the expected lifetime of a device is ten million hours, or 1200 years. However, a machine made of one hundred similar devices would likely to fail in an application life of 12 years only. In the revised goal set for the year 1994, a failure rate of 10 FITs has been selected.

Several microelectronic degradation mechanisms become very profound because of the extremely high electrical stress on small-geometry transistors. Figure 2.1 shows the impact of scaling to a popular bathtub curve with associated reliability concerns [2.11]. These key failure mechanisms include [2.11]-[2.22]:

. hot-carrier damage,

. electromigration,

. time-dependent dielectric breakdown (TDDB),

. electro-static discharge (ESD),

. packaging damage,

. radiation damage, and

. contamination of oxides and junctions.

These degradation mechanisms pose threats to the reliability of electronic and optoelectronic integrated circuits.

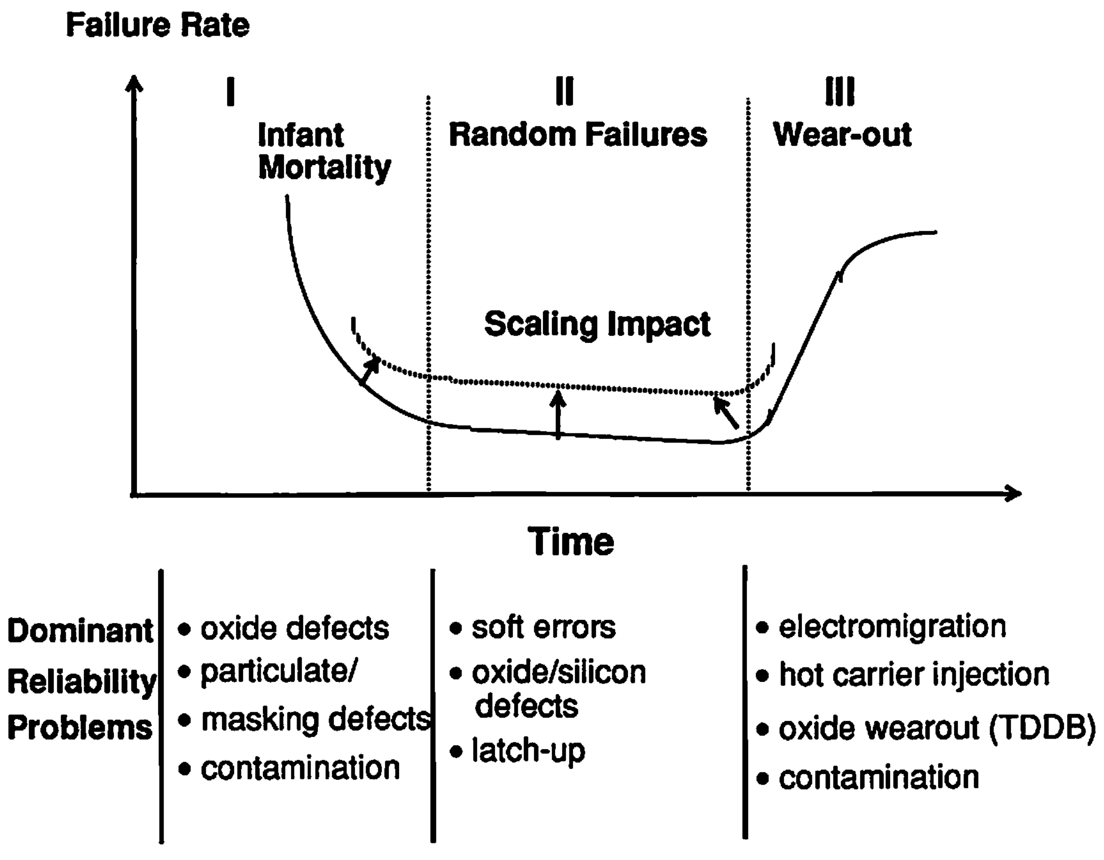

Fig. 2.1 The reliability failure rate bathtub curve and the impact of feature size scaling [2.11]

2.2.1 Hot-Carrier Damage

Hot-carrier damage occurs in MOS transistors with effective channel lengths in the range of 2 μm or less as a result of the high electric field gradient near the drain electrode. The origin of hot-carrier effects is a process involving hot-carrier generation near the drain diffusion area, injection and trapping of these high-energy carriers in the gate oxide. Some of the carriers traversing the channel acquire enough energy from the electric field to cause impact ionization which generates electron-hole pairs. Hot electrons trapped in the gate oxide of an N-channel transistor will cause the threshold voltage to increase, and transconductance to decrease in proportional to the amount of trapped charge. Over the past decade, several research efforts were concentrated on the device-level hot-carrier damage [2.12]-[2.16]. Various enhanced device structures have also been proposed to reduce hot-carrier induced damages from drain engineering techniques [2.22]. However, as device dimensions continue to reduce in the sub-micron era, the existing hot-carrier-resistant structures exhibit non-negligible degradation in the electrical characteristics.

2.2.2 Electromigration

Electromigration is a chip-life limiting mechanism that is of primary concern to designers of microelectronic circuits in all technologies in current use. It is a process of electron wind-assisted atom diffusion along the metal grain boundaries in the direction of electron flow in the conductor. In some early work, an empirical model of electromigration mean time to failure (MTTF) was developed [2.19],

$$\mathrm{MTTF} = \alpha \cdot J_{eff}^{-n} \cdot \exp(E_a/kT) \, . \tag{2.1}$$

Here, α is the pre-exponential constant, J_{eff} is the effective current density in the metal conductor, n is a current density dependent parameter, E_a is the activation energy of electromigration, T is the temperature in degree Kelvin, and k is the Boltzmann's constant. As finer metal interconnects are required to scale down the overall chip area, electromigration will remain a major factor in the design of reliable integrated-circuits.

2.2.3 Time-Dependent Dielectric Breakdown (TDDB)

Time-dependent dielectric breakdown is a process in which the thin insulator between two conductors spontaneously fails to insulate after being exposed to a strong electric field for some period of time. A semi-empirical expression has been derived [2.20],

$$\mathrm{MTTF}_{TDDB} = \alpha_{TDDB} \cdot \exp\left[E_a/k \, (1/T - 1/T_0) \right] \cdot \exp\left[A_f \cdot (1/E - 1/E_0) \right] . \tag{2.2}$$

Here, α_{TDDB} is the pre-exponential constant, T is elevated test temperature, T_0 is the normal circuit operating temperature, E_a is the activation energy, k is the Boltzmann's constant, A_f is the field acceleration factor, E is the stress field, and E_0 is the operating field.

2.2.4 Electro-Static Discharge (ESD)

ESD-induced damages to integrated circuits are due to direct transfer of electronic charges. Various failure mechanisms associated with it include dielectric breakdown, junction breakdown, and metallization damages due to high instantaneous power density. Two circuit models are generally used in the study of ESD phenomenon: the Human Body Model and the Charged Device Model [2.22]. Design issues in the prevention of ESD damages lie in the protection circuits and the judicial choice of design rules used in computer-aided design tools, especially for the input/output pads of an chip.

2.3 Importance of Circuit-Level Reliability Assessment

Efforts to improve integrated-circuit reliability have been concentrated on the device level including further understanding and modeling of the failure mechanisms [2.12]-[2.20], design of innovative test structures to improve reliability control [2.24], and design of degradation-resistant device structures [2.21, 2.25]. The impact of device degradation to the circuit performance in application-specific integrated circuits needs careful investigation. Circuit reliability performance becomes a critical design factor in the design flow instead of a simple accept/reject criterion for assessing integrated circuit quality in the production line.

Several approaches may be utilized to ensure integrated circuit reliability. The conventional screening approach is to eliminate infant mortality failures of the fabricated parts by burn-in tests. Such failures highly depend on material properties and fabrication sequence. Substrate defects, process contamination,

and manufacturing equipment inaccuracy are common causes of these failures. Several wafer-level reliability screening techniques have been proposed that have the capability of detecting global reliability hazards and potentially replace the need for periodic life tests on IC chips [2.24].

However, many circuit defects are modeled as simple logical stuck-at faults in functional testing. The stuck-at fault model cannot cover many new failure phenomena. Delay failures resulting from the gradual degradation of key circuit components are often undetected in the conventional tests for stuck-at faults [2.26, 2.27]. Due to the continued increase in chip functionality, design verification and manufacture testing have become very complicated. In order to account for the delay faults in digital circuits and to address issues in the testing of analog circuits, circuit simulation techniques become very crucial in reliability assessment of integrated circuits.

Simulation-based design verification can predict the circuit performance accurately before committing the design to silicon fabrication. It is not adequate to bypass detailed circuit simulation and analysis but rely entirely on the testing of a small sample of fabricated integrated circuits to discover design errors or out-of-specification performance. Prediction of circuit reliability at the design stage is highly desirable.

Accurate prediction of integrated circuit lifetime is of particular concern in the development of application specific ICs (ASICs). In the case of standard IC parts, there is a long history of use upon which reliability estimation may be made. Standard parts are manufactured in large volume which leads to them being well characterized. The knowledge obtained from the characterization of standard parts can be used to facilitate accurate prediction for ASICs. Such

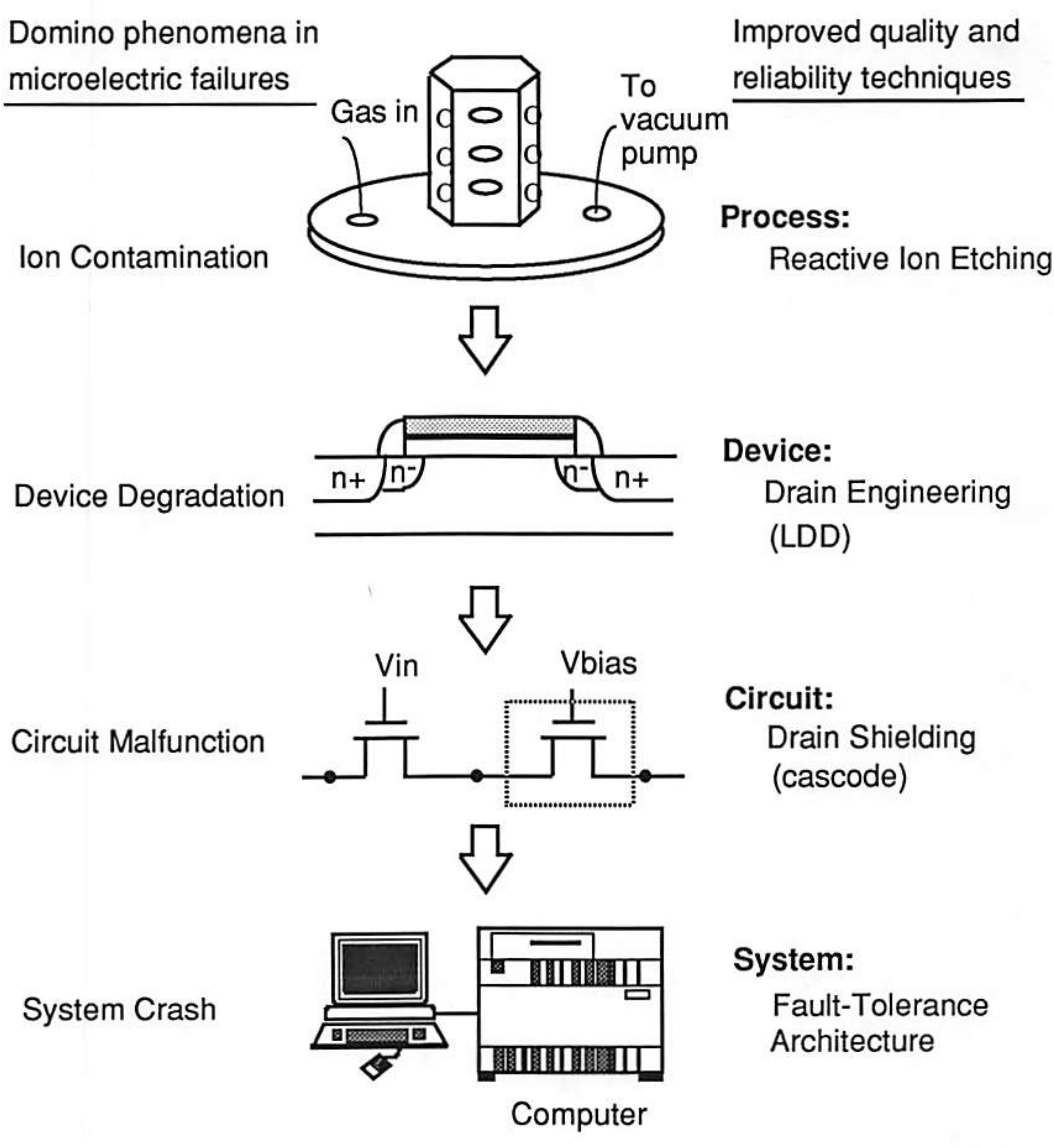

Fig. 2.2 Extension of device-level reliability enhancement to meet circuit- and system-level challenge.

predictions would be more effective than stipulating a blanket tolerance for the deviation of performance.

Design-for-reliability techniques exist at various levels of VLSI development as shown in Fig. 2.2 [2.28]. At the fabrication level, the reactive-ion etching technique is used to produce lightly-doped drain devices in order to reduce the high electric field in the channel. At the system-architecture level, redundant modules may be used to achieve high fault tolerance. Insufficient research and development efforts were spent on circuit-level design for reliability. In the sub-micron era, computer-aided design tools are very essential in the analysis and design of VLSI circuits. Integrated circuits can greatly benefit from the full capabilities of advanced fabrication processes only when appropriate CAD tools are available to facilitate circuit reliability assessment [2.29]-[2.33]. In a VLSI circuit, the amount of stress received by each device is a complex function of the transistor location, bias conditions, etc. A circuit may become inoperative or malfunctioning due to the failure of some critical devices. Detailed reliability measurements were usually conducted only on simple modules to obtain design parameters. Circuit designers used to have little control over integrated circuit reliability. Due to large number of devices contained in each VLSI circuit, it is impossible to accurately infer circuit lifetime through simple human interpretation of the raw test data. Reliability simulation becomes an indispensable task in the design for reliable circuits. The microelectronic circuit lifetime and system stability can be greatly enhanced by identifying critical devices and applying novel design techniques with the aid of reliability simulation tools.

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Chapter 3

Physics and Modeling of Integrated-Circuit Reliability

The understanding and modeling of physical failure mechanisms in integrated circuits are very important in predicting the integrated-circuit reliability. Computer-aided analysis results are only as accurate as the models used. Accurate circuit-level reliability models and the associated parameter extraction procedures are essential to the successful assessment of integrated circuits and microsystem reliability. In this chapter, failure mechanisms for hot-carrier effects and metal electromigration, and the corresponding electrical models for circuit reliability simulation are described. In section 3.1, physics and models of hot-carrier effects are presented. Modeling for simulation of hot-carrier effects includes regular transistor models used in the SPICE circuit simulator, substrate current model for monitoring the stress level, and degradation models for calculating transistor degradation. The associated parameter extraction procedures are described. An AC degradation factor to include excessive degradation under dynamic stress conditions is also presented. In section 3.2, electrical models to describe metal electromigration in the circuit level are presented.

Measurement results on single devices for hot-carrier effects and electromigration are also presented in this chapter. The test devices used in the experiments are experimental wafers from a production 1.2-μm process of TRW Inc., industrial 1.6-μm processes through the MOSIS Service, and a 0.8-μm experimental process of Hewlett-Packard Inc.

3.1 Hot-Carrier Effects

Previous research efforts on understanding of physical mechanisms and modeling of hot-carrier effects have led to the achievements of (i) determination of the electrical stress monitor such as the substrate current [3.1]-[3.4]; (ii) correlation of degradation in transistor characteristics with the stress monitor [3.5]-[3.8]; and (iii) discovery of failure mechanisms due to carrier trapping and interface trap state generation [3.9]-[3.11]. Physical origin of hot-carrier effects is an electron-hole generation process due to impact ionization near the drain diffusion region followed by carrier injection, carrier trapping and interface states generation. The substrate current can be used as an effective monitor of the amount of carriers created due to impact ionization [3.1]. The hot-carrier-induced device failure has usually been represented by a specific percentage change in common device variables such as the threshold voltage, transconductance, and subthreshold slope. Laboratory experiments under a fixed biasing condition (either in the saturation region with high V_{ds} and low V_{gs}, or in the triode region with moderate V_{gs} and low V_{ds}) were used to study single transistor behavior. An essential SPICE MOS model for circuit reliability simulation should possess the following features:

. a compact set of model parameters which minimizes parameter value updating overhead,

. accurate prediction of device output characteristics, and

. strong physical meanings to facilitate the establishment of parameter degradation relationships.

In order to achieve accurate simulation of circuit behavior as the exact function of in-use time, the challenging modeling effort is to derive expressions for the changes of SPICE model parameter values as functions of time and stressing levels. It will allow the designers to achieve the highest level of system reliability possible with the given fabrication technology. The integration of circuit reliability modeling for hot-carrier effects needs a strongly physical-based transistor model including short-channel and narrow-width effects, accurate substrate current model for monitoring the stress level, and effective degradation model to assess the rate of change in transistor characteristics. Special attention has been paid to handle the degradation characteristics under DC and AC voltage stresses. The quasi-static approximation in circuit simulation will still be useful if judicious choices of adjustment parameters can be made to account for the effects of high-speed circuit operation.

3.1.1 Transistor Model

To serve the purpose of circuit simulation, an MOS transistor model must be not only physically meaningful and accurate, but also computationally efficient and memory effective [3.12]. A good SPICE MOS transistor model for submicron VLSI technologies is essential to facilitate accurate and efficient circuit reliability simulation.

There are four MOS transistor models implemented in the SPICE-2G6B and SPICE-3E1 Programs. Each model differs in complexity and accounts for various first-order and second-order physical effects. The Level-1 model contains fairly simple expressions developed by Shichman et al. [3.13]. It is based on

fundamental device physics but excludes second-order effects. The Level-2 model developed by Vladimirescu et al. [3.14] accounts for several second-order effects such as velocity saturation, transverse field induced mobility degradation. There are 23 parameters to model the channel-region characteristics. The semi-empirical modeling approach for short-channel devices is attempted in the Level-3 model by S. Liu et al. [3.14]. It approximates basic device physics while allows empirical parameters to more accurately represent the device characteristics. Though the Level-3 model is used for 1.2-μm CMOS technology, it's also commonly applied to submicron devices.

The Level-4 model (BSIM) [3.15] developed by Sheu et al. marks a significant progress in the semi-empirical approach. The BSIM takes into account more short-channel and narrow-width effects. Both the channel length and width dependencies of electrical parameters are incorporated into the model. It requires 67 parameters to model the channel-region characteristics. A methodology to include temperature dependence modeling for the Level-4 model is described in [3.12]. The BSIM_plus model by Sheu and Gowda [3.16] represents a further improvement in modeling for deep-submicron MOS transistors. A pseudo-boundary method is used for simulation over the entire geometric space.

Figure 3.1 shows a comparison of simulated and measured drain-current characteristics for an NMOS transistor with the use of the Level-4 model. Table 3.1 depicts a comparison of important features from the four SPICE MOS transistor models.

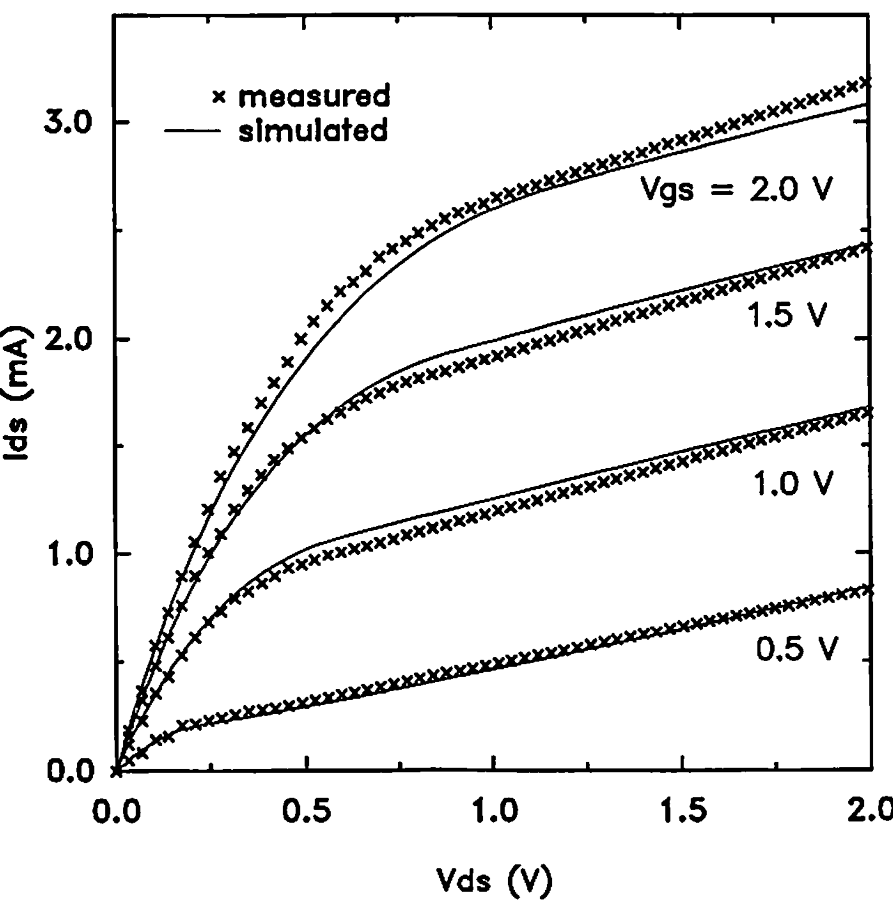


Fig. 3.1 Comparison of measured and simulated I_{ds} - V_{ds} characteristics for a W/L = 10 μm/0.15 μm NMOS transistor [3.44]. The Level-4 model is used.

Table 3.1 Comparison of features among various SPICE MOS models.

Features \ Models	Level-1	Level-2	Level-3	BSIM
Developer	Schiman et al. (1968)	Vladimirescu et al. (1980)	Vladimirescu et al. (1980)	Sheu et al. (1985)
Number of parameters	8	23	21	67
Subthreshold conduction	No	Equation matching	Euqation matching	Linear summation
Substrate current expression	No	No	No	No
Charge-based capacitance model	Yes	Yes	No	Yes
Temperature dependence	No	Yes	Yes	No
Applicable technology	4 μm	2 μm	1.2 μm	0.8 μm

3.1.2 Substrate Current Model

The hot-carrier charge trapping involves charge injection efficiency over the oxide barrier, the gate current is a natural monitor of hot-carrier effects. Figure 3.2 shows the generation of electron-hole pairs due to impact ionization and the carrier injection in a cross section of an NMOS transistor. Gate current can be expressed as [3.1]

$$I_g = C_1 \cdot I_{ds} \cdot e^{-\phi_b / q\lambda E_m} \tag{3.1}$$

where C_1 is a process-dependent parameter, ϕ_b is the barrier energy at the Si–SiO_2 interface, λ is the hot-electron mean-free-path, and E_m is the maximum channel electric field. Typically, the gate current is four orders of magnitude smaller than the substrate current and is in the range of a few femto amperes. The easily measurable substrate current has been widely used as an effective monitor for hot-carrier effects. Both the gate current and the substrate current are produced by a common driving force - the maximum channel electric field. The substrate current can be expressed as [3.1]

$$I_{sub} = C_2 \cdot I_{ds} \cdot e^{-\phi_i / q\lambda E_m} \tag{3.2}$$

where C_2 is a process dependent parameter and ϕ_i is the minimum required energy for a carrier to cause impact ionization. A simple model for the E_m was introduced by considering velocity saturation region near the drain [3.2]. Modeling of transistor degradation can be done by using the substrate current as an indicator. Figure 3.3 shows the measured substrate current characteristics as a function of the gate bias for the NMOS transistor and PMOS transistors, respectively, with W/L = 11 μm/0.75 μm. Figure 3.4 shows the dependence of the

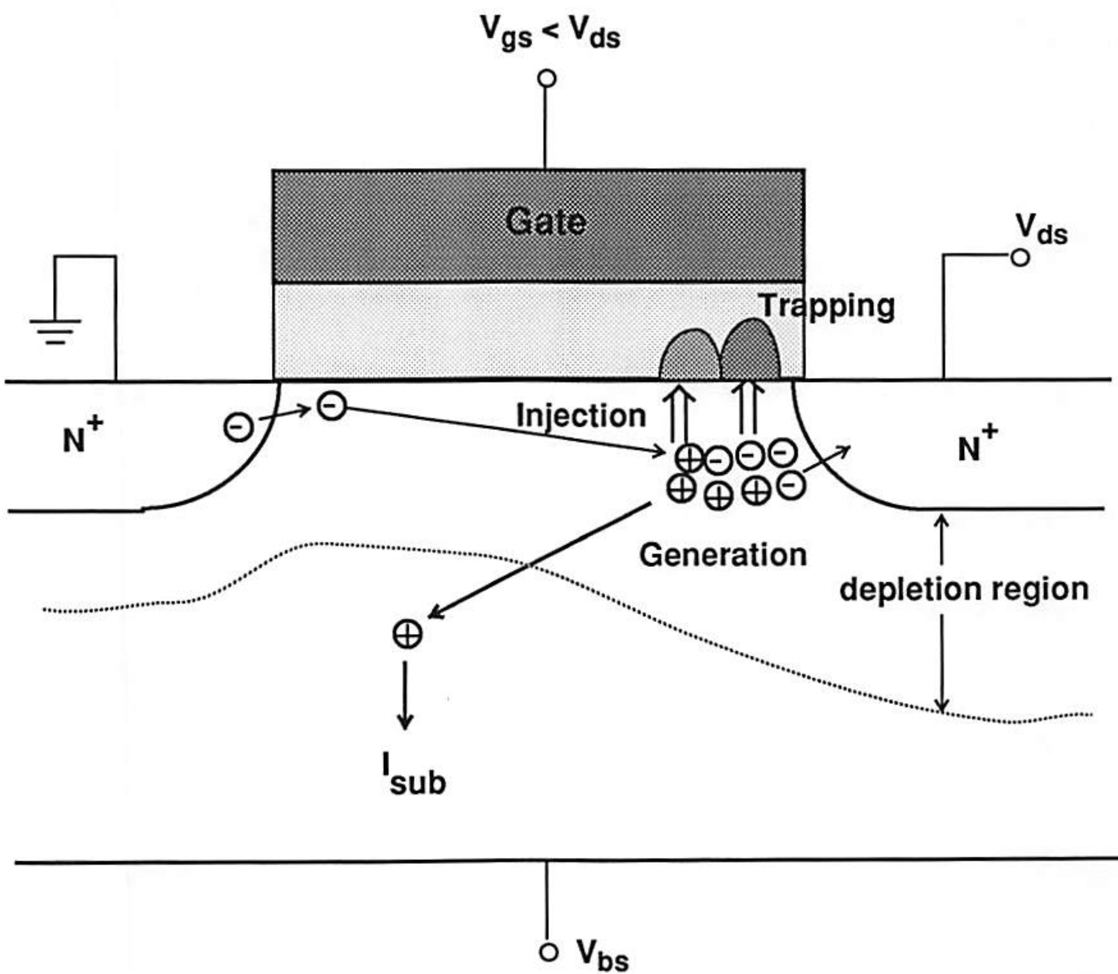
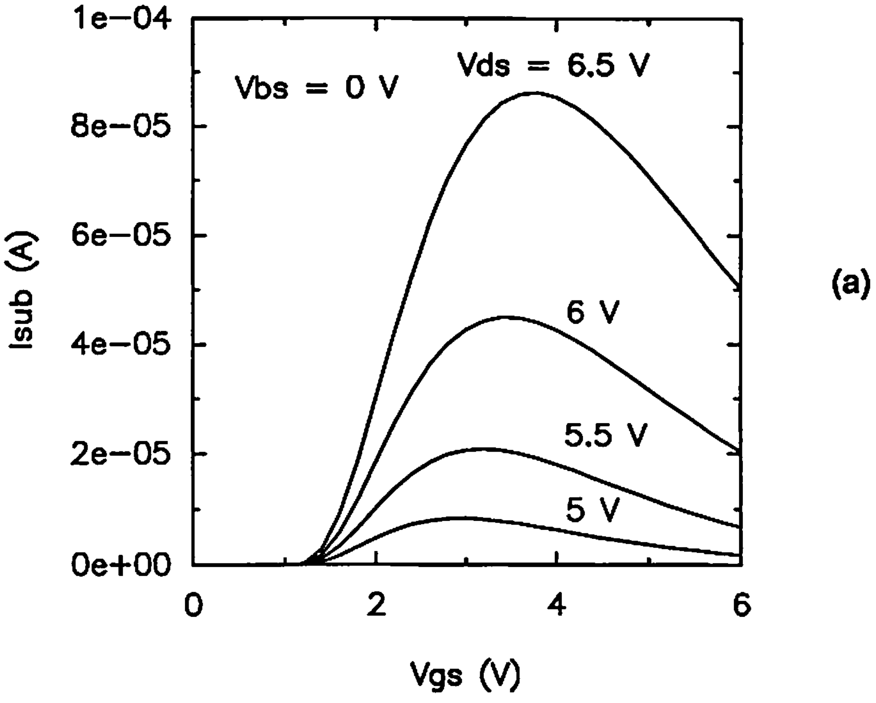


Fig. 3.2 Physical mechanisms of hot-carrier effects in an NMOS transistor.



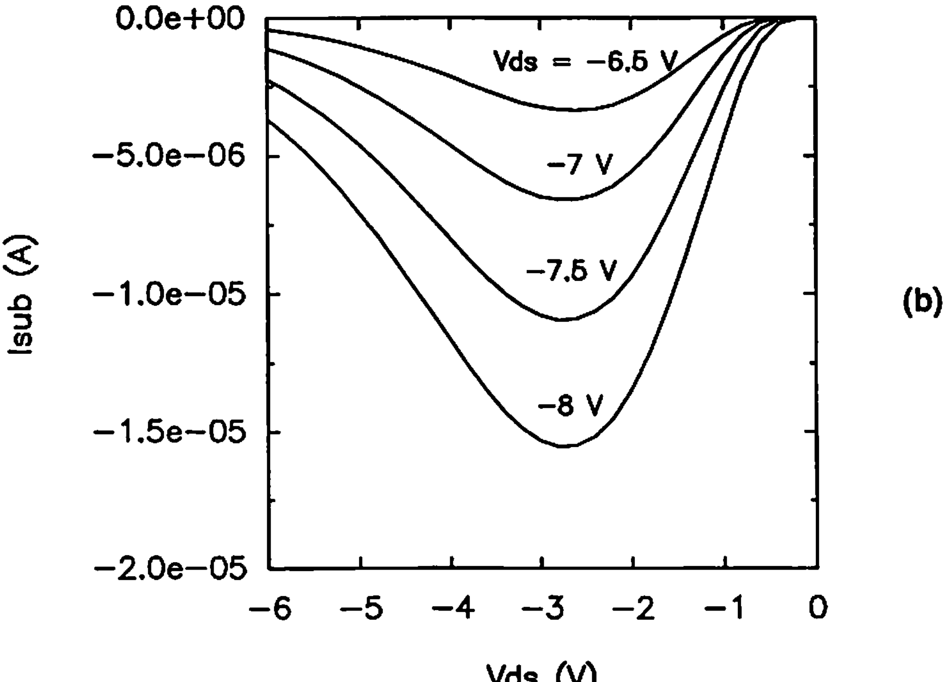


Fig. 3.3 Measured substrate current characteristics for the W/L = 11 μm/0.75 μm transistors.
(a) An NMOS transistor. (b) A PMOS transistor.

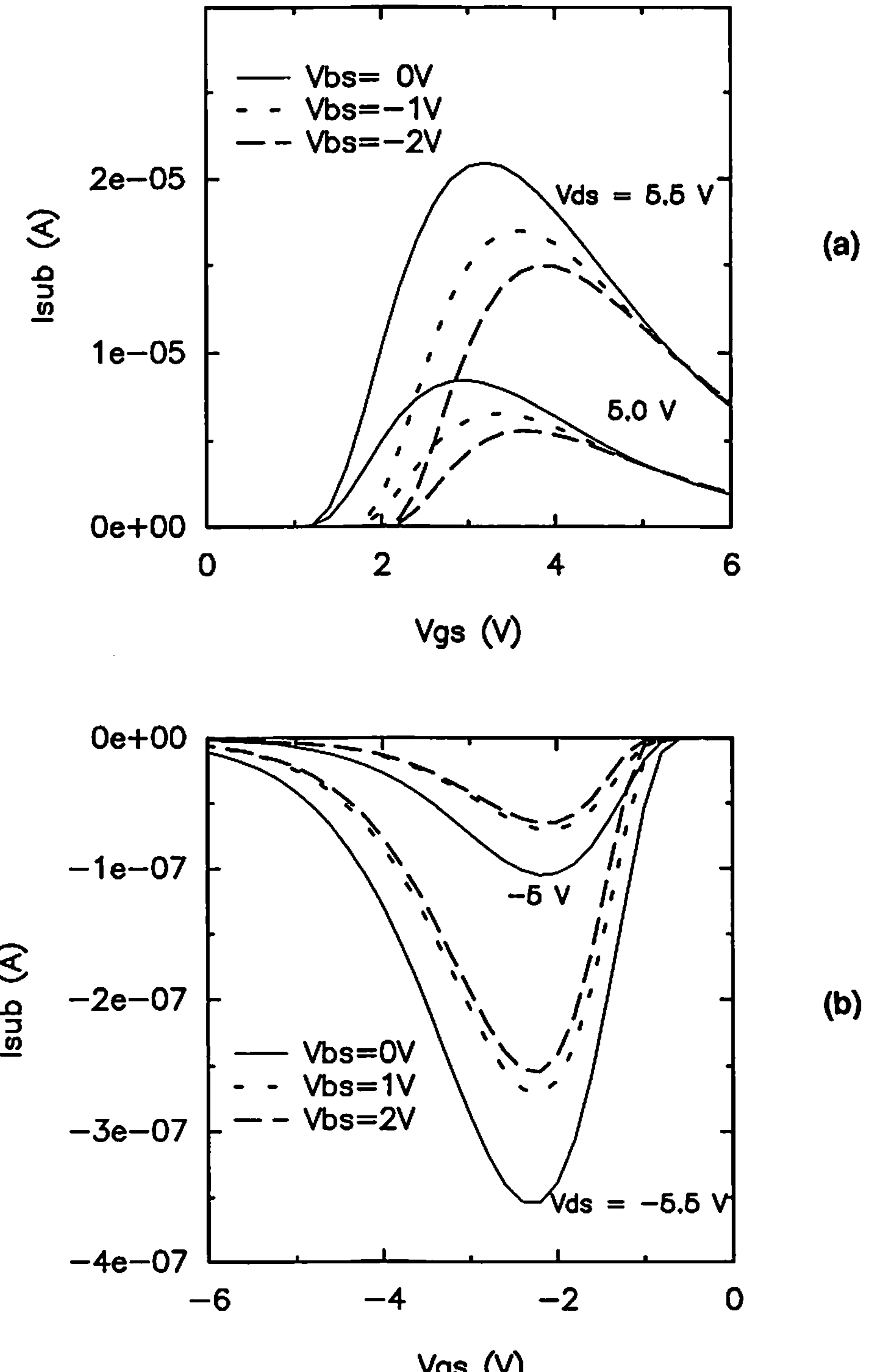


Fig. 3.4 Measured voltage dependence of the substrate current on the substrate bias for the W/L = 11 μm/0.75 μm transistors.
(a) An NMOS transistor. (b) A PMOS transistor.

measured substrate currents on the substrate bias for the same set of transistors.

3.1.2.1 Formulation of Substrate Current Model

The substrate current model used for monitoring hot-carrier effects is based on work done by El-Mansy et al. [3.17] and Mar et al. [3.18]. Channel regions are partitioned into the low-field gradual channel region and the high-field impact ionization region. By using field criterion for impact ionization region, Mar et al. derived expressions for the length of the impact ionization region, ΔL_i , and average tangential electric field as functions of N_A, V_{gs}, V_{ds}, and V_p where V_p is the channel potential at the boundary between the low-field gradual channel region and the high-field impact ionization region. A brief derivation is shown below [3.18]. The average tangential field in the impact ionization region based on pinch-off condition can be expressed as [3.18]

$$E_{Ti} = \sqrt{\frac{q \cdot N_A \cdot (V_{ds} - V_p)}{2\varepsilon_{Si}}} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{Si} \cdot \Delta L_i}(V_{ds} - V_p). \tag{3.3}$$

The second term represents the fringing-field contribution to the average field. Since the length of the impact ionization region ΔL_i can be related by

$$\Delta L_i = \frac{(V_{ds} - V_p)}{E_{Ti}}. \tag{3.4}$$

Both (3.3) and (3.4) can be combined for the expressions of ΔL_i and E_{Ti},

$$\Delta L_i = \sqrt{\frac{2\varepsilon_{si} \cdot (V_{ds} - V_p)}{qN_A}} \left(1 - \frac{\varepsilon_{SiO_2}}{\varepsilon_{Si}}\right) = 2357 \cdot \sqrt{\frac{V_{ds} - V_p}{N_A}} \tag{3.5}$$

and

$$E_{Ti} = \sqrt{\frac{q \cdot N_A \cdot (V_{ds} - V_p)}{2\varepsilon_{Si}}} \left(\frac{\varepsilon_{Si}}{\varepsilon_{Si} - \varepsilon_{SiO_2}}\right) \tag{3.6}$$

$$= 4.2426 \cdot 10^{-4} \cdot \sqrt{N_A \cdot (V_{ds} - V_p)}.$$

The channel potential V_p can be expressed in a modified form as

$$V_p = \frac{L \cdot E_{sat} \cdot (V_{gs} - V_{th})}{L \cdot E_{sat} + (V_{gs} - V_{th})}. \tag{3.7}$$

The substrate current due to impact ionization is calculated by integrating the electron impact ionization coefficient α_i which is a function of the tangential electric field, E_T [3.18],

$$I_{sub} = I_{ds} \cdot \int_0^L \alpha_i(E_T) \cdot dx = I_{ds} \cdot \int_0^L A \cdot e^{-B/E_T}\, dx. \tag{3.8}$$

By using equations (3.3) and (3.4), the impact ionization substrate current can be expressed in a simple form [3.18]:

$$I_{sub} = I_{ds} \cdot \Delta L \cdot A \cdot e^{-B/E_{Ti}}. \tag{3.9}$$

Calculation of E_{Ti} and ΔL_i can be done by substituting (3.7) into (3.4) and (3.5), respectively. In the modified model, three parameters are needed to model the impact ionization substrate current. These parameters include A, B, and E_{sat}. Voltage dependence of parameter E_{sat} can be further replaced by two additional parameters as explained in the following section.

3.1.2.2 Extraction of parameters A and B

The objective of the parameter extraction procedure is to obtain a set of A and B values which will enable an accurate calculation of the substrate current. Equation (3.9) can be rewritten as,

$$\frac{I_{sub}}{I_{ds}} = \Delta L_i \cdot A \cdot e^{-B/E_{Ti}}. \tag{3.10}$$

By taking the natural logarithm on both sides, it can be written as

$$\log_n \left[\frac{I_{sub}}{I_{ds}}\right] = \log_n(\Delta L_i \cdot A) - \frac{B}{E_{Ti}}. \tag{3.11}$$

The value of $\log_n \left[\frac{I_{sub}}{I_{ds}}\right]$ is to be determined from the measured data. If the value of the intermediate variable E_{Ti} is obtained, a curve of $\log_n \left[\frac{I_{sub}}{I_{ds}}\right]$ vs. $\frac{1}{E_{Ti}}$ can be plotted. By fitting the curve with a straight line, both $\log_n(\Delta L_i \cdot A)$ and B can be obtained from the y-intercept and the slope of the fitted line, respectively. Another parameter in this plot is E_{sat}, whose value is needed to determine E_{Ti}.

3.1.2.3 Parameter extraction of E_{sat}

Parameter E_{sat} is used in (3.6) and (3.7) to calculate V_P and E_{Ti}. The extraction strategy for A and B described in the previous section hence depends strongly on the value of E_{sat}. The effect of E_{sat} on the $\log_n\left[\frac{I_{sub}}{I_{ds}}\right]$ vs. $\frac{1}{E_{Ti}}$ plot

is shown in Fig. 3.5 for a W/L = 11 μm/0.625 μm NMOS transistor. The strategy used to extract E_{sat} involves trying to obtain a linear relationship between $\log_n\left[\frac{I_{sub}}{I_{ds}}\right]$ vs. $\frac{1}{E_{Ti}}$. Having this linear relationship, impact ionization parameter A and B can be extracted from the fitted line.

Figure 3.6 shows the flowchart of extracting substrate current parameters. An initial value of E_{sat} is selected first. The objective is to minimize the deviation of the curve of $\log_n\left[\frac{I_{sub}}{I_{ds}}\right]$ vs. $\frac{1}{E_{Ti}}$ from a straight line by stepping through different values of E_{sat} in a binary search fashion. The deviation of the $\log_n\left[\frac{I_{sub}}{I_{ds}}\right]$ vs. $\frac{1}{E_{Ti}}$ curve from a straight line is calculated in each step. Finally, the appropriate value of E_{sat} is determined when the deviation is below a pre-set tolerance value. The value of E_{sat} is used to obtain the values of parameters A and B from the y-intercept and the slope of the fitted $\log_n\left[\frac{I_{sub}}{I_{ds}}\right]$ vs. $\frac{1}{E_{Ti}}$ straight line.

The measurement data for the extraction includes the drain current and the substrate current characteristics as a function of the gate voltage, measured at a high drain bias. A high drain bias is used so that a large portion of the data is collected from the saturation region where the impact ionization is large. In fact, only data in this region is primarily used in the extraction of the parameters A, B, and E_{Ti} .

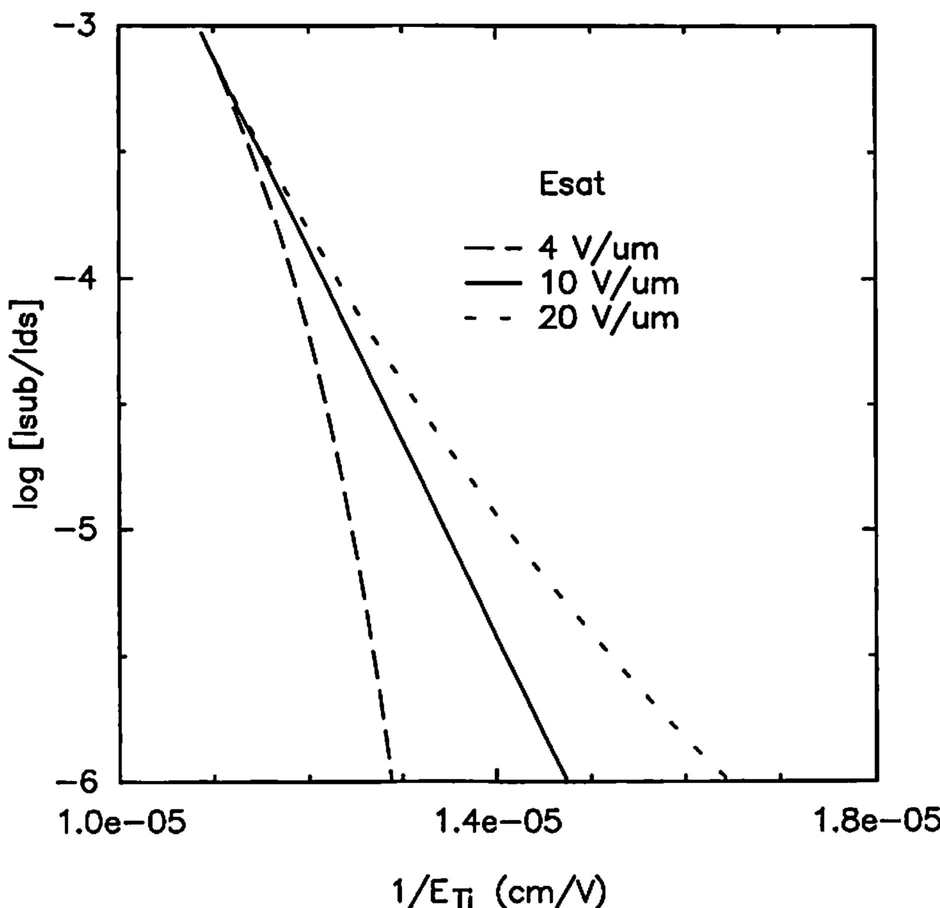


Fig. 3.5 Comparison of $\log_n\left[I_{sub}/I_{ds}\right]$ vs. $1/E_{Ti}$ at different E_{sat} values for a W/L = 11 μm/0.625 μm NMOS transistor at V_{ds} = 5 V.

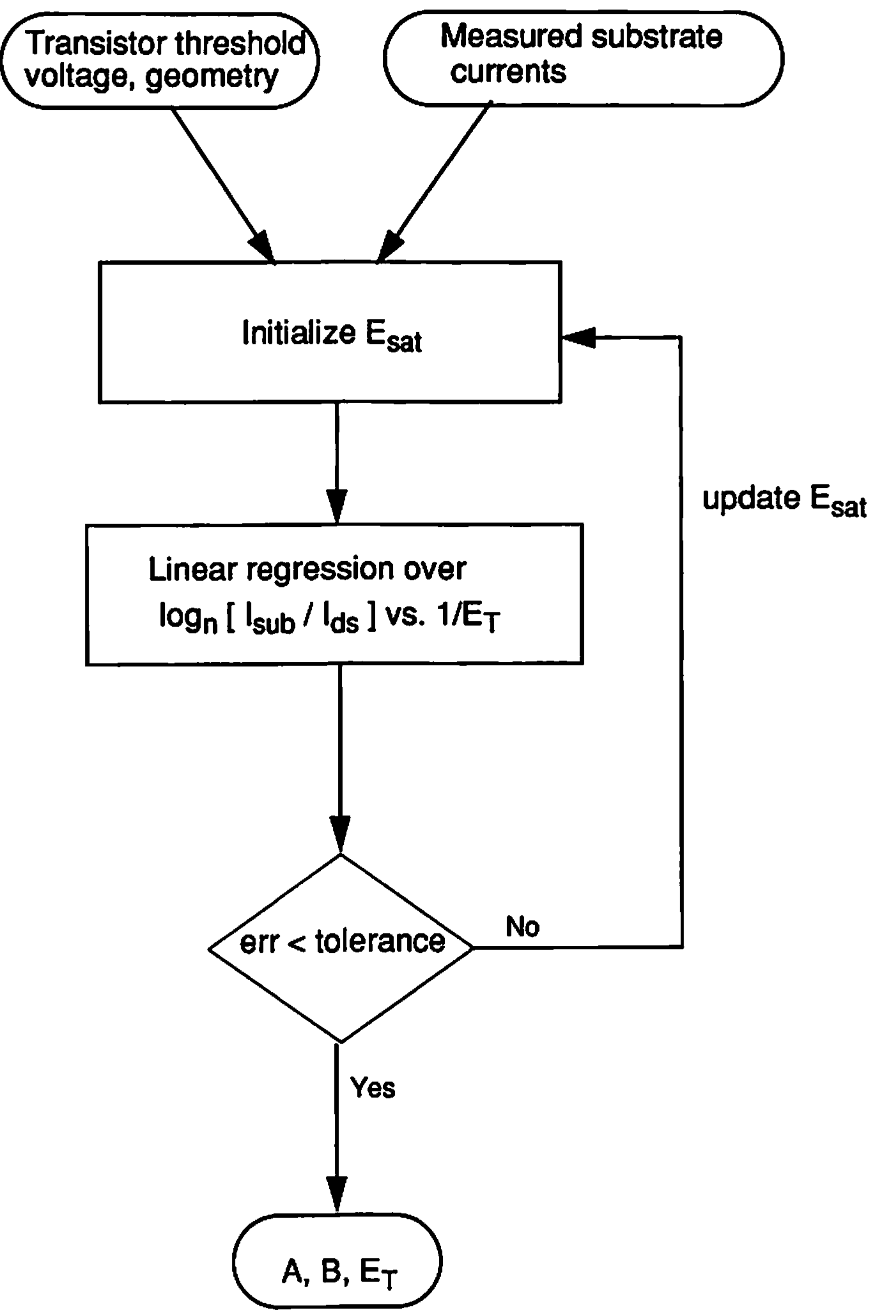


Fig. 3.6 Extraction flowchart for substrate current parameters.

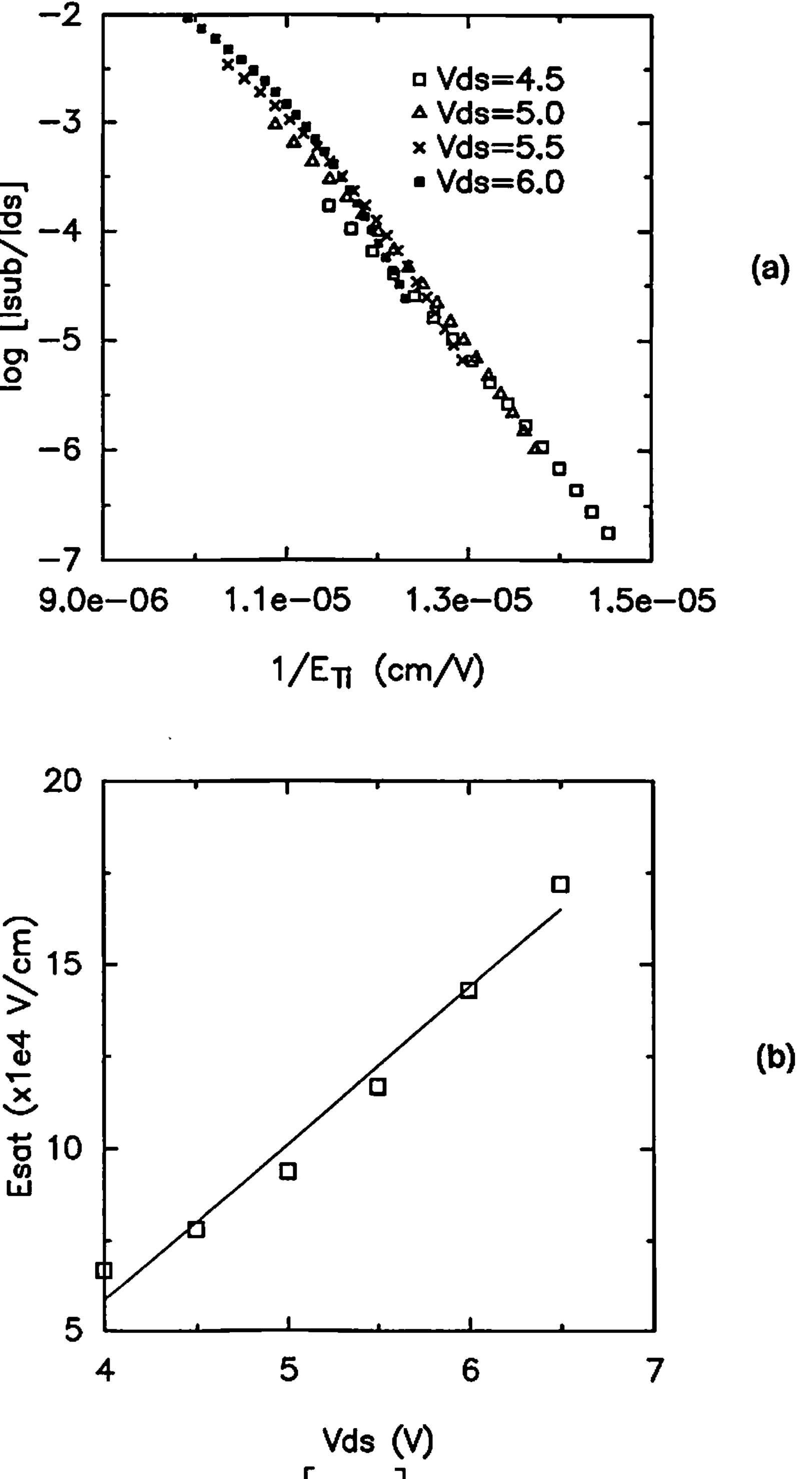


Fig. 3.7 (a) Comparison of $\log_n\left[I_{sub}/I_{ds}\right]$ vs. $1/E_{Ti}$ at different V_{ds} values for a W/L = 11 μm/0.625 μm NMOS transistor. $E_{sat} = 6.4\text{x}10^4$ V/cm.

(b) Dependence of E_{sat} on the drain bias.

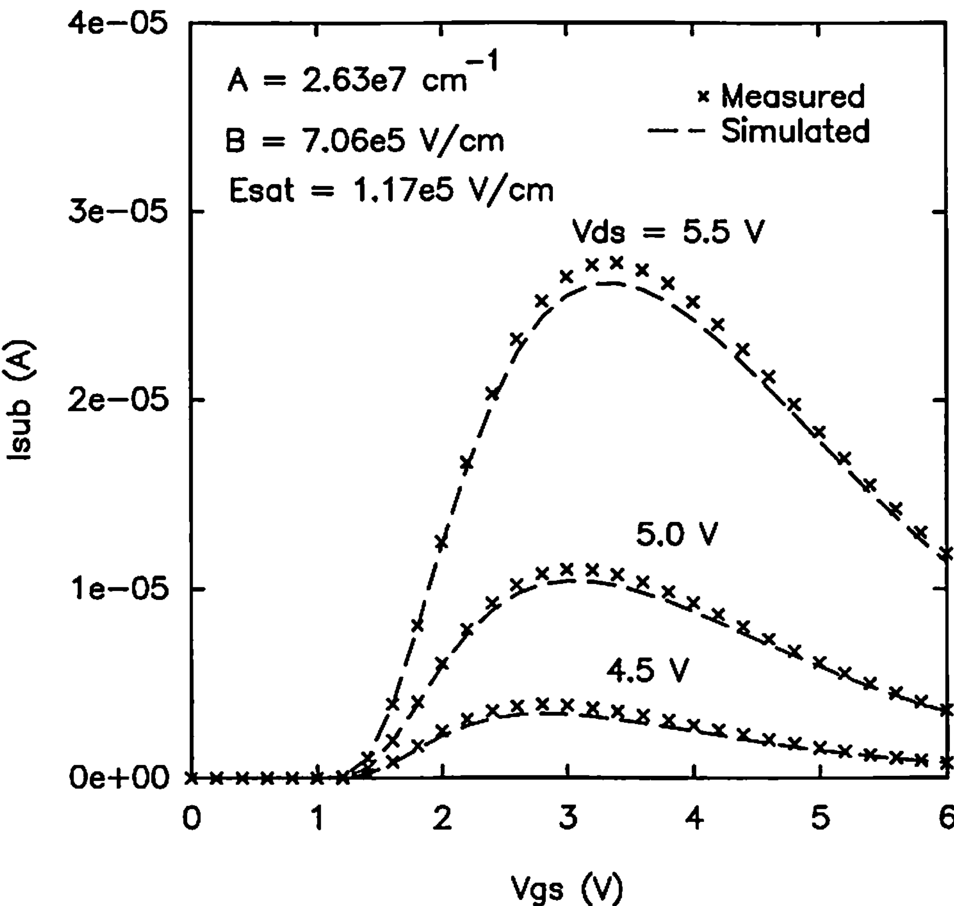


Fig. 3.8 Comparison of measured and simulated substrate current characteristics for a W/L = 11 μm/0.625 μm NMOS transistor.

Instead of using a global E_{sat} value, by performing parameter extraction for each drain voltage level, the voltage dependence of E_{sat} on the drain bias as shown in Figure 3.7 can be utilized to improve accuracy. First-order linear dependence is used to approximate the drain voltage dependence of E_{sat}. Figure 3.8 shows the measured and the simulated substrate current characteristics.

3.1.3 Hot-Carrier Induced Degradation Model

Hot-carrier induced damages are often described by the amount of changes in transistor parameters. The amount of degradation due to hot-carrier stress strongly depends on the stress conditions. Correlation of degradation with the bias condition can be made by using the substrate current level. Detailed physical mechanisms associated with hot-carrier stress have been investigated in terms of carrier injection and trapping [3.5]. Hot-hole injection has been found to be much more effective in generating interface traps than hot-electron injection. The experimental results [3.10, 3.25] from NMOS transistors showed that hot-hole injection dominates and results in hole trapping as being the major degradation factor in the low gate voltage region. Interface traps are also generated but are masked by the trapped holes. In the intermediate bias region ($V_{gs} \approx V_{ds}/2$), the substrate current is maximum because both electrons and holes can be injected into the gate oxide. Hole trapping gradually disappears as the gate bias increases and the hot-electron-induced interface traps also contribute to the transistor degradation. In the high gate bias region ($V_{gs} \approx V_{ds}$), high-energy electrons are injected into the gate oxide and can be measured as the gate current.

PMOS transistors show different degradation behaviors [3.25]. For very low and intermediate gate voltages ($V_{gs} \approx V_{th}$ and $V_{gs} \approx V_{ds}/2$), electron trapping is the dominant degradation mechanism. For high gate voltages ($V_{gs} \approx V_{ds}$), the increase of absolute value in threshold voltage ($\Delta|V_{th}|$) is likely due to the generated interface traps.

3.1.3.1 Characterization of Degradation under DC Stress

The constant voltage stressing method has been used to study hot-carrier generation in transistors by biasing the transistor at the maximum substrate current condition ($V_{gs} \approx V_{ds}/2$). The I_{ds}-V_{ds} and I_{sub}-V_{gs} characteristic curves for an NMOS transistor with W/L = 11 μm/0.625 μm before and after electrical stress are shown in Fig. 3.9. The transistor was stressed at a substrate current level of 109 μA for 6 hours. Figure 3.10 shows the similar characteristics for a PMOS transistor with W/L = 11 μm/0.75 μm. Figure 3.11 shows the the drain current and gate capacitance characteristics for a W/L_{eff} = 50 μm/0.9 μm N-channel transistor before and after a 12-hour DC stress. The hot-carrier-induced damage in the MOS transistor can be represented as shifts in the transistor output characteristics and parameters. Figure 3.12 shows changes of threshold voltage and mobility as functions of the stress time at different I_{sub} levels (stress levels) for an NMOS transistor with W/L = 11 μm/0.625 μm. ΔV_{th} and Δg_m have been found to increase with time according to a power law formula such as t^n. In general, the power law relationship between transistor degradation and stress time holds for transistor parameters:

$$\Delta P_i = a_i \cdot t^{n_i} \tag{3.12}$$

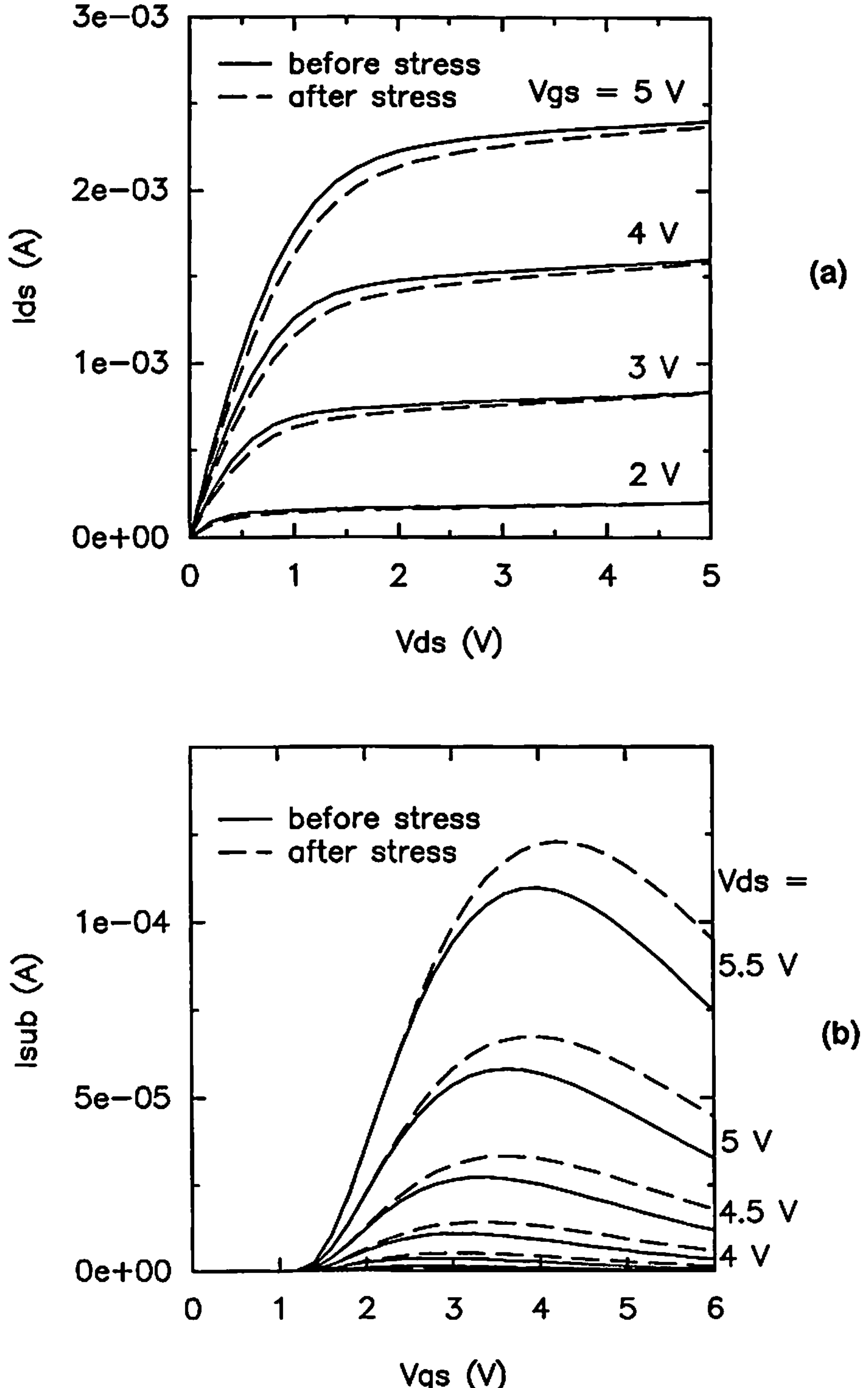


Fig. 3.9 Comparison of measured transistor output characteristics before and after stress for a W/L = 11 μm/0.625 μm NMOS transistor. The device is stressed at I_{sub} = 109 μA for 6 hours. (a) Drain current. (b) Substrate current.

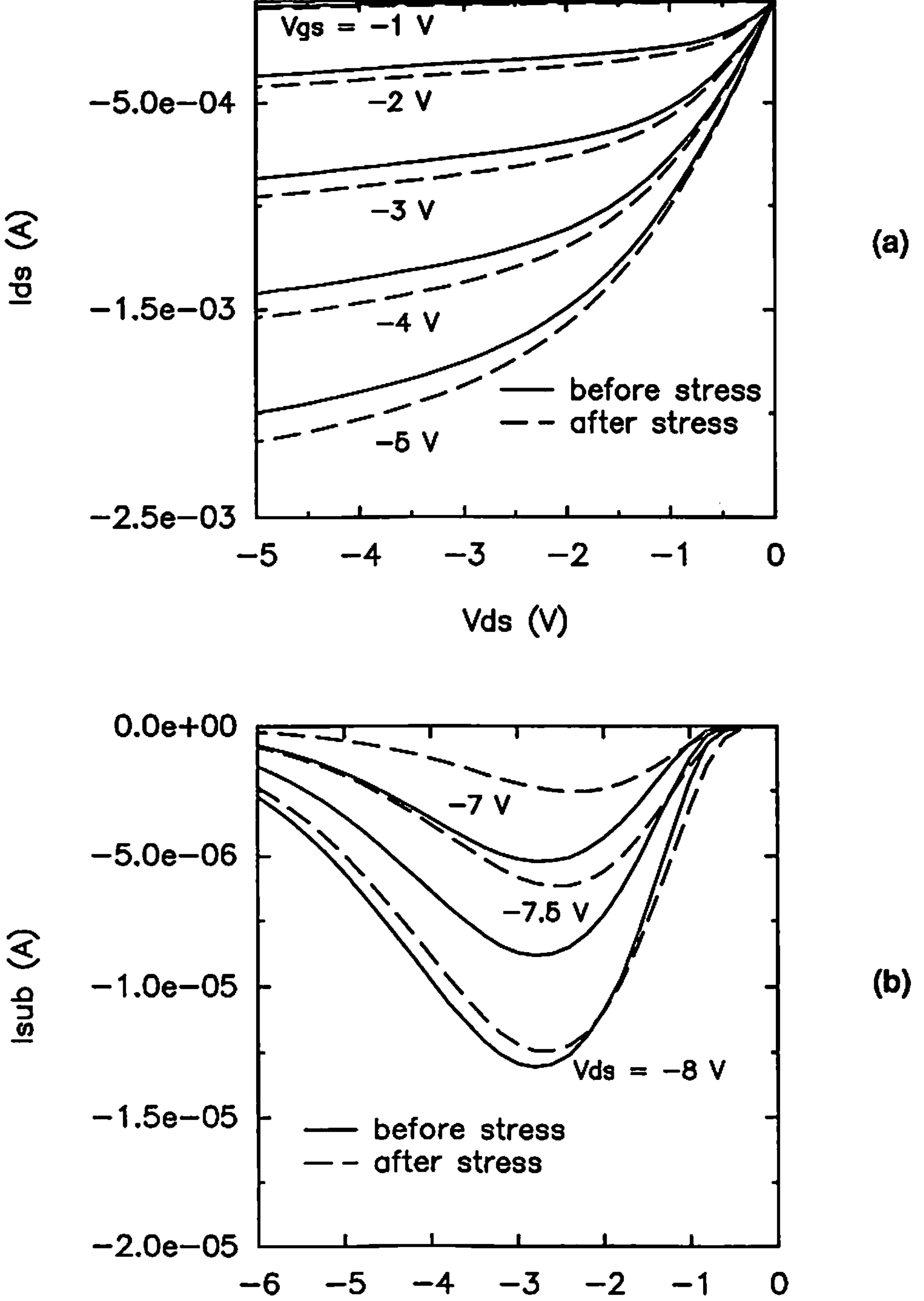


Fig. 3.10 Comparison of transistor output characteristic before and after stress for a W/L = 11 μm/0.75 μm PMOS transistor. The device is stressed at V_{ds} = −8 V and V_{gs} = −2.8 V for 6 hours. (a) Drain current. (b) Substrate current.

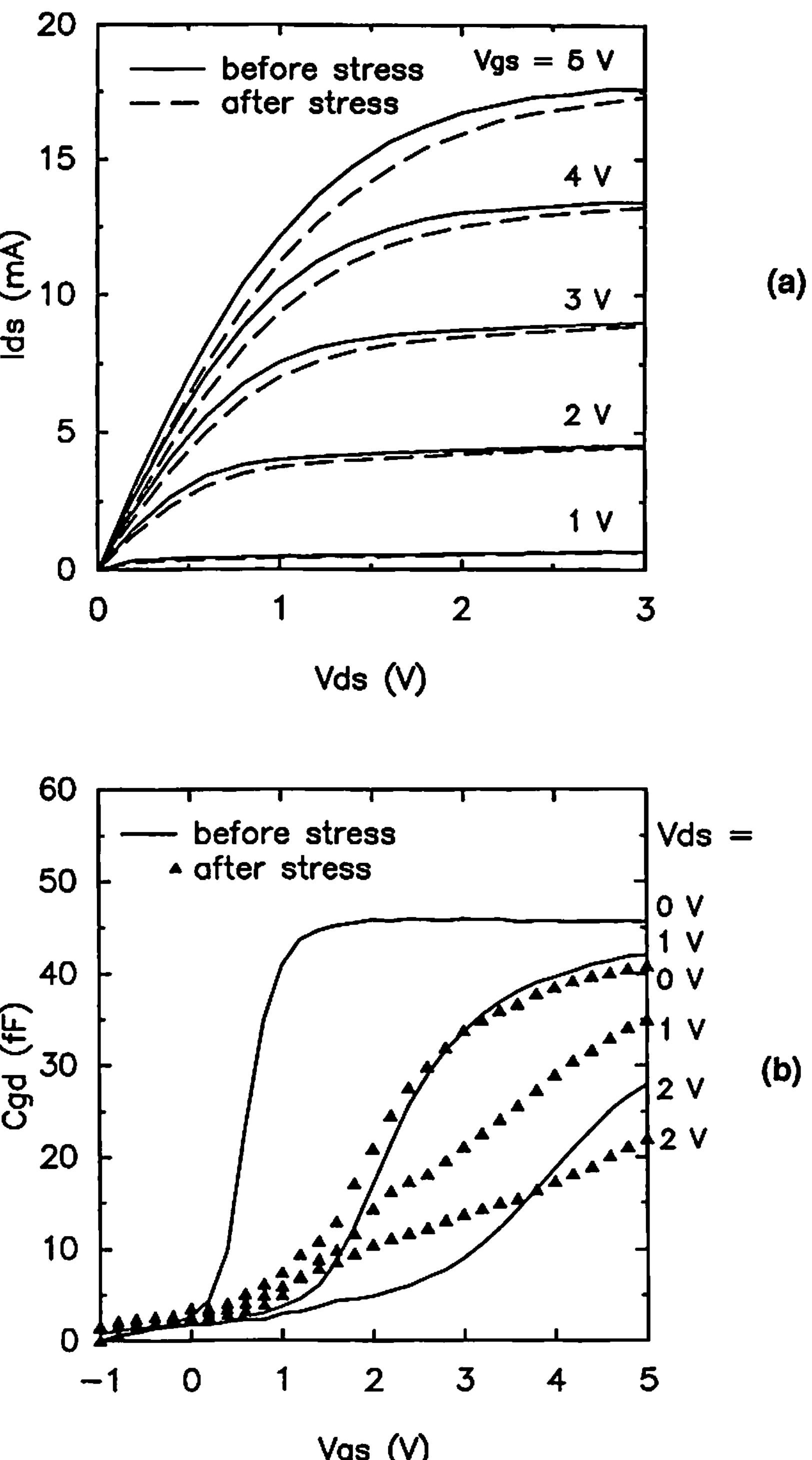


Fig. 3.11 Comparison of measured transistor output characteristics before and after stress for a W/L = 50 μm/0.9 μm NMOS transistor. The device is stressed at V_{ds} = 6.0 V and V_{gs} = 3.0 V for 12 hours. (a) Drain current. (b) Gate capacitance characteristics.

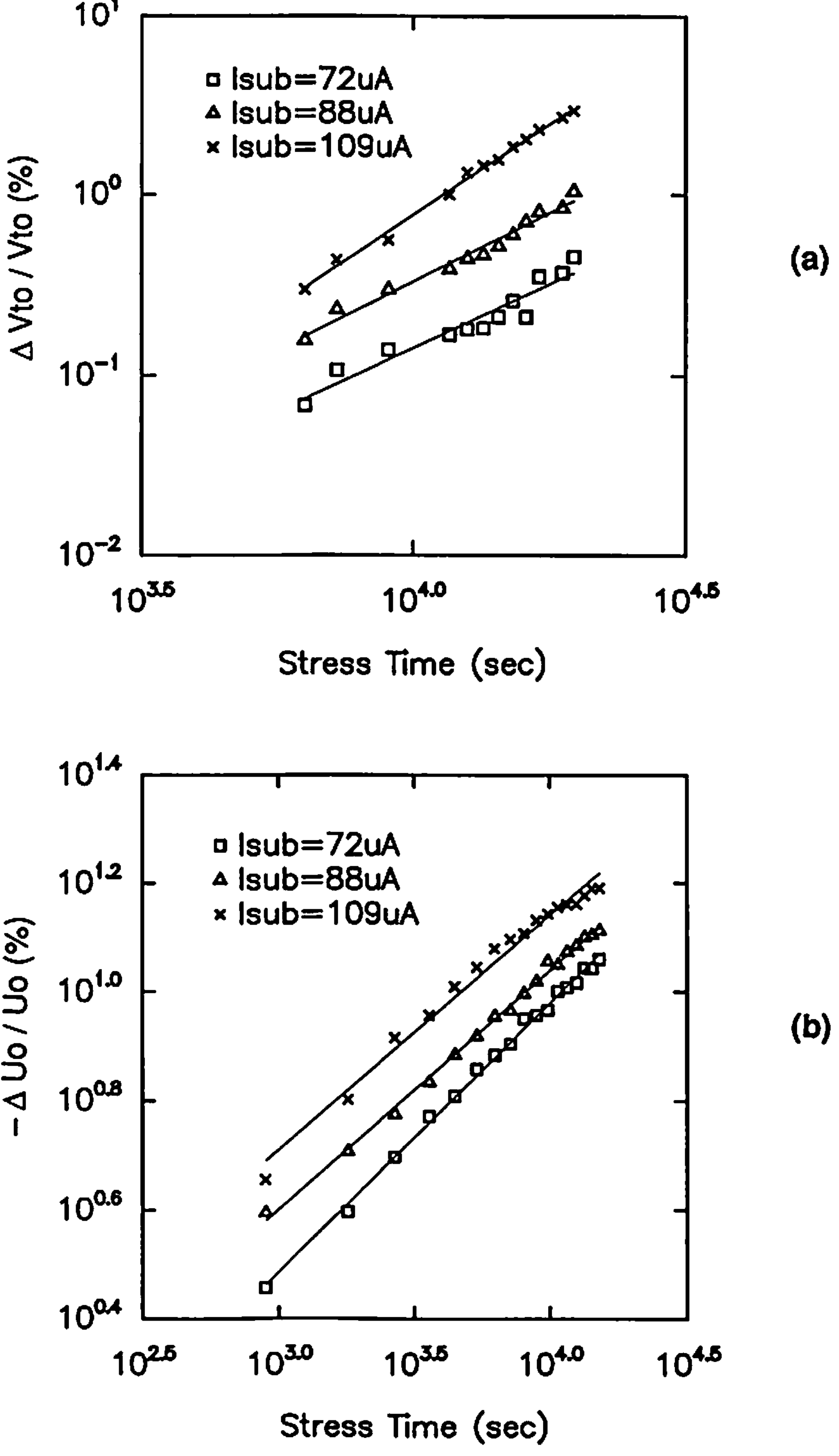


Fig. 3.12 Changes in transistor parameters as functions of stress time for a W/L =11 μm/0.625 μm NMOS transistor. Model parameter values are listed in Table 3.2. (a) Threshold voltage. (b) Mobility.

where P_i represents each transistor parameter, a_i and n_i are the fitting coefficients. While some researchers suggested parameter n is insensitive to the device parameters [3.1], others reported n to vary for different transistor parameters [3.19]. Key device parameters include threshold voltage, transconductance, body-effect coefficient, drain-induced-barrier lowering coefficient etc. Table 3.2 summarizes experimental results for an NMOS transistor stressed at various substrate current levels. This expression can be re-written to include the stress and geometric dependence as [3.20, 3.21]

$$\Delta P_i = A_i \cdot (I'_{sub})^{m_i} \cdot t^{n_i} \tag{3.13}$$

where I'_{sub} is the effective substrate current normalized by the transistor geometric aspect ratio. Constants A_i, n_i, and m_i are fitting parameters. This expression can be used to determine the transistor lifetime for a given amount of degradation (e.g. a shift in threshold voltage by 10 mV). Table 3.3 lists the degradation parameter values for prototyping NMOS and PMOS transistors with L = 0.5 μm from the industry. The absolute value of the threshold voltage increases for the NMOS transistor while it decreases for the PMOS transistor. The mobility decreases for the NMOS transistor while it increases for the PMOS transistor.

3.1.3.2 Hot-Carrier Effects under Dynamic Stress

In real-world applications, integrated circuits are usually operated under AC conditions. Though the DC stressing experiments have been used for the assessment of hot-carrier-induced damage, it is essential to assess the damages under

Table 3.2 Extracted degradation parameter results at thress different stress levels for an NMOS transistor with W/L = 11 μm/ 0.625 μm.

degr. parameters \ (% change)	ΔVth/Vth	−ΔUo/Uo	Δγ/γ	−ΔIds/Ids (lin. reg.)	−ΔIds/Ids (sat. reg.)	Isub (uA)
n	1.370	0.472	0.189	0.413	0.516	72
$\log_{10} a$	- 6.329	- 0.923	-0.467	- 0.995	- 2.201	
n	1.423	0.444	0.127	0.431	0.454	88
$\log_{10} a$	- 6.038	- 0.784	- 0.181	-1.052	-1.750	
n	1.479	0.360	0.312	0.539	0.392	109
$\log_{10} a$	- 5.963	- 0.286	- 0.680	- 1.349	- 1.399	

Table 3.3 Degradation parameters for prototyping NMOS and PMOS transistors with L = 0.5 μm from the industry.

degradation parameters \ transistor parameters		Δ Vth / |Vth|	Δ Uo/Uo	$\Delta\gamma/\gamma$
NMOS	A	10^{-8}	$-10^{-11.3}$	$10^{-3.14}$
	m	2.05	1.59	3.28
	n	1.42	0.46	0.16
PMOS	A	10^{-9}	$10^{-2.5}$	$10^{-5.32}$
	m	2.38	1.88	2.94
	n	0.19	0.23	0.22

AC conditions. Comparative studies on the degradation under AC and DC stresses were performed in the past [3.22]-[3.29]. While excessive degradation under AC stress has been reported [3.22, 2.26], the quasi-static approximation based on effective duty cycles is also found to be applicable in other experiments [3.23]. A comparison of degradation in mobility for an NMOS transistor under both AC stress and DC stress is shown in Figure 3.13. Excessive degradation under AC stress over that under DC stress with a ratio of 1.6 is found for this case.

For the quasi-static approximation without excessive degradation under AC stress conditions, the device degradation can be calculated by the stress duty cycle using the DC stress data [3.23]. Waveforms of the applied gate and drain biases are analyzed in the time domain, and the device degradation as a function of time is calculated by using the same parameter values for the DC stress condition. Since in DC stress, device degradation is expressed as a function of the substrate current, the degradation due to AC stress can be estimated by integration of the substrate current over time as

$$I_{sub,AC} = \frac{1}{T} \int_0^T I_{sub,DC} \, dt. \tag{3.14}$$

The transistor lifetime under AC stress can then be estimated as in the DC stress case [3.23].

To include the excessive degradation under certain AC stress condition, we have developed a systematic approach by using an AC degradation factor [3.30]. Table 3.4 lists several published results comparing the AC and DC degradation

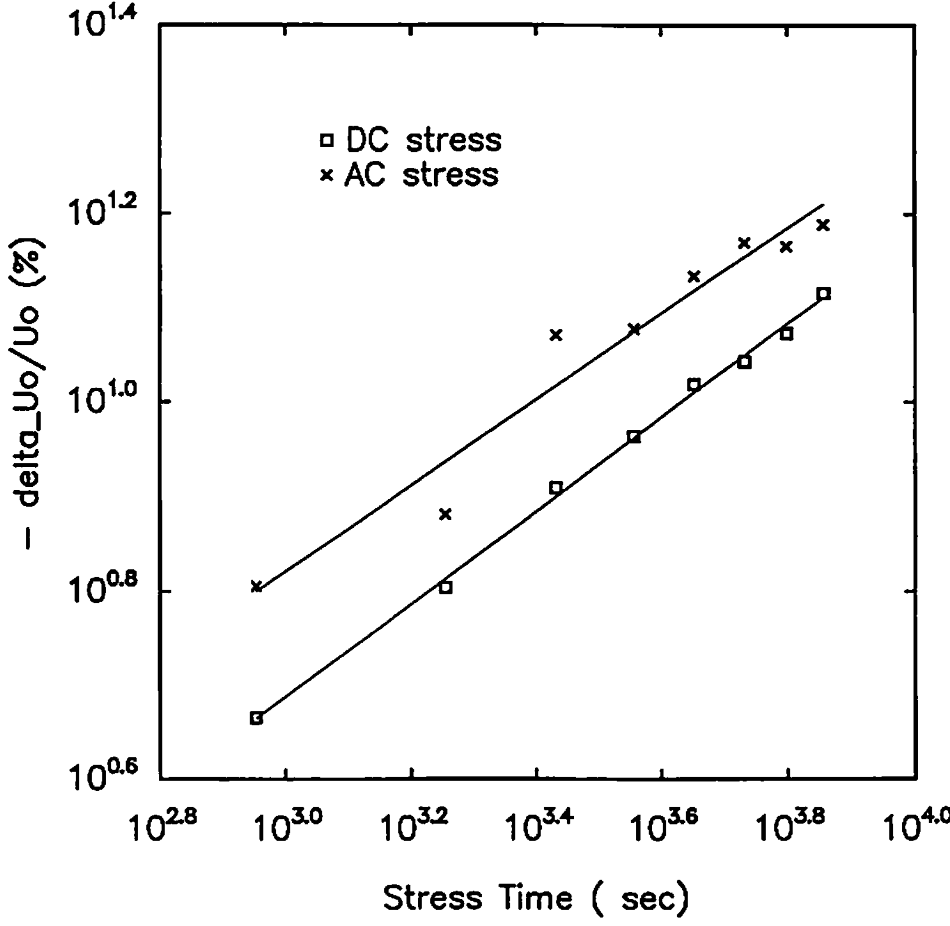


Fig. 3.13 Excessive degradation in mobility under dynamic stress vs. static stress for an NMOS transistor with W/L = 11 μm/0.7 μm. For dynamic stress, a 20 MHz gate pulse with a 50 % duty cycle is applied. The turn-on voltage levels are maintained at V_{ds} = 7 V and V_{gs} = 4 V.

Table 3.4 Summary of pulsed hot-carrier stress experiments with calculated values of the degradatoin factor $\Delta P_{AC\text{-}DC}$.

Pulse type		Stress conditions	Ref.	Monitored parameter	Degradation $\Delta P_{AC\text{-}DC}$
single pulse	high static Vds, pulsed Vgs	$V_{gs,peak}$=2V, V_{ds}=6.2V,P_w=100ns,10us	[3.23]	ΔV_{th}	1
		$V_{gs,peak}$=3V,50MHz, R=50%, V_{ds}=7V	[3.27]	Δg_m	1
		$V_{gs,peak}$=2,4,6,8,10V @1MHz, R=50%, V_{ds}=8V	[3.26]	ΔV_{th}	3.5
		$V_{gs,peak}$=3.25V,1.6MHz,R=50%,t_r=t_f=15ns,V_{ds}=6.5V	[3.28]	ΔI_{ds}	2
		$V_{gs,peak}$=3.5V,10-50MHz,R=50%,t_r=t_f=0.7ns V_{ds}=6.5V	[3.29]	ΔI_{ds}	1.6
	high static Vds, high pulsed Vgs	$V_{gs,peak}$=7V,50MHz,R=50%,V_{ds}=7V	[3.27]	Δg_m	10
	static Vgs, pulsed Vds	$V_{ds,peak}$=6.2V,Pw=500ns,V_{gs}=2V	[3.23]	ΔV_{th}	1
		$V_{ds,peak}$=8V,1MHz,R=50%,V_{gs}=2~10V	[3.26]	ΔV_{th}	1
		$V_{ds,peak}$=5 to 7.8V, 100KHz,R=50%,t_r=t_f=6ns	[3.25]	ΔI_{cp}	15
dual pulses	complete overlap	$V_{ds,peak}$=8V, $V_{gs,peak}$ = 0 to 8V, P_w=40ns	[3.22]	Δg_m	5
	partial overlap with leading Vgs	$V_{ds,peak}$=8V, $V_{gs,peak}$= 0 to 8V, P_w=40ns	[3.22]	Δg_m	4
		$V_{ds,peak}$=$V_{gs,peak}$=7V	[3.24]	Δg_m	5
		$V_{ds,peak}$=$V_{gs,peak}$=6.5V, 0.5MHz, V_{gs} : t_r=4ns,.1us, t_f=0, t_{ov}=.1us, V_{ds}:t_r=t_f=0	[3.26]	ΔV_{th}	3
	partial overlap with leading Vds	$V_{ds,peak}$=8V, $V_{gs,peak}$= 0 to 8V, P_w=40ns	[3.22]	Δg_m	3.3
		$V_{ds,peak}$=$V_{gs,peak}$=6.5V,0.5MHz V_{gs} : t_r=0, t_f=4ns,.1us, t_{ov}=.1us, V_{ds}: t_r=t_f=0	[3.26]	ΔV_{th}	1
	edge-overlapping	$V_{gs,peak}$=5.3, 1MHz,t_r=t_f=100ns,V_{DD}=5.3V	[3.20]	ΔI_{ds}	2

effects on the transconductance, threshold voltage and drain current characteristics of individual MOS transistors. Our calculated values of the degradation factor for AC stress, ΔP_{AC-DC}, for these experiments are also included. This factor is defined as,

$$\Delta P_{AC-DC} \equiv \frac{\Delta P_{AC}}{\Delta P_{DC}} \tag{3.15}$$

where ΔP_{AC} and ΔP_{DC} are the transistor parameter degradations under AC stress and DC stress, respectively. Excessive AC degradation such as that under the falling edge of the gate pulse in the presence of a high drain voltage is effectively predicted using the AC degradation factor. While the actual physical mechanism is not conclusive, the excessive degradation under AC stress is strongly related with the pattern of terminal voltage stresses. A conceptual two-carrier model has been used to explain the excessive degradation [3.5]. In this model, strong hole injection in the rising edge of the gate pulse followed by electron trapping in the falling edge of the gate pulse at the high drain voltage explains the excessive degradation in the dynamic stress conditions. The procedure to incorporate the AC degradation factor into circuit reliability simulation will be presented in Chapter 4.

3.2 Electromigration

Metal systems in use in most of today's silicon IC technologies are primarily aluminum alloys. Studies of electromigration have been focused on (i) physics and modeling of metal failure mechanisms [3.31]-[3.36], (ii) improvement of metal lifetime using composite metal structures [3.37]-[3.40], and (iii)

new characterization techniques to improve testing efficiency and accuracy [3.41]-[3.43] In the Al-based metals, a popular expression for the assessment of the Mean-Time-to-Failure factor is [3.31],

$$MTTF = \alpha \cdot J_{eff}^{-n} \cdot \exp(E_a/kT) \tag{3.16}$$

where J_{eff} is the effective current density, n is a fitting parameter, E_a is the activation energy, and α is cross-section dependent parameter. Figure 3.14 shows the measured values [3.31]-[3.33] of current density parameter that can be used in the analysis of electromigration for Al-based metals. These measured data are used to approximate the current density factor, n, for all conditions. At a high stressing current density, the actual metal temperature is increased due to the metal heating effect. A common current density factor, n, can be used for all current density ranges if a proper temperature correction is made to include the joule heating effect [3.33]. A value of around 1.5 [3.33] for the common current density factor is also shown in Fig. 3.14. Figure 3.15 shows the measured MTTF data for metal lines with a width of 2.4 μm. The MTTF values were extracted from the corresponding group of metal lines that follow a lognormal distribution in the lifetime test. The temperature dependence of the MTTF factor is shown in Fig. 3.15(a). The dependence of the MTTF factor on the current density is shown in Fig. 3.15(b). The current density parameter and the activation energy parameter in (3.16) are then determined. For electromigration under pulsed stress, a similar expression as (3.16) can be used to calculate metal lifetime using effective current density based on stress duty cycle [3.35]. For AC stress, a larger parameter α is used to model the longer metal lifetime due to the recovery of electromigration [3.36].

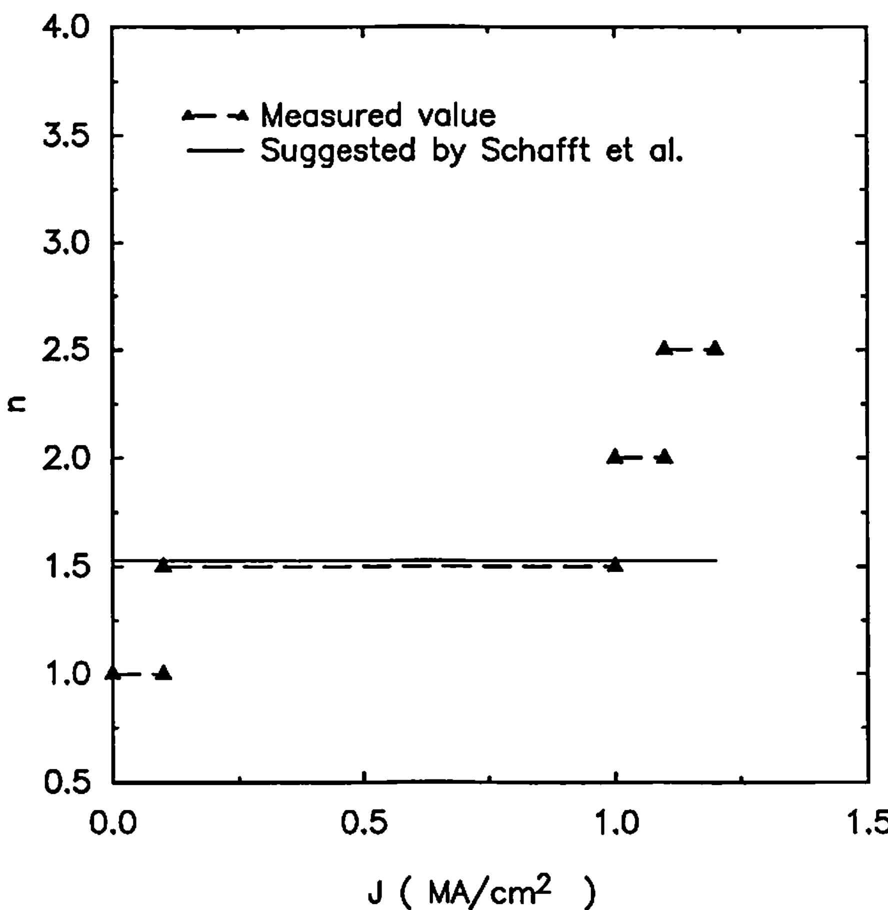


Fig. 3.14 Values of current density dependent parameter used in the electromigration simulation of Al-Si based metals [3.33].

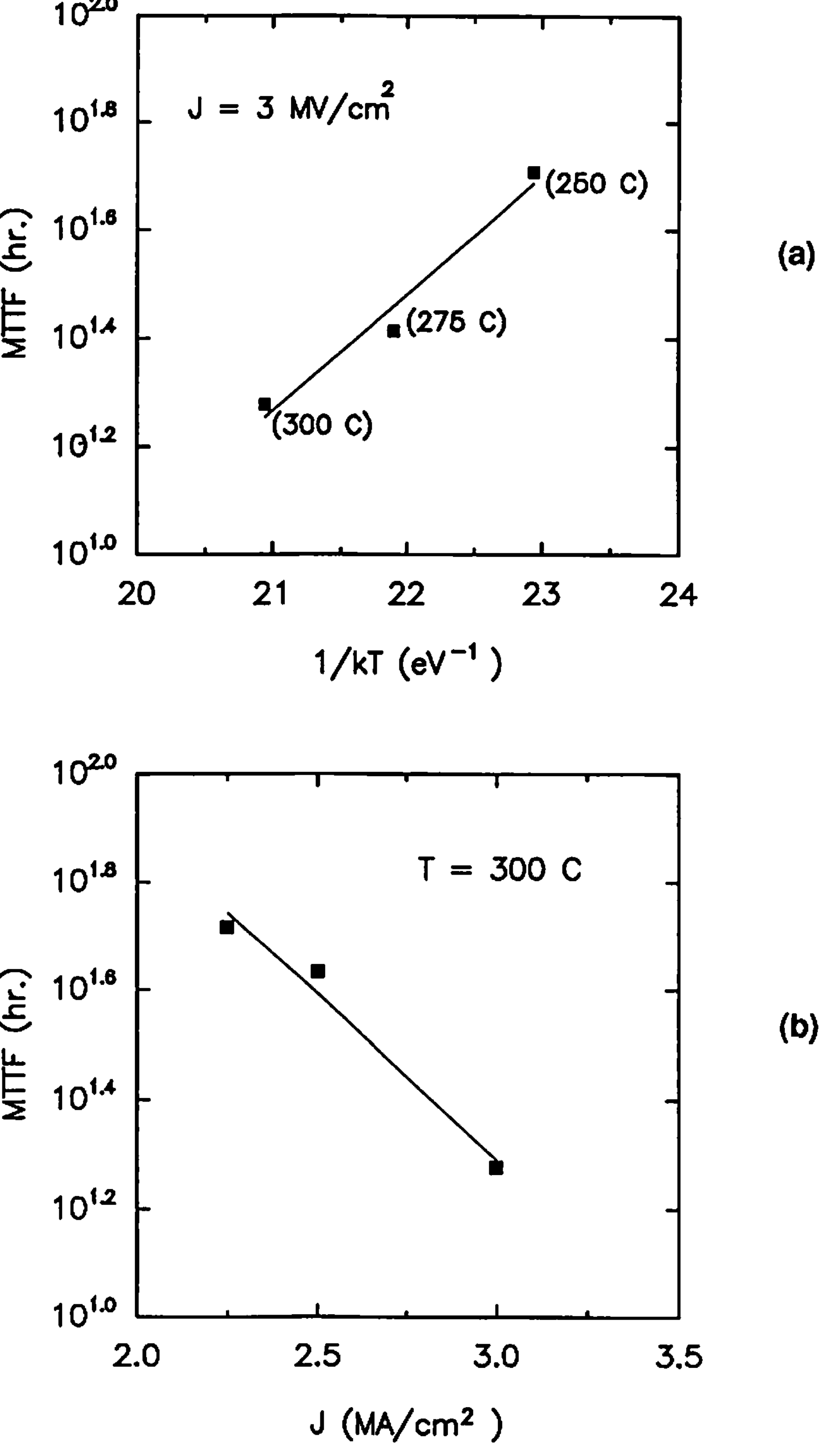


Fig. 3.15 Measured MTTF at various current stress conditions. The metal width is 2.4 μm. (a) Temperature dependency. (b) Current density dependency.

In order to reduce electromigration in the contact regions, it has become a common practice to use barrier materials in the form of refractory metal alloys [3.38]-[3.40]. Instead of experiencing precipitous open electromigration failures, the composite metal systems slowly degrade in the conductivity. The composite metal system usually includes refractory metals below the aluminum layer. Table 3.5 summarizes the extracted electromigration parameters for different types of metals according to (3.16). The functional dependence of the resistance degradation model can be expressed as,

$$R_t = f(R_i, P, t) \tag{3.17}$$

where R_t is the resistance at time t, R_i is the initial resistance value, power dissipation P is the product of terminal current and branch voltage. A resistometric method can be used to study electromigration for the reduction of test time [3.41]. Additional advantage is provided in this method to monitor progressive change in metal resistance instead of an absolute failure criterion based on open/short circuit. To monitor the gradual resistance change in interconnects using composite metals, the following model is also used in our software simulation according to a resistometric method:

$$\Delta R = \sum R_i \, \alpha \cdot J_{eff}^{\,n} \cdot \exp(-E_a/kT) \cdot \Delta t_j \tag{3.18}$$

where R_i is the initial resistance. Based on the characteristic of resistance degradation, the designers can incorporate the information into a design to improve the performance of an IC chip by using reliability simulation. Interconnection topology and widths can be modified to satisfy the reliability constraints inferred from circuit reliability simulation results.

Table 3.5 Electromigration parameters used in the assessment of composite metals. Failure criterion is set at $\Delta R/R = 20$ % [3.39][3.40].

Composite metal	Current density dependent parameter n	Activation energy Ea (eV)
Al-SI/W	2.1	0.46
Al-Cu/W	2.2	0.75
Al-Si/TiW	2.0	0.46
Al-Si/Ti/W	2.1	0.49

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Chapter 4

Integrated-Circuit Reliability Simulation

In a VLSI circuit, the amount of electrical stress received by each device is a complex function of the transistor location, terminal voltage/current magnitude, duty cycle, etc. A circuit may become inoperative due to the failure of some critical devices or interconnect wires. Computer-aided reliability analysis is essential in assessing circuit lifetime in the presence of stress-induced failures. In this chapter, the methodology for integrated-circuit reliability simulation is presented. The basic concept toward simulation of circuit degradation is described in Section 4.1. The organization of the IC reliability simulator, RELY, is presented in Section 4.2. In section 4.3, both the one-cycle and repetitive reliability simulation schemes are presented. A systematic approach to include dynamic stress effects by using an AC degradation factor is presented in Section 4.4. In section 4.5, the sensitivity analysis results are presented. In order to apply the computer-aided reliability simulation to a complete VLSI chip, a hierarchical reliability simulation environment is developed as described in Section 4.6. At the end of this chapter, the methods to simulate electromigration are presented in Section 4.7.

Based on the device degradation information, circuit-level simulation can be used to evaluate the impact of progressive device degradation due to common microelectronic failure mechanisms using a quasi-static approach [4.1]-[4.9]. The circuit reliability simulation tasks include (i) assessing individual device lifetime in circuit operation [4.1, 4.7, 4.8, 4.9], (ii) quick estimation of degraded circuit

performance [4.2, 4.3, 4.4, 4.6], and (iii) sensitivity analysis for circuit-reliability simulation [4.2, 4.4]. In addition, in order to account for different input patterns methods have also been reported such as the use of stochastic current waveform to predict metal electromigration [4.10] and and the combined Boolean and graph manipulation method to estimate power dissipation in combinational circuits by solving a weighted max-satisfiability problem [4.11].

4.1 Monitoring Stress and Degradation

When a transistor in a circuit is subjected to electrical stress, its output characteristic degrades accordingly. The degradation is described by the transistor parameter shifts. Each parameter shift during a period of time [0, T] is expressed as,

$$\Delta P_i = \int_0^T D_i(S(t))dt, \tag{4.1}$$

where ΔP_i is the change in the parameter P_i, D_i is the degradation function associated with parameter P_i, and S(t) is the stress function. For hot-carrier effects, S(t) is the normalized substrate current. The integration is carried out by trapezoidal summation as,

$$\Delta P_i = \sum_{k=1}^{n} D_i(S_k) \cdot \Delta t_k \, , \tag{4.2}$$

where $\Delta t_k = t_k - t_{k-1}$ and $t_n = T$. The effective stress S_k in each time interval, $[t_{k-1}, t_k]$, is determined by a weighted average,

$$S_k = \frac{S(t_{k-1}) + S(t_k)}{2} \, . \tag{4.3}$$

4.2. RELY: Integrated-Circuit Reliability Simulator

The flowchart of the RELY integrated-circuit reliability simulator is shown in Fig. 4.1. It consists of several major software modules including pre-processing modules, core circuit simulators, stress monitor modules, degradation modules, and post-processing modules.. The pre-processing module of the RELY simulator translates the user's input file into a format compatible with the core circuit simulator and stores the reliability information in the database. In the core circuit simulator, SPICE [4.12, 4.13] or HSPICE [4.14] analog circuit simulators are used for detailed analysis of small circuits and the mixed-mode simulator iSPLICE [4.15] can be used for timing verification of large circuits. Here, the core circuit simulator is used to determine terminal voltage and current waveforms. Stress monitor modules determine the corresponding electrical stresses according to various physical failure mechanisms such as hot-carrier damages, electromigration, oxide breakdown and radiation effects. Each degradation mechanism requires one monitoring module to calculate the amount of electrical and/or environmental stress. Based on the level of electrical stresses, the corresponding degradation within devices is determined in the degradation module. The post-processing module which provides X-window based graphic interface has also been developed to facilitate the understanding of transistor and circuit performance degradation. The whole simulation procedure mimics the in-use operation of integrated circuits. The C-language implementation of the RELY simulator contains around 4800 lines of code.

The simulation tool and technological support system for VLSI circuit reliability assessment is shown in Fig. 4.2. Reliability-parameter values are extracted

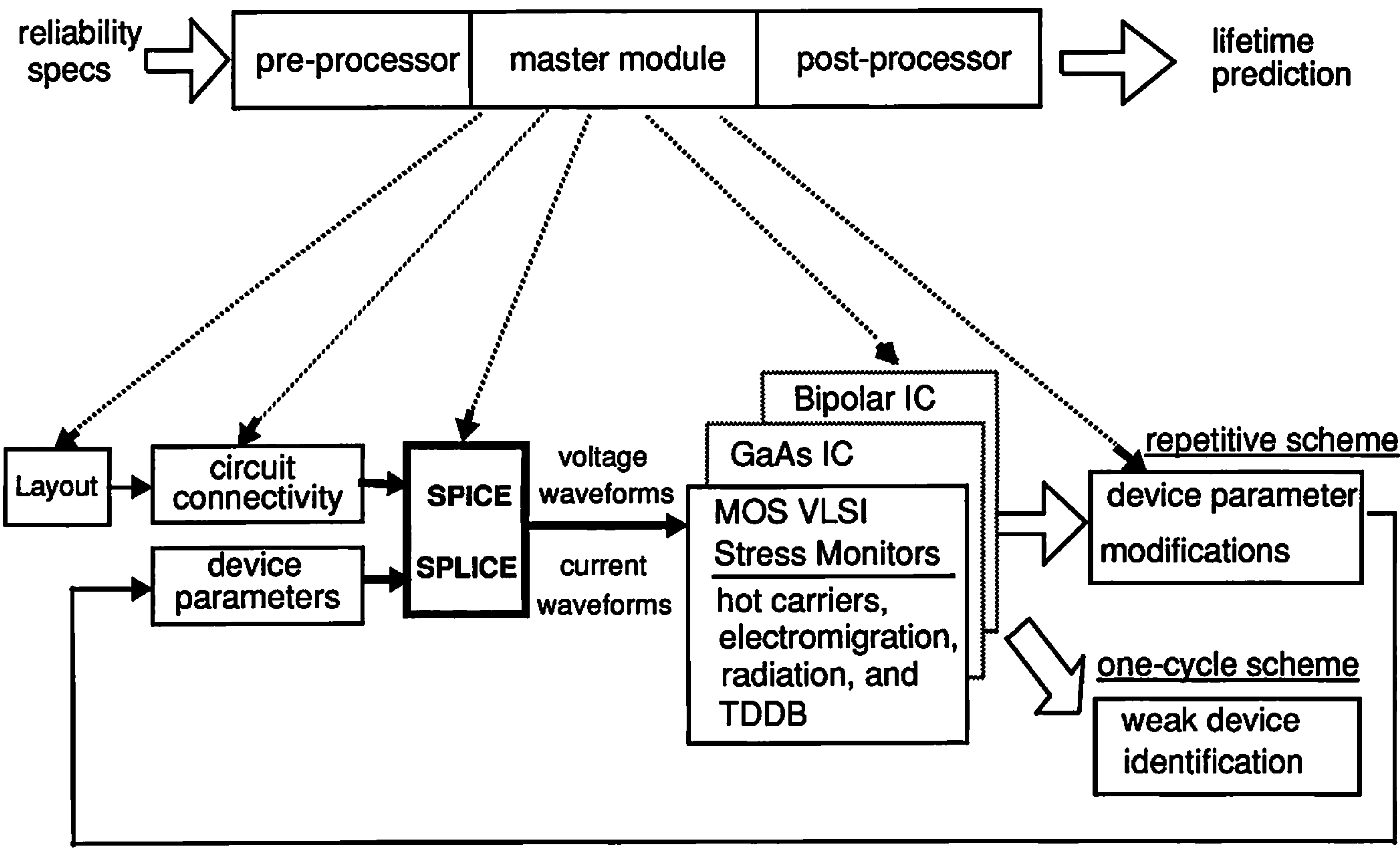


Fig. 4.1 Organization of the RELY circuit reliability simulator.

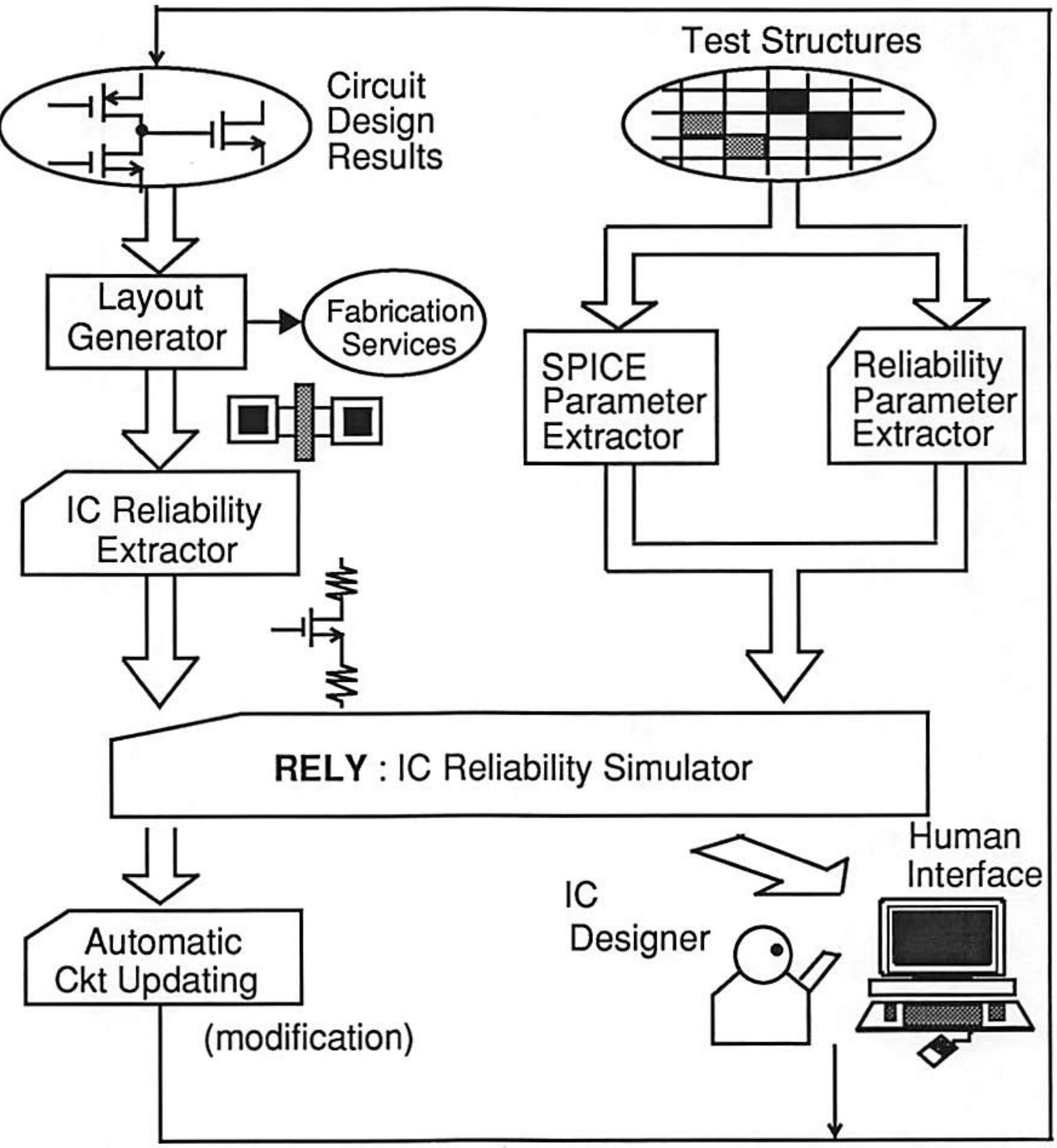


Fig. 4.2 Design of advanced integrated circuits using reliability simulation with transistor and reliability parameter extraction.

from measured output characteristics of stressed test structures. A general-purpose parameter extraction software such as SUXES [4.16, 4.17] or TECAP [4.18] can be extended for this task. The reliability parameter set is combined with the SPICE parameter set and sent to the core circuit simulator. The IC reliability simulator predicts long-term circuit behavior based on the design result and reliability parameter information. The simulation output can be interpreted by the VLSI designers for circuit topology modification and transistor sizing, or linked to physical-layout generators for automated layout modification. Weighted sum of the stress information is also available for identification of weak devices.

4.3. Simulation Schemes

In the organization of the RELY circuit simulator as shown in Fig. 4.1, there are two basic reliability simulation schemes: one-cycle simulation and repetitive simulation. Assume that the total life span of the circuit of interest is divided into N progressively larger intervals. The total amount of degradation is accumulated as,

$$\Delta P_{i,total} = \sum_{j=1}^{N} \Delta P_i(T_j). \tag{4.4}$$

The one-cycle simulation scheme, which was used in many other reported reliability analysis results [4.1, 4.8, 4.9], is a special case of the repetitive simulation scheme. In the one-cycle simulation, conventional circuit simulation is performed once and long-term IC reliability is predicted by using a large extrapolation ratio.

4.3.1 One-Cycle Simulation

In the one-cycle simulation approach, the stress information for a relatively short period of time is available based on one conventional circuit simulation run. This information is used for quick identification of weak devices. Transistor degradations are determined according to (4.2). In the one-cycle simulation method, the waveform of the stress is assumed to be unchanged throughout the life span of the chip and $\Delta P_{i,total}$ is rewritten as $N \cdot \Delta P_i$ which is a gross approximation of the actual amount of degradation. Prediction of the device lifetime is made by calculating the time taken to reach a preset maximum tolerable device parameter change. The impact of transistor degradation on circuit performance is then determined based on a single updating of the parameter set.

4.3.2 Repetitive Simulation

The repetitive simulation scheme is also supported in the RELY simulator where multiple simulation cycles are required. The reliability simulation scheme can closely mimic actual circuit operation in which bias conditions of a circuit are changing as wear-out proceeds in the devices. The operation time period of interest is divided into several intervals. The device parameter values are updated according to accumulative device degradation at the end of each time interval. This incorporates the effect of a gradual change in the node voltages and reliability monitor values. The degradation prediction information is available repetitively at each user-specified time point (T_1, ..., T_N). Figure 4.3 shows the flowchart of the repetitive reliability simulation scheme. For example, the cumulative degradation due to stress during the period of r cycles ($r \cdot T$) is,

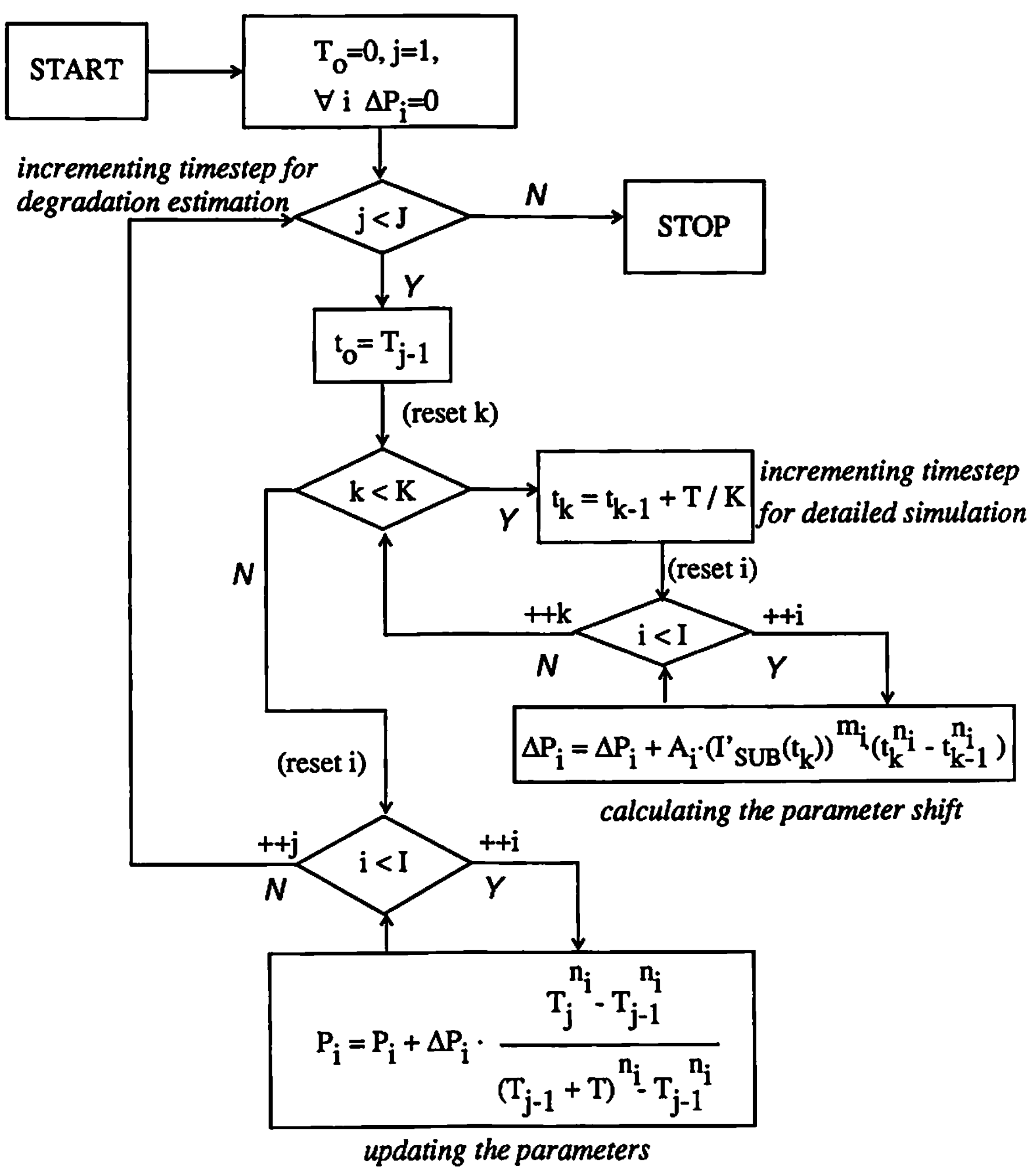


Fig. 4.3 Flowchart of the repetitive reliability simulation scheme.

$$\frac{\Delta P_i(r \cdot T)}{\Delta P_i(T)} = \left[\frac{r \cdot T}{T}\right]^{n_i}, \tag{4.5}$$

where n_i is extracted degradation parameter for the transistor parameter P_i.

The difference between one-cycle degradation simulation and repetitive simulation for devices in a two-input NAND-gate cell is shown in Fig. 4.4. In the one-cycle scheme, detailed simulation is done in one time interval and the degradation is extrapolated. In the repetitive simulation scheme, parameter updating and detailed simulation are done every 5 x 10^6 sec. Degradation of threshold voltage and carrier mobility are examined. Updating the bias conditions of the circuit in the repetitive simulation scheme causes the degradation rate of the threshold voltage to increase, but that of the carrier mobility to decrease. In both cases, however, a significant difference is observed between the one-cycle and repetitive simulation results.

4.3.3 Time-Dependent Degradation Rate

Trapped charges in the gate oxide produce a retarding force to reduce the amount of energetic carriers that breach across the semiconductor-oxide energy barrier. The device degradation rate is not a constant over the lifetime of the circuit. The degradation rate is high for the initial period of circuit operation. It then decreases as the retarding force is built up by the trapped charges.

A single set of degradation parameter values does not always give the best description of the overall circuit lifetime behavior. Hence, a multiple-set simulation method is proposed. As shown in Fig. 4.5, the reliability measurement is done and the degradation parameters are obtained for the first time period (0 to

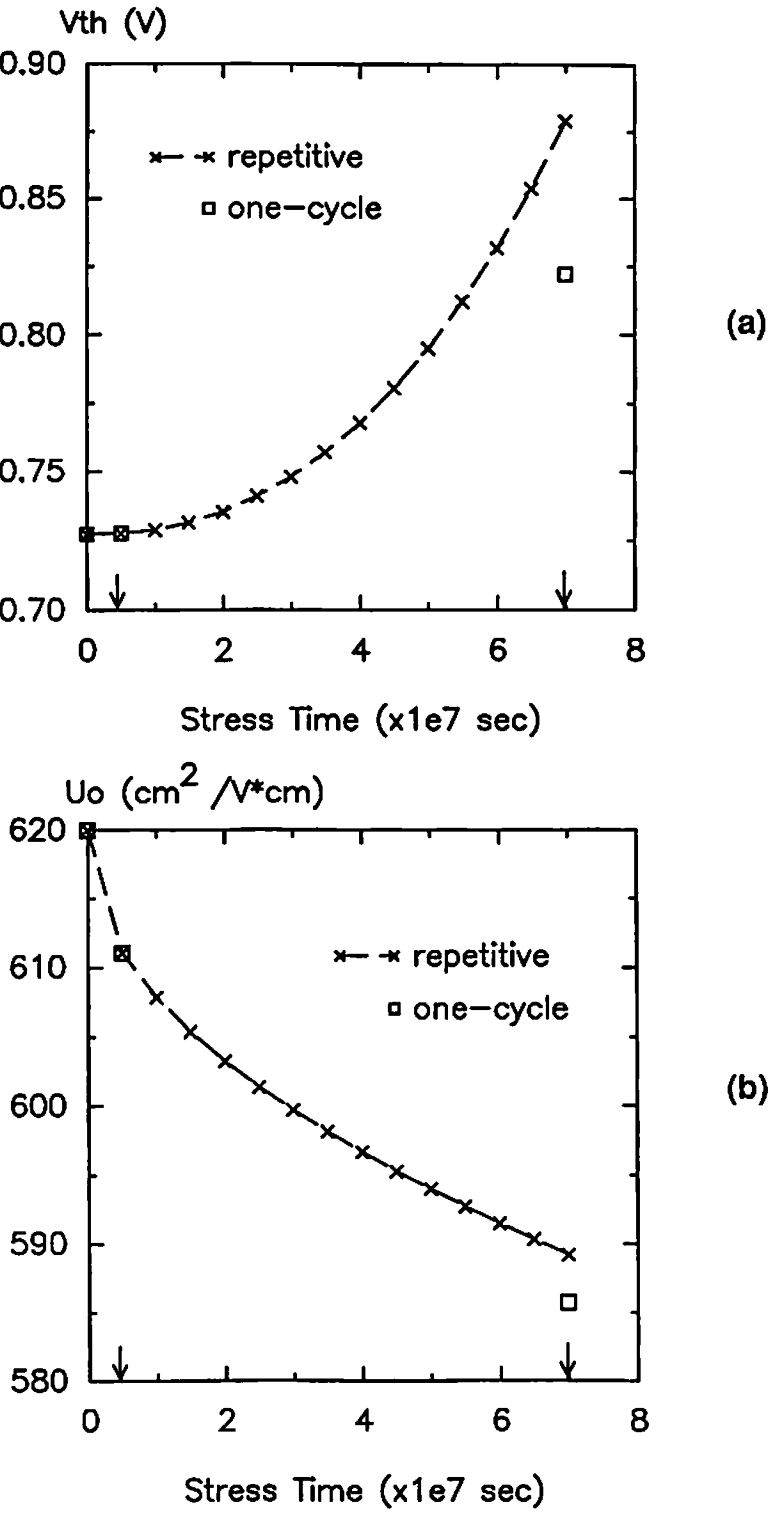


Fig. 4.4 Comparison of the one-cycle and repetitive simulation schemes for a two-input NAND-gate cell. (a) Threshold voltage. (b) Mobility.

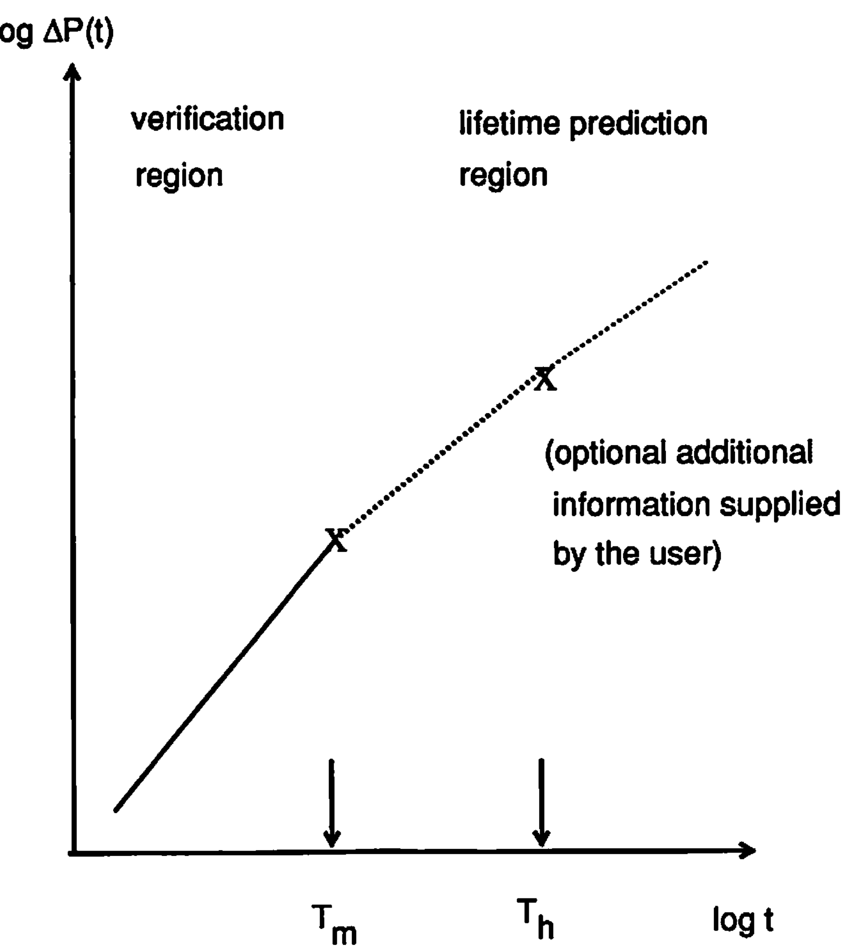


Fig. 4.5 Multiple-rate simulation over the lifetime of the circuit

T_m). Simulation of degradation over this range serves to confirm the degradation mechanism. The user can supply some additional degradation information based on a real product history to guide the simulation over the second period of time. A simple linear combination of the degradation rate at T_m (in the practical laboratory measurable region) and that at T_h (based on product history) is used here. Simulation according to this approach over the actual product operation range can predict the IC chip reliability more accurately.

4.4 Quasi-Static and Pulsed/AC Electrical Stresses

Early work in reliability prediction assumed that the transistors were subjected to static stress. This progressed to the assumption that the stress level changed slowly with time in response to the degradation of the transistors. During the normal operating conditions of a VLSI circuit, the inputs and outputs consist of constantly changing waveforms. This results in constantly changing AC stress waveforms on the individual transistors in the circuit. A systematic approach is needed to incorporate the AC stress waveforms into the degradation simulation in order to provide a closer imitation to actual circuit operation.

4.4.1 AC Stress Waveforms and The AC Degradation Factor

In the quasi-static simulation approach, transistor parameter shifts are correlated with the magnitude of the stress monitor using degradation parameters directly obtained from static stress experiments. During actual operation, circuits are subjected to AC stress waveforms rather than static stress. The degradation under the AC operating conditions is of great interest to the VLSI circuit

designers. Transistors subjected to AC stress waveforms are usually found to have excessive degradation when compared to the DC stress condition. In performing AC stressing measurements, careful design to minimize parasitic capacitive loading needs to be done to account for the large capacitive loading associated with probe pads. Transistors within a circuit will not have the large capacitive load as associated with pads. A list of published results comparing the AC and DC degradation effects on the transistor parameters with the effective values of the AC degradation factor [4.19], ΔP_{AC-DC}, is summarized in Table 3.4. This factor ΔP_{AC-DC} has been defined in (3.15). These experimental results are classified according to the types of drain and gate voltage waveforms. The factor ΔP_{AC-DC} value is determined according to the bias conditions under which AC stress is performed. In the single pulse mode either the drain or the gate terminal voltage is held constant. Hence, there are two distinct stress conditions:

. the gate-to-source voltage is kept constant while the drain-to-source voltage is pulsed, and

. the drain-to-source voltage is kept constant while the gate-to-source voltage is pulsed.

In the dual pulse mode, both the drain and the gate voltages are pulsed. There are four distinct stress conditions:

. complete overlap of both pulse streams,

. partial overlap of both pulse streams with leading drain pulse,

. partial overlap of both pulse streams with leading gate pulse, and

. both pulses overlap only at the edges.

Each of these conditions mimics the normal operating conditions of some circuit. Table 4.1 lists the correlation between the bias conditions in the stress experiments and the circuit operating conditions. Measured data described in Chapter 3 for both static and dynamic stresses are used to obtain the degradation factor ΔP_{AC-DC} value for the results described in the previous section.

4.4.2 DC Degradation Monitor for Transient Analysis

The DC stress experiment is used to characterize the degradation rate while the AC stressing experiment is used to obtain the AC degradation factor. So far, the DC substrate current is used as the degradation monitor for most laboratory experiments. Accuracy in simulation is ensured by careful correlation of simulated substrate currents with measured DC stress data. In circuit simulation, the unwanted capacitive components of the drain current in transient analysis can be significantly large, especially during fast rising and falling edges of voltage waveforms. In the case of hot-carrier effects, the DC substrate current is calculated in a two-pass procedure by the circuit simulator SPICE to accurately determine the corresponding degradation. In the first pass, simulation of the actual circuit operation including all transient components is performed. Node voltages are extracted in this step. In the second pass, the terminal voltage information is used to determine the corresponding DC drain current components through the DC analysis of the SPICE simulator. The DC drain current values from this simulation are used to calculate the substrate current at the end of this step. In this scheme, the correct DC stress monitor is determined. Figure 4.6 shows the flowchart of the two-pass simulation procedure to determine the DC component

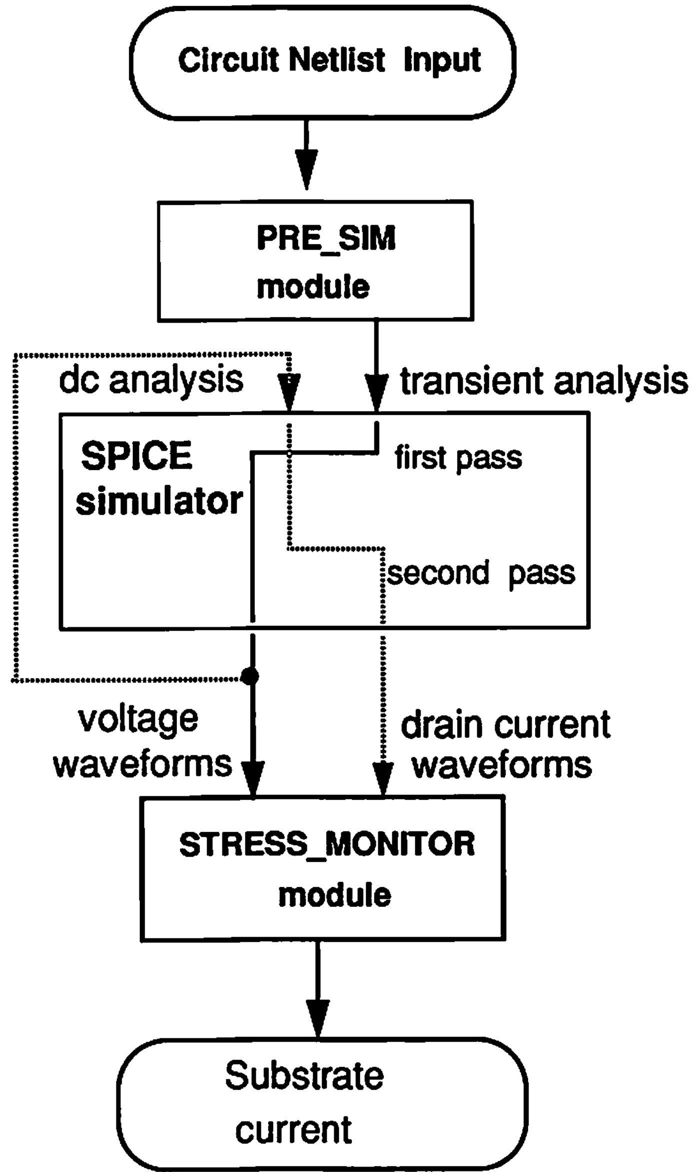


Fig. 4.6 Two-pass reliability simulation procedure to determine the proper DC degrdation monitor.

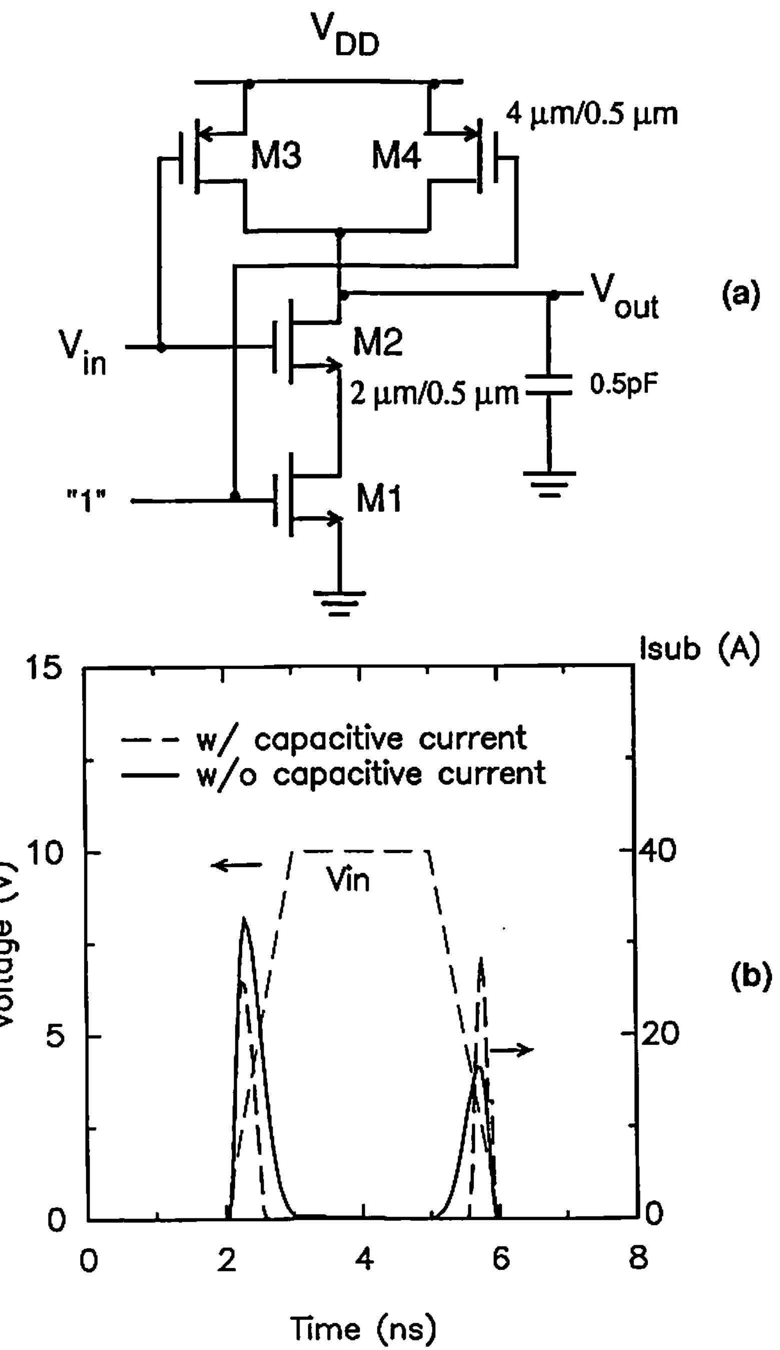


Fig. 4.7 Comparison of substrate currents for transistor M2 in a two-input NAND gate cell with and without capacitive current component.
(a) Circuit schematic.
(b) Simulated substrate current characterisitics.

of the substrate current in a transient circuit simulation. The schematic of a two-input NAND gate cell is shown in Fig. 4.7. A significant substrate current is observed in transistor M2 during the rising edge of V_{in} for a high value of the gate bias at transistor M1. Figure 4.7(b) shows substrate current calculation results for a NAND gate cell. After removing the capacitive component of the drain current, significantly less substrate current is obtained at the falling edge of V_{in}, while the substrate current is higher at the rising edge. Degradation in transistor in transistor M2 is lower than that predicted with the total transient substrate current.

4.4.3 Degradation Prediction

A detailed flowchart that describes the complete simulation procedure for AC stress conditions is shown Fig. 4.8. To incorporate the AC degradation information into the quasi-static reliability simulation scheme, the degradation factor ΔP_{AC-DC} is used. Dynamic gate-to-source and drain-to-source voltages for various transistors in the circuit are analyzed and classified according to the type of stress conditions listed in Table 3.4. The shape parameters of stress waveforms including rise/fall time, frequency, and drain-high time are also calculated and used to classify the circuit for the computation of AC-induced degradation. A group of representative analog and digital circuits classified according to different types of AC stress conditions are selectively listed in Table 4.1. For example, transistors in the CMOS inverter or the buffer chain are subjected to drain and gate pulses that overlap only at the edges as in class G. Diode-connected transistors, on the other hand, are subjected to completely overlapping

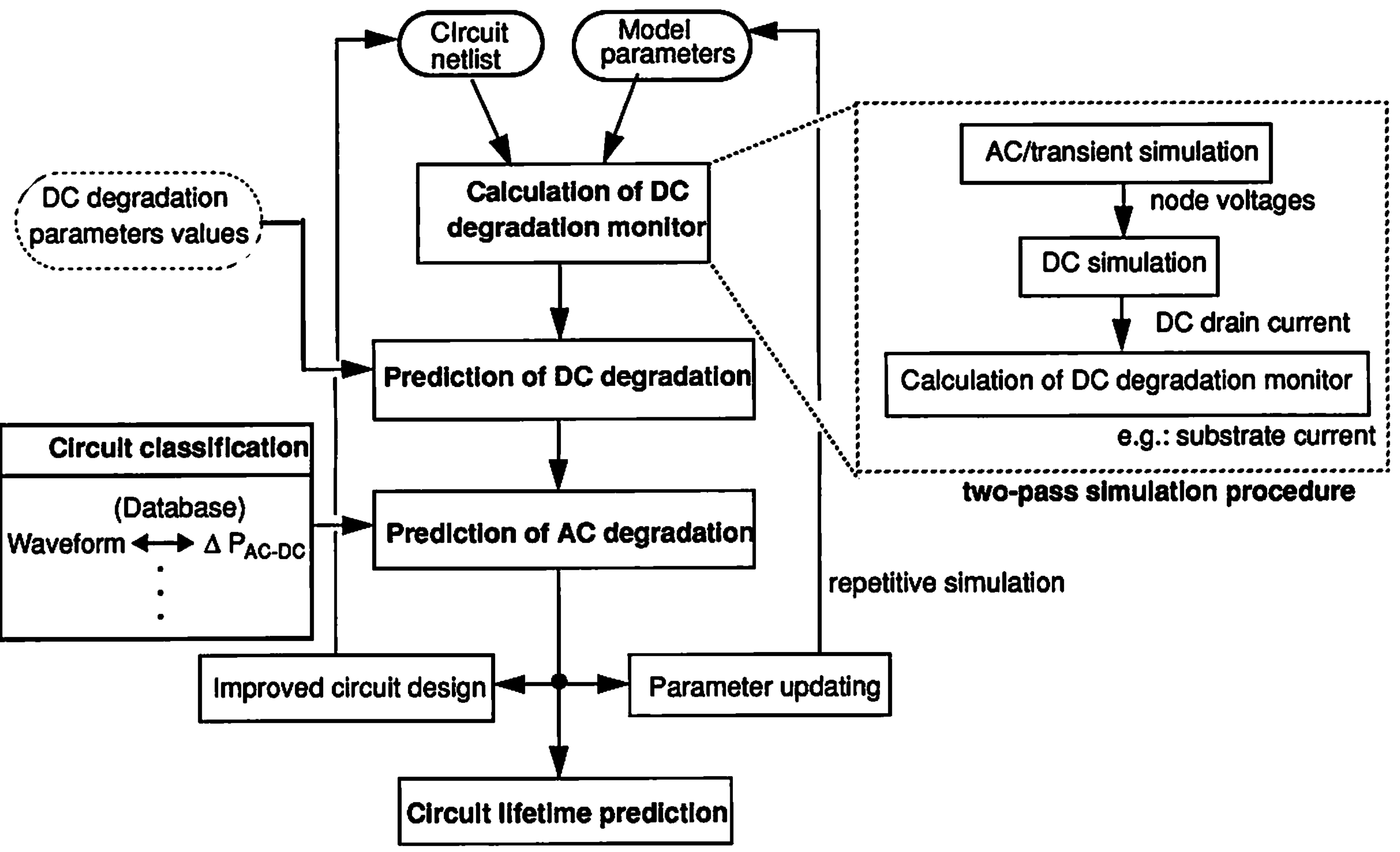


Fig. 4.8 Flowchart of reliability simulation including AC stress effects.

Table 4.1 Types of voltage stress waveforms in CMOS application circuits with typical values of the AC degradation factor.

Type of stress	Class ID	Stress condition		Representative circuit example	$\Delta P_{AC\text{-}DC}$	
		Pulse type	waveform		typ.	max.
constant voltage	A	static Vds, static Vgs	Vds Vgs	fully DC stress	1	1
single pulse	B	static Vds, pulsed Vgs		pass transistors in a 6-transistor SRAM cell	2.0	3.5
	C	static Vgs, pulsed Vds		op-amp (unity-gain buffer) ROM charge-sharing sense amp.	1.1	1.5
dual pulses	D	complete overlap		diode-connnected transistor	1.2	5.0
	E	partial overlap with leading Vgs		BiCMOS SRAM cell(pull down trans.,"0" write)	4.0	5.0
	F	partial overlap with leading Vds		DRAM cell (one-transistor, "1" read) ROM charge-sharing sense amp.	1.3	3.0
	G	edge-overlapping Vds, Vgs		inverter chain DRAM cell (one-transistor, "0" read) DRAM precharging circuit	2.0	4.0

drain and gate pulses as in class D. Pass transistors in an SRAM cell are subjected to constant drain-to-source voltage and pulsed gate-to-source voltage as in class B. Similarly, the voltage waveforms during the operation of different memory cells and digital processing circuitry can be classified according to the seven stress conditions listed in Table 4.1. The corresponding typical values of the AC degradation factor are also listed in Table 4.1. To begin the simulation procedure, the two-pass simulation is performed and the DC stress monitor is obtained. Based on the classification of the waveform, the appropriate value for the degradation factor ΔP_{AC-DC} is retrieved from the database which should be established for each fabrication technology. In combination with degradation parameters for the technology, the effective amount of AC degradation is then calculated with the inclusion of this factor. The whole simulation process accurately predicts the transistor degradation characteristics under AC stress conditions.

There are two different schemes for updating the transistor parameters in circuit simulation under AC stress conditions. To simplify data storage and parameter extraction tasks, an averaged AC degradation factor can be used for all the transistor parameters. Such a global multiplicative factor gives the circuit designer a simple and efficient way to include the AC degradation effect in predicting the circuit lifetime. For greater accuracy, each transistor parameter could require a different AC degradation factor. Such a simulation scheme would have increased the extraction and data storage cost.

4.5 Sensitivity Analysis

Circuit-performance degradation due to stress is not solely determined by the amount of stress received in devices. The effect of the degradation of each device on the performance of the whole circuit must also be considered. A sensitivity function of variable Q with respect to variable P can be expressed as,

$$S_{Q|P} = \frac{(\partial Q/\partial P)}{(Q/P)}. \tag{4.6}$$

Sensitivity of circuit performance to electrical stress can be described by three items:

- sensitivity of circuit performance to device characteristics,
- degradation of device characteristics as a function of stress, and
- stress received by each device.

All of these components are taken into account by describing the total performance degradation as the summation of total contribution from all devices, namely

$$\Delta\Phi = \sum_j \left[\frac{\partial \Phi}{\partial P_i}\right]_j \cdot \left[\frac{\partial P_i}{\partial S}\right]_j \cdot \left[S\right]_j, \tag{4.7}$$

where j signifies different devices, Φ is the circuit performance, P_i is the device parameter, and S is the stress received by the device. The performance-to-parameter sensitivity is intrinsically included during numerical matrix solving procedure in a common circuit simulator. Typical circuit performance measures include delay time, rise and fall time, voltage gain etc. The conventional approach of grossly setting a critical level of stress in an indicator such as setting the normalized substrate current level larger than 50 μA may overestimate

Table 4.2 SPICE Level-2 model sensitivity analysis results from a 1.2 μm technology.

Model Parameter	Drain Current Sensitivity $S_{IDS, P}$	Model Parameter	Output Conduc. Sensitivity $S_{gd, P}$
TOX	- 0.717	LD	0.999
VTO	- 0.644	LAMBDA	0.973
UO	0.605	TOX	- 0.877
LD	0.527	VMAX	0.613
VMAX	0.272	VTO	- 0.464
UEXP	- 0.172	UO	0.362
PHI	0.083	GAMMA	0.268
GAMMA	- 0.078	XJ	0.182
LAMBDA	0.068	NSUB	- 0.150
NSUB	- 0.056	UEXP	- 0.113
UCRIT	0.052	PHI	0.088
XJ	0.049	UCRIT	0.025
NFS	0.001	DELTA	- 0.001
DELTA	0.001	NFS	0.001
NEFF	< 0.001	NEFF	< 0.001

Table 4.3 BSIM sensitivity analysis results from a 0.8 μm process.

Model Parameter	Drain Current Sensitivity $S^{I_{DS}}_{P}$	Model Parameter	Output Conduc. Sensitivity $S^{g_d}_{P}$
T_{OX}	- 0.839	μ_S	4.765
k_1	- 0.723	μ_Z	- 3.911
μ_S	0.701	T_{OX}	- 0.909
Φ_S	- 0.625	η_0	0.836
U_{0Z}	- 0.535	U_{0Z}	- 0.765
V_{FB}	0.459	U_{1Z}	- 0.372
μ_Z	0.390	η_B	0.278
k_2	0.260	k_1	- 0.080
η_0	0.178	U_{1D}	0.079
U_{1Z}	- 0.171	Φ_S	0.075
η_B	0.073	μ_{SB}	- 0.073
μ_{SB}	- 0.013	V_{FB}	- 0.046
U_{1B}	- 0.011	μ_{ZB}	0.035
μ_{ZB}	- 0.004	k_2	- 0.028
U_{1D}	- 0.003	U_{1B}	- 0.025
U_{0B}	- 0.001	η_D	0.006
η_D	< 0.001	U_{0B}	- 0.002
μ_{SD}	< 0.001	μ_{SD}	< 0.001

the importance of one device while it may also underestimate the significance of other devices. The normalization factor is the transistor geometric aspect ratio.

The performance-to-parameter sensitivity gives rise to a set of critical parameters. The circuit response time which is a performance characteristic is determined by the current driving capability. Table 4.2 lists the drain current and output conductance sensitivity analysis results with the SPICE LEVEL-2 model from a 1.2-μm fabrication technology. For the circuit-level consideration such as the drain current and output conductance, most sensitive parameters are TOX (oxide thickness), UO (mobility), GAMMA (body effect coefficient), VTO (threshold voltage), LD (channel length reduction), LAMBDA (channel length modulation), and VMAX (saturation velocity). Table 4.3 lists sensitivity analysis results for the SPICE BSIM, Level-4 MOS model, for a 0.8-μm fabrication technology. The critical parameter set includes k_1, μ_s, T_{ox}, Φ_s, and V_{FB}. The simulation task is reduced by nearly 40% when both performance-to-parameter sensitivity and parameter-to-stress sensitivity are considered as described in (4.7). The sensitivity calculation is embedded in the extracted reliability parameter set and the simulation process. It doesn't require extra effort to account for sensitivity analysis results.

4.6 A Hierarchical Reliability Simulation Environment

The framework of a hierarchical reliability simulation environment shown in Fig. 4.9 exploits the hierarchy in the design of a VLSI chip. Both the top-down and the bottom-up approaches may be used to exploit this hierarchy in reliability prediction. At any level of the hierarchy, the critical components that influence

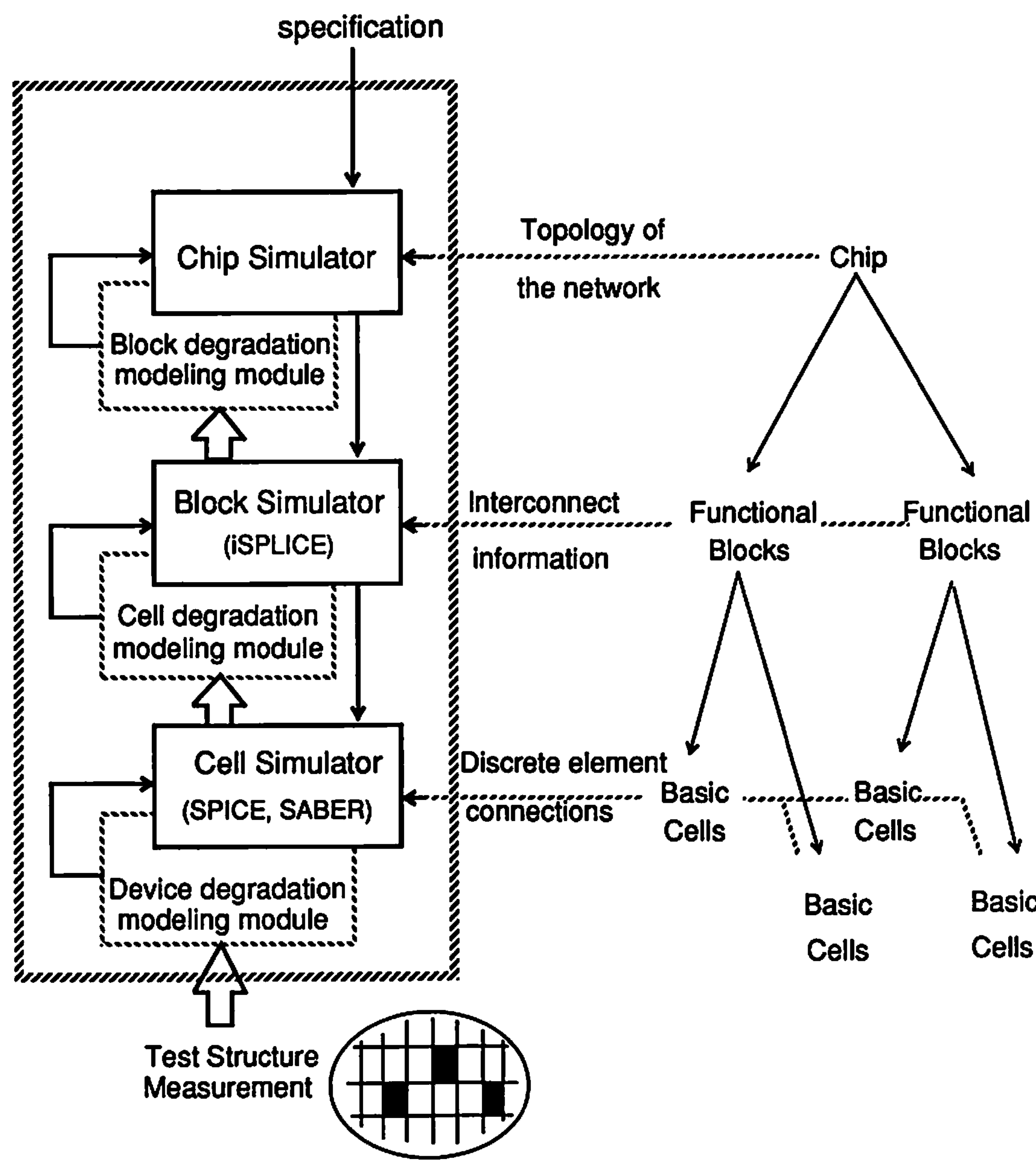


Fig. 4.9 Framework of a hierarchical reliability simulation environment.

the reliability of the module under consideration at that level are identified. To accomplish the complete design verification from transistor geometry specification to choice of system architecture, specialized simulators exist at each level. In ascending the hierarchy, the data at each design level is represented in more abstract forms. The abstraction of data results in a reduction in the complexity of simulation.

4.6.1 Circuit-Cell Level Reliability Simulation

At the lowest level of the hierarchical simulation environment, the degradation is represented in terms of the change in the transistor parameters. Performance change of analog cells and digital building blocks as a function of the usage time is calculated by the detailed transistor-level circuit simulation. For an operational amplifier, the important output characteristics include the DC voltage gain, unity-gain frequency, settling time, etc. Failure mechanisms are monitored by observing physical quantities in the circuit. For example, the substrate current is used to predict the hot-carrier effects. In a reliability simulation environment, modeling studies of both the stress monitor and the actual degradation function are required.

The organization of the circuit-cell level reliability simulation modules is described in Section 4.2. The whole simulation procedure mimics the in-use operation of integrated circuits. The reliability simulation output which contains information about stress levels and weak devices can be interpreted by the VLSI designer for topology and transistor-geometry modifications.

With the increasing importance of reliability assurance, IC databooks also need to specify the degradation information of these performance characteristics. In [4.20], for example, the maximum input offset voltage drift has been specified as 0.1 μV/Month for a particular programmable low-power operational amplifier. The circuit-cell level reliability simulation module provides prediction of cell performance drift due to physical wear-out processes. The information can be utilized to predict the performance of a more complex component in the next simulation level.

4.6.2 Circuit-Block Level Reliability Simulation

The cell performance degradation prediction that was obtained at the detailed transistor level is used here in conjunction with circuit-cell macro-models to predict the reliability of circuit-block level circuits. Mixed-mode simulators use analog and digital macro-models to simulate circuits containing several analog cells such as operational amplifiers and digital building blocks such as adders and multipliers. In the physical-layout design, such modules may exist in standard-cell libraries and can be called as required.

With the assistance of detailed layout and circuit performance information of modules in standard-cell libraries, block-level circuit performance degradation can be assessed based on cell degradation information available in the database through hierarchical reliability simulation. Hence for the circuit-block that has been designed, the fresh circuit performance and the degraded performance after some period of operation may be obtained by computer simulation. The organization of the simulator at this level is similar to that shown in Fig. 4.1.

The hierarchy at this level may be demonstrated using the example of an 8th-order switched-capacitor filter. Such a filter may be designed using standard-cell operational amplifiers. Degradation in the gain and bandwidth of an operational amplifier integrated circuit will affect the center frequency and pass-band of the 8th-order switched-capacitor filter designed using the op-amp module. The degradation in the characteristics of the filter is stored in the data-base along with its fresh performance characteristics and used in the next level of the hierarchy to predict the reliability of a complete IC chip.

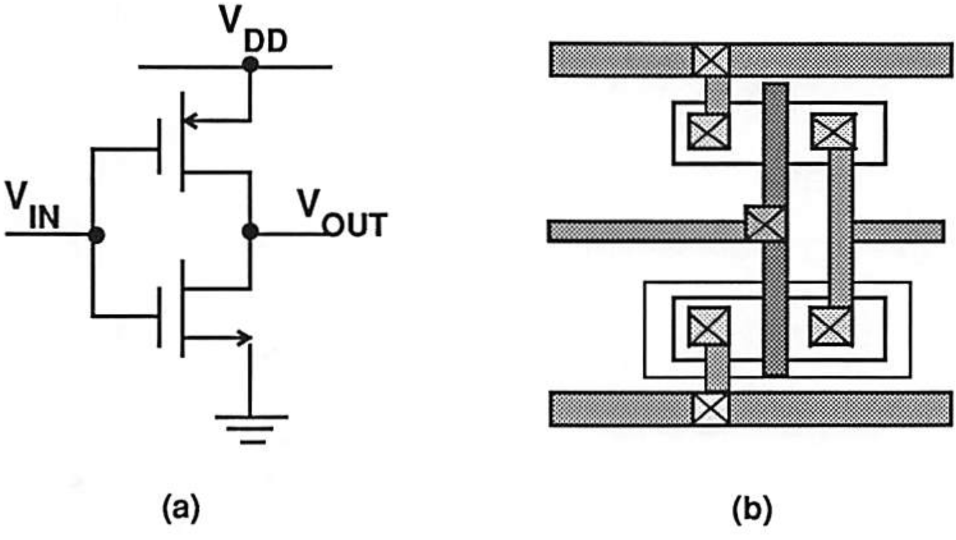
4.6.3 Chip Level Reliability Simulation

Both fresh and the degraded performances of the circuit blocks are available for the chip-level reliability simulation in the design database. Several of these circuit-blocks can be called from the library and assembled to synthesize a signal processing chip. An example is a modem chip that uses the 8th-order filter mentioned earlier. The performance of the modem chip degrades because of the change of the filter's center frequency and pass-band characteristics. The degraded performance of the modem chip after some period of operation time is obtained from the simulation and entered into the data book. The VLSI system designer can make use of the chip-level reliability prediction in order to estimate the lifetime of an electronic system.

A hierarchical reliability simulation environment is envisioned where the vertical flow of reliability information serves to link system-level requirements with technological information. Such an environment is essential in successful analog/digital design for the development of reliable VLSI computing systems.

4.7 Reliability Simulation of Electromigration

Circuit-level reliability simulation can provide valuable information for VLSI designers to improve the lifetime of the metal network. Electromigration in the metal interconnection of an IC chip can cause excessive voltage drop and even leads to open/short-circuited failures. In the RELY simulator, metal lines are represented by the resistive elements to monitor electromigration. Circuit extraction can be done through an enhanced layout extraction procedure. Figure 4.10 shows the electromigration modeling for a CMOS inverter. Resistive elements are used to monitor the branch current density through metal interconnects of interest. The flowchart of such an electromigration-based reliability simulation system is shown in Fig. 4.11. The layout of a user's design is first parsed to produce circuit-level representation of interconnects and metal contacts. In an accurate timing simulation, capacitive representation of the interconnects is included. For simulation efficiency on electromigration, resistive representation is used in the implementation. Electromigration parameters are extracted from measured characteristics of stressed test structures. Burn-in experiments on packaged devices or wafer-scale tests with on-chip heating circuitry can be performed at an elevated temperature. Effective metal temperature is determined by the temperature mapping based on power consumption density and thermal response of the substrate. Based on the electromigration simulation results, warning flags are assigned to the weak interconnects that need further modifications. The top-down simulation approach starts from the chip level. The global interconnect wires to link subcircuits for the complete chip can be represented in a resistive network with current loading information from each subcircuit as shown in Fig.



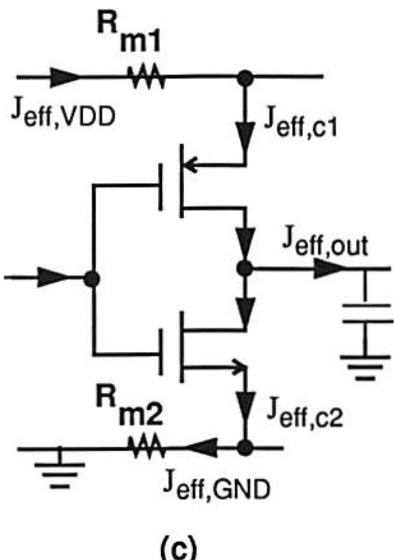


Fig. 4.10 Representation of electromigration for reliability simulation.
(a) Circuit design result.
(b) Physical layout.
(c) Circuit reliability representation.

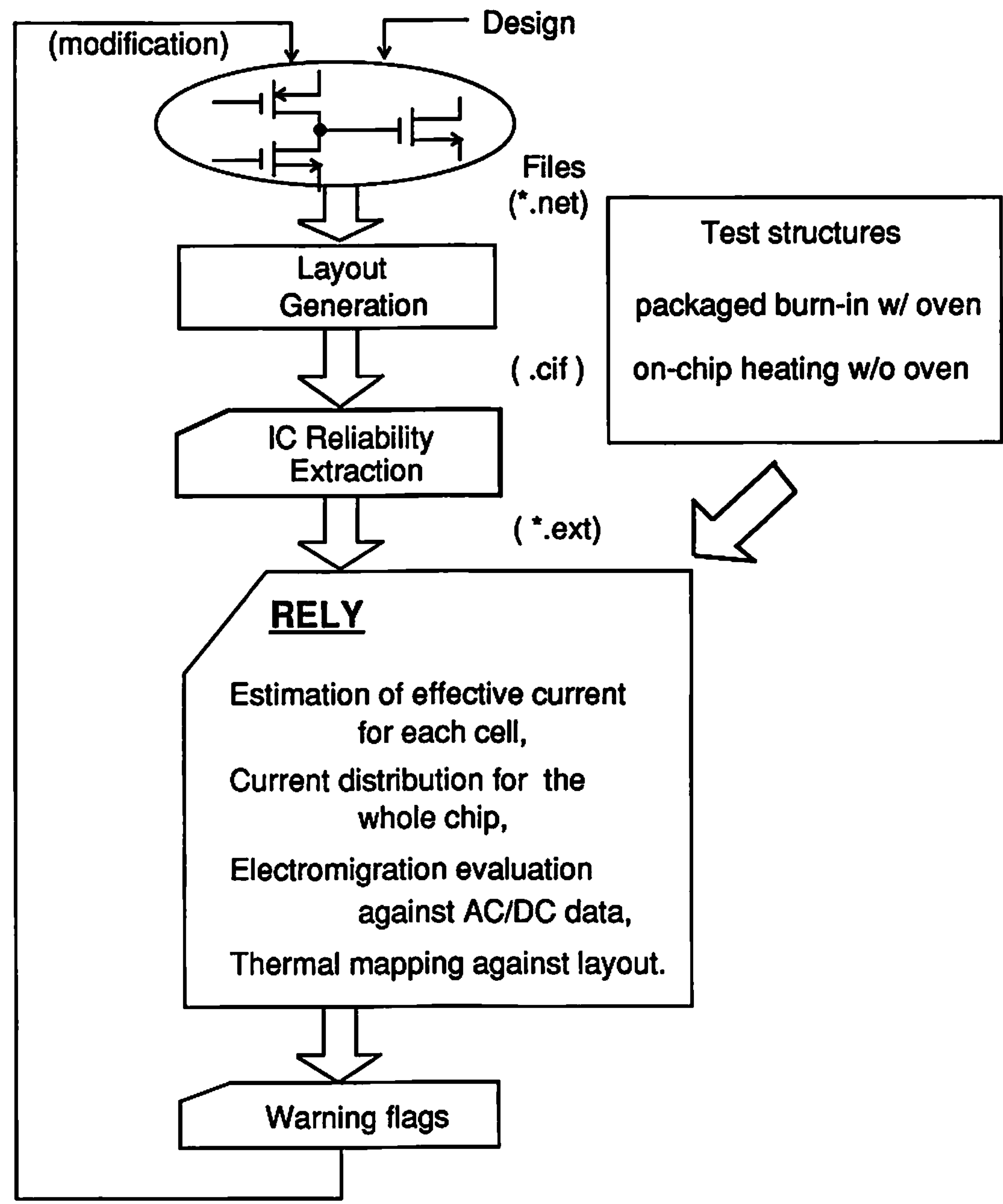


Fig. 4.11 Flowchart of reliability simulation of electromigration.

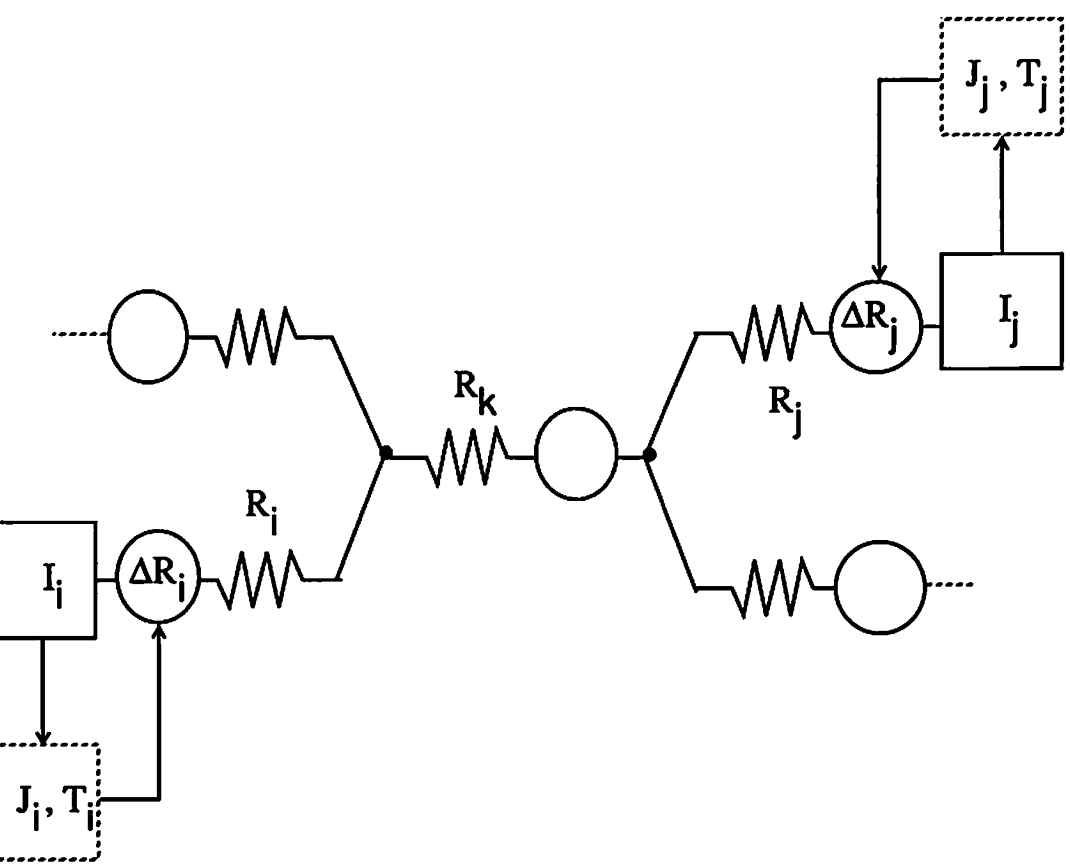


Fig. 4.12 Reliability characteristics of the metal/contact resistive network can be described by distributed current density and temperature information.

4.12. Power consumption and current loading information for subcircuits are characterized by detailed simulation. With this top-down simulation scheme, high simulation efficiency for a large circuit can be achieved.

The one-cycle and repetitive reliability simulation schemes described earlier are supported for electromigration prediction. In the one-cycle reliability simulation scheme, current density waveforms of each interconnect and metal contact are calculated in one transient simulation cycle. Prediction of electromigration effects is performed based on the average current density. The effective current density is to be averaged over the interested time period including the probabilistic distribution of possible input waveforms. In the repetitive reliability simulation scheme, multiple simulation cycles are used. The repetitive method is more applicable to composite-metal wires in which the resistance changes gradually as a function of time. The resistance values are updated at the end of each cycle.

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Chapter 5

Integrated-Circuit Reliability Simulation Using the RELY Program

This chapter describes the operating procedure of the RELY circuit reliability simulator and the experimental results of representative circuit examples. A description of the software, installation notes for the program, and a summary of commands are presented in Section 5.1. In Section 5.2, experimental results on both digital and analog computing circuits using an industrial 0.5 μm and 0.8 μm fabrication technologies are presented. A summary of program structures of the RELY simulator is presented in Appendix E. Examples of input files and typical model parameters are included in the Appendices F and G.

5.1 Software Configuration

The organization of the major software modules is briefly described in Chapter 4. Figure 5.1 shows the data structure along with the flow of the program control of the RELY simulator. The user provides an input file which contains the circuit description, the analysis under which the substrate current or branch current is to be monitored, the names of the device elements of interest and the corresponding device and reliability parameters. The pre-processing module translates the user's input file into a format compatible with the core circuit simulator and stores the reliability information in the database. The corresponding stress representation for devices is also stored in the database. The layout parser can be used to process the circuit layout to generate the corresponding netlist input. The RELY program calls upon the core circuit

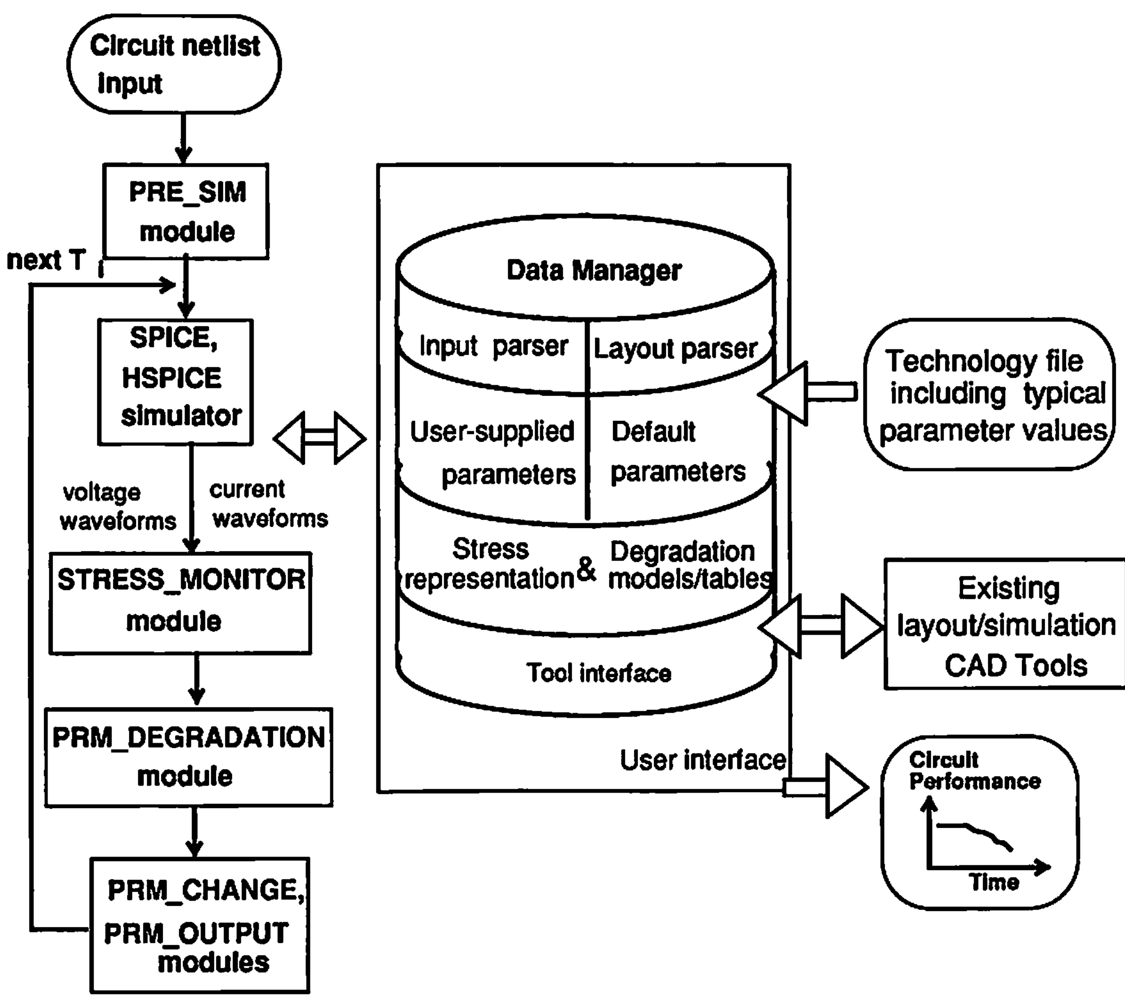


Fig. 5.1 Data structures and the program control used in the RELY simulator.

simulators such as SPICE [5.1] or HSPICE [5.2] for detailed circuit simulation. The circuit simulator is used to determine terminal voltage and current waveforms. Stress monitor modules determine the corresponding electrical stresses for various physical failure mechanisms such as hot-carrier damages and electromigration. Degradation within devices is then determined in the degradation module based on the stress level. Updated parameters are stored in the database for simulation in the next time period in the repetitive simulation scheme. Updated parameter sets at each user-specified time point are also stored in the database. The post-processing modules facilitate long-term circuit performance prediction based on the updated parameter sets. Communication link with new simulation tools is made easy by the modular implementation in the RELY simulator. Detailed program structure is summarized in Appendix E.

5.1.1 Parameter Extraction and Measurements

A computer-automated measurement system as shown in Fig. 5.2 has been established to facilitate stressing experiments. An H.-P. desk-top computer functions as the measurement system controller. Both DC and AC electrical stresses can be conducted. The extracted stress and degradation information is transmitted to the SUN workstation for circuit reliability simulation.

Test structures were fabricated by the MOSIS Service of USC/Information Sciences Institute [5.3], by Hewlett-Packard Corp., and by TRW, Inc. The layout of specially designed test structures including N-channel and P-channel transistors, metal stripes and metal contacts, and thin-oxide capacitors, is shown in Fig. 5.3 [5.4]. For hot-carrier effects, model parameter degradation

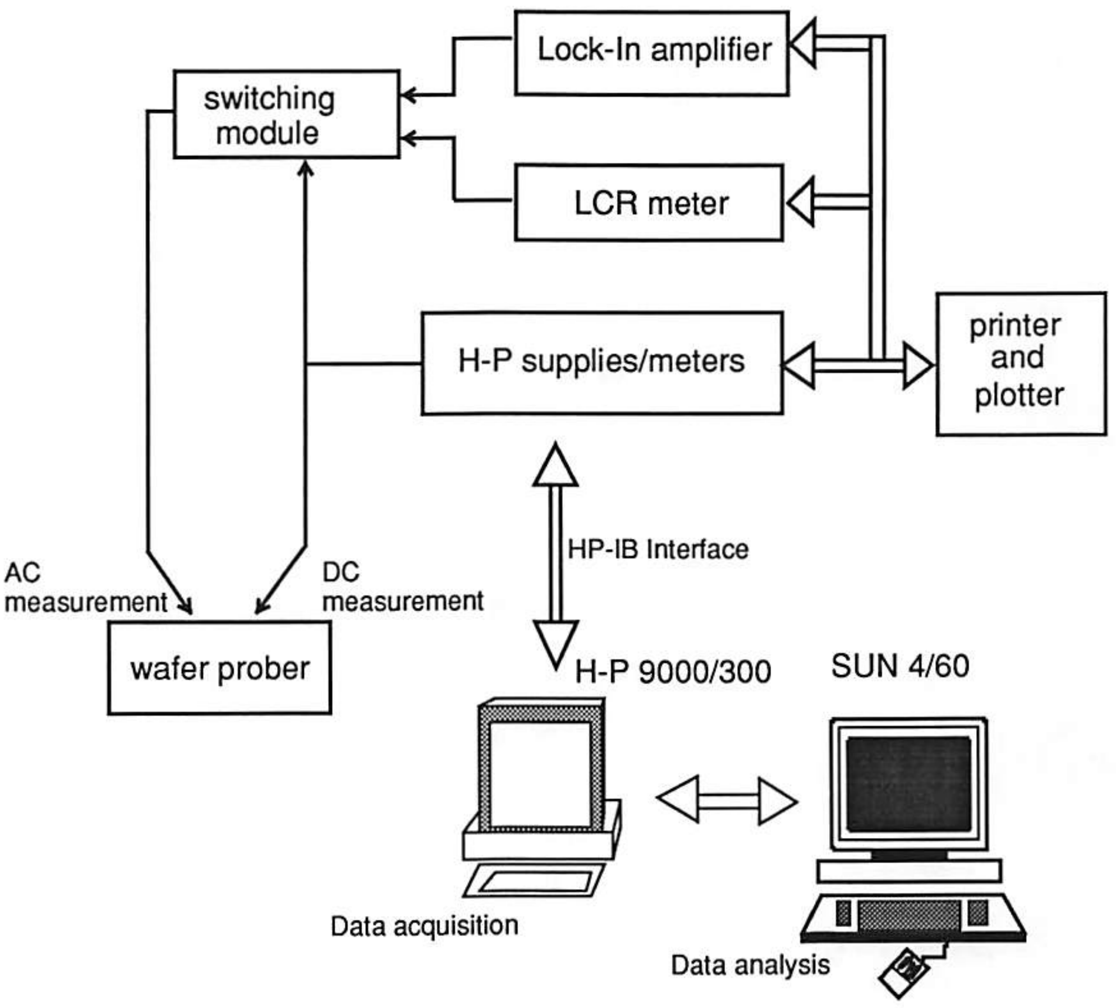


Fig. 5.2 Computer-automated measurement system for reliability parameter extraction.

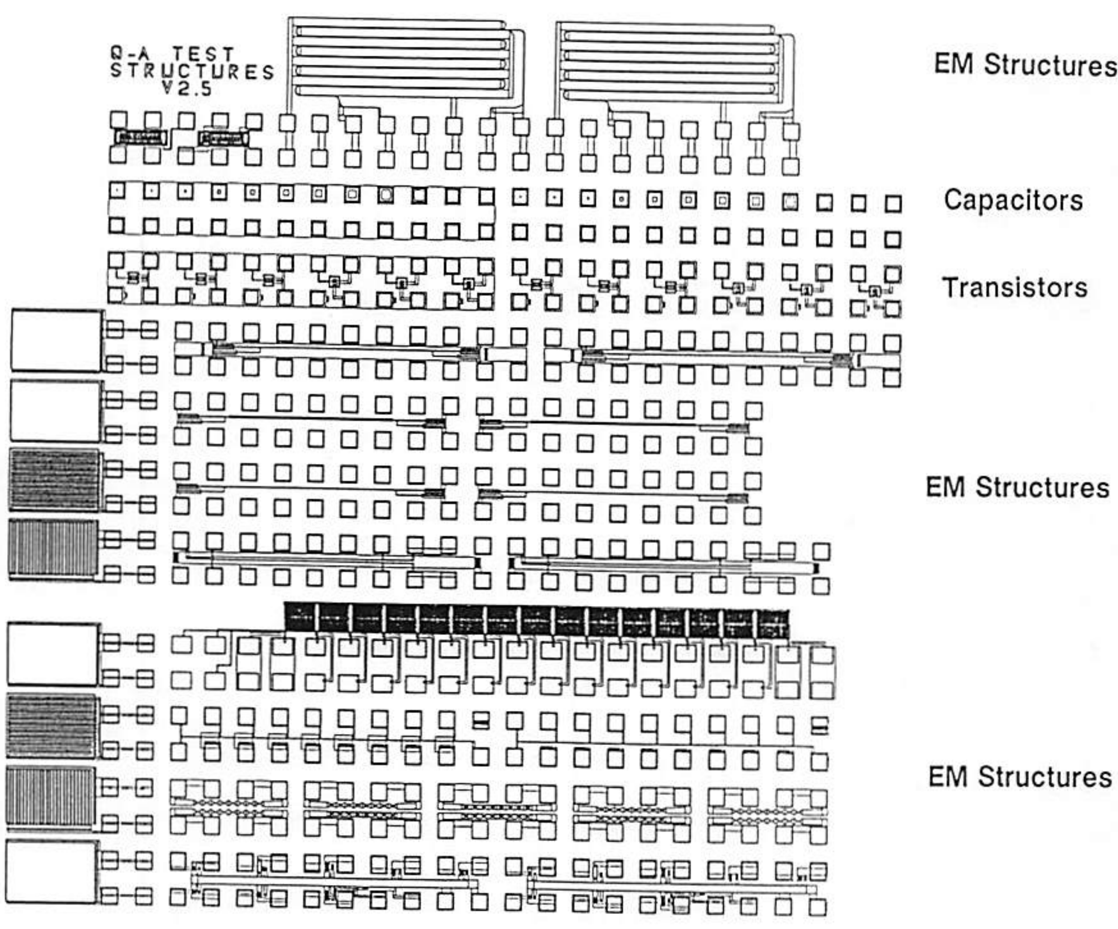


Fig. 5.3 Layout of the reliability test structure [5.4].

information is established by stressing MOS transistors at various I_{sub} levels for a pre-determined interval of time and extracting primary transistor parameters as well as output characteristics. Extracting the SPICE parameter values at each stressing period is done using the SUXES or TECAP software.

The degradation coefficients of hot-carrier effects for transistor model parameters from an industrial L = 0.5 μm transistor have been depicted in Table 3.3. These degradation parameters are used for reliability simulation of integrated circuits.

5.1.2 Installation of the RELY Program

A makefile is created to compile the whole program. By typing 'make' on UNIX systems, all modules will be compiled and linked to create the executable code. A makefile option to link with X-window environment also exists. The graphic modules to display substrate current is modified from a public-domain SPICE output graphic program [5.5]. A separate post-processing module, *pos-trely,* is also created to facilitate estimation of circuit performance degradation at specified time points. To execute the program, the following commands can be used:

```
> rely [input] [output]
```

or

```
> rely -t (simulator) -s (scheme) -x [input] [outfile]
```

or

```
> rely -a std_spice_input [input] [output]
```

The first example illustrate how to generate device model parameter files at specified time points. The second example illustrates that different optional arguments can be used to access other simulators or simulation scheme. The third example will continue the circuit performance simulation after generating model parameters.

5.1.3 RELY Command Description

The commands described here are to be used in conjunction with the regular SPICE user's guide [5.6]. In addition to the standard SPICE commands, the following new commands are added for hot-carrier effects and electromigration analyses:

(1) Element Command (Electromigration):

General form:

OXXXXXXX N+ N- MNAME VALUE W= WIDTH L= LENGTH

Example:

OM1 100 0 EMDEG 100 W= 4.5U L= 1000U

This element describes parameter values of a metal line for the simulation of electromigration. N+ and N- are the node numbers. VALUE is the resistance of the metal line. Resistance value will be calculated according to the geometric parameters if it's not given. MNAME is the electromigration model parameters information. Width is also used to determine the current density flowing through the conductor.

(2) Analysis Commands:

(a) Substrate current

General form:

.PRINT ISUB ISUBNAME MXX1 <MXX2 <MXX3 ...>>

Example:

.PRINT ISUB ISUBMODN M1 M2 M3

This command is used to request substrate current calculations for MOS transistors. ISUB is the reserved key word for substrate current analysis. The substrate current data are stored in the output file.

(b) Hot-carrier induced degradation

General form:

.PRINT HOT ISUBNAME MODNAME MXX1 <MXX2 <MXX3 ...>>

Example:

.PRINT HOT ISUBMODN HOTN M1 M2 M3

This command specifies the selected transistors to be analyzed for hot-carrier degradation at each designated time point. HOT is the reserved key word for hot-carrier degradation analysis in addition to substrate current analysis. The substrate current waveform for each selected transistor will be calculated automatically. An individual model parameter set for each selected transistor will be created based on this command. Changes of parameters for each selected transistor will be made to the corresponding .MODEL command line during the reliability simulation process.

(c) Metal Electromigration

General form:

.PRINT EM MODNAME OXX1 <OXX2 <OXX3 ...>>

Example:

.PRINT EM EMDEG1 OM1 OM2 OM3

This command is used to request the calculation of resistance change for metal lines. EM is the reserved key word for electromigration analysis.

(d) .TRAN command

General form:

.TRAN TSTEP TSTOP <TSTART>

Example:

.TRAN 1NS 160NS

This standard SPICE command is required in time-domain reliability simulation.

(3) Control command:

General form:

.DEGTIME DEC ND TSTART TSTOP

or

.DEGTIME LINEAR TSTART TSTOP TSTEP

Example:

.DEGTIME DEC 2 1E-2 1E+05

.DEGTIME LINEAR 0 1.0E+7 5E+5

This command assigns the specific time points when degradation calculations are to be computed. DEC stands for decade variation, and ND is the number of time points per decade. LINEAR stands for linear variation and TSTEP is the step size. TSTART and TSTOP are the starting and final analysis time points in the units of seconds.

(4) Model Commands:

(a) Substrate current

General form:

.MODEL ISUB MODNAME MODSUB=X ...

Example:

```
.MODEL ISUB MODN MODSUB= 1
+ P1= 2.24E-5 P2= 0.1E-5 P3= 6.4 P4= 0.13
+ P5= 0.25 P6= 1.1E7 P7= 0.25E7
```

This command specifies the substrate current model parameters. It is to be used with both .PRINT ISUB and .PRINT HOT analyses. MODSUB is the key word to select various levels of the substrate current models. In the current version of RELY, five different substrate current models are implemented. Detailed expressions for the models are listed in the Appendix C.

(b) Hot-carrier induced degradation

General form:

.MODEL HOT MODNAME MODHOT=X ...

Example:

```
.MODEL HOT MODN MODHOT=2
+ AVTOSlope= 0.1277419E-01 AVTOInt= -0.24838710E+01
+ AUOSlope= 0.29677419E-02 AUOInt= -0.69687E+01
+ AGAMMASlope= 0.58709677E-2 AGAMMAInt= -0.26793548E+01
```

This command specifies the degradation parameters for each transistor parameter. HOT is the reserved key word for hot-carrier effect degradation. MODHOT is used to select the different degradation models. At present, no

default is given in the present version. There are two degradation models currently implemented: one with merely power-law dependency in stress time as in (3.12) and one with additional substrate current dependence factor as in (3.13).

(c) Electromigration

General form:

.MODEL EM MNAME MODEM=X ...

Example:

```
.MODEL  EM  EMDEG1 MODEM=1
+ RHO = 1.0e2 TMETAL = 0.75e-6 TCR = 0.025e-1
+ RINT = -20.2085 RSLOPE = 2.5
+ TNOMIAL = 200 EA = 0.8
```

This command specifies the electromigration parameters. EM is the reserved key word for metal electromigration degradation. MODEM is used to select the different degradation models. Default parameters values associated with different metal systems are to provided in the future. Three different electromigration degradation models are implemented. including the MTTF model as in (3.16), progressive resistance change model as in (3.18) and improved progressive resistance change model with coefficient table for joule heating effect.

5.1.4 Flow of Program Control

The input to the RELY program consists of a user-specified design file and additional database files of AC degradation factors for hot-carrier effects and joule-heating factor for electromigration. The preprocessing modules parses the

design files and generates corresponding intermediate files to store model parameters. The file names have the extensions such as _DEGMOD and _EMMOD. A SPICE-compatible file is created for subsequent circuit simulation using the specified core circuit simulator. The output is stored in a file with a _RAWOUT extension. This file is read by the RELY program and the terminal voltages and drain currents of the target devices are stored in a file with a _OUT extension. The data in this file is used in conjunction with the model parameters to calculate the corresponding stress levels. The degradation module then calculates effective device degradation based on the monitored stresses. In the repetitive simulation scheme, the updated device parameters at each time point are stored as files with a extension _DEGPRM. The files are enumerated such as out_DEGPRM1 to facilitate circuit performance simulation by a post-processing module *postrely*. SPICE-compatible input files with updated device parameters is created at the end of each specified time period for degradation prediction.

An accurate method of calculating the DC substrate current using SPICE transient analysis has also been implemented. At present, this option has been tested with the use of HSPICE simulator. In the first pass, the pre-processing module of the RELY program filters the input deck and stores the substrate current model parameter information and identifies the "target transistors." An HSPICE output deck is created which contains the valid HSPICE statements from the user input deck. The program inserts .PRINT statements to make HSPICE print the voltages of all circuit nodes for the specified time points during the transient analysis. This information is stored in intermediate output files and used at the next stage. Files that are created by the program include

. input files for various HSPICE runs, and

. raw output files from the HSPICE runs.

The second stage of the simulation consists of performing a DC analysis to obtain the DC component of the drain current. During this stage, the circuit is handled at the individual transistor level to simulate only the targeted transistors. The terminal voltages of the transistors are determined from the previous transient analysis and a .DC analysis is performed. The output from the second run of HSPICE is filtered to obtain the corresponding drain current. The resulting DC drain current is used to calculate the DC component of the substrate current using the substrate current.

5.2 Case Studies for High-Performance Computing Circuits

Reliability simulation of various benchmark circuits commonly used in digital and analog processors are presented in this section.

5.2.1 CMOS Inverter

Substrate current generation during switching transient for a CMOS inverter with an effective channel length of 0.5 μm was studied under input pulse trains of various rise and fall rates [5.7]. Figures 5.4(a) shows the simulated transient results of substrate currents in the inverter. For an input pulse with a short transition time, significant current generation occurs only at the rising edge. The corresponding degradation in the circuit performance is shown in Fig. 5.4(b). The output response time during the high-to-low transition is greatly increased

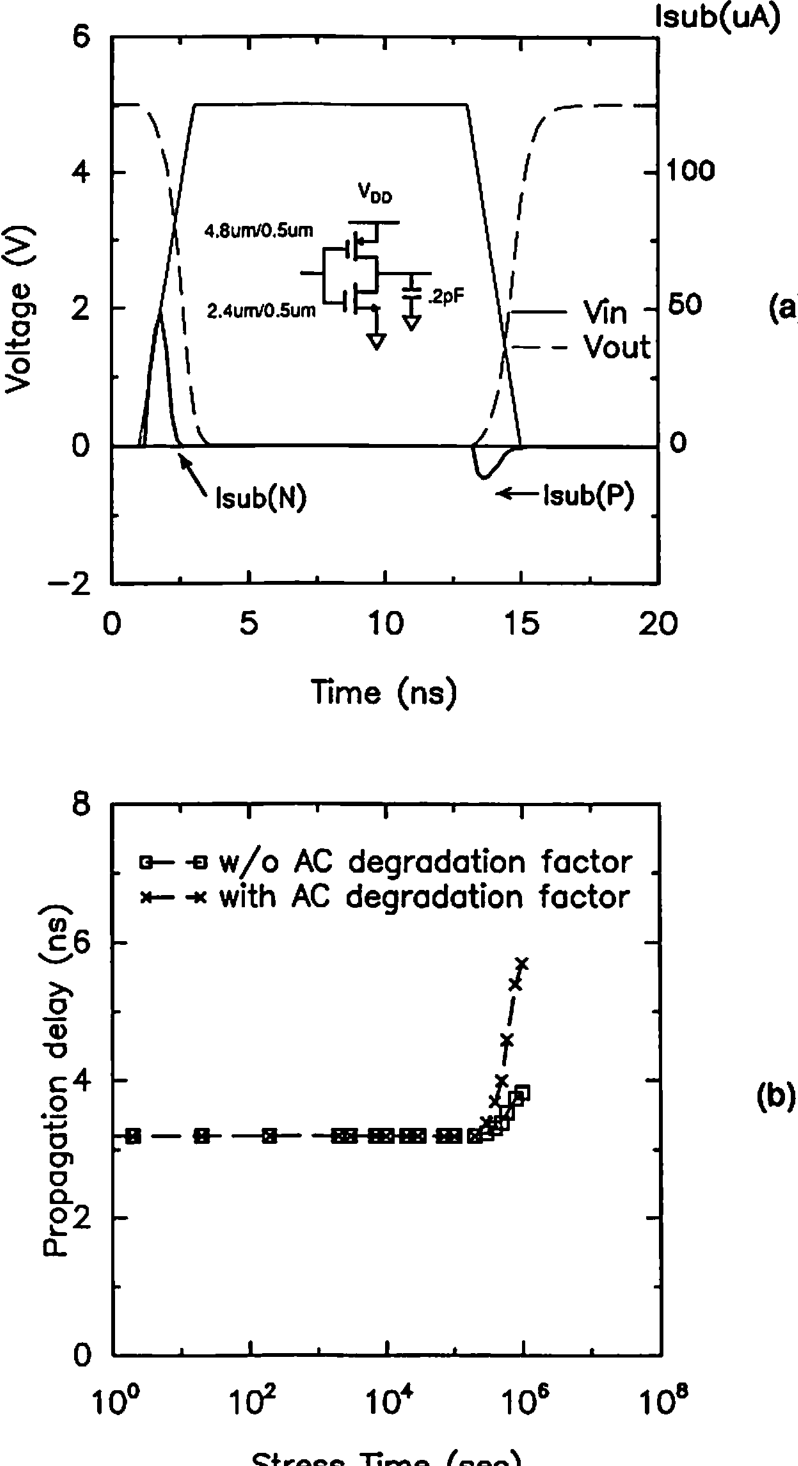
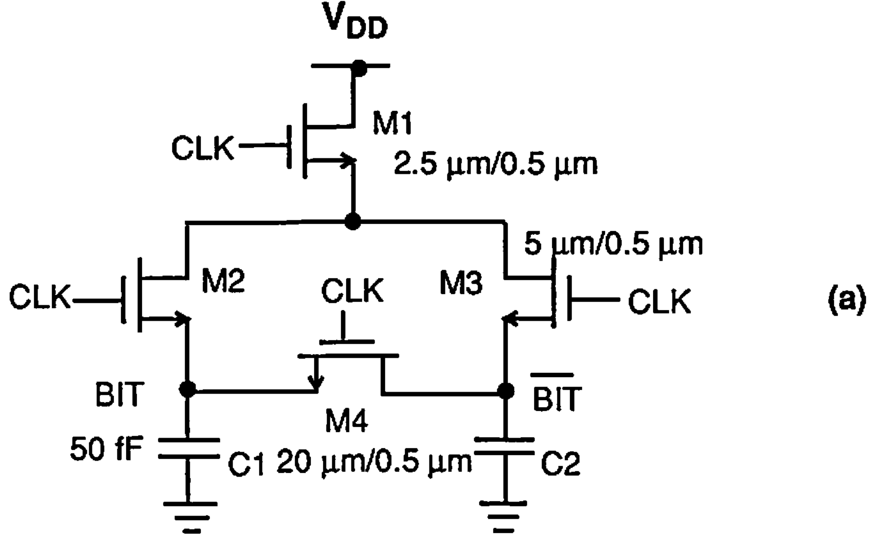


Fig. 5.4 Simulated substrate current waveforms and the degradation for a CMOS inverter due to pulse train.
(a) Substrate current characteristic. (b) Change in propagation delay for short-transition time.

while the response time during the low-to-high transition is slightly decreased. The averaged propagation delay of the inverter is increased accordingly. A larger degradation is predicted by inclusion of the AC degradation factor due to the edge-overlapping voltage waveforms as also shown in Fig. 5.4(b). Here, the stress waveform on transistor M1 is classified as class G with a value of 2.5 for the AC degradation factor.

5.2.2 Memory Precharging Circuit

The sense amplifier in a DRAM chip plays an important role in determining the memory access time [5.8]. The NMOS precharging circuitry for a sense amplifier from an industrial 0.5-µm technology is shown in Fig. 5.5(a). Transistors are subjected to high electrical stress during the precharging period. The voltage waveforms in the bit lines are shown in Fig. 5.5(b). Transistor M2 and M3 are the most critical devices to the precharging time performance of the circuit. The corresponding stress waveforms for transistor M2 are also shown in Fig. 5.5(b). This circuit is an example of digital circuitry whose analog behavior greatly affects circuit characteristics. In such a case, detailed reliability simulation provides important information about performance degradation. Reliability simulation including the AC degradation factor was performed on this circuit for 10^7 seconds. The measured value of the AC degradation factor ΔP_{AC-DC} is 1.5. The threshold voltage and carrier mobility changes for transistor M2 are shown as functions of the stress time in Fig. 5.5(c). Larger degradation is predicted due to AC stress effects. According to Table 4.1, this type of stress waveforms is classified as the edge-overlapping case, class G. Change in the response time



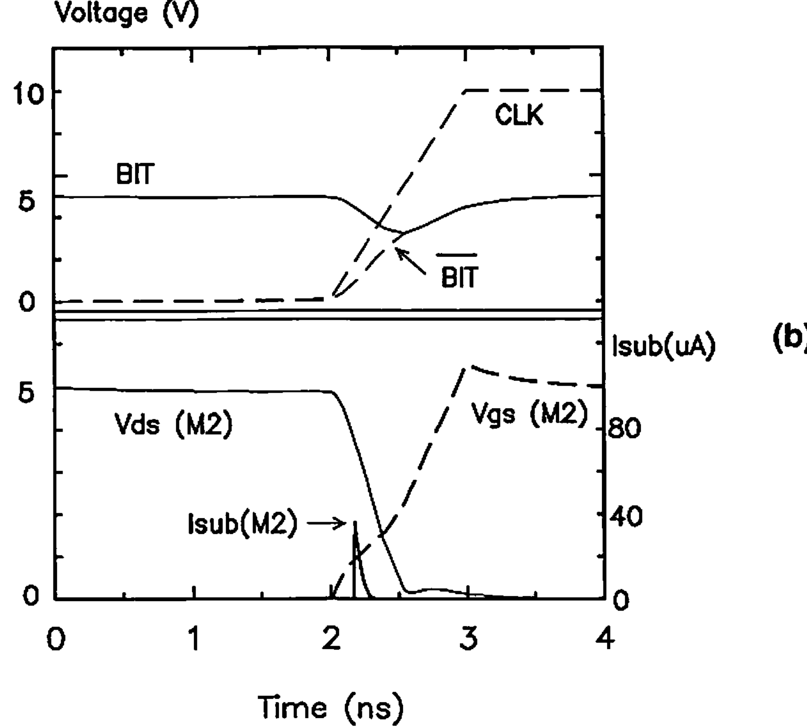


Fig. 5.5 Simulation of a precharging circuit cell with L = 0.5 µm.
(a) Circuit schematic.
(b) Voltage waveforms in the circuit and AC stress waveforms in transistor M2.

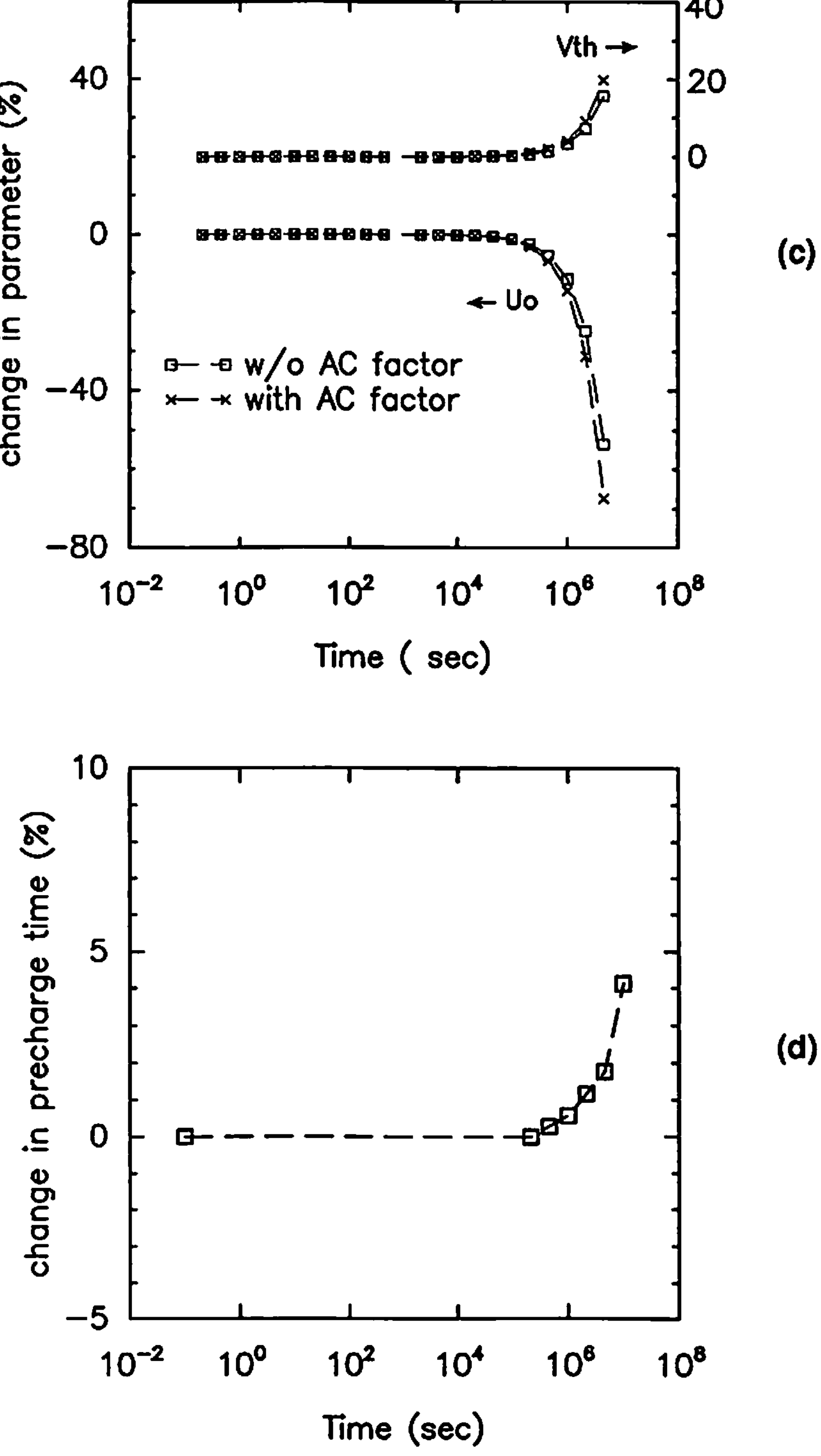


Fig. 5.5 (c) Effect of AC degradation factor on transistor parameter values. (d) Change in the circuit precharging time.

of the precharging circuit due to degradation from all transistors is shown in Fig. 5.5(d).

5.2.3 NAND Gates

(a) Two-input NAND gate

Less hot-carrier damage occurs in the NAND gate than in the inverter [5.9] because the cascode configuration reduces the voltage stress level on N-channel transistors. Figure 5.6(a) shows a conventional NAND gate. A significant substrate current occurs in transistor M2 during the rising transient of V_{in1} at a high value of V_{in2}. A modified NAND gate operation can be used to increase the resistance to hot-carrier effects if the transistor M2 turns on before transistor M1.

The bootstrapping technique can also be used to reduce hot-carrier damages [5.10]. An NMOS transistor M5 is added to the conventional NAND circuit as shown in Fig. 5.6(b). The voltage at node A is temporarily increased during the transient with the insertion of M5. Therefore, V_{ds} of transistor M2 is reduced as compared to the same transistor in the conventional NAND gate. A significant reduction in substrate current is achieved as shown in Fig. 5.6(c) and (d).

(b) Four-input NAND gate

In a CMOS NAND gate, NMOS transistors are connected in series and PMOS transistors are connected in parallel. Figure 5.7 shows the circuit schematic of a single stage four-input NAND gate cell. Due to the skew in signal transmission, some signals may arrive at the logic gate slower than other input signals. As a result, the response time will be determined by which input

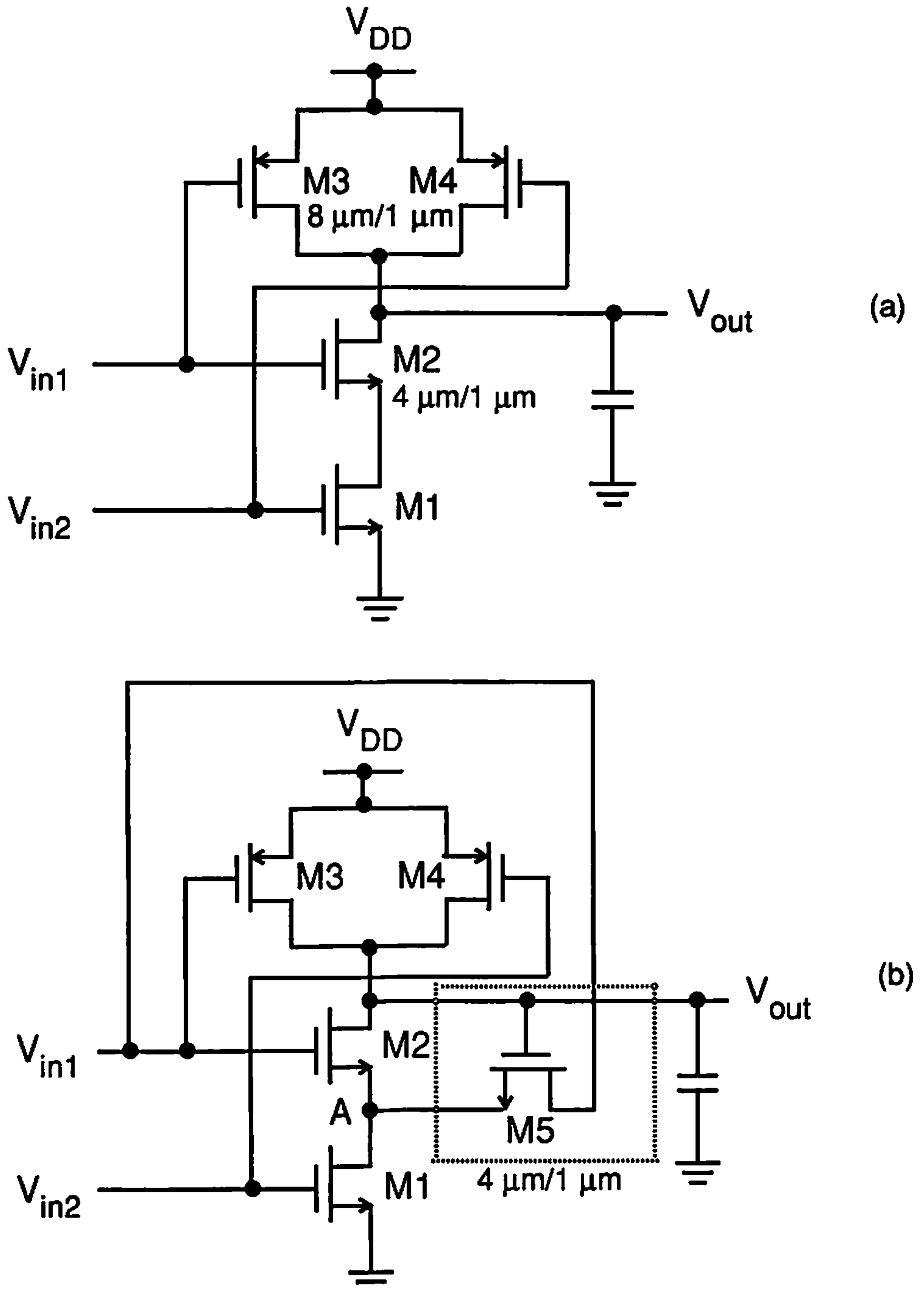


Fig. 5.6 Suppression of hot-carrier damages in a CMOS two-input NAND gate cell.
(a) Conventional circuit.
(b) Hot-carrier-resistant circuit [5.10].

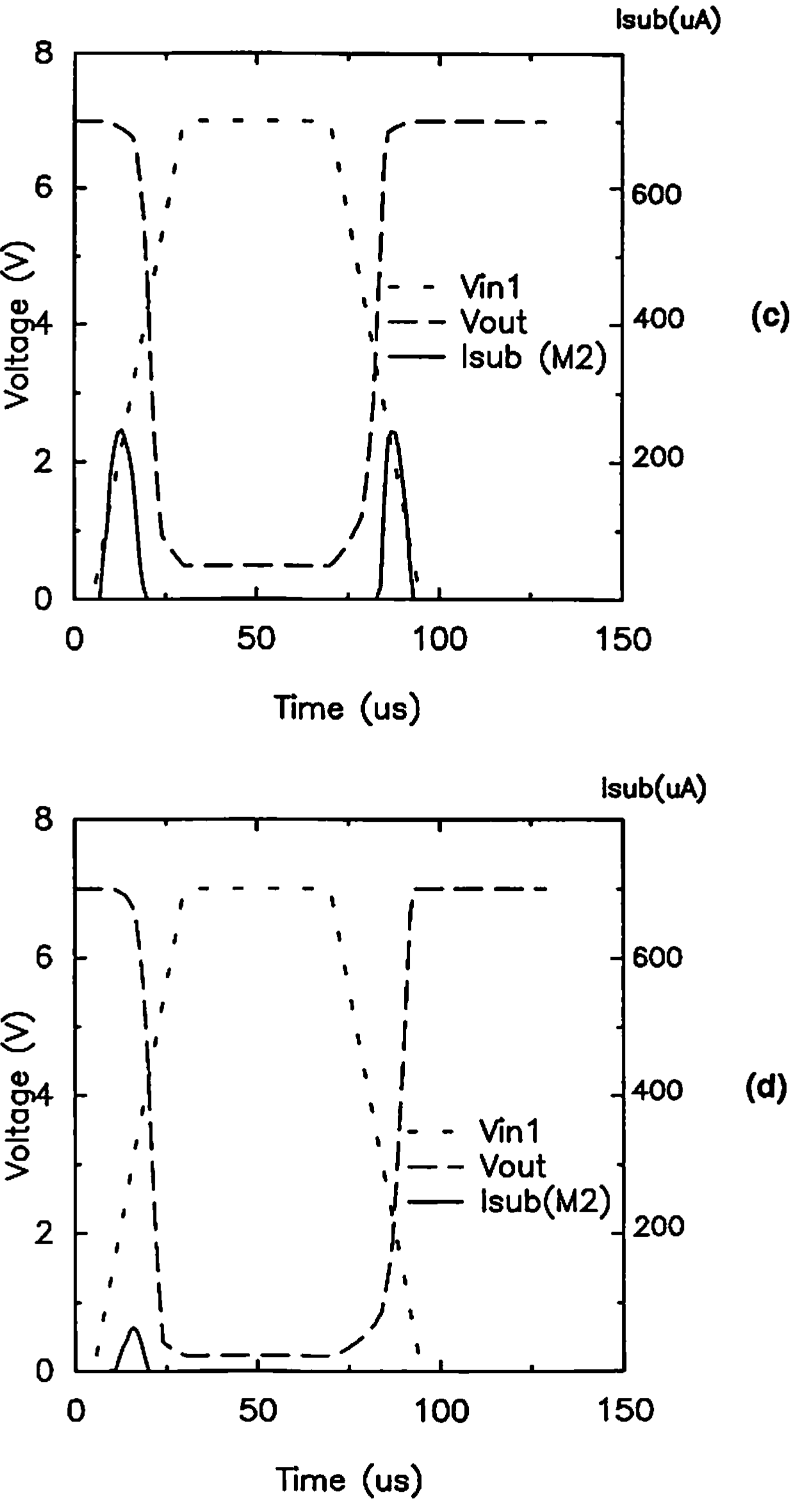


Fig. 5.6 (c) Substrate current in the conventional NAND gate. (d) Significant reduction of substrate current in the modified NAND gate.

signal arrives last. A good design rule is to route the slowest signal to the transistors connected to the output node of the logic gate. Notice that in Fig. 5.7(a) transistors M_{1N} and M_{1P} are connected to the output node of the four-input NAND gate and these transistors should be driven by the slowest signal. Figure 5.7(b) shows a comparison of the best case and the worst case in delay for the four-input NAND gate. While the switching speed is fastest if the input V_{in1} is the last arriving signal, the largest effective substrate is also created. From the reliability perspective, a design optimization is required in selecting the proper signal path. Figure 5.7(c) summarizes the comparison of speed performance and reliability characteristics for four different signal routing cases in the four-input NAND gate. Notice that the transistor size for each transistor can also be adjusted individually to minimize the difference in the delay time among different signal paths.

5.2.4 Ring Oscillator

A ring oscillator circuit is a commonly used benchmark circuit to characterize the frequency performance of a fabrication process. The oscillation frequency in this circuit is a strong function of the current driving capability of the inverters. Figure 5.8(a) shows the measured oscillation frequency of a fresh 31-stage ring oscillator from a 1.6 μm fabrication process. Fig. 5.8(b) shows the oscillation frequency of the circuit after being stressed at a 7.5-V power supply for 11 hours. The oscillation frequency is found to decrease from 54.3 MHz to 45.7 MHz.

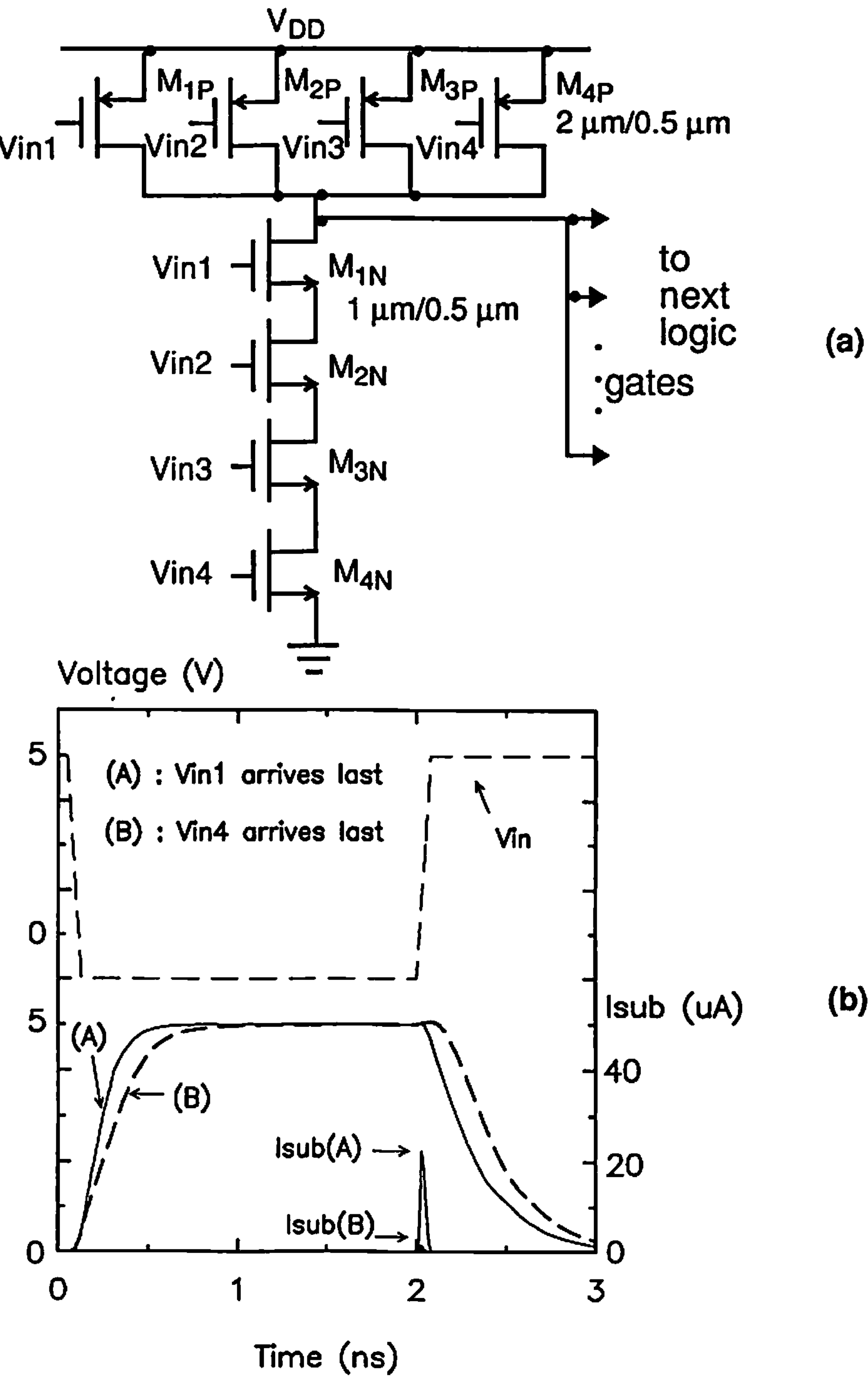


Fig. 5.7 Comparison of reliability performance vs. speed perfromance in a four-input NAND gate cell.
(a) Circuit schematic.
(b) Substrate current and signal waveforms.

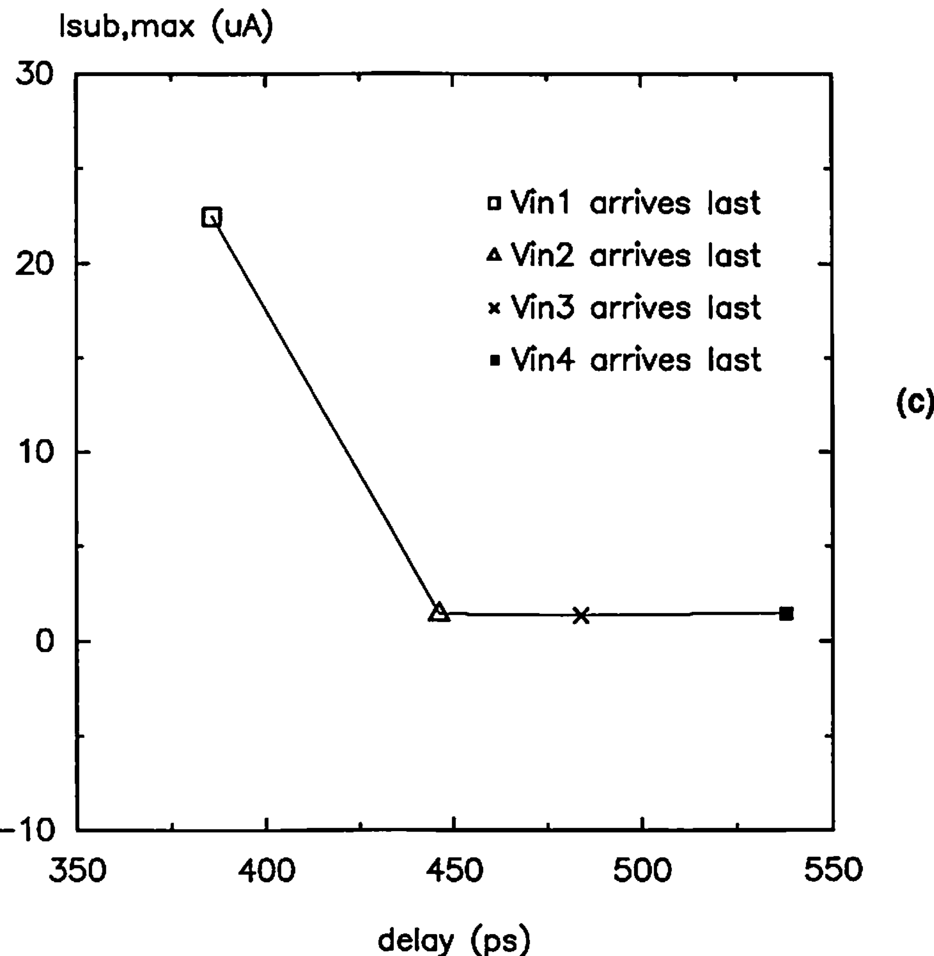
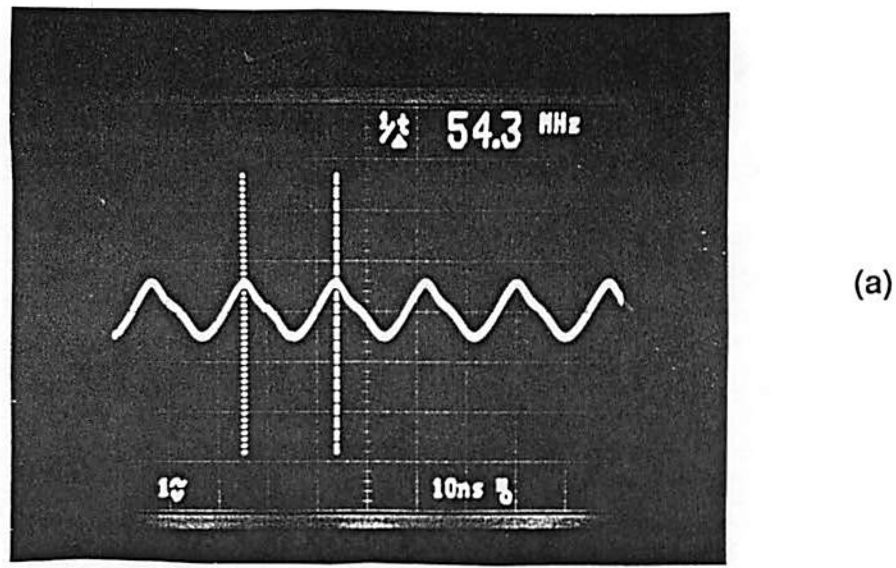
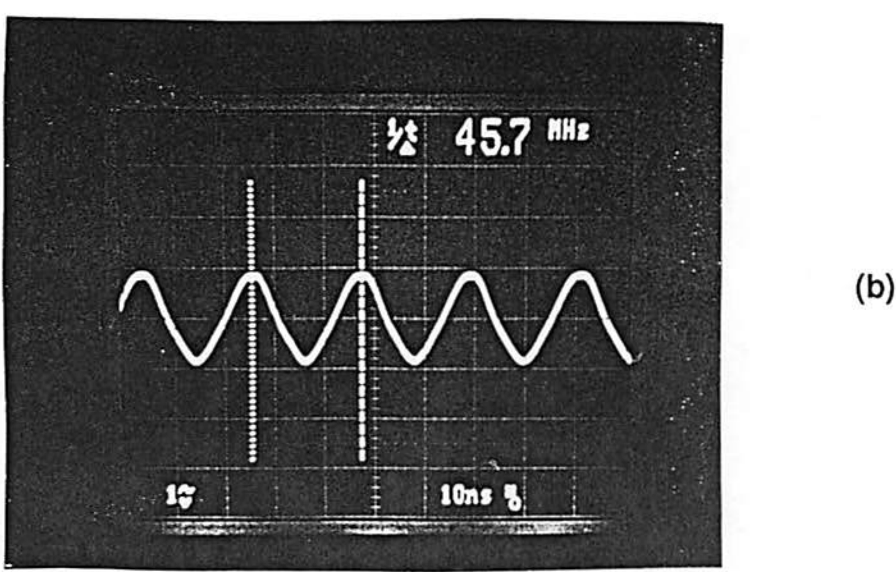


Fig. 5.7 (c) Peak substrate current vs. logic gate speed with different latest arriving signals.



(a)



(b)

Fig. 5.8 Hot-carrier effects on the ring oscillator operation.
(a) The fresh ring oscillator has a fresh oscillation frequency of 54.3 MHz.
(b) Frequency response after 11-hour stress at a 7.5 V power supply is reduced to 45.7 MHz.

5.2.5 SRAM Cell And Peripheral Circuits

A basic SRAM circuit with memory cell, write control circuitry and precharging circuitry is shown in Fig. 5.9(a). PMOS transistors are used as load devices in the memory cell instead of high-resistance polysilicon line to achieve low standby current in the high density memory design. Fig. 5.9(b) shows the voltage waveforms in both WRITE and READ cycles from the simulation. The word line is enabled in each WRITE or READ cycle. Bit lines controlled by PRE are precharged before the word lines are enabled. Significant substrate currents in the transistors occur during voltage transition. The data write time after 3 years of continuous operation at V_{DD} = 5 V and V_{PRE} = 10 V is increased by around 9% as shown in Fig. 5.9(b). Table 5.1 lists the simulated results with the corresponding AC degradation classification for both NMOS and PMOS transistors in the memory circuit. Transistor degradation is predicted by combining the substrate current and a suitable AC degradation factor. The reliability flags are assigned based on a user-specified degradation threshold value. In this example, the threshold value for the substrate current is 20 μA.

5.2.6 Operational Amplifiers

Operational amplifiers have been used as a key module in the recent development of analog neural computing chips [5.11]. To implement large neural networks as well as advanced communication ICs, analog circuits using submicron technology are important modules. Despite of the intrinsic fault-tolerance in an artificial neural network, the processing speed can be limited as circuit performance is shifted due to the device parameter degradation [5.12]

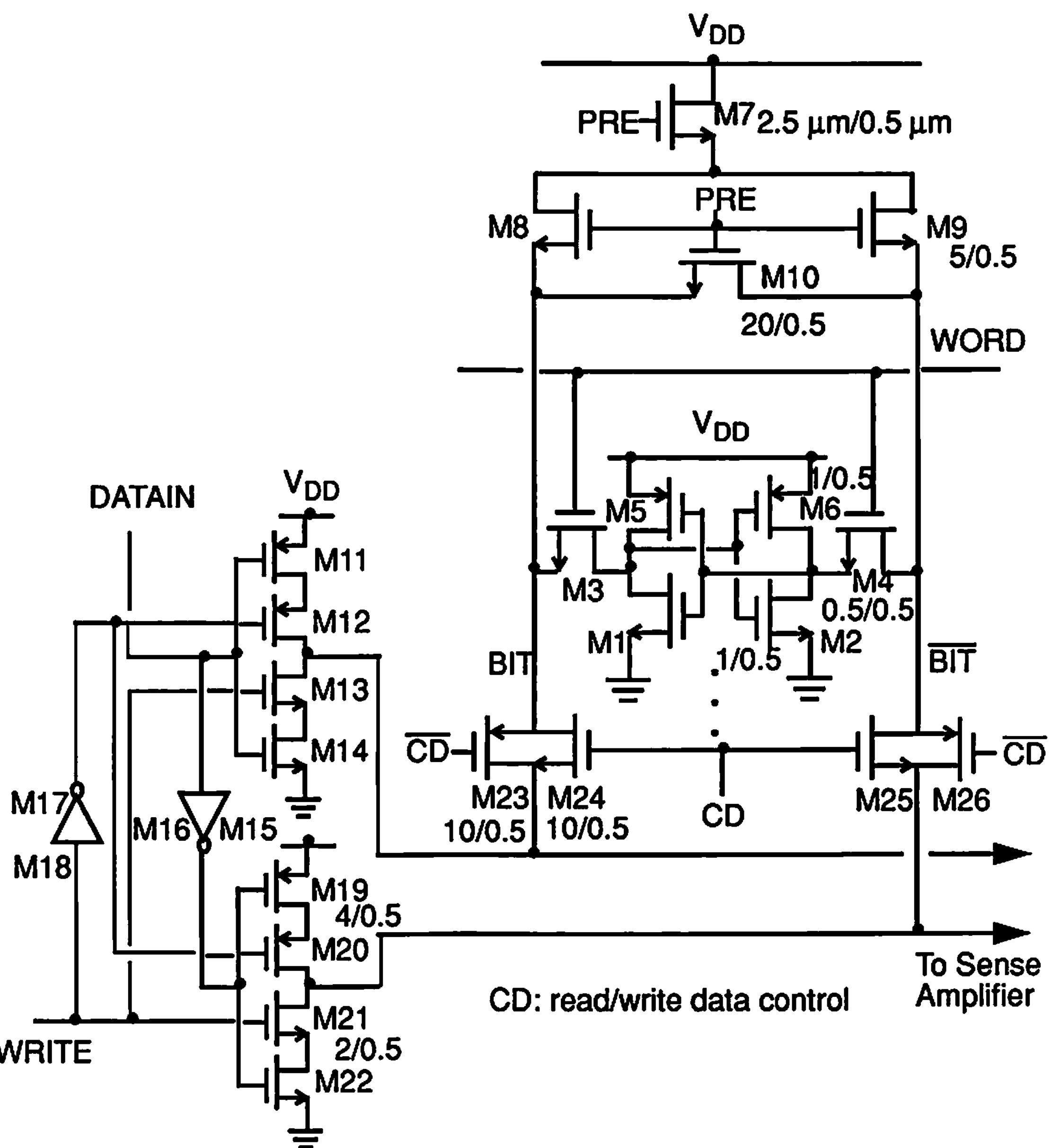


Fig. 5.9 Hot-carrier effects in an SRAM circuit with memory cells and peripheral control circuits.
(a) Circuit schematic.

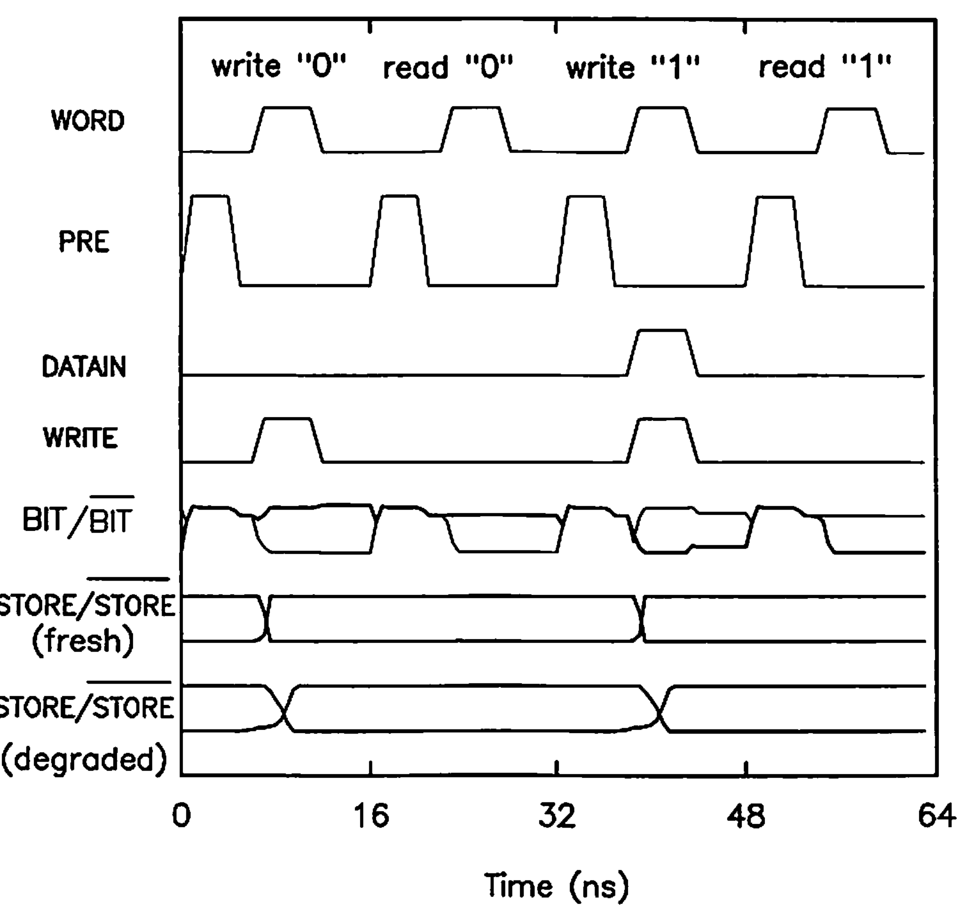


Fig. 5.9 (b) Voltage waveforms in the SRAM circuit. Data write time is increased after 3 years of continuous usage.

Tabl 5.1 Simulation results in an SRAM circuit with classified AC stress types and reliability warning flags.

Transistor	Isub,max (A)	Waveform class (as in Table 3)	Reliability warning flag
M1	6.14e-8	F	
M2	9e-8	F	
M3	< 1e-8	A	
M4	2e-8	A	
M5	-1.9e-6	F	
M6	-5.1e-6	F	
M11	< 1e-8	F	
M12	8e-6	F	
M13	7.5e-6	F	
M14	6.5e-5	C	x
M15	-8.5e-6	F	
M16	-7.2e-6	F	
M17	2.39e-5	F	x
M21	2.1e-5	F	x
M23	-2.4e-5	F	x
M24	1.5e-5	F	
M25	-2.5e-5	F	x
M26	1.7e-5	F	

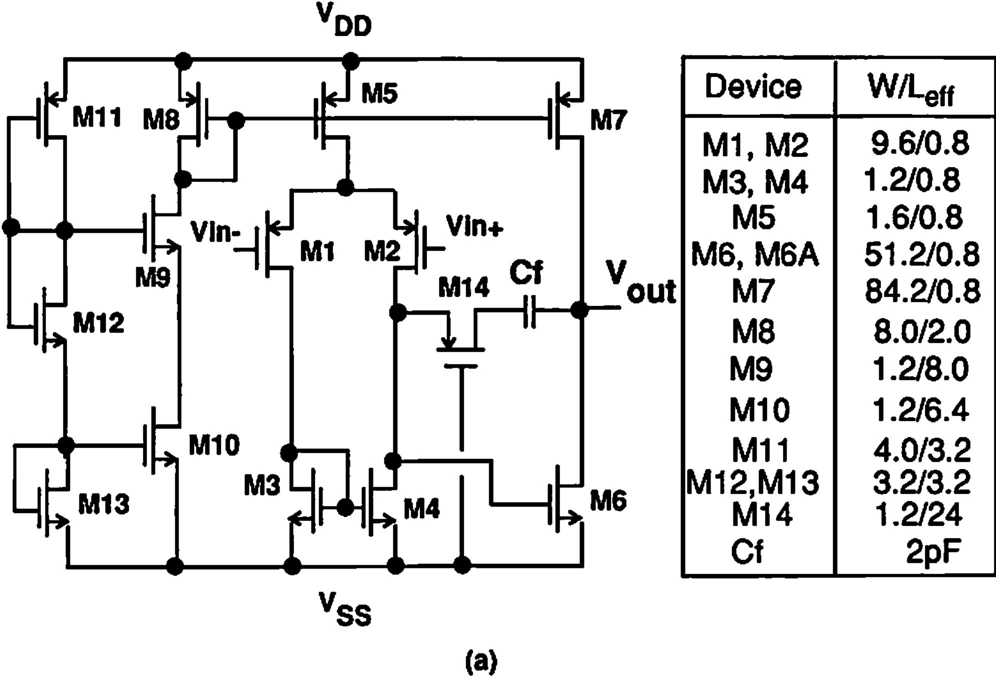
which is caused by reliability problems.

A two-stage CMOS operational amplifier [5.13] with a simple class-A output stage is shown in Fig. 5.10(a). Due to a large voltage stress of being close to 10 V received by the driver transistor M6 in the unity-gain operation, voltage gain and current-driving capability of the output stage could severely degrade [5.14]. To reduce the voltage stress, circuit design techniques can be applied. Figure 5.10(b) shows an amplifier with a common-gate buffering transistor M6A inserted to convert the output driving circuitry into a cascode configuration. Voltage stress on transistor M6 is greatly reduced by this technique. The substrate currents for selective transistors in these two amplifiers are shown in Fig. 5.10(c). Significant reduction of the substrate current is found in the operational amplifier with a cascode output driver indicating that the new circuit is more resistant to hot-carrier damages.

Changes of the voltage gain due to hot-carrier stress for both amplifiers are shown in Fig. 5.10(d). From the simulated result of the amplifiers in use for 162 days, the change of voltage gain in the simple amplifier is around 40 % while that in the cascode amplifier is negligible. The second-stage voltage gain can be expressed as

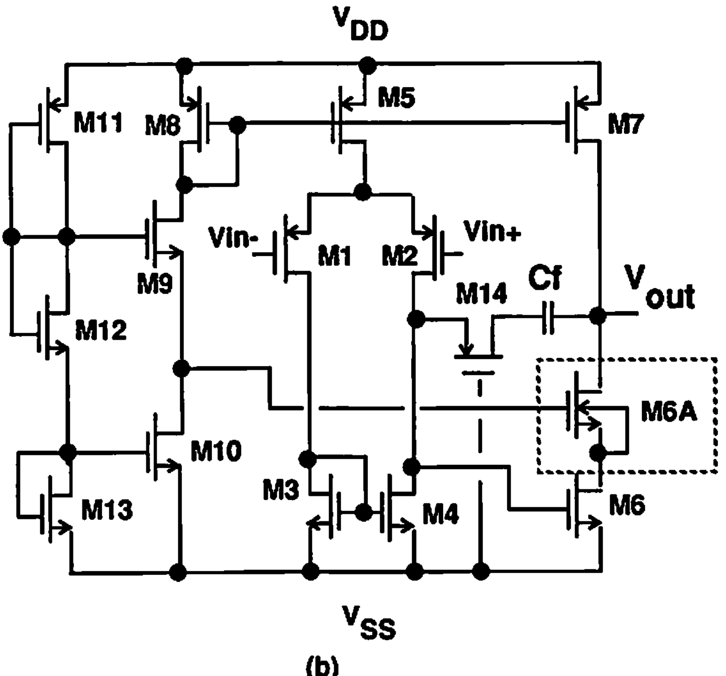
$$A_v = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_{ds6}(\lambda_6 + \lambda_7)}, \tag{5.1}$$

where g_m is the transistor transconductance, g_{ds} is the output conductance and λ is the channel-length modulation parameter. The percentage change of voltage gain can be approximated as



Device	W/Leff
M1, M2	9.6/0.8
M3, M4	1.2/0.8
M5	1.6/0.8
M6, M6A	51.2/0.8
M7	84.2/0.8
M8	8.0/2.0
M9	1.2/8.0
M10	1.2/6.4
M11	4.0/3.2
M12,M13	3.2/3.2
M14	1.2/24
Cf	2pF

(a)



(b)

Fig. 5.10 Suppression of hot-carrier induced damages using a cascode output stage for operational amplifiers.
(a) Amplifier with a simple class-A output stage.
(b) Amplfier with a cascode output stage.

$$\frac{\Delta A_v}{A_v} = \frac{\Delta g_{m6}}{g_{m6}} - \frac{\Delta I_{ds6}}{I_{ds6}}. \tag{5.2}$$

Both terms in (5.2) decrease as a result of hot-carrier stress. Notice that the threshold voltage for NMOS transistors is increased due to hot-carrier stress. For the simple output stage, voltage gain is slightly increased as the second term dominates in the initial stage of hot-carrier stress. Due to the parabolic dependence of the drain current on the threshold voltage, the rate of change in the drain current becomes less significant as the hot-carrier stress proceeds. The voltage gain then decreases as shown in Fig. 5.10(d). For the amplifier with a cascode output stage, the voltage gain stays nearly constant because the change of transconductance as well as the biasing current in the output stage are very small. A summary of the fresh circuit performances and the aged performances after 162 days of operation for both operational amplifiers is listed in Table 5.2. For the amplifier with a simple output stage, the performance items which are sensitive to hot-carrier effects include low-frequency voltage gain, unity-gain bandwidth and power supply rejection ratio. While large performance changes are found in the amplifier with a simple output stage, the amplifier with a cascode output stage is significantly more resistant to hot-carrier damages.

5.2.7 Power Line Connected to an Output Driver

Figure 5.11 shows the schematic of a bus line connected to an output driver. Large current density will flow in the bus line during circuit operation. The resistance R_{EM} monitors the electromigration level through the power line. The circuit schematic of the output driver is shown in Fig. 5.11(a). Width

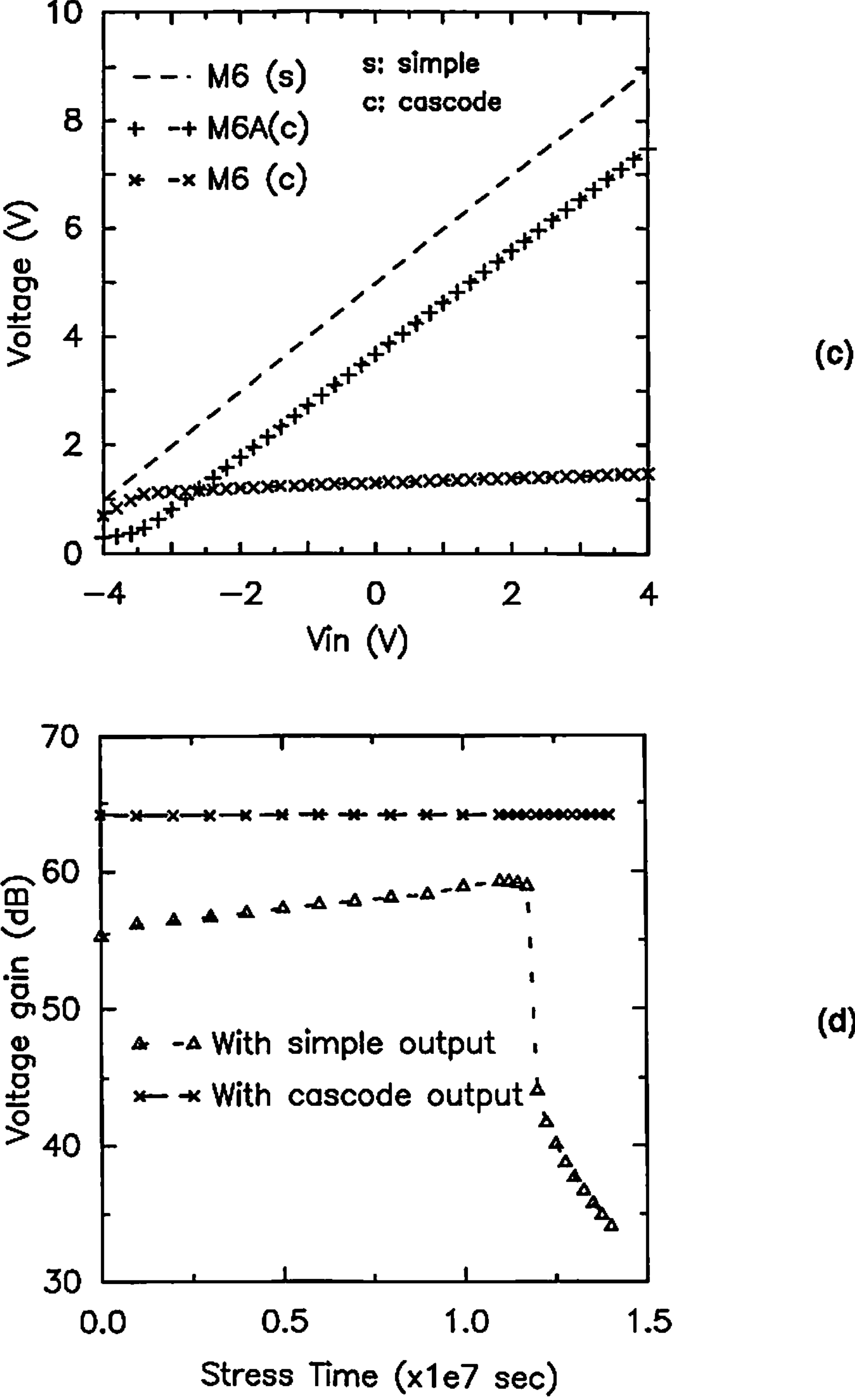


Fig. 5.10 (c) Drain-to-source voltage for NMOS transistors in the output stages.
(d) Change of voltage gain in unity-gain configuration for both output stages.

Table 5.2 Comparison of fresh and stressed performances of operational amplfiers with simple and cascode output stages.

	Simple output stage		Cascode output stage	
	t =0	% change @ t =1.2e7 s	t =0	% change @ t =1.2e7 s
Offset Voltage (mV)	4	0%	0.5	0%
Unity-gain bandwidth (MHz)	80	- 15%	58	0%
DC Gain (dB)	55	- 25.4%	64	0%
CMRR (dB)	72	0.05%	66	0%
PSRR+ @1kHz (dB)	56	- 25.4%	75	0.1%
PSRR- @1kHz (dB)	100	- 32.5%	88	0%
Input Range (V)	(-4.2, 4.9)	- 1.6%	(-4.2, 4.9)	0%
Output Swing (V)	(-4.3, 5.0)	- 0.4%	(-4.25, 5.0)	0%

effects on change of metal resistance due to electromigration is shown in Fig. 5.11(a). The rate of electrical resistance change in the metal line is determined by the duty cycle of the operation. Figure 5.11(b) shows change of metal resistance as a function of duty cycle. Signal strength is reduced due to excessive voltage drop along the interconnects as the resistance is increased.

5.2.8 Sigma-Delta A/D Converter

A sigma-delta A/D converter with high resolution of 16-bits can be used as an analog front-end used in high-speed telecommunication circuits [5.15]-[5.17]. The 4th-order A/D converter circuit consists of 4 integrators, 2 summing amplifiers, a 1-bit A/D converter, and a 1-bit D/A converter. The 4th-order noise-shaping filter is constructed by cascading switch-capacitor integrators. Figure 5.12 shows the metal interconnect network of the circuit. It is targeted for a 5 MHz sampling rate in a 2-μm CMOS technology. Reliability performance of interconnect metal lines in this circuit by using the simulation hierarchy is explored here. Interconnects are extracted and represented by resistive elements before proceeding to electromigration simulation. The simulation results on electromigration for individual interconnect among subcircuits are listed in Table 5.3.

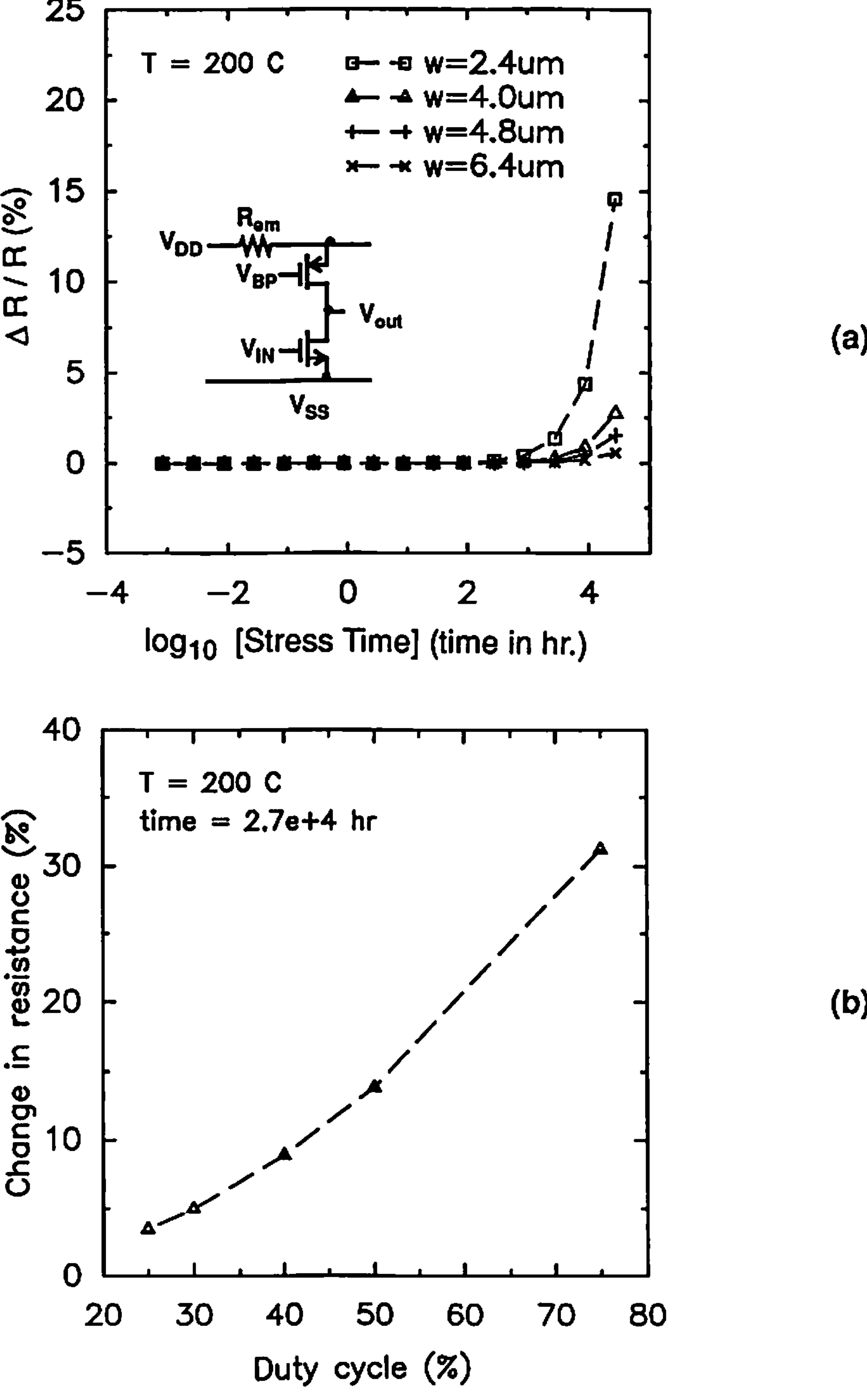


Fig. 5.11 Change of the metal resistance due to metal electromigration in an output driver.
(a) Circuit schematic and the width dependence.
(b) Dependence of resistance change on voltage duty cycle assuming no annealing effect.

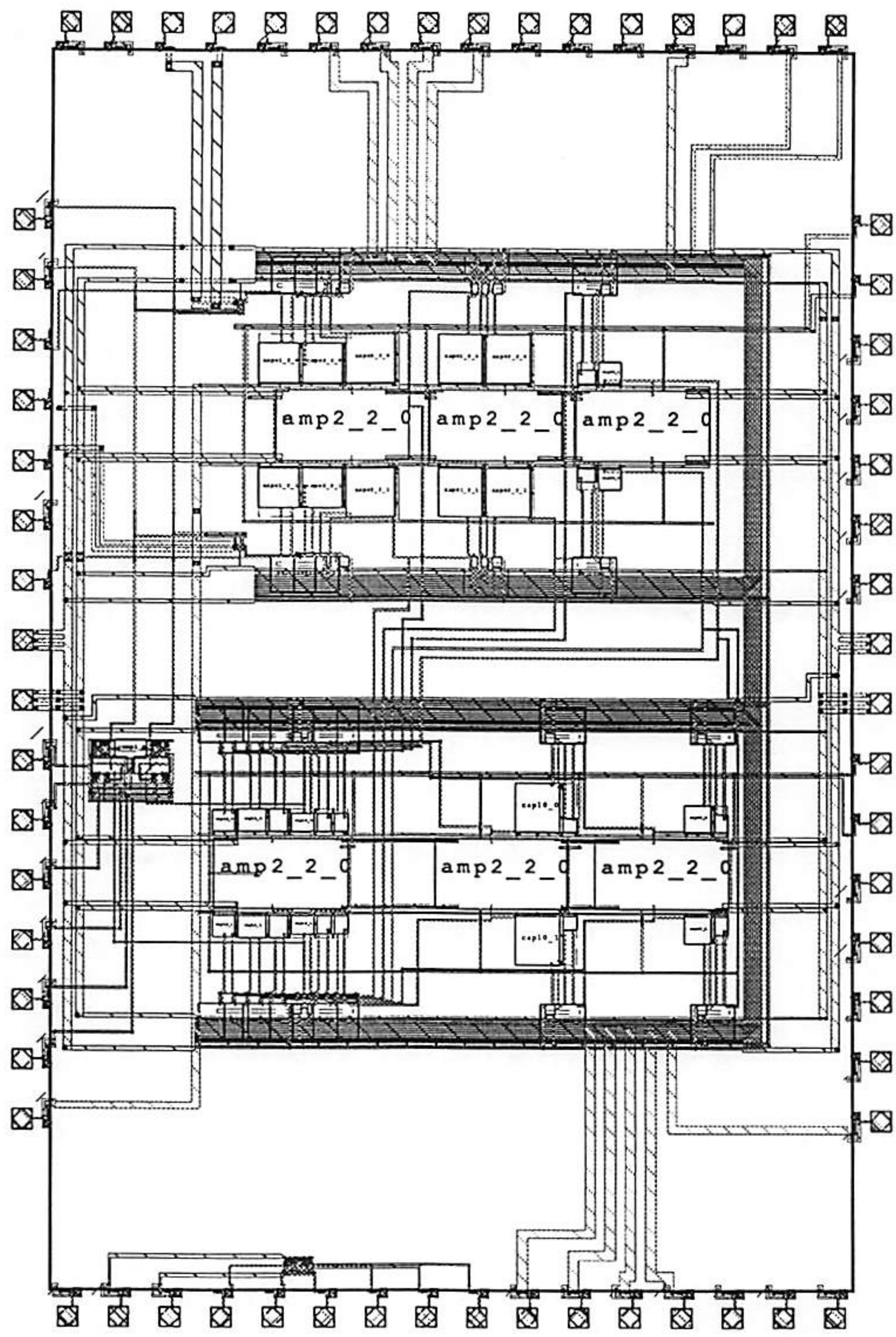


Fig. 5.12 Layout of the interconnect/contact network in a 4th-order sigma-delta modulator.

Table 5.3 Electromigration simulation of a sigma-delta modulator.

Routing Interconnect	Effective current density (MA/cm^2)	MTTF
Vdd bus	1.04	1.19×10^7
Vss bus	1.04	1.18×10^7
Rin+(stage_0,stage_1)	9.7×10^{-3}	2.2×10^{12}
Rin-(stage_0,stage_1)	9.7×10^{-3}	2.2×10^{12}
Rin+(stage_1,stage_2)	1.02×10^{-2}	1.97×10^{12}
Rin-(stage_1,stage_2)	1.02×10^{-2}	1.97×10^{12}
Rin+(stage_2,stage_3)	3.2×10^{-3}	4.0×10^{13}
Rin-(stage_2,stage_3)	3.2×10^{-3}	4.0×10^{13}
Rout+(stage_3,stage_4)	2.4×10^{-3}	8.5×10^{13}
Rout-(stage_3,stage_4)	2.4×10^{-3}	8.5×10^{13}
Rout+(stage_5,stage_6)	1.41×10^{-2}	8.52×10^{11}

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[5.15] B. E. Boser, B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE J. of Solid-State Circuits*, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

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Chapter 6

Conclusion

Submicron CMOS technologies make possible the implementation of VLSI computing circuits with high computation throughput and low chip area requirement. Reliability issues can limit the trend to scale down the device feature size. Vertical integration of VLSI technologies demands the assessment of circuit reliability from the process level to the system level.

In this dissertation we have presented the need to address circuit-level reliability study that leads to the development of the RELY circuit reliability simulator. This program together with SUPREM, PISCES and other interface simulators will form a technology-based integrated simulation environment for reliability analysis in a computer-aided manufacturing system. Reliability modeling requirements including fresh SPICE device models as well as degradation models to account for both physical effects and computation efficiency are presented. Circuit-level reliability analysis for hot-carrier damages and electromigration has been concluded to effectively use the stress monitors including effective substrate current and current density.

A unified methodology of simulation schemes has been developed to facilitate circuit-level reliability simulation. Quick identification of weak devices in an integrated circuit can be achieved using the one-cycle simulation scheme. To account for progressive change in circuit performance due to the changing bias conditions caused by device degradation, the repetitive simulation scheme is used

to improve the simulation accuracy. While DC stressing is common in reliability experiments, many circuits are operated under AC waveforms. The two-pass simulation procedure to find the corrsponding DC stress monitor can achieve accurate quasi-static simulation results. Excessive hot-carrier induced degradation under AC stress was reported by other researchers. A systematic reliability simulation approach including the dynamic stress effects is presented.

Within the circuit, the sensitivity of the circuit performance to reliability effect is not only a function of received stresses but also a strong function of the location of individual devices. While the weight of individual device is determined implicitly in circuit simulation, sensitivity analysis of transistor parameters has greatly reduced the efforts to monitor stressing experiments, and improved the efficiency in circuit reliability simulation.

Finally, design of several computing application circuits using the RELY simulator has been demonstrated. Inclusion of circuit reliability assessment into the design flow helps to improve the the long-term circuit reliability performance before committing to the design to silicon fabrication. Application of circuit techniques to reduce hot-carrier damages is also presented.

By predicting the progressive circuit performance based on the concepts of device degradation, it is hoped that higher long-term circuit performance can be achieved before going to actual silicon manufacturing. To extend this work, integration of the reliability simulator into Computer-Integrated Manufacturing (CIM) systems can be of fundamental importance in technology development and yield optimization. More experimental verification of the simulation results on large-scale circuits and continuous improvement of modeling efforts can be made

to improve the simulation accuracy. Extension of the RELY simulator can also be made to include software modules for TDDB, radiation effects, bipolar circuits, and compound circuits such as GaAs MESFET and HBT circuits.

Appendix A

Journal and Conference Publications Out of the Dissertation Work

A.1 Journal Publications

1. W.-J. Hsu, B. J. Sheu, S. M. Gowda, "Design of reliable VLSI circuits using simulation techniques," *IEEE J. of Solid-State Circuit*, vol. 26, no. 3, pp.452-457, March 1991.
2. W.-J. Hsu, B. J. Sheu, V. Tyree, "Computer-aided VLSI circuit reliability assurance," *Int. J. of Modeling & Simulation*, vol. 9, no. 4, pp. 118-123, 1989.
3. B. J. Sheu, W.-J. Hsu, B. W. Lee, "An integrated-circuit reliability simulator - RELY," *IEEE J. of Solid-State Circuit*, vol. 24, no. 2, pp. 473-476, Apr. 1989.
4. B. J. Sheu, W.-J. Hsu, P. K. Ko, "An MOS transistor charge model for VLSI design," *IEEE Tran. on Computer-Aided Design*, vol. 7, no. 4, pp. 520-527, Apr. 1988.

A.2 Conference & Workshop Publications

1. W.-J. Hsu, S. M. Gowda, B. J. Sheu, "Testing of analog array-processor neural chips," *Proc. IEEE Int. Conf. Computer Design*, to be published, Cambridge, MA, Oct. 1991.
2. W.-J. Hsu, B. J. Sheu, "Integrated-circuit reliability simulation including dynamic stressing effects," *Proc. IEEE Custom Integrated Circuit Conf.*, pp. 4.2.1-4, San Diego, CA, May 1991.
3. W.-J. Hsu, C.-C. Shih, B. J. Sheu, "RELY: A reliability simulator for VLSI circuits," *Proc. IEEE Custom Integrated Circuit Conf.*, pp. 27.4.1-4, Rochester, NY, May 1988.
4. W.-J. Hsu, B. J. Sheu, V. Tyree, "Digital and analog integrated-circuit design with built-in reliability," *Proc. IEEE Int. Conf. on Computer Design*, pp.496-499, Cambridge, MA, Oct. 1989.
5. B. J. Sheu, W.-J. Hsu, V. Tyree, "Reliabiilty assurance of application-specific microelectronic circuits," *Proc. IEEE Reliability and Maintainability Symp.*, pp. 381-388, Los Angeles, CA, Jan. 1990.
6. B. J. Sheu, W.-J. Hsu, "Modeling requirements for computer-aided VLSI circuit reliability assessment," *Proc. IEEE University/Government/Industry Symp.*, pp. 199-204, Westborough, MA, Jun. 1989.
7. B. J. Sheu, C.-P. Wan, W.-J. Hsu, M. C. Hsu, "Determination of process-dependent critical SPICE parameters for application-specific ICs," *Proc. IEEE Conf. on Microelectronic Test Structures*, pp. 73-78, Anaheim, CA, Feb. 1988.
8. W.-J. Hsu, B. J. Sheu, "Computer-aided VLSI reliability studies," Tech. Dig. DARPA Wafer Reliability Workshop, pp. 195-206, Lake Tahoe, CA, Oct. 1987.
9. W.-J. Hsu, C.-C. Shih, B. J. Sheu, "Cicuit reliability simulation for ASIC design," Tech. Dig. DARPA Wafer Reliability Workshop, pp. 233-243, Lake Tahoe, CA, Oct. 1987.

Appendix B

List of Symbols

A	fitted substrate current prefactor parameter
A_f	field acceleration factor
A_i	degradation prefactor parameter
A_V	voltage gain
a	substrate current prefactor parameter
B	fitted substrate current exponent parameter
C_1	gate current process-dependent parameter
C_2	substrate current process-dependent parameter
D_i	degradation function for parameter P_i
E	stress field
E_a	activation energy
E_i	effective field in impact ionization region
E_m	maximum channel electric field
E_{sat}	electric field at velocity saturation
E_T	tangential electric field in the impact ionization region
E_{Ti}	average tangential electric field in the impact ionization region
E_0	operating field
g_m	transistor transconductance
Ig	gate current
I_{ds}	drain current
I'_{ds}	normalized drain current
I'_{sub}	normalized substrate current
$I_{sub,AC}$	average substrate current under AC bias condition
$I_{sub,DC}$	substrate current under DC bias condition
J_{eff}	effective current density
k	Boltzmann's constant
k_1	body-effect coefficient including short- and narrow- channel effects
k_2	source and drain depletion charge sharing effect coefficient
L	drawn channel length
MTTF	electromigration mean-time-to-failure factor
$MTTF_{TDDB}$	TDDB mean-time-to-failure factor
m_i	current-related degradation exponent parameter
N_A	channel doping concentration
n	current density dependent parameter

n_i	time-related degradation exponent parameter
P	power dissipation
q	elementary charge
r	number of time intervals
R_i	initial metal interconnect resistance
R_t	metal interconnect resistance at time t
S	stress function
$S_{Q\|P}$	sensitivity function of variable Q with respect to variable P
t	operating time
T	test temperature in degree Kelvin
T_j	reliability simulation time interval
T_0	normal circuit operating temperature in degree Kelvin
U_0	vertical field mobility degradation coefficient
U_{0B}	sensitivity of U_0 to the substrate bias
U_{0Z}	U_0 at zero substrate bias
U_1	carrier velocity saturation coefficient
U_{1B}	sensitivity of U_1 to the substrate bias
U_{1D}	sensitivity of U_1 to the drain bias at $V_{ds} = V_{DD}$
U_{1Z}	U_1 at zero substrate bias
V_{FB}	flat-band voltage
V_{bs}	substrate-to-source voltage
V_{ds}	drain-to-source voltage
V_{dsat}	drain saturation voltage
V_{gs}	gate-to-source voltage
V_p	channel potential at the boundary between low-field gradual channel to high field impact ionization region
V_{th}	threshold voltage
W	drawn channel width
α	electromigration cross-section dependent parameter
α_{TDDB}	TDDB pre-exponential parameter
ΔL_i	length of impact ionization region
ΔP_{AC-DC}	AC degradation factor
ΔP_i	change in transistor parameter P_i
ΔR_i	change in metal interconnect resistance R_i
ε_{Si}	silicon dielectric constant
ε_{SiO_2}	silicon dielectric constant
λ	hot-electron mean-free-path

μ_0	intrinsic surface mobility
μ_S	μ_0 at zero substrate bias and V_{ds}=V_{DD}
μ_{SB}	sensitivity of μ_0 to the substrate bias at V_{ds} = V_{DD}
μ_{SD}	sensitivity of μ_0 to the drain bias at V_{ds} = V_{DD}
μ_Z	μ_0 at zero substrate bias and drain biases
μ_{ZB}	sensitivity of μ_0 to the substrate bias at V_{ds} = V_{DD}
Φ	circuit performance function
Φ_S	surface potential at strong inversion
ϕ_b	barrier energy at the Si–SiO_2 interface
ϕ_i	minimum required energy for a carrier to cause impact ionization
η_0	drain-induced barrier lowering coefficient
η_B	sensitivity of η_0 to the substrate bias
η_D	sensitivity of η_0 to the drain bias
η_Z	η_0 at zero substrate bias and V_{ds} = V_{DD}

Appendix C

Substrate Current Models

C1. Substrate Current Model - Toshiba Corp. (1986)

Symbols

I_{sub} : substrate current
I_{ds} : drain current
V_{ds} : drain-to-source voltage
V_{gs} : gate-to-source voltage
V_{bs} : bulk-to-source voltage
V_{dsat} : saturation voltage
V_{th} : threshold voltage
L_{eff} : effective channel length
E_{sat} : electric field at velocity saturation

Reference:

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The Model:

(I) Analytical Expressions:

$$I_{sub} = I_{ds} \cdot a \cdot \left(\frac{V_{ds} - V_{dsat}}{V_o}\right)^b$$

where

$$a = P_1 - P_2 \cdot V_{ds}$$
$$b = P_3$$
$$V_{dsat} = \frac{V_{gsth} \cdot L_{eff} \cdot E_{sat}}{V_{gsth} + L_{eff} \cdot E_{sat}}$$
$$V_{gsth} = V_{gs} - V_{th} - P_4 \cdot V_{bs} - P_5 \cdot V_{gs}$$
$$E_{sat} = P_6 + P_7 \cdot V_{gs}$$
$$V_o = 1$$

(II) Parameters

(a) substrate current parameters

parameter	unit	reported value
P_1	(V^{-1})	$2.24 \cdot 10^{-5}$

P_2	(V^{-1})	$0.1\cdot10^{-5}$
P_3	(-)	6.4
P_4	(-)	0.13
P_5	(-)	0.25
P_6	(V/m)	$1.10\cdot10^{7}$
P_7	(m^{-1})	$0.25\cdot10^{7}$

(b) parameters from drain current expressions:

L_{eff} : effective channel length(m)

Note: SPICE level 3 model is suggested for the drain current.

C2. Substrate Current Model - Intel (1982)

Symbols

I_{sub} : substrate current

I_{ds} : drain current

V_{ds} : drain-to-source voltage

V_{gs} : gate-to-source voltage

ΔL : size of the impact ionization region

A,B : impact ionization constants

E_T : average tangential electric field in the impact ionization region

V_P : channel potential at the boundary between the "gradual channel region" and the "impact ionization region"

N_A : channel doping

C_{ox} : gate capacitance/unit area

Reference:

[1] Jerry Mar, Sheau-Suey Li and Swei-Yam Yu,"Substrate Current Modeling for Circuit Simulation," *IEEE Trans. on Computer-Aided Design,* vol. 1, no. 4, pp. 183-186, Oct. 1982.

The Model:

(I) Analytical Expressions :

$$I_{sub} = I_{ds} \cdot \Delta L \cdot A \cdot e^{-B/E_T}$$

where

$$\Delta L = \sqrt{\frac{2\varepsilon_{si}(V_{ds}-V_P)}{qN_A}}\left(1 - \frac{\varepsilon_{SiO_2}}{\varepsilon_{Si}}\right) = 2357\sqrt{\frac{V_{ds}-V_P}{N_A}}$$

$$E_T = \sqrt{\frac{qN_A(V_{ds}-V_P)}{2\varepsilon_{Si}}} \left(\frac{\varepsilon_{Si}}{\varepsilon_{Si} - \varepsilon_{SiO_2}}\right) = 4.2426\cdot10^{-4}\sqrt{N_A(V_{ds}-V_P)}$$

$$V_P = \frac{V_{gs}-V_{th}}{1 - \frac{\varepsilon_{Si}}{a\cdot C_{ox}\cdot(L-\Delta L)}}$$

(II) Parameters

(a) substrate current parameters:

parameter	unit	reported value
A : impact ionization constant	(m^{-1})	$9\cdot10^8$
B : impact ionization constant	(V/m)	$1.3\cdot10^8$
a : fitting parameter	(-)	0.05 to 0.1

(b) parameters from drain current expression:

parameter	unit
t_{ox} : oxide thickness	(m)
N_A : substrate doping	(m^{-3})
V_{th} : threshold voltage	(V)
L: unbiased channel length	(m)

C3. Substrate Current Model - HP Labs. (1985)

Symbols

I_{sub} : substrate current
I_{ds} : drain current
V_{ds} : drain-to-source voltage
V_{gs} : gate-to-source voltage
V_{dsat} : saturation voltage
V_{th} : threshold voltage
L : effective channel length
A_i,B_i : impact ionization constants
E_m : maximum channel electric field
E_{sat} : electric field at velocity saturation
T_{ox} : oxide thickness
X_j : junction width

References:

[1] F.-C. Hsu, K. Y. Chiu, "Hot-Electron Substrate-Current Generation during Switching Transients," *IEEE Trans. on Electron Devices*, vol. 32, no. 2, pp. 394-399, Feb., 1985.

[2] C. Hu, "Hot-electron effects in MOSFETs," *Tech. Dig. IEEE Electron Devices Meeting*, pp. 176-1779, Washington, D.C., Dec. 1983.

The Model

(I) Analytical Expressions:

$$I_{sub} = I_{ds} \left(\frac{A_i}{A}\right)\left(\frac{E_m}{B_i}\right)e^{-B_i / E_m}$$

where

$$E_m = A \cdot (V_{ds} - V_{dsat})$$

$$V_{dsat} = L \cdot E_{sat} \cdot \frac{V_{gs} - V_{th}}{L \cdot E_{sat} + V_{gs} - V_{th}}$$

$$A = \frac{1}{\sqrt{3 T_{ox} X_j}}$$

(II) Parameters

(a) substrate current parameters:

parameter	unit	reported value
A_i : impact ionization constant	(m^{-1})	$2 \cdot 10^8$
B_i : impact ionization constant	(V/m)	$1.7 \cdot 10^8$
E_{sat} : electric field at velocity saturation	(V/m)	

(b) parameters from drain current expression:

parameter	unit
T_{ox} : oxide thickness	(m)
X_j : junction depth	(m)
V_{th} : threshold voltage	(V)
L_{eff} : effective channel length	(m)

C4. Substrate Current Model - UCB/Hu (1985)

Symbols

I_{sub} : substrate current

I_{ds} : drain current

V_{dsat} : saturation voltage

E_m : maximum channel electric field

E_{sat} : critical field at velocity saturation
β_i : impact ionization constants
Φ_i : activation energy for a hot-electron to create an impact ionization
λ : hot-electron mean-free path
q : electronic charge

Reference:

[1] C. Hu et al., "Hot-Electron-Induced MOSFET Degradation - Model, Monitor, and Improvement," *IEEE Trans. on Electron Devices*, vol. 32, no. 2, pp. 375-385, Feb. 1985.

The Model:

(I) Analytical Expressions:

$$I_{sub} = C_1 I_{ds} e^{-\beta_i / E_m}$$

and $\beta_i = \Phi_i / q\lambda$

where

$$E_m = \frac{V_{ds} - V_{dsat}}{l}$$

$$V_{dsat} = \frac{L \cdot E_{sat} \cdot V_{gs} - V_{th}}{L \cdot E_{sat} + V_{gs} - V_{th}}$$

$$l = \sqrt{3 T_{ox} X_j'}$$

(II) Parameters

(a) substrate current parameters

parameter	unit	reported value
C_1 : constant	(-)	2
β_i : impact ionization constant	(V/m)	$1.7 \cdot 10^8$
Φ_i : gained energy without collision	(eV)	1.3
λ : hot-electron mean-free-path	(m)	$7.8 \cdot 10^{-9}$
E_{sat} : critical field for velocity saturation	(V/m)	$5 \cdot 10^6$
X_j': junction depth related parameter	(m)	

(b) parameters from drain current expression:

parameter	unit
t_{ox}: oxide thickness	(m)
X_j: junction depth	(m)

C5. Substrate Current Model - UCB/Ko (1986)

Symbols

I_{sub} : substrate current
I_{ds} : drain current
V_{ds} : drain-to-source voltage
V_{gs} : gate-to-source voltage
V_{bs} : bulk-to-source voltage
V_{dsat} : saturation voltage
V_{th} : threshold voltage
L : channel length
A_i : impact ionization constants
B_i : impact ionization constants
l_c : substrate-current-related empirical parameter
E_{crit} : extracted electric field parameter from measured V_{dsat}

References:

[1] M. M. Kuo, et al, "Quasi-Static Simulation of Hot-Electron-Induced MOSFET Degradation Under AC (Pulse) Stress," *Tech. Dig. IEEE Electron Devices Meeting*, pp. 47-50, Washington, D.C., Dec. 1987.

[2] Peter Lee, "BSIM - Substrate Current Modeling," *University of California, Berkeley, ERL Memo* UCB/ERL M86/49, July 1986.

[3] T. Y. Chan, P. K. Ko, and C. Hu,"A Simple Method to Characterize Substrate Current in MOSFETs," *IEEE Trans. Electron Device Letters*, vol. 5, no. 12, pp. 505-507, Dec. 1984.

The Model :

(I) Analytical Expressions :

$$I_{sub} = \frac{A_i}{B_i} I_{ds} \cdot (V_{ds} - V_{dsat}) \cdot e^{-\frac{B_i l_c}{(V_{ds} - V_{dsat})}}$$

where

$$V_{dsat} = \frac{E_{crit} \cdot L \cdot (V_{gs} - V_{th})}{E_{crit} \cdot L + (V_{gs} - V_{th})}$$

$$E_{crit} = E_{crit0} + E_{critg} \cdot V_{gs} + E_{critb} \cdot V_{bs}$$

$$l_c = \sqrt{t_{ox}} \left[l_1 + \frac{l_2}{V_{gs}+2} \right]$$

$$l_1 = l_{c0} + \frac{l_{c1}}{V_{bs}-4} + \left[l_{c2} + \frac{l_{c3}}{V_{bs}-4} \right] \cdot V_{ds}$$

$$l_2 = l_{c4} + \frac{l_{c5}}{V_{bs}-4} + \left[l_{c6} + \frac{l_{c7}}{V_{bs}-4}\right]\cdot V_{ds}$$

(II) Parameters

(a) substrate current parameters :

parameter	unit	reported value
A_i : impact ionization constant	(m^{-1})	$2\cdot10^8$
B_i : impact ionization constant	(V/m)	$1.7\cdot10^8$
E_{crit0} E_{crit0l} E_{crit0w}	(V/m)	
E_{critg} E_{critgl} E_{critgw}	(m^{-1})	
E_{critb} E_{critbl} E_{critbw}	(m^{-1})	
l_{c0} l_{c0l} l_{c0w}	(m)	
l_{c1} l_{c1l} l_{c1w}	(m)	
l_{c2} l_{c2l} l_{c2w}	(m)	
l_{c3} l_{c3l} l_{c3w}	(m)	
l_{c4} l_{c4l} l_{c4w}	(m)	
l_{c5} l_{c5l} l_{c5w}	(m)	
l_{c6} l_{c6l} l_{c6w}	(m)	
l_{c7} l_{c7l} l_{c7w}	(m)	

(b) parameters from drain current expression:

parameter	unit
L : effective channel length	(m)

Appendix D

Program Listing of Substrate Current Parameter Extraction Software

```
/*************************************************************************************
This program takes in the mesured data file including terminalvoltages, drain current, and substrate current.
Linearly fitting ofthe substrate current model is performed and thefitted impact ionization parameters with
correlation coefficient are returned . Values of Esat are determined iteratively using binary search. This pro-
gram is used as an alternative to a modified SUXES program.
*************************************************************************************/

# include <stdio.h>
# include <math.h>
# define ITMAX 100
# define EPS 3.0e-7
# define CORR 0.999
# define SIZE 500
#define LSIZE 5000

FILE *ifp, *ofp;
char infile[20], ofile[20], ofile2[20], ofile3[20], line[LSIZE];
char *targv[100];
int mwt, ndata, targc;
double et[SIZE],x[SIZE],y[SIZE];
double vds,vbs,vgs,ids,isub, vp;
double vth, length, nsub, esat_ini,esat;
double exp();

main()
{
        int i;
        double sig[SIZE],*intercept, *slope, *siga,*sigb,*chi2,*q, *rab;
        char tmpstr[20];

        printf("Enter input file: ");
        scanf("%s", infile);
        strcpy(ofile,infile);
        strcat(ofile,".log_et");
        strcpy(ofile2,infile);
        strcat(ofile2,".sim_isub");
        strcpy(ofile3,infile);
```

```
strcat(ofile3,".isubprm");
printf("Enter channel length (um): ");
scanf("%s", tmpstr);

length=atof(tmpstr);
length=1e-4*length;/*cm*/
printf("Enter zero-bias threshold voltage: ");
scanf("%s", tmpstr);
vth=fabs(atof(tmpstr));
printf("Enter Nsub (1/cm**3): ");
scanf("%s", tmpstr);
nsub=atof(tmpstr);

while (esat >= 0.0) {
        printf("Enter Esat (V/cm) (e.g. 15e4): ");
        scanf("%s", tmpstr);
        esat=atof(tmpstr);
        intercept=(double *) malloc(sizeof(intercept));
        slope=(double *) malloc(sizeof(slope));
        siga=(double *) malloc(sizeof(siga));
        igb=(double *) malloc(sizeof(sigb));
        chi2=(double *) malloc(sizeof(chi2));
        q=(double *) malloc(sizeof(q));
        rab=(double *) malloc(sizeof(rab));

        /*add Esat search algorithm here*/
        procdata();/*calculate vp[i], et[i]*/
        fitline(x,y,ndata,intercept,slope,siga,sigb,chi2,rab);
        /*output fitted data*/
        ofp=fopen(ofile3, "w");
        fprintf(ofp,"* Substrate current model parameters - Modified Mar's model\n");
        fprintf(ofp,"* Esat in V/cm, Ai1 in cm**-1 and Bi1 in V/cm\n");
        fprintf(ofp,".model isub isubmod1 modsub=2 esat=%e ai1=%e\n+ bi1=%e\n",
                esat,exp(*intercept)/5.e-6,-1.0*(* slope));
        fclose(ofp);

        printf("Esat=%e\n",esat);
        printf("Intercept(log(delta_L*A)) =%eSlope=%e\n",*intercept, *slope);
        printf("(delta_L*A) =%eB=%e\n",exp(*intercept), -1.0*(*slope) );
        printf("sigma_a=%e sigma_b=%e\n",*siga, *sigb);
        printf("chi**2=%e \n",*chi2);
        printf("rab=%e \n",*rab);
```

```
			simdata(*intercept,*slope);
			free(intercept);
			free(slope);
			free(siga);
			free(sigb);
			free(chi2);

			free(q);
		}
}

/*process input data*/
procdata()
{
		int i;

		i=0;
		/*add vth later*/
		ifp = fopen (infile, "r");
		ofp = fopen (ofile, "a");
		fprintf(ofp,"# Esat=%e\n", esat);
		fprintf(ofp,"# 1/Et[i] (in cm/V) log(Isub/Ids)\n");
		while (fgets(line, LSIZE, ifp) != NULL) {
			if(line[0]=='#') continue;
			if(line[0]=='&') {
			fprintf(ofp, "%s", line);
			continue;
			}
			parseline(line);
			if (targc !=5) {
			printf("Input file format error: expect 5 col. of data!\n");
			exit (1);
			}
			vds=fabs(atof(targv[0]));/*absolute value for n & pmos*/
			vgs=fabs(atof(targv[1]));
			vbs=fabs(atof(targv[2]));
			ids=fabs(atof(targv[3]));
			isub=fabs(atof(targv[4]));
			if (vds < vgs || vgs < vth) continue; /*ignore*/
			vp=(vgs-vth)*length*esat/(length*esat+(vgs-vth));/*V*/
			et[i]=4.1427e-4*sqrt(nsub*(vds-vp));/* V/cm */
			x[i]=1.0/et[i];
			y[i]=log(isub/ids);
```

```
		fprintf(ofp, "%e %e\n", 1.0/et[i], y[i]);
		++i;
	} /*while*/
	fclose(ifp);
	fclose(ofp);
	ndata=i;
}
/*simulated substrate current based on extracted data*/
simdata(a,b)
double a, b;

	{
	int i;
	double delta_l;

	i=0;
	ifp = fopen (infile, "r");
	ofp = fopen (ofile2, "w");
	fprintf(ofp,"# Simulated Isub\n");
	fprintf(ofp,"# L=%e cm, Nsub=%e cm**-3, Vto=%f\n", length, nsub, vth);
	fprintf(ofp,"# delta_L*A=%e B=%e\n", exp(a), -1.0*b);
	fprintf(ofp,"# Esat=%e\n", esat);
	while (fgets(line, LSIZE, ifp) != NULL) {
		if(line[0]=='#') continue;
		if(line[0]=='&') {
		fprintf(ofp, "%s", line);
		continue;
		}
		parseline(line);
		if (targc !=5) {
		printf("Input file format error: expect 5 col. of data!\n");
		exit (1);
		}
		vds=fabs(atof(targv[0]));
		vgs=fabs(atof(targv[1]));
		vbs=fabs(atof(targv[2]));
		ids=atof(targv[3]);/*preserve minus sign for pmos*/
		vp=(vgs-vth)*length*esat/(length*esat+(vgs-vth));/*V*/
		delta_l=2414*sqrt((vds-vp)/nsub);/*cm*/
		et[i]=4.098e-4*sqrt(nsub*(vds-vp));/* V/cm */
		isub = ids*exp(a)*exp(b/et[i]);
		fprintf(ofp, "%e %e\n", vgs, isub);
		++i;
	} /*while*/
```

```
	fclose(ifp);
	fclose(ofp);
}
/*fit n data pairs into a straight line*/
fitline(x,y,ndata,,a,b,siga,sigb,chi2,rab)
double *a, *b, *siga, *sigb, *chi2, *rab;
double x[], y[];
{
	int i;
	doublet, sxoss, sx=0.0, sy=0.0, st2=0.0, ss, sigdat;
	double sx2=0.0,sy2=0.0,sxy=0.0,xa,ya;

	double temp;
	d
	/*a=(double *) malloc(sizeof(a));
	b=(double *) malloc(sizeof(b));
	siga=(double *) malloc(sizeof(siga));
	sigb=(double *) malloc(sizeof(sigb));
	chi2=(double *) malloc(sizeof(chi2));
	q=(double *) malloc(sizeof(q));*/

	*b=0.0;
	for (i=0;i<ndata;++i) {
		sx += x[i];
		sy += y[i];
		sx2 += x[i]*x[i];
		sy2 += y[i]*y[i];
		sxy += x[i]*y[i];
	}
	ss=ndata;
	sxoss=sx/ss;/*Sx/S*/
	for (i=0;i<ndata;++i) {
		t=x[i]-sxoss;
		st2 += t*t;
		*b += t*y[i];
	}
	xa=sx/ss;
	ya=sy/ss;
	*b /=st2;
	*a = (sy-sx*(*b))/ss;
	*rab = (sxy-sx*sy/ss)/sqrt((sx2-sx*sx/ss)*(sy2-sy*sy/ss));
	*siga=sqrt((1.0+sx*sx/(ss*st2))/ss);
	*sigb=sqrt(1.0/st2);
	*chi2=0.0;
```

```
	for (i=0;i<ndata;++i) {
		temp=(y[i]-(*a)-(*b)*x[i]);
		*chi2 +=temp*temp;
	}
	sigdat=sqrt((*chi2)/(ndata-2));
	*siga *= sigdat;
	*sigb *= sigdat;

	free(a);
	free(b);
	free(siga);
	free(sigb);
	free(chi2);
	free(q);

}
/* parse input line into tokens, filling up targv and setting targc */
parseline(line)
register char *line;
{
	register char **carg = targv;
	register char ch;

	targc = 0;
	while (ch = *line++) {
		if (ch <= ' ') continue;
		targc++;
		*carg++ = line-1;
		while ((ch = *line) && ch > ' ') line++;
		if (ch) *line++ = '\0';
	}
	*carg = 0;
}
```

Appendix E

The RELY Program Reference

****

The RELY program is written in the C programming language. The present version comprises about 4800 lines of code. The program has been compiled on a SUN 4/60 SparcStation-1 running SunOS Release 4.0.3c.

****

E.1 List of Files and Functions

Program Files

create_input.c

create_input(), create_input3().

err.c

err_msg(err_flag), printflag().

hotsim.c

hotsim(), printhotstr(number).

prehspice.c

prehspice(), check_err(), store_mosprm(), store_keymos(), store_keyrem().

rely.c

main(argc,argv), printhead(), check_file().

stress_monitor.c

read_isubprm(), stress_monitor(), isub(modtype).

util.c

capital(), itoa(number,string), reverse(string), parseline(string,length), getline(fp,s,lim), svalue(s).

Preprocessor Files

isubmod.h

This file sets up the substrate current model and its parameters.

model.h

The data format of the substrate current model is described in this file.

prehspice.h

The data format for preprocessing the initial input deck and creating intermediate HSPICE input decks is given in this file.

rely.h

The global data format and values of various constants are defined in this file.

E.2 Individual Function Descriptions

create_input()

This function uses information from the user input deck to generate a new input deck for HSPICE. After running HSPICE, the output from this deck gives the DC drain current at the specified node voltages for the target transistors.

create_input3()

This function is called when a transient analysis is requested by the user. It creates an HSPICE input deck which is used to perform the transient analysis and obtain the voltages of all nodes in the circuit. These node voltages are printed in groups of 4 into intermediate output files that are created by the program.

err_msg(err_flag)

This function is called to print out an error message when an error is detected. (some more infor).

printflag()

Errors in the use of commands or keywords are flagged and corresponding mesages are printed out by this function.

hotsim()

Within this function the program flow for the substrate current calculation is controlled. Depending on the type of analysis requested by the user, the sequence of calling the preprocessing, HSPICE running and output filtering modules is selected correctly by this function.

printhotstr()

Various messages to the user are printed out by this function to monitor the progress of the program run.

prehspice()

This function performs the preprocessing of the initial input deck.

check_err()

The format of special commands that are unique to RELYS is verified in this function.

store_mosprm()

Information on all the MOS transistors in the user input deck is placed in a data array by this function.

store_keymos()

This function stores information on only the target MOS transistors in a data array.

main(argc,argv)

This is the main program. It manages the user interface by prompting the user for information such as file names and performs high-level control of the program flow.

printhead()

This function prints out a header with the name of the program and the version number.

check_file()

Before opening an output file this function verifies if a file with the specified file name already exists. If it does, it gives the user the choice of specifying a new file name or of overwriting the old file.

read_isubprm()

Depending on the substrate current model that has been specified, this function reads the relevant data and stores it in a specific array.

stress_monitor()

This function reads the intermediate output files that HSPICE creates and filters out information such as node voltages and branch current that may be required in subsequent steps of the program.

isub(modtype)

This function contains the substrate current model equations. It is called for the computation of the substrate current depending on the model requested by the user.

capital()

To make the intermediate files created by RELYS to have a uniform format, this function is used to change all character strings to upper case.

itoa(number,string)

This functions converts an integer to a string.

reverse(string)

This function takes in a character string and returns the same string in a reverse order.

parseline(string,length)

The character string of specifed length that is given to this function is parsed and each word is stored in an element of an array.

getline(fileptr,

This function reads a single line from a file.

svalue(string)

This function translates character symols into corresponding multipliers, such as "m" and "u" to 0.001 and 0.000001.

Appendix F

Example Circuit Input File

Example - 1: CMOS Inverter

```
cmos inverter
m1 2 1 0 0 cmosn w=2.4u l=0.5u ad=2.4p as=2.4p pd=4.4u ps=4.4u
m2 2 1 3 3 cmosp w=4.8u l=0.5u ad=4.8p as=4.8p pd=5.8u ps=5.8u
* sources
vdd 3 0 5
v1 1 0 pulse(0 5 1ns 2ns 2ns 10ns 50ns)
c1 2 0 .2pf
* analysis
tran .2ns 20ns
.print hot isubmodn hotmod m1
*
* model parameters
* hot-carrier parameters
***********************************************************
* substrate current parameters
.model isub isubmodn modsub=1
+ p1=2.24e-5 p2=0.1e-5 p3=6.4 p4=0.13 p5=0.25 p6=1.1e7 p7=0.25e7
**********************************************************
* degradation parameters
.degtime dec 3. 1e6 1e9
.model hot hotmod1 modhot=2 mvto=2.05 avto=-8 nvto=1.42
+ mbeta=1.59 abeta=-11.3 nbeta=0.46
+ mgamma=3.28 agamma= - 3.14 ngamma=0.16
**********************************************************
* 0.5um SPICE prm*
.model cmosn nmos (level = 3
+ tox = 12.5n uo = 449.3 vto = 0.925
+ nsub = 1.11e17 rsh = 306.1 xj = 142.6n ld = 81.5n theta = 78.1m
+ nfs = 1.69e12 vmax = 158.9k kappa = 0.0 delta = 0.0
+ cj = 870u pb = 0.577 mj = 0.296 cjsw = 1.51n mjsw = 0.317 is = 0.0)
.model cmosp pmos (level = 3
+ tox = 12.5n uo = 130.5 vto = -0.99
+ nsub = 1.27e17 rsh = 698.9 xj = 68.7n ld = 110.8n theta = 119.3m
+ nfs = 1.77e12 vmax = 180.5k eta = 12.3m kappa = 0.0 delta = 1.4
+ cj = 475u pb = 0.844 mj = 0.46 cjsw = 1.23n mjsw = 0.216 is = 0.0
.options itl5=0 limpts=2000
.end
```

Example - 2: Four-Input NAND Gate Cell

```
*
*Subject: One stage Four-input NAND gate
*11-14 input, 21:output 1:Vdd
m1 21 11 1 1 cmosp w=2.0u l=0.5u ad=2.0p as=2.0p pd=4.0u ps=4.0u
m2 21 12 1 1 cmosp w=2.0u l=0.5u ad=2.0p as=2.0p pd=4.0u ps=4.0u
m3 21 13 1 1 cmosp w=2.0u l=0.5u ad=2.0p as=2.0p pd=4.0u ps=4.0u
m4 21 14 1 1 cmosp w=2.0u l=0.5u ad=2.0p as=2.0p pd=4.0u ps=4.0u
m5 21 11 22 0 cmosn w=1.0u l=0.5u ad=1.0p as=1.0p pd=3.0u ps=3.0u
m6 22 12 23 0 cmosn w=1.0u l=0.5u ad=1.0p as=1.0p pd=3.0u ps=3.0u
m7 23 13 24 0 cmosn w=1.0u l=0.5u ad=1.0p as=1.0p pd=3.0u ps=3.0u
m8 24 14 0 0 cmosn w=1.0u l=0.5u ad=1.0p as=1.0p pd=3.0u ps=3.0u
*fanout=4
m11 102 21 1 1 cmosp w=2.0u l=0.5u as=2.0p ad=2.0p ps=4.0u pd=4.0u
m12 102 21 0 0 cmosn w=1.0u l=0.5u as=1.0p ad=1.0p ps=3.0u pd=3.0u
m21 102 21 1 1 cmosp w=2.0u l=0.5u as=2.0p ad=2.0p ps=4.0u pd=4.0u
m22 102 21 0 0 cmosn w=1.0u l=0.5u as=1.0p ad=1.0p ps=3.0u pd=3.0u
m31 102 21 1 1 cmosp w=2.0u l=0.5u as=2.0p ad=2.0p ps=4.0u pd=4.0u
m32 102 21 0 0 cmosn w=1.0u l=0.5u as=1.0p ad=1.0p ps=3.0u pd=3.0u
m41 102 21 1 1 cmosp w=2.0u l=0.5u as=2.0p ad=2.0p ps=4.0u pd=4.0u
m42 102 21 0 0 cmosn w=1.0u l=0.5u as=1.0p ad=1.0p ps=3.0u pd=3.0u
* sources
vdd 1 0 dc 5
vina 11 0 pwl(0 5 50p 5 130p 0 2n 0 2080ps 5 3n 5)
vinb 12 0 dc 5
vinc 13 0 dc 5
vind 14 0 dc 5
*
.ic v(21)=0 V(102)=5
*.options limpts=3000 gmin=1e-15 pivtol=1e-15
* analysis
.tran 10p 3000p 50p
.print hot isubmodn hotmodn m5 m6 m7 m8
.print hot isubmodp hotmodp m1 m2 m3 m4
*
****************************************************************
*---------Substrate current parameters-------------------------------------
.model isub isubmodn modsub =1
+ P1=2.24E-5 P2=0.1E-5 P3=6.4 P4=0.13 P5=0.25 P6=1.1E7 P7=0.25E7
.model isub isubmodp modsub =1
+ P1=2.0E-5 P2=0.8E-6 P3=4.6 P4=0.11 P5=0.23 P6=0.8E7 P7=0.25E7
****************************************************************
```

```
.degtime linear 0 1e8 5e6
.model hot hotmod1 modhot=1 MVTO=2.05 AVTO=-8.0 NVTO=1.42
+ MBETA=1.59 ABETA=-11.3 NBETA=0.46
+ MGAMMA=3.28 AGAMMA= -3.14 NGAMMA=0.16
.model hot hotmod2 modhot=1 MVTO=2.01 AVTO=-12.0 NVTO=1.04
+ MBETA=2.44 ABETA=-12.3 NBETA=0.48
+ MGAMMA=2.02 AGAMMA= -13.14 NGAMMA=0.34
****************************************************************************
*
*transistor parameters
.model cmosn nmos ( LEVEL=3
+ TOX=12.5N UO=449.3 VTO=0.925 NSUB=1.11E17 RSH=306.1
+ XJ=142.6N LD=81.5N THETA=78.1M NFS=1.69E12 VMAX=158.9K
+ KAPPA=0.0 DELTA=0.0 CJ=870U PB=0.577 MJ=0.296 CJSW=1.51N
+ MJSW=0.317 IS=0.0)
*
.model cmosp pmos (LEVEL=3
+ TOX=12.5N UO=130.5 VTO=-0.990 NSUB=1.27E17 RSH=698.9
+ XJ=68.7N LD=110.8N THETA=119.3M NFS=1.77E12 VMAX=180.5K
+ KAPPA=0.0 DELTA=1.40 CJ=475U PB=0.844 MJ=0.460 CJSW=1.23N
+ MJSW=0.216 IS=0.0)
*
.end
```

Example 3: SRAM circuit

```
sram characteristics
*ram cell
m1 2 3 0 0 cmosn w=1.0u l=0.5u ad=1p as=1p pd=3u ps=3u
m2 3 2 0 0 cmosn w=1.0u l=0.5u ad=1p as=1p pd=3u ps=3u
m3 2 6 0 0 cmosn w=0.5u l=0.5u ad=1p as=1p pd=3u ps=3u
m4 3 6 4 0 cmosn w=0.5u l=0.5u ad=1p as=1p pd=3u ps=3u
m5 2 3 1 1 cmosp w=0.5u l=0.5u ad=1p as=1p pd=3u ps=3u
m6 3 2 1 1 cmosp w=0.5u l=0.5u ad=1p as=1p pd=3u ps=3u
* precharging circuit
m11 1 11 12 0 cmosn w=2.5u l=0.5u ad=2.5p as=2.5p pd=4.5u ps=4.5u
m12 12 11 5 5 cmosn w=5u l=0.5u ad=5p as=5p pd=7u pd=7u
m13 12 11 4 4 cmosn w=5u l=0.5u ad=5p as=5p pd=7u pd=7u
m14 5 11 4 0 cmosn w=20u l=0.5u ad=20p as=20p pd=22u ps=22u
*1: input, 2:output 3:vdd 4:vss
*inv
m23 23 21 1 1 cmosp w=4.0u l=0.5u ad=4p as=4p pd=6u ps=6u
m24 23 21 0 0 cmosn w=2.0u l=0.5u ad=2p as=2p pd=4u ps=4u
m25 24 22 1 1 cmosp w=4.0u l=0.5u ad=4p as=4p pd=6u ps=6u
m26 24 22 0 0 cmosn w=2.0u l=0.5u ad=2p as=2p pd=4u ps=4u
*tristatable inv
m15 31 21 1 1 cmosp w=4u l=0.5u ad=4p as=4p pd=6u ps=6u
m16 33 24 31 31 cmosp w=4u l=0.5u ad=4p as=4p pd=6u ps=6u
m17 33 22 32 32 cmosn w=2u l=0.5u ad=2p as=2p pd=4u ps=4u
m18 32 21 0 0 cmosn w=2u l=0.5u ad=2p as=2p pd=4u ps=4u
*
m19 41 23 1 1 cmosp w=4u l=0.5u ad=4p as=4p pd=6u ps=6u
m20 43 24 41 41 cmosp w=4u l=0.5u ad=4p as=4p pd=6u ps=6u
m21 43 22 42 42 cmosn w=2u l=0.5u ad=2p as=2p pd=4u ps=4u
m22 42 23 0 0 cmosn w=2u l=0.5u ad=2p as=2p pd=4u ps=4u
*tg
m31 43 22 4 0 cmosn w=10u l=0.5u ad=10p as=10p pd=12u ps=12u
m32 33 22 5 0 cmosn w=10u l=0.5u ad=10p as=10p pd=12u ps=12u
m33 43 24 4 1 cmosp w=10u l=0.5u ad=10p as=10p pd=12u ps=12u
m34 33 24 5 1 cmosp w=10u l=0.5u ad=10p as=10p pd=12u ps=12u
* analysis
vdd 1 0 5.0
vword 6 0 pulse(0 5.0 8ns 1ns 1ns 4ns 16ns)
vclk 11 0 pulse(0 5.0 2ns 1ns 1ns 3ns 16ns)
vwrite 22 0 pulse(0 5 8.01ns 1ns 1ns 4ns 32ns)
vdatain 21 0 pulse(0 5 40ns 1ns 1ns 4ns 64ns)
```

```
.print isub isubmodn m1 m3 m4
.print isub isubmodp m5 m6
.model isub isubmodn modsub=1
*+ p1=2.24e-5 p2=0.1e-5 p3=6.4 p4=0.13 p5=0.25 p6=1.1e7 p7=0.25e7
.model isub isubmodp modsub=1
+ p1=2.24e-5 p2=0.1e-5 p3=6.4 p4=0.13 p5=0.25 p6=1.1e7 p7=0.25e7
***************
****************
* 0.5um prm*
****************
.model cmosn nmos level = 3
+ tox = 12.5n uo = 449.3 vto = 0.925 kp=1.24e-4 gamma=0.695
+ nsub = 1.11e17 rsh = 306.1 xj = 142.6n ld = 81.5n theta = 78.1m
+ nfs = 1.69e12 vmax = 158.9k kappa = 0.0 delta = 0.0
+ cj = 870u pb = 0.577 mj = 0.296 cjsw = 1.51n
+ mjsw = 0.317 is = 0.0
* wd = 0.0
.model cmosp pmos level = 3
+ tox = 12.5n uo = 130.5 vto = -0.99 gamma=0.743
+ nsub = 1.27e17 rsh = 698.9 xj = 68.7n ld = 110.8n theta = 119.3m
+ nfs = 1.77e12 vmax = 180.5k kappa = 0.0 delta = 1.4
+ cj = 475u pb = 0.844 mj = 0.46 cjsw = 1.23n
+ mjsw = 0.216 is = 0.0
* wd = 82.2n

*
.tran 2ns 65ns
.ic v(4)=0 v(5)=5
.nodeset v(2)=4.8 v(3)=0
+ v(4)=0 v(5)=4.8 v(23)=5
+ v(24)=5 v(12)=4.2
.op
*.graph tran v(5) v(4) v(2) v(3)
.options itl5=0 itl3=100 itl4=500 limpts=5000
*.options post ingold=2
*.options gmin=1e-8 pivtol=1e-8 abstol=1u
.end
```

Appendix G

G.1 Parameter Files for SPICE Level-2 CMOS Models

```
* Extracted in May 1988 by the MOSIS Services
*MOSIS M82X
.MODEL CMOSN NMOS LEVEL=2 LD=0.331237U TOX=442.0E-10
+ NSUB=2.50165E+15 VTO=0.727393 KP=48.4E-06 GAMMA=0.369
+ PHI=0.6 UO=620 UEXP=0.109593 UCRIT=94840.6
+ DELTA=0.64863 VMAX=63412.6 XJ=0.300U LAMBDA=0.0330068
+ NFS=1E+11 NEFF=1.001 NSS=1E+12 TPG=1.000000
+ RSH=28.6200 CGDO=2.5877E-10 CGSO=2.5877E-10 CGBO=6.2066E-10
+ CJ=0.0001581 MJ=0.464900 CJSW=3.26E-10 MJSW=0.310000 PB=0.750000
+ XQC=0.4
* Weff = WDrawn - Delta_W
* The suggested Delta_W=0.7826 UM
.MODEL CMOSP PMOS LEVEL=2 LD=0.459128U TOX=442.00E-10
+ NSUB=4.29402E+15 VTO=-0.7892 KP=18.9E-06 GAMMA=0.483
+ PHI=0.6 UO=242.502 UEXP=0.275439 UCRIT=29523.9
+ DELTA=1.26247E-05 VMAX=37102 XJ=0.30U LAMBDA=0.0396894
+ NFS=2.76925E+12 NEFF=1.001 NSS=1E+12 TPG=-1.000000
+ RSH=86.449997 CGDO=3.58681E-10 CGSO=3.58681E-10 CGBO=6.3446E-10
+ CJ=0.0002738 MJ=0.504800 CJSW=5.36E-10 MJSW=0.297800 PB=0.70000
+ XQC=0.4
* Weff = WDrawn - Delta_W
* The suggested Delta_W=0.7991 UM
*
```

G.2 Parameter Files for SPICE Level-3 CMOS Models

Example-1:

```
* Extracted in Jun. 1991 by the MOSIS Services
***************************************************************************
* MOSIS N14P SPICE LEVEL-3 PARAMETERS FOR 1.2um PROCESS
***************************************************************************
.MODEL CMOSN NMOS LEVEL=3 PHI=0.600000 TOX=2.2500E-08 XJ=0.200000U TPG=1
+ VTO=0.8186 DELTA=1.7570E+00 LD=1.1340E-07 KP=9.1547E-05
+ UO=596.5 THETA=1.0850E-01 GAMMA=0.5266 NSUB=1.9680E+16
+ NFS=5.5000E+12 VMAX=1.9420E+05 ETA=6.6540E-02 KAPPA=1.1210E-01
+ RSH=116.5 CGDO=2.6106E-10 CGSO=2.6106E-10 CGBO=6.3402E-10
+ CJ=3.1146E-04 MJ=1.0667 CJSW=4.3777E-10 MJSW=0.154230 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.9970E-07
.MODEL CMOSP PMOS LEVEL=3 PHI=0.600000 TOX=2.2500E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9456 DELTA=1.5520E+00 LD=1.1720E-08 KP=3.1646E-05
+ UO=206.2 THETA=1.6900E-01 GAMMA=0.4619 NSUB=1.5140E+16
+ NFS=4.9990E+12 VMAX=4.4410E+05 ETA=1.6350E-01 KAPPA=1.0000E+01
+ RSH=129.5 CGDO=2.6981E-11 CGSO=2.6981E-11 CGBO=8.6508E-10
+ CJ=4.7864E-04 MJ=0.4973 CJSW=1.4771E-10 MJSW=0.190593 PB=0.850000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 3.1280E-07
```

Example-2

```
*Extracted in Dec. 1990 by TRW, Inc.
******************
* For 0.5um process*
******************
.MODEL CMOS NMOS LEVEL = 3
+ TOX= 12.5n UO= 449.3 VTO= 0.925
+ NSUB = 1.11e17 RSH= 306.1 XJ= 142.6n LD= 81.5n THETA= 78.1m
+ NFS= 1.69e12 VMAX = 158.9k ETA = 22.3m KAPPA= 0.0 DELTA= 0.0
+ CJ= 870u PB= 0.577 MJ= 0.296 CJSW= 1.51n
+ MJSW= 0.317 IS = 0.0
* wd = 0.0
.MODEL CMOSP PMOS LEVEL = 3
+ TOX = 12.5n UO = 130.5 VTO = -0.99
```

+ NSUB = 1.27e17 RSH = 698.9 XJ = 68.7n LD = 110.8n THETA = 119.3m
+ NFS = 1.77e12 VMAX = 180.5k KAPPA = 0.0 DELTA = 1.4
+ CJ = 475u PB = 0.844 MJ = 0.46 CJSW = 1.23n
+ MJSW = 0.216 IS = 0.0

G.3 Parameter Files for SPICE Level-4 CMOS Models

```
NM1 PM1 DU1 DU2 ML1 ML2
*
*PROCESS=hp
*RUN=n14p
*WAFER=10
*Gate-oxide thickness= 225.0 angstroms
*Geometries (W-drawn/L-drawn, units are um/um) of transistors measured were:
* 1.8/1.2, 3.6/1.2, 10.8/1.2, 3.6/3.6, 3.6/10.8
*Bias range to perform the extraction (Vdd)=5 volts
*DATE=06-10-91
*
*NMOS PARAMETERS
*
-1.04093E+00, 1.21036E-02, 5.94839E-02
 8.23794E-01,-7.49792E-25, 0.00000E+00
 1.25539E+00, 1.06514E-02, 2.56406E-02
 1.85597E-01, 4.80329E-02,-6.27418E-02
-6.90217E-03, 1.43957E-02, 9.16454E-03
 5.30471E+02,4.53242E-001,3.71837E-001
 7.80476E-02, 1.17262E-01,-6.19337E-02
 5.50861E-02, 1.22336E-01,-5.91140E-02
 5.66746E+00,-4.18211E+00, 4.53065E+01
-2.65265E-03,-4.86670E-03, 4.12438E-03
 5.86337E-04,-2.55781E-04,-7.11669E-03
-2.66457E-03,-1.43909E-04, 3.17273E-02
-1.39008E-02, 9.20089E-03, 9.69573E-03
 6.54522E+02, 9.00539E+01,-1.08281E+02
-6.48459E+00, 8.99306E+00, 6.82742E+01
 1.39295E+01, 1.71674E+01,-2.33754E+01
 2.00682E-02, 5.24336E-03,-1.54952E-02
2.25000E-002, 2.70000E+01, 5.00000E+00
5.21703E-010,5.21703E-010,3.42731E-010
1.00000E+000,0.00000E+000,0.00000E+000
1.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
*
* Gate Oxide Thickness is 225 Angstroms
*PMOS PARAMETERS
*
```

-3.47438E-01, 1.21428E-01,-9.25825E-03
7.35997E-01,-2.38789E-25, 1.49453E-24
5.91405E-01,-1.58253E-01, 1.52785E-01
-7.91690E-06,-5.25062E-03, 2.79849E-02
-1.12225E-02, 2.41533E-02, 1.39444E-02
1.94815E+02,1.76877E-001,4.74331E-001
1.38344E-01, 6.70098E-02,-6.50691E-02
-3.99382E-03, 1.13970E-01,-1.62249E-02
8.70704E+00,-1.33328E+00, 3.60333E+00
-2.28338E-03, 2.34520E-04,-7.96621E-04
1.28394E-03,-1.64516E-03,-4.36691E-03
6.20155E-03,-1.90254E-06, 5.59655E-03
4.17527E-05, 2.27273E-03, 2.17625E-03
1.94002E+02, 6.67286E+01,-1.46903E+01
7.59244E+00, 2.28400E+00, 6.62960E+00
-2.34857E-01, 3.59465E+00,-1.54543E-01
-1.11698E-02, 1.64413E-03,-3.31896E-04
2.25000E-002, 2.70000E+01, 5.00000E+00
2.03594E-010,2.03594E-010,3.74901E-010
1.00000E+000,0.00000E+000,0.00000E+000
1.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
*
*N+ diffusion::
*
116.5, 3.114600e-04, 4.380000e-10, 0, 0.8
0.8, 1.06666, 0.154, 0, 0
*
*P+ diffusion::
*
129.5, 4.786400e-04, 1.477100e-10, 0, 0.85
0.85, 0.497251, 0.190593, 0, 0
*
*METAL LAYER -- 1
*
6.030000e-02, 0, 0, 0, 0
0, 0, 0, 0, 0
*
*METAL LAYER -- 2
*
3.910000e-02, 0, 0, 0, 0
0, 0, 0, 0, 0

Appendix H

Testing of Analog Neural Array-Processor Chips

H.1 Introduction

Testing of a VLSI neural chip is a crucial task in constructing artificial neural systems. Testing of analog circuits has been a great challenge to VLSI system designers. Analog circuits process signals using continuous voltage representation. A circuit with 8-bit resolution has 256 signal levels. The mismatch among circuit cells can result in serious timing discrepancies and performance variation. The dynamic range of the analog circuit within which a linear operation can be achieved is important and has to be accurately characterized. In addition, due to the high-resolution requirement for some analog components, the manufacturing costs of these products can be dominated by the test costs.

Some testing methods for conventional analog LSI circuits, such as switched-capacitor filters, D/A and A/D converters have been reported [H.1, H.2]. However, very little effort has been directed toward testing analog chips with massively parallel architecture, such as the neural network chips. These chips have recently received much attention in image and control processing applications due to their ability to perform high-speed computation [H.3, H.4]. Concurrent with rapid advances in VLSI design and fabrication technologies, the development of an effective testing methodology for analog and mixed-signal

neural chips is urgently needed. The testing method and experimental results for a programmable VLSI neural chip are presented.

H.2 The Analog VLSI Neural Chip

Several VLSI neural chips have been reported [H.5, H.6]. The functional diagram of a general-purpose neural chip is shown in Fig. H.1. The network consists of an input buffer array, an output neuron array, and a synapse matrix. In the DRAM-type programmable neural chip, the synapse weight is stored in a capacitor and refreshed dynamically. Each output neuron with its associated synapse cells acts as a unit processor, which performs a parallelled inner-product computation.

The circuit schematic of the electrically programmable synapse cell with input buffer and output neuron is shown in Fig. H.2. A transconductance amplifier consisting of transistors M1-M4 produces synapse output current $I^s_{i,j}$, which is a function of the neuron input voltage V_j and weight voltage $V^s_{i,j}$. The input voltage V_j steers the dynamic range control current $I_{\max}$ into a current mirror which is used to bias multiple synapse cells. A two-stage operational amplifier is used to implement an analog neuron cell. The voltage gain of the output neuron can be controlled externally.

H.3 The Test Methodology

The analog neural circuit has inherently limited computational precision due to the imperfection in the analog devices. The nonlinearity of each synapse cell and the mismatch among the output neurons are important sources of

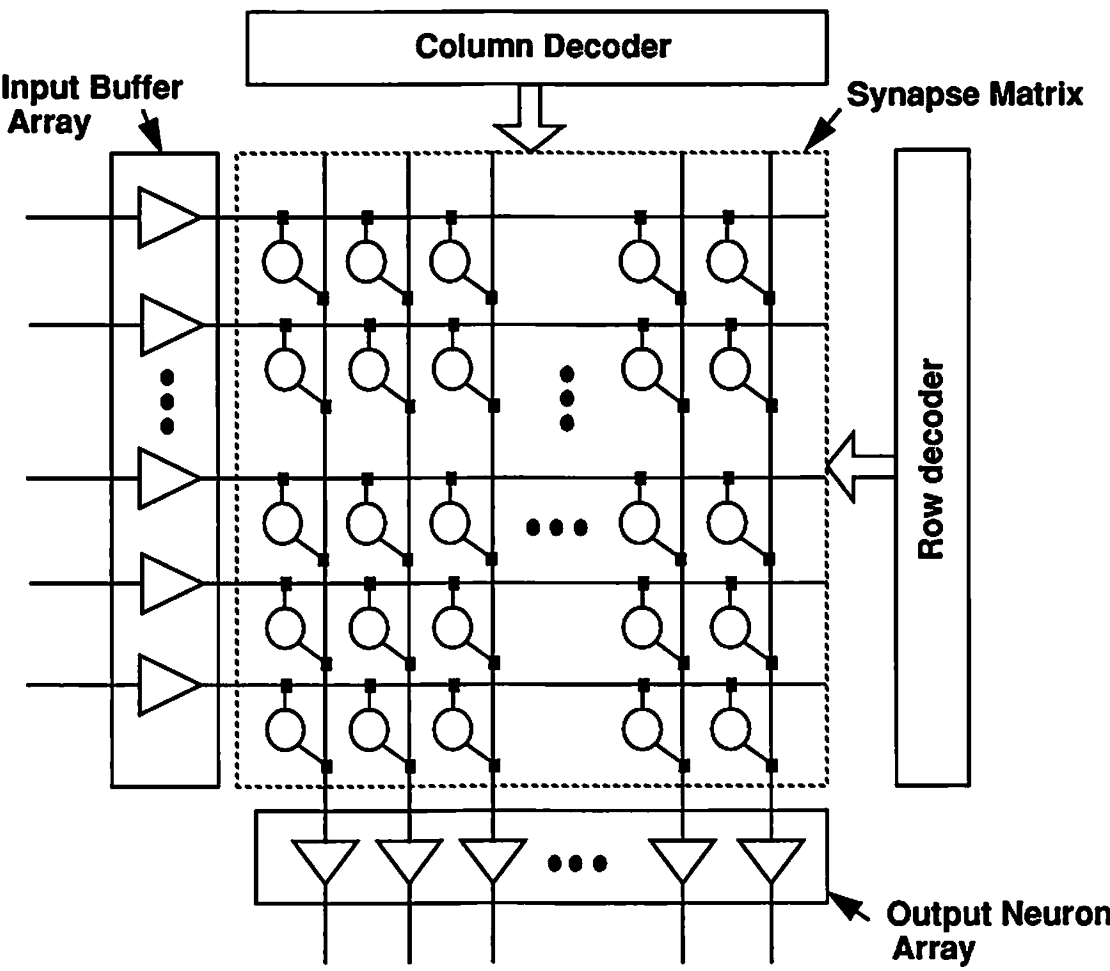


Figure H.1 Functional diagram of a neural array-processor.

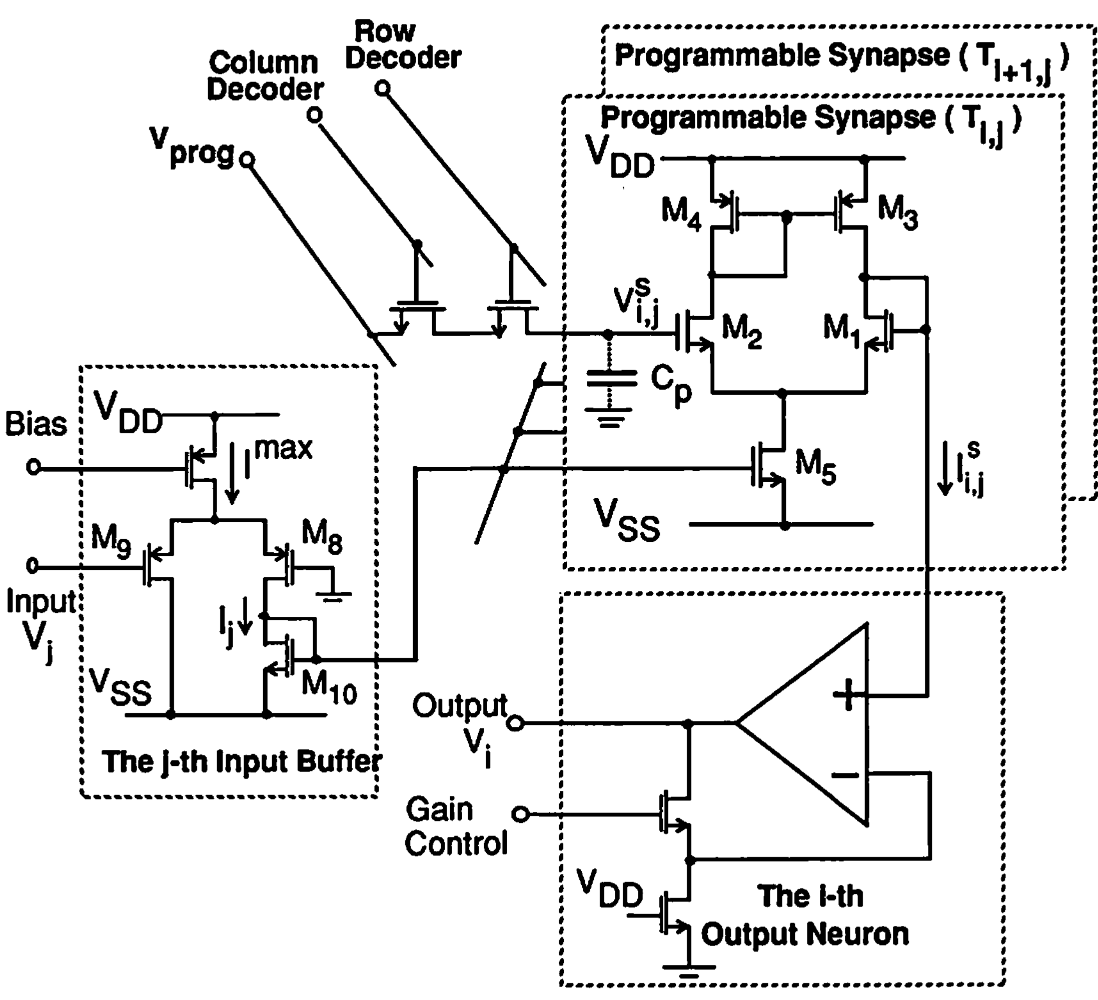


Figure H.2 Circuit schematic of the analog neural-array processor.

computational errors. The saturation behavior observed in the transfer curve of the synapse cell could limit the dynamic range of the circuit. The proposed test methodology is based upon the detection of out-of-specification faults. The following method has been developed for testing of analog neural chips. Major items to be tested include the dc transfer characteristic in a neuron cell, and the dynamic range, linearity, and charge retention in a synapse cell. Open faults and short-circuited faults are covered implicitly in the testing of the above-mentioned items.

Testability of individual analog cells is achieved through the use of unique circuit properties. It is performed by combining input vector stimuli, synapse address control and voltage gain control in the output neuron. Selection of output neurons is done by forcing a high voltage to one input neuron. All other input levels are inhibited by maintaining the input level at V_{ss}. Selection of individual synapse cell is achieved by the address decoder while the output neuron is configured as a unity-gain source follower.

The testing procedure is partitioned into parametric test and functional test. Not only is the functionality of the chip verified, but also the process variance/faults is detected. The detailed flowchart for the systematic testing methodology is shown in Fig. H.3.

H.3.1 Parametric test of neurons

The DC and AC characteristics of each single output neuron are measured in this step. The voltage transfer curves with only three different gain-controlling voltages are measured. In the high-gain configuration, a relatively

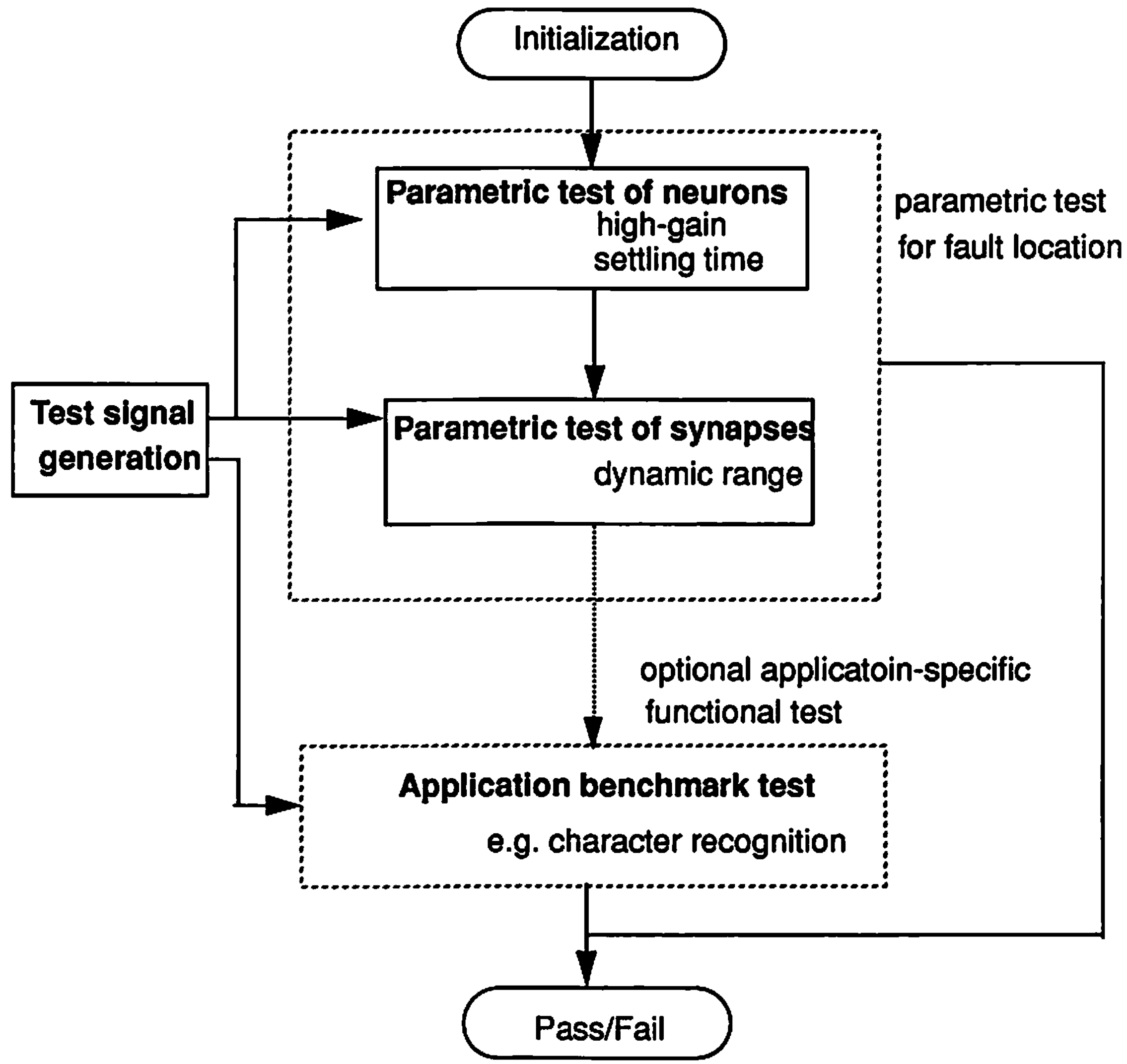


Figure H.3 Flowchart of an efficient testing method for the analog neural chips.

high voltage gain has to be achieved such that the output neuron can function as an ideal comparator. The monotonicity of the transfer curve is important while the network is operated in the learning phase. In the unity-gain configuration, the input offset voltage of the output neuron can be measured. For a differential operational amplifier, the input offset voltage can be compensated by adjusting the voltage level of the reference input which can be accessed externally. The settling time and slew rate are measured to determine the operational speed of the circuit. A typical loading of 0.5 pF is added to the neuron during the settling time and slew rate measurements.

H.3.2 Parametric test of synapses

After the output neurons have been tested, the synapse transfer characteristics can be monitored by applying a weight voltage on the synapse capacitor and measuring the output of the neuron. In this step, the output neuron operates as a unity-gain buffer. As in the digital memory testing, every synapse cell in the matrix has to be tested. Individual synapse cells can be selected through the decoder circuitry. The unselected synapses which are connected to the same output neuron are disabled by applying inhibiting voltage values to their inputs. The saturation behavior observed in the transfer curve of the synapse cell can limit the dynamic range of the synapse weight value. For a DRAM-type synapse cell, the charge retention time of the synapse cell is needed to determine the resolution of the synapse weight and the minimum refreshing clock frequency. The offset voltage resulting from the imperfections of the synapse cell is measured in order to modify the weight voltage.

H.3.3 Functional test

The testing procedures described in steps 1 and 2 form a systematic approach to characterize the basic circuit cells in the neural chips. In the functional testing step, the functionality of the complete neural chip is tested. For a programmable neural chip, one example application is used to evaluate the effect of imperfections or mismatches among the devices. A fully interconnected single-layered network to recognize printed characters is a good example. The synapse weight values are calculated according to the synapse transfer characteristics and will be kept constant during the network operation. In feedforward operation, output characteristic is compared to the target (trained) set to determine the functionality of the chip. The tolerance of imperfections or mismatchness among the analog circuit cells can be verified by using this method. Other effects such as short-circuited effects in interconnection wires and transistor terminals will appear in the measurement procedure mentioned above and cause significant degradation on circuit performance. As a result, the faulty chip can be identified.

H.4 Test System

The schematic diagram of a test system is shown in Fig. H.4. It consists of an IBM PC/AT personal computer, an HP 1650A logic analyzer, and an HP 4145B semiconductor parameter analyzer. By including a data pattern generator board and an I/O interface board, the PC/AT computer provides the input patterns for the neural chip and monitors the corresponding outputs. The HP 4145B is used to measure the transfer curves of the output neuron and the synapse cell.

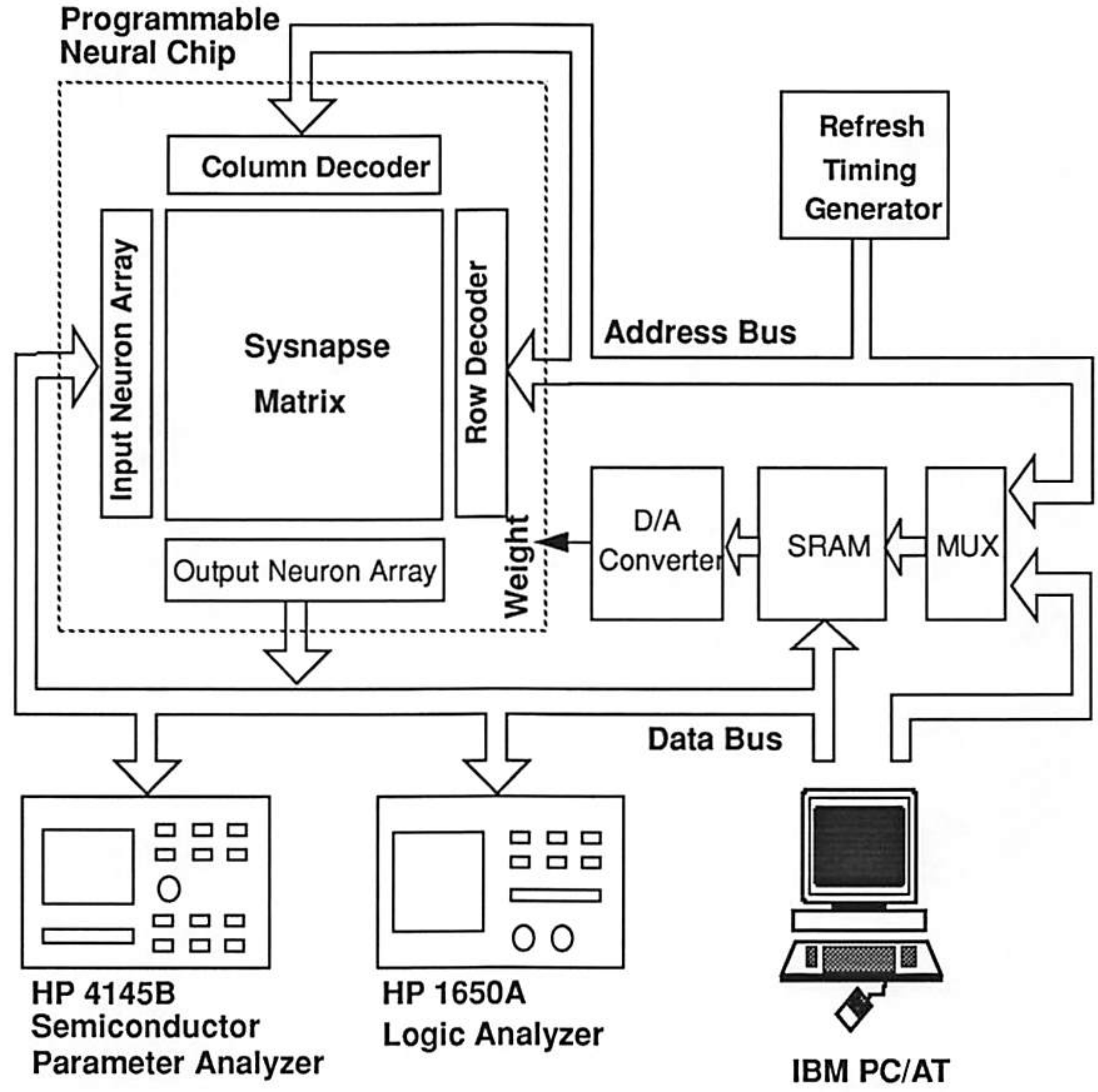


Figure H.4 Schematic of test system to characterize the programmable neural chip.

The logic analyzer is used for diagnosis and debugging of digital functions. During the chip functionality test, the required synapse weights are calculated by the computer and stored in an SRAM. A control program written in Turbo-C language with around 50 command lines can generate the addresses for SRAM writing, and control the testing procedure. The synapse weights are dynamically refreshed by reading data from the SRAM, converting them into analog voltages, and charging on the corresponding synapse capacitors. The refresh timing generator controlled by the computer can provide the refreshing addresses for the synapse matrix. With a PC/AT computer, 30 μs is needed for one I/O data transfer. For a neural chip with a 64x25 synapse matrix, and 25 neurons, 50 ms is required for functional test.

H.5 Experimental Results

The die photo of a general-purpose analog neural chip is shown in Fig. H.5. It contains 25 array processors with 64x25 synapse cells. The chip is mounted on a 108-pin PGA package. The transfer curves of the output neuron in the high-gain configuration and the low-gain (unity-gain) configuration are shown in Figs. H.6(a) and H.6(b) respectively. The maximum voltage gain is 2,400 and the offset voltage is 5 mV. Figure H.7 shows the distribution of the voltage gain of the output neurons. The total sample size under measurement is 50.

The transfer curves of one synapse cell with different bias voltages are shown in Fig. H.8. The high-gain region varies with the bias voltage. An appropriate bias voltage is selected according to the resolution requirement of the

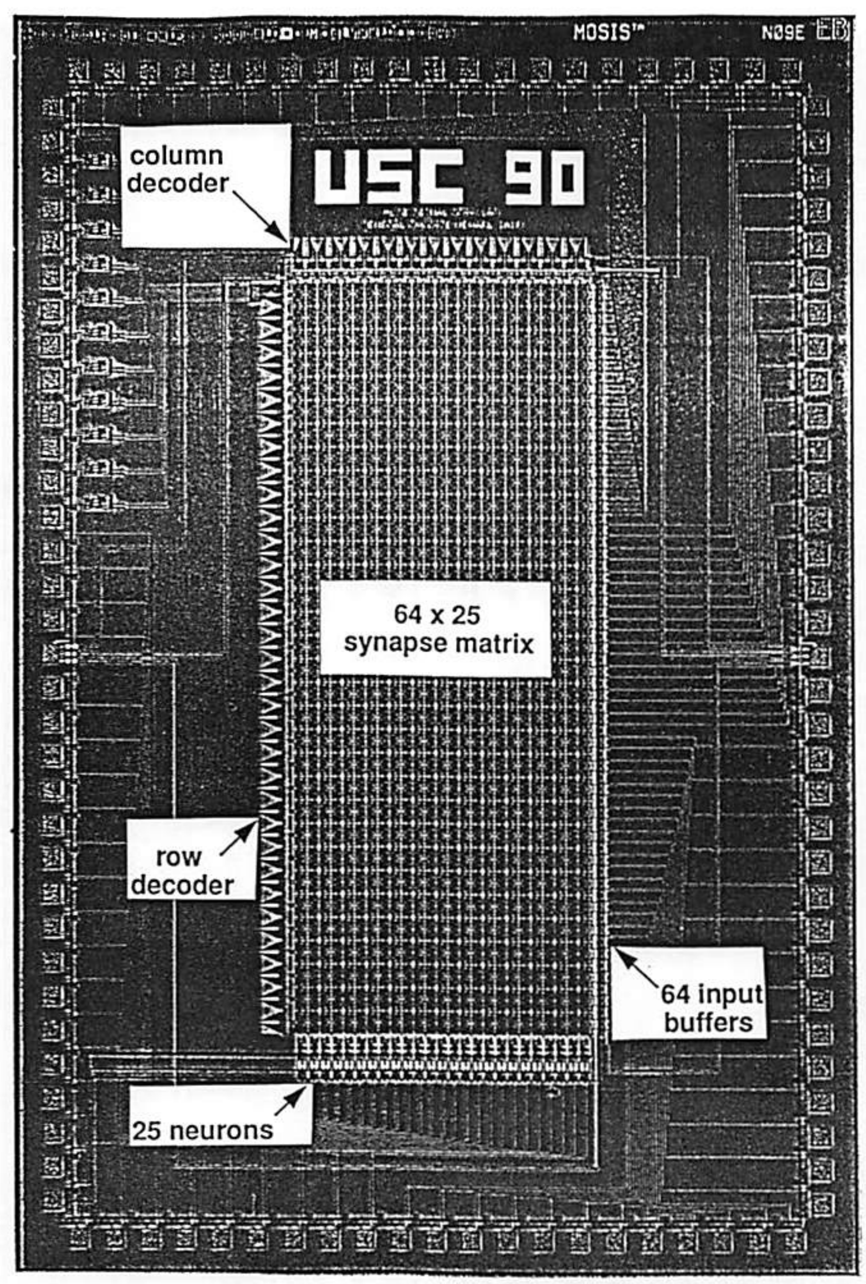
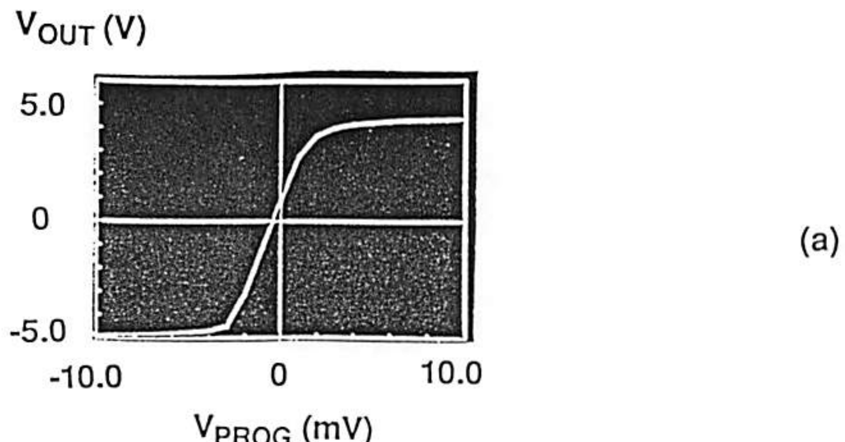


Figure H.5 Die photo of the programmable VLSI neural chip.



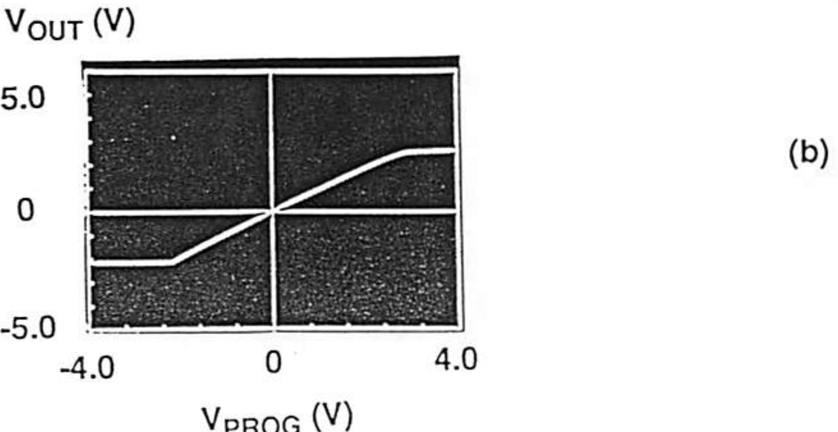
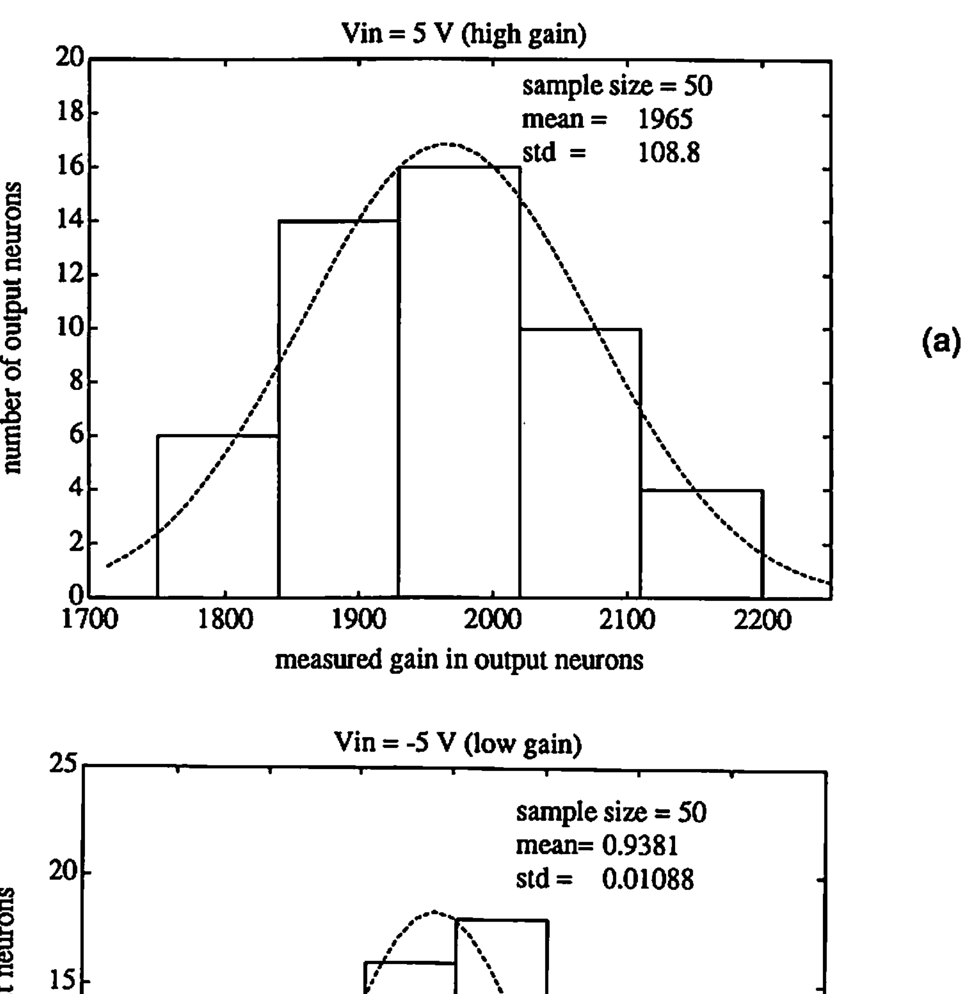


Fig. H.6 Transfer characteristics of the output neurons.
(a) High gain region.
(b) Low gain region.



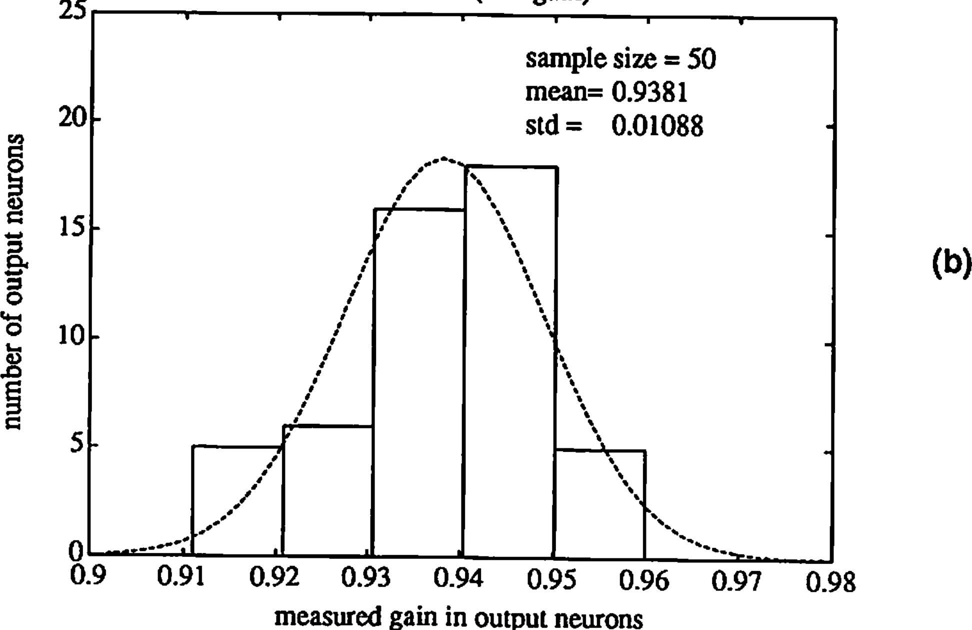


Fig. H.7 Gaussian distribution of measured voltage gain in the output neurons.
(a) High gain region.
(b) Low gain region.

weights. In the charge retention experiment, 64 synapse cells are tied together to minimize the effect of external stray capacitance. The RC time constant is about 50 sec as shown in Fig. H.9. A refreshing cycle of 0.2 sec is adequate for 8-bit synapse accuracy. Figure H.10 shows the statistical distribution of the measured synapse response to the weight value. The total sample size is 320 synapses. Comparison of the expected testing time for three published analog neural chips is listed in Table H.1. Note that test time for functional test is not included in this table. Settling time behavior in the analog circuits does not pose a limit to the speed of testing.

H.6 Conclusion

A systematic approach to test analog array-processor neural chips has been presented. Unique testing problems for analog neural chips are described and effective solutions are discussed. Based on the hierarchical methodology, testing of analog array-processor neural chips can be systematically addressed.

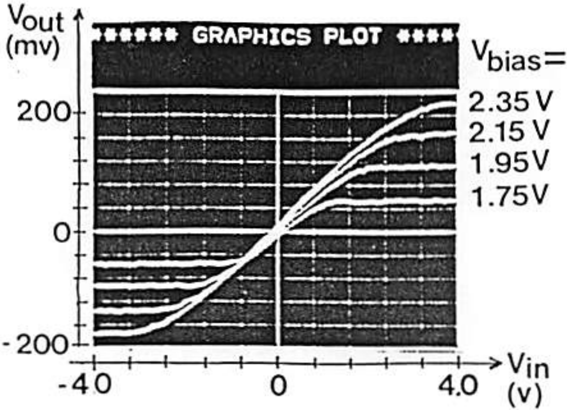


Fig. H.8 Measured synapse characteristics with different bias voltages.

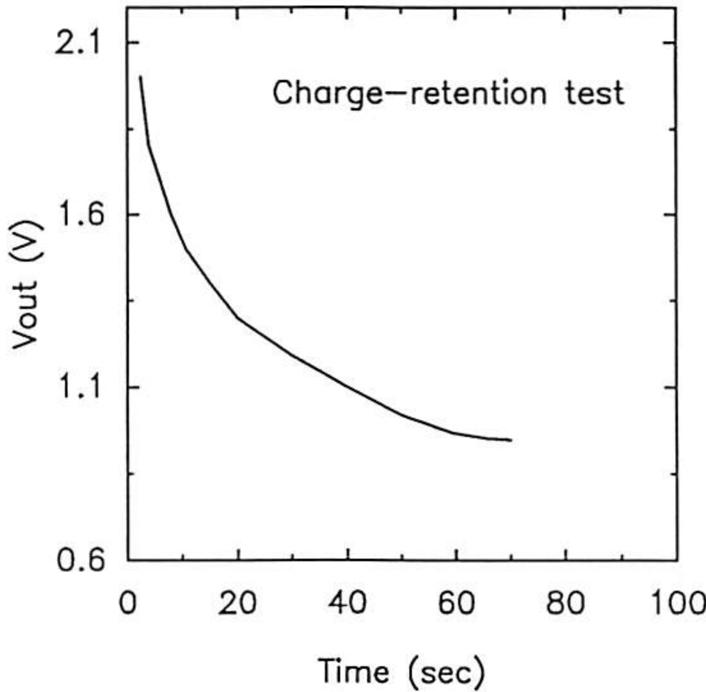


Fig. H.9 Measured charge-retention time for the DRAM-type synapse cells.

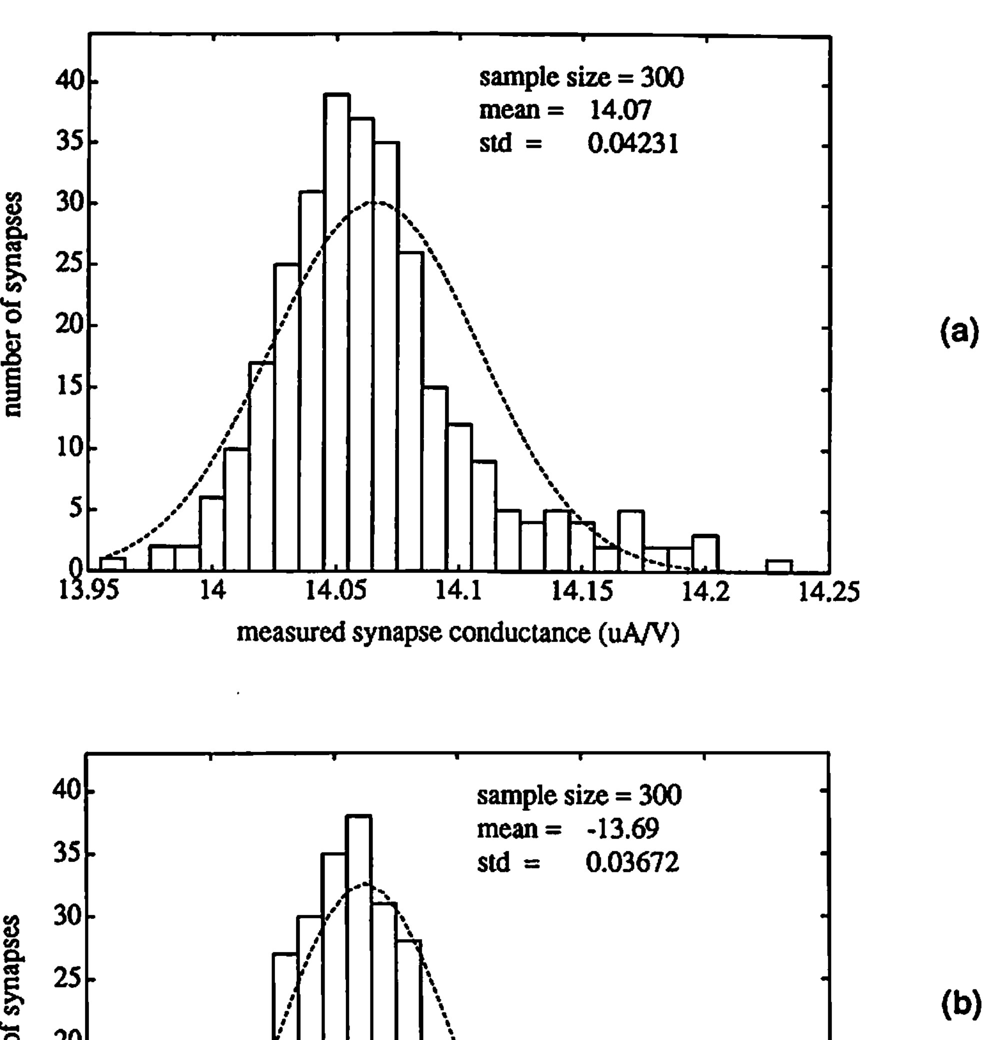


Fig. H.10 Gaussian distribution of measured synapse conductance.
(a) $V_{prog} = 2V$.
(b) $V_{prog} = -2V$.

Table H.1 Estimated testing time for three published general-purpose neural chip.

	USC	Intel/ETANN [H.4]	Matsushita [H.5]
Technology	2.0μm CMOS	1.0μm E^2PROM, CMOS	2.2μm BiMOS
Complexity	64 input neurons 25 output neurons 1600 synapses	64 input neurons 64 output neurons 8192 synapses	32 input neurons 16 hidden neurons 16 output neurons 768 synapses
Estimated Time (sec)	37.2	183	18.3

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