USC–SIPI REPORT #330

High Throughput Optoelectronic Smart Pixel Systems Using Diffractive Optics

by

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May 1999

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Acknowledgements

I am deeply thankful to my thesis advisor, Dr. Alexander A. Sawchuk, for his invaluable support, guidance and encouragement throughout the course of this work. With his broad knowledge and insight, not only am I able to finish my study and dissertation, I also enjoyed this research field with great freedom and fun.

I also like to thank my dissertation committee members: Prof. B. Keith Jenkins, Prof. Christos Kyriakakis, Prof. Bing J. Sheu, and Prof. Wlodek Proskurowski for their constructive suggestions and comments.

The smart pixel research is truly a collaborative endeavor. All these results would not be possible without the team efforts of my colleagues and officemates Dr. Charlie Kuznia, Dr. Jen-Ming Wu, and Bogdan Hoanca. We have been a remarkable team and have accomplished many excellent work on SPARCL, SAPIENT, TRANSPAR-MQW, to TRANSPAR-VM. I will always remember the times when we all worked till late at night trying to solve the problems and finish the designs right before the project submission deadline. I have enjoyed working with them and shared valuable ideas. I have also learned a lot through the process of working on those projects together.

I would also like to thank Dr. Allan Weber and Seth Scafani for their valuable help and patience in providing computer and network assistance. They can always clear the obstacles in time for our projects to finish successfully. I also thank Gloria Halfacre, Linda Varilla, Regina Morton and all the staff of SIPI for their tremendous administrative help. I also like to thank Joe F. Ahadian for help with SAPIENT project, and the OE/VLSI team in Lucent Technologies for help on CMOS/MQW foundry run, and Prof.

Ravi Athale for help on VCSEL-MSM CO-OP program. I'm also thankful to Prof. Timothy M. Pinkston, Prof. C.-C. Jay Kuo, Dr. Sabino Piazolla, Dr. Wei-Feng Hsu, Dr. Jeng-Feng Lin, Dr. Adam Goldstein, Dr. Tien-Ying Kuo, Dr. Hung-Kai Tsai, Dr. Hua-Shih Lin, Dr. Cheng-Ta Hsieh, Mr. Yung-Song Huang, Mr. Dhawat Pansatiankul, and Ms. Li-Ping Zhang for their fruitful discussions, encouragement and friendship.

Finally, I am sincerely grateful to my parents, Ping-Tao Chen, May-Tsao Shih, and my sister, Pei-Ling Chen, for their love and persistent encouragement. My special thanks go to my wife, Yi-Chia Chen, and her family for their incredible patience, encouragement, and confidence in me. Without the support from my family, it would be much harder for me to accomplish this research work.

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Table of Acronyms and Symbols

Table of Acronyms

ADC	Analog to Digital Converter
AGE	Average Group Error
ALU	Arithmetic Logic Unit
APE	Average Percentage Error
AR	Anti-Reflection
BFT	Bessel Fourier Transform
BIST	Built In Self Testing
CCD	Charge Coupled Device
CMOS	Complementary Metal Oxide Silicon
CSMA/CD	Carrier Sense Multiple Access/Collision Detection
DAC	Digital Analog Converter
DOE	Diffractive Optical Elements
FFT	Fast Fourier Transform
FIFO	First In First Out
FSDO	Free Space Digital Optics
FZP	Fresnel Zone Plate
GNU	Group Non-Uniformity
IFT	Iterative Fourier Transform
LED	Light Emitting Diode
MPEG	Motion Picture Expert Group
MQW	Multiple Quantum Well
MSE	Mean Square Error
MSM	Metal Semiconductor Metal
NLS	Nonlinear Least Square
NZAPE	Non-Zero Average Percentage Error
OE	Optoelectronic
OEIC	Optoelectronic Integrated Circuit
OPDP	Optical Parallel Data Packet
OPFET	Optical-Field-Effect Transistor
PBS	Polarization Beam Splitter
PE	Processing Element
PM	Pattern Mirror
RTL	Register Transfer Level
SAPIENT	Smart Pixel Array Network Interface
SBWP	Space Bandwidth Product
SEED	Self-Electro-Optical Device
SIMD	Single Instruction Multiple Data

SNR	Signal Noise Ratio
SPARCL	Smart Pixel Array Cellular Logic
TRANSPAR	Translucent Smart Pixel Array
TRANSPAR-MQW	TRANSPAR using MQW devices
TRANSPAR-VM	TRANSPAR using VCSEL-MSM devices
VCSEL	Vertical Cavity Surface Emitting Laser

Table of Symbols

Symbol	Description
Δx	Feature size of DOE
Θ	Phase element matrix of DOE
λ	Operation wavelength
$\theta(j, k)$	Phase value of element (j, k) in DOE
η_g	Diffraction grating efficiency
α_l	Step size in NLS iteration
η_o	Objective efficiency
η_w	Observation window efficiency
A_n	Coefficient *n* in Fourier series expansion
D	Lens diameter
E_m	Mechanical error
$E_{Q,max}$	Maximum quantization error
F/#	F-number
f_m	Minimum feasible focal length of diffractive microlens
I_{noise}	Diffraction intensity for noise orders
$\mathbf{I_r}$	Reconstructed diffraction pattern
I_{signal}	Diffraction intensity for signal orders
J_1	First order Bessel function
L	Number of phase level
$\mathbf{N_r}$	Reconstructed diffraction pattern for the noise orders
P	Number of period in DOE
QF	Quality factor
r_p	Ring period in FZP
r_{pm}	Minimum feasible ring period
S_{max}	Maximum intensity in the signal diffraction orders
S_{min}	Minimum intensity in the signal diffraction orders
$\mathbf{S_r}$	Reconstructed diffraction pattern for the signal orders
T	Period size in DOE
U	Non-uniformity
U_{dsp}	Diffraction field derived by Direct Synthesis method
U_{fdp}	Diffraction field derived by Fresnel Diffraction method
U_{fsp}	Diffraction field derived by Fresnel Synthesis method
U_{obj}	Object transmittance
U_p	Pairwise non-uniformity
w	Minimum linewidth in diffractive microlens
λ_{opt}	Optimum scaling factor in APE derivation
$\sigma_{0.25}$	Standard deviation of power for signal orders in 0.25 normalized power
$\sigma_{0.5}$	Standard deviation of power for signal orders in 0.5 normalized power
σ_1	Standard deviation of power for signal orders in normalized power
τ	Time required to execute the BFT function

Abstract

Recent developments in digital video, multimedia technology and data networks have greatly increased the demand for high bandwidth communication channels and high throughput data processing. Electronics is particularly suited for switching, amplification and logic functions, while optics is more suitable for interconnections and communications with lower energy and crosstalk. In this research, we present the design, testing, integration and demonstration of several optoelectronic smart pixel devices and system architectures. These systems integrate electronic switching/processing capability with parallel optical interconnections to provide high throughput network communication and pipeline data processing.

The Smart Pixel Array Cellular Logic processor (SPARCL) is designed in 0.8μm CMOS and hybrid integrated with Multiple-Quantum-Well (MQW) devices for pipeline image processing. The Smart Pixel Network Interface (SAPIENT) is designed in 0.6μm GaAs and monolithically integrated with LEDs to implement a highly parallel optical interconnection network. The Translucent Smart Pixel Array (TRANSPAR) design is implemented in two different versions. The first version, TRANSPAR-MQW, is designed in 0.5μm CMOS and flip-chip integrated with MQW devices to provide 2-D pipeline processing and translucent networking using the Carrier-Sense-Multiple-Access/Collision-Detection (CSMA/CD) protocol. The other version, TRANSPAR-VM, is designed in 1.2μm CMOS and discretely integrated with VCSEL-MSM (Vertical-Cavity-Surface-Emitting-Laser and Metal-Semiconductor-Metal detectors) chips and driver/receiver chips on a printed circuit board. The TRANSPAR-VM provides an

option of using the token ring network protocol in addition to the embedded functions of TRANSPAR-MQW.

These optoelectronic smart pixel systems also require micro-optics devices to provide high resolution, high quality optical interconnections and external source arrays. In this research, we describe an innovative algorithm to design Diffractive Optical Elements (DOEs) having higher uniformity and better signal-to-noise ratio. The algorithm is based on nonlinear least-square optimization procedures and phase-shifting quantization scheme to minimize the reconstruction error of DOEs. We also describe a modified diffractive microlens design algorithm to overcome linewidth limitations in fabrication while achieving higher numerical aperture and better power efficiency. Several diffractive optical devices used in our smart pixel systems, including microlens arrays and spot array generators, are designed by these algorithms, and have been fabricated and characterized for system integration.

Chapter 1 Introduction

1.1 Motivation

Free space optical interconnection systems have received considerable interest for their potential to relieve bottlenecks associated with electrical board-to-board and chip-to-chip communications [1]. These systems rely on smart pixel technology, which integrates optics and electronic circuitry for high throughput optoelectronic parallel information processing and communication. Smart pixel arrays provide the designer many degrees of freedom by integrating electronic circuits, optoelectronic devices, and refractive, reflective, and diffractive optical components into a compact system. In addition, the development of advanced lithography fabrication techniques have made the fabrication of high resolution and high efficiency diffractive optics with finer features and more complicated diffractive pattern possible [2]. The advantages of VLSI process compatibility, high precision fabrication technology and better design techniques for diffractive optics make it very suitable for integration into smart pixel system applications.

New applications of smart pixel systems have been widely explored in the area of image processing, video processing, networking, parallel switching and 2D/3D displays. In addition, smart pixel technology enables off-chip communications at Terabit-per-second aggregate bandwidth [3]. In smart pixel systems, diffractive devices are capable of providing optical interconnections, beam steering, image manipulation and external source modulation. New design methods, modeling analyses, fabrication processes and

applications of diffractive optical components are important components in optoelectronic smart pixel architectures.

The goal of this research is to advance the technology of diffractive optics and its use in high throughput smart pixel systems. The technology advances include new techniques for their design, test and optoelectronic integration. In this research, I develop new Diffractive Optical Element (DOE) design algorithms with better reconstruction performance, propose modified design and analysis methods for diffractive microlenses, evaluate and characterize the various fabricated diffractive optical devices, design and demonstrate smart pixel systems which are integrated with diffractive optical devices.

1.2 Research Contributions

The tasks of this research work fall into three major areas:

(1) Optoelectronic smart pixel system design and integration

- CMOS VLSI design simulation for the smart pixel array cellular logic (SPARCL) processor
- Optical system design and simulation using OSLO® design software for the integration of SPARCL chip and optical devices
- Characterization of the fabricated 5×20 spot array generator DOEs used in the SPARCL system.
- GaAs VLSI design and simulation for the smart pixel parallel data packet network interface (SAPIENT) chip
- Testing and demonstration of the SAPIENT chip and optical network system

- 3×3 high numerical aperture diffractive microlens array design for the optical module of SAPIENT system
- Smart pixel design and simulation for the Translucent smart pixel array (TRANSPAR) processor using MQW devices and VCSEL-MSM devices
- High performance 5×16 spot array generator DOEs design and 5×20 diffractive microlens array design for the TRANSPAR system
- Characterization of the 4:2:1 analog weighted fanout DOEs used in the smart pixel neural network system.

(2) Phase-only diffractive optical element (DOE) design and testing

- Development of a nonlinear least square algorithm for the design of phase-only DOEs and comparison of the simulation results with other commonly used algorithms.
- Invention of a phase-shifting quantization scheme to derive the optimized quantization levels for the DOE phase elements.
- Defining a set of parameters, which are applicable to any diffraction pattern (analog or digital) of the fabricated DOEs to evaluate their reconstruction performance.
- Design of a testing system to measure the various DOE diffraction patterns, including cellular hypercube, uniform spot array, analog weighted fanout pattern...etc.
- Characterization of the fabricated DOEs and invention of the etch depth revision method to compensate the reconstructed zero diffraction order.

(3) Diffractive microlenses design, testing and analyses

- Development of an integrated diffractive optics design program, which includes innovated DOE design algorithms and the modified hybrid phase level design method

[36]-[38] for the diffractive microlenses. This hybrid phase level design method is used to extend the feature size limitation of the VLSI fabrication process.

- Test and experimental evaluation of diffractive microlens arrays designed and fabricated using hybrid phase level method and those with traditional methods.
- Proposed a thin-lens decomposition method to synthesize the diffraction pattern of diffractive lenses with limited phase quantization levels.
- Simulation of the thin-lens decomposition method and comparison with the regular Fresnel diffraction computation algorithm.

1.3 Thesis Organization

This thesis is organized as follows:

- Chapter 2 describes the background of this research, including the basic theories of phase-only DOEs, diffractive microlenses, and the state-of-the-art smart pixel technology.
- Chapter 3 describes the proposed nonlinear least square algorithm and the phase-shifting quantization scheme for DOE design. The simulations for the cellular hypercube pattern are illustrated and also compared with the results using the two-stage iterative Fourier transform method.
- Chapter 4 describes the hybrid phase level method for diffractive lens design. The reduced F/# and increased efficiency of the microlenses designed by this method are illustrated. The second part of this chapter illustrates the concept of the thin-lens decomposition method for the phase quantized diffractive lenses or the so-called

Fresnel Zone Plates (FZPs). The simulations using this method for the FZP illuminated by Gaussian beam are shown.

- Chapter 5 discusses the testing setup and evaluation parameters for the fabricated DOEs and microlenses. The effects, measurement errors and fabrication errors are presented. The effect of anti-reflection coating, feature shrinkage, etch depth error are also evaluated for some of the fabricated DOEs.
- Chapter 6 demonstrates the design and testing of three separate smart pixel systems integrated with various diffractive devices. The first is the smart pixel cellular logic SPARCL system, which is a hybrid CMOS/SEED chip integrated with 5×20 spot array generator DOEs. The second is the smart pixel 2-D parallel data network interface (SAPIENT) system, which is a monolithic GaAs chip integrated with diffractive microlens array. The third is the translucent smart pixel array (TRANSPAR) processor. The same TRANSPAR design is implemented with two different transmitting/receiving optical devices. One uses the SEED modulators, and the other one uses the VCSEL/MSM active devices. We also describe the design of the 5×16 spot array generator DOEs for the modulator based system and the diffractive microlens array for the VCSEL based system.
- Conclusions and discussions are given in Chapter 7. Some possible future extensions are described in Chapter 8.

Chapter 2 Preliminaries

2.1 Diffractive Optical Elements

In this section, we describe basic theories for phase-only diffractive optical elements (DOEs). In this research, we assume that the paraxial approximation for the modeling of DOEs is applied, which means the smallest transverse feature is several times larger than the operation wavelength of the illuminating beam [4]. Therefore, the scalar diffraction theory [5] is assumed to be accurate to describe the diffraction effect of DOEs. We assume that the DOE is a 2-D inseparable periodic grating and that we are only interested in Fourier-plane DOEs, that generate the desired diffraction pattern in the focal plane of the corresponding Fourier transforming lens.

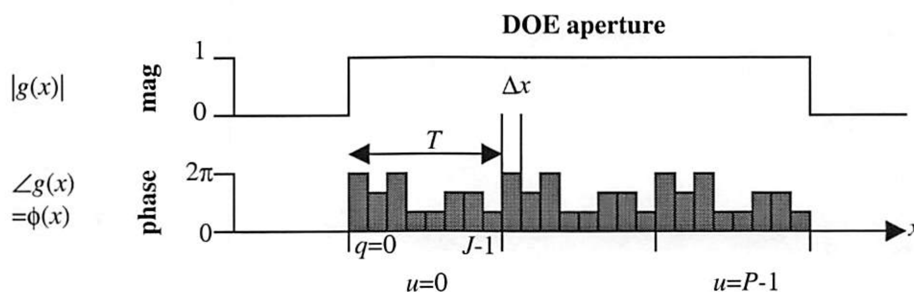


Figure 2-1: Grating profile $g(x)$ of a 1-D DOE with J phase elements in a single period, feature size Δx, and P periods of size T.

Figure 2-1 illustrates the grating profile of a 1-D DOE. The DOE consists of P periods of grating with size T and J phase elements in a single period. Each phase element has feature size Δx and one of L possible phase levels. The phase difference between adjacent phase quantization levels is $2\pi/L$. Since we focus on phase-only DOEs,

each phase element has unit amplitude as shown in Figure 2-1. Based on these parameters, we are able to write the grating equation as

$$g(x) = \sum_{u=0}^{P-1}\sum_{q=0}^{J-1} g(q\Delta x)\cdot \mathrm{rect}(\frac{x - q\Delta x - uT}{\Delta x}), \tag{2.1}$$

where $g(q\Delta x)=\exp(i\phi(q\Delta x))$, and the definition

$$\mathrm{rect}(x) = \begin{cases} 1 & |x| \le \frac{1}{2} \\ 0 & \text{otherwise} \end{cases}. \tag{2.2}$$

Assuming unit amplitude beam illumination, the complex amplitude of the v-th diffraction order $G(v)$ of the DOE reconstruction on the Fourier focal plane is derived by taking a Fourier transform of Eq. (2.1) and given by

$$G(v) = v\Delta x\cdot(-1)^{v(J-1)} e^{-i\pi v(J-1)}\cdot \mathrm{sinc}(\frac{v}{J})\cdot \mathrm{DFT}\{g(q\Delta x)\}. \tag{2.3}$$

The corresponding power spectrum is also derived as

$$|G(v)|^2 = |v\Delta x\cdot \mathrm{sinc}(\frac{v}{J})\cdot \mathrm{DFT}\{g(q\Delta x)\}|^2 \tag{2.4}$$

The Eq. (2.1) to (2.4) are the basic equations used in the computation of the DOE reconstruction patterns [6].

2.2 Diffractive Lenses (Fresnel Zone Plates)

The Fresnel Zone Plate (FZP) is one kind of diffractive optical element with a special grating structure. It can be used as a phase grating or an amplitude grating device. Here, I focus only on the phase-only multiple-phase-level grating structure of the FZP for its

higher diffraction efficiency. Phase-only FZPs are also known as diffractive lenses or Fresnel lenses.

Figure 2-2 shows the phase profile of a FZP with L phase levels. We notice that the phase pattern is periodic on the r^2 axis with period r_p^2 and that r_p is called the *Ring Period.*

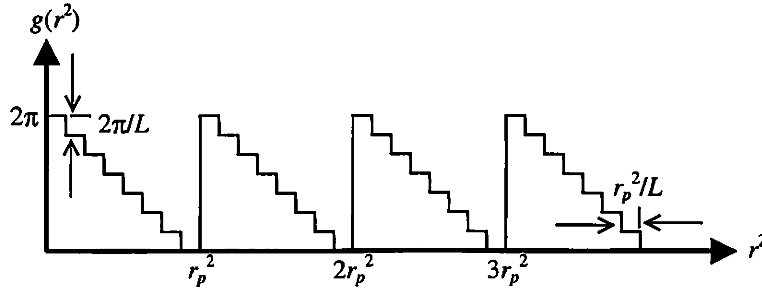


Figure 2-2: Phase profile of multiple-phase-level FZP (L=8 in this plot).

In Figure 2-2, the grating function of FZP $g(r)$ is represented as

$$g(r) = \mathrm{circ}(\frac{r}{r_p\sqrt{P}})\sum_{k=-\infty}^{\infty}\exp(\frac{-i2k\pi}{L})\mathrm{rect}(\frac{r^2 - k\frac{r_p^2}{L} - \frac{r_p^2}{2L}}{r_p^2 / L}) = \mathrm{circ}(\frac{r}{r_p\sqrt{P}})h(r^2), \tag{2.5}$$

where the rectangular function is defined in Eq. (2.2) and P is the total number of periods [7]. Taking the Fourier series expansion of $h(r^2)$ in Eq. (2.5), we rewrite the Eq. (2.5) as

$$g(r) = circ(\frac{r}{r_p\sqrt{P}})\sum_{n=-\infty}^{\infty}A_n\exp(\frac{i2\pi nr^2}{r_p^2}), \tag{2.6}$$

where the Fourier series coefficients A_n is

$$A_n = \exp(\frac{-in\pi}{L})\mathrm{sinc}((\frac{n}{L})\delta(n-[mL-1])). \tag{2.7}$$

The $|A_n|^2$ represents the power spectrum for the n-th longitudinal diffraction component of the FZP. Figure 2-3 illustrates the power spectrum of different longitudinal diffraction orders for the number of phase levels L equal to 2 and 4. In Figure 2-3, we see that the -1 longitudinal diffraction order has the highest power efficiency when the number of phase level L increases. The power efficiency for the n-th longitudinal diffraction order is proportional to $|\mathrm{sinc}(n/L)|^2$. We also notice that A_n equals zero for those longitudinal diffraction order $n=mL-1$, where m is an integer. Thus, there are two well-known characteristics of FZPs:

1) Multiple focal length

2) The diffraction efficiency of each focus is related to the square of sinc function.

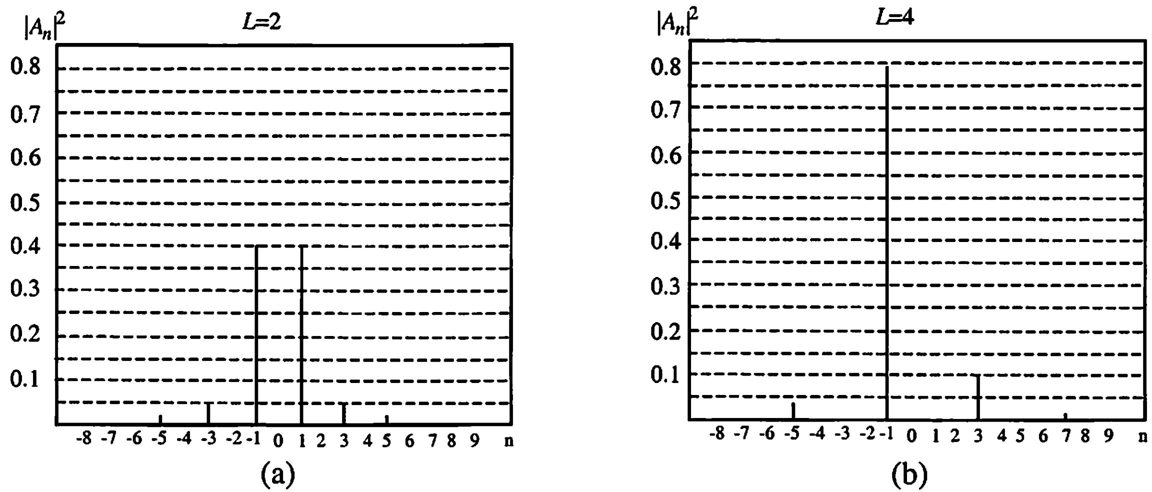


Figure 2-3: Power spectra of FZP for (a) two phase levels (b) four phase levels.

2.3 Smart Pixel Technology

Smart pixels are a rapidly growing research topic in the general area of optoelectronic. A smart pixel device contains an array of individual pixels, each with intelligence for performing logic operations and providing the individual input/output interconnections. Smart pixel optoelectronic devices are particularly suitable to implement systems which are parallel, fine-grained and highly interconnected, such as parallel signal (image/video) processors [8], photonic switching networks [9], local area networks (LANs) and optical neural network systems [10]. There are basically two types of transmitting devices for smart pixels: (1) passive devices, such as Multiple Quantum Well (MQW) modulators [11] and polymer Electro-Optic modulators [12]; and (2) active devices, such as Light Emitting Diodes (LEDs) [13] and the Vertical Cavity Surface Emitting Laser (VCSEL) [14].

For optoelectronic device integration, there are two different kinds of processes: one is hybrid integration technology and the other is monolithic integration technology. The hybrid integration technology integrates GaAs optical devices, transmitters or receivers into the CMOS electronic circuitry. Several hybrid integration methods have been developed, for example, the flip-chip bonding process [15], the epitaxial lift-off process [16] and the fluidic-self assembly process [17]. In flip-chip attachment, solder bump contacts can be placed anywhere on the electronic circuit chip. There is a corresponding mirror image contact pattern on the optical device chip. These two chips are then flipped and connected through the bump bonding contacts. In the epitaxial lift-off process, the optical devices are epitaxially grown on the GaAs substrate with an intermediate lift-off layer. Then, the intermediate layer is lifted off and the thin-film

devices are attached to the flat surface contacts on the circuitry side substrate through Van der Waals bonding. In the fluidic self-assembly process, the GaAs devices are fabricated into trapezoidal blocks, which are freed from the substrate into a carrier liquid. This solution is then dispensed over a Si receptor wafer which has correspondingly-shaped holes etched into it. Under the ensuing fluid transport, blocks self-assemble into the holes [17]. The advantages of the hybrid integration methods are their simple integration process, compatibility with mature CMOS VLSI fabrication processes and low static power consumption.

On the other hand, monolithic integration technology integrates the optical devices and electrical circuitry on the same substrate material, generally GaAs [18][19]. The electrical circuitry is first fabricated through standard IC processes, then prepared for dielectric material growth. The optical devices are epitaxially grown in designated wells on the GaAs chip through molecular beam epitaxy (MBE) processes in a low temperature environment. The advantages of the monolithic integration technology are that common materials technology is used for both optical and electrical devices, and the high-speed logic operations possible with GaAs circuitry.

Chapter 3 Design Methods for Phase-only Diffractive Optical Elements

The role of diffractive optical elements (DOEs) has been increasingly important in the field of optical information processing [20]. Some useful applications include weighted optical interconnections in neural networks, spot array generators in smart pixel systems, shuffle networks in photonic switching, and image display. In most applications, the reconstruction accuracy is crucial and directly affected by the design of DOEs. Figure 3-1 shows the optical neural network system using weighted fanout DOEs to provide analog weighted interconnections between two neuron layers [21].

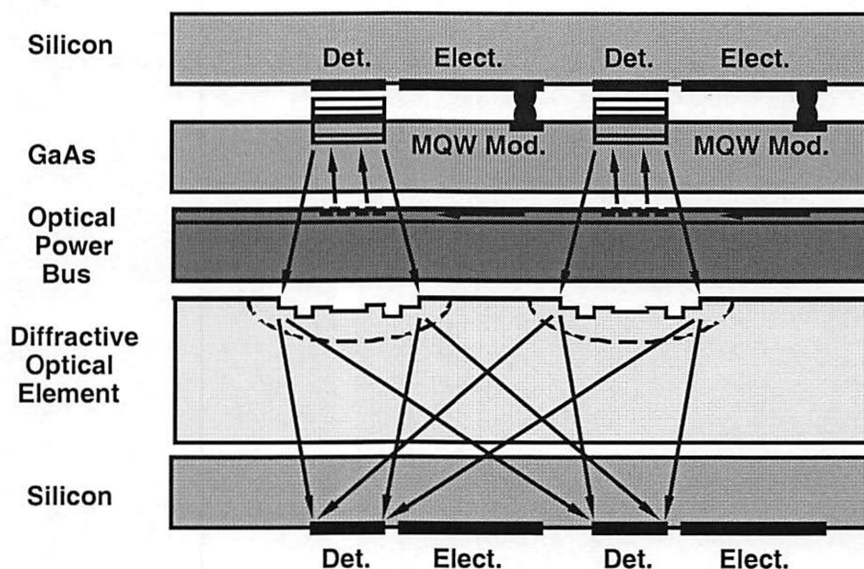


Figure 3-1: Structure of the optical neural network using weighted fanout DOEs.

Currently, there exist many different kinds of DOE design algorithms. Two of the most popular ones are the iterative Fourier transform (IFT) method and simulated

annealing [22]. The IFT method suggested by Gerchberg and Saxton [23] employs the fast Fourier transform algorithm and thus has a very low computation cost for each iteration. However, this method tends to converge to a local optimum with slow improvement after further iterations.

Modified methods [23][24] introduce the concept of a dummy area and place different constraints on the noise diffraction orders in two stages as the algorithm processes to increase the diffraction efficiency and uniformity. On the other hand, simulated-annealing methods can achieve a global optimum, but the computation cost for the larger number of discrete-phase level DOEs can be enormous.

In the research, we focus only on the phase-only DOEs for its highest diffraction efficiency. In this chapter, we propose using the nonlinear least square (NLS) and phase shifting quantization methods to design DOEs to reconstruct a diffraction pattern that accurately represents the desired pattern with high uniformity, efficiency, signal-to-noise ratio and an acceptable computation cost. In the following sections, we first describe the mathematical model of DOE design problem then introduce the NLS algorithm and the phase shifting quantization scheme. For comparison, the two-stage IFT method combined with stepwise phase quantization is also described. At last, the performance simulations using proposed methods are presented.

3.1 Mathematical Model

Using the notation of Wyrowski [20], given a desired known diffraction intensity matrix $\mathbf{I}$ containing an $M \times N$ array of real, non-negative elements indexed by $I(m, n)$, we want to

obtain a DOE matrix $\mathbf{G}$ whose complex-valued elements $G(j, k)$ have unit magnitude (a phase-only matrix), that is

$$G(j,k) = \exp(i\theta(j,k)), -\pi \le \theta(j,k) \le \pi . \tag{3.1}$$

The quantity $G(j, k)$ is chosen such that the reconstructed complex amplitude matrix [4]

$$\mathbf{g} = \mathbf{W} \times FT^{-1}\{\mathbf{G}\} \tag{3.2}$$

having element $g(m, n)$ minimizes the Mean Square Error,

$$\text{MSE} = \{\frac{1}{MN}\sum_{m,n} | \|g(m,n)\|^2 - I(m,n) | \}^{1/2} . \tag{3.3}$$

Here, $FT^{1}\{\}$ denotes the inverse Discrete Fourier Transform and $\mathbf{W}$ is a window function whose matrix elements $W(m, n)=\text{sinc}(m/M)\text{sinc}(n/N)$ are derived from Eq. (2.3). This window function effect is caused by the finite feature size limitation of DOE. The indices m and j range from 0, 1, 2,..., M-1 and the indices n and k range from 0, 1, 2,..., N-1 in Eq. (3.1), (3.2) and (3.3). In order to perform the minimization of Eq. (3.3), we apply a Nonlinear Least Square algorithm and redefine the mathematical model as an optimization problem on a nonlinear function. The DOE design problem then can be expressed as choosing a set of phases $\Theta=\{\theta(j, k) \mid j=0, 1,..., M-1, k=0, 1,..., N-1\}$ to minimize the norm of a nonlinear residue function

$$\mathbf{F}=\{F(m, n) \mid m=0, 1,..., M-1, n=0, 1,..., N-1\} \text{ and } F(m, n)=\|g'(m, n)\|^2-I'(m, n) \tag{3.4}$$

where

$$I'(m, n)=I(m, n)/[\text{sinc}(m/M)\cdot\text{sinc}(n/N)]^2, \tag{3.5}$$

$$g'(m, n)=g(m, n)/[\text{sinc}(m/M)\cdot\text{sinc}(n/N)], \tag{3.6}$$

and $g(m, n)$, $I(m, n)$, and $\theta(j, k)$ are defined as above. From Eq. (3.2) and Eq. (3.6), we know that $\mathbf{g}'=FT^{1}\{\mathbf{G}\}$, that is

$$g'(m,n)=\sum_{j=0}^{M-1}\sum_{k=0}^{N-1}G(j,k)\exp\{-i2\pi(\frac{jm}{M}+\frac{kn}{N})\}. \tag{3.7}$$

From Eq. (3.7), we derive an analytic formula for the residue matrix elements in the form

$$F(m,n)=\sum_{j=0}^{M-1}\sum_{k=0}^{N-1}\sum_{p=0}^{M-1}\sum_{q=0}^{N-1}\exp\{i[2\pi(\frac{(p-j)m}{M}+\frac{(q-k)n}{N})+\theta(j,k)-\theta(p,q)]\}-I'(m,n). \tag{3.8}$$

Thus, the problem is to find the optimum DOE phase matrix Θ which will minimize $\|\mathbf{F}\|^2$. At this point, we apply the Nonlinear Least Square algorithm as described in the next section.

3.2 Nonlinear Least Square Design Algorithm

There are several different ways to solve nonlinear least square problems. Here, we describe the damped first order Gauss-Newton type iteration algorithm because it produces fairly good results and is relatively easy to explain. This procedure for the first order Gauss-Newton type Nonlinear Least Square method has the following steps:

1. Generate an initial phase matrix Θ_0, whose elements $\theta_0(j, k)$ are random numbers between $-\pi$ and π.

2. $\Theta_{l+1}=\Theta_l+\alpha_l\mathbf{H}_l$, (3.9)

where l is the iteration number = 0, 1, 2,...etc, α is a step control scalar factor and $\mathbf{H}$ is the steepest descent direction of the nonlinear residue function $\mathbf{F}$. By rewriting the matrices $\mathbf{H}$ and $\mathbf{F}$ into equivalent column vector forms $\mathbf{h}$ and $\mathbf{f}$, the descent direction is given by multiplying the pseudo-inverse of the Jacobian matrix $\mathbf{J}$ by the residue vector $\mathbf{f}$, as given by

$$\mathbf{h}_l = -(\mathbf{J}^H\mathbf{J})^{-1}\mathbf{J}^H\mathbf{f}\,, \tag{3.10}$$

where $\{\cdot\}^H$ denotes the Hermitian matrix operation, the elements of $\mathbf{h}$ are

$$h(v)=h(jN+k)=H(j,k),\ v=0,1,2,\ldots,MN\text{-}1,\ j=0,1,2,\ldots,M\text{-}1,\ k=0,1,2,\ldots,N\text{-}1, \tag{3.11}$$

and the elements of $\mathbf{f}$ are

$$f(u)=f(mN+n)=F(m,n),\ u=0,1,2,\ldots,MN\text{-}1,\ m=0,1,2,\ldots,M\text{-}1,\ n=0,1,2,\ldots,N\text{-}1. \tag{3.12}$$

The elements of the Jacobian matrix $\mathbf{J}$ are defined as

$$J(u,v) = J(mN+n, jN+k) = \frac{\partial F(m,n)}{\partial \theta(j,k)}\ . \tag{3.13}$$

From Eq. (3.8) and Eq. (3.13), an analytic expression for the Jacobian matrix can be derived as

$$J(u,v) = J(mN+n, jN+k) = \sum_{\substack{p=0\\ p\neq j}}^{M-1}\sum_{\substack{q=0\\ q\neq k}}^{N-1} -2\sin\{\theta(j,k)-\theta(p,q)+2\pi[\frac{m(p-j)}{M}+\frac{n(q-k)}{N}]\}. \tag{3.14}$$

Even with this analytic expression, using the numerical evaluation of the derivative in Eq. (3.13) is a more efficient way to evaluate the Jacobian matrix. The cost of numerically generating the Jacobian matrix in each iteration is on the order of $(MN)^2\log_2(MN)$, that is $O(N^4\log_2 N^2)$ if $M=N$, while the cost is $(MN)^3$, that is $O(N^6)$ if $M=N$, for a direct evaluation of Eq. (3.14). To further reduce the computation cost, after the first iteration, the Broyden algorithm [25] is applied to estimate the Jacobian matrix, which has a cost on the order of $(MN)^2$, that is $O(N^4)$ if $M=N$. If the Jacobian matrix $\mathbf{J}$ is singular, we need to use Singular Value Decomposition or QR decomposition to derive the pseudo-inverse of $\mathbf{J}$.

Two common ways to determine the step coefficient α_l are [26][27]:

choosing α_l=max{1, 1/2, 1/4, 1/8,...} such that

$$\|\mathbf{f}(\Theta_l)\|^2 - \|\mathbf{f}(\Theta_l + \alpha_l \mathbf{H}_l)\|^2 \geq \frac{1}{2}\alpha_l \|\mathbf{J}(\Theta_l)\mathbf{h}_l\|^2. \tag{3.15}$$

Taking α_l as the solution of the one-dimensional minimization problem

$$\min_{\alpha_l} \|\mathbf{f}(\Theta_l + \alpha_l \mathbf{H}_l)\|^2. \tag{3.16}$$

3. Repeat step 2 until the norm of the residue function $\|\mathbf{f}(\Theta_l)\|$ is less than the predefined tolerance or exceeds a predefined maximum number of iterations.

In actually implementing this algorithm, we used the routine ***leastsq*** in the MATLAB® optimization toolbox [28], which applies the first order Newton method along with a further stabilized damped Gauss-Newton method suggested by Levenberg and Marquardt [29][30] to overcome possible stabilization difficulties.

3.3 Two-stage Iterative Fourier Transform Design Algorithm

For comparison, we describe here the commonly used 2-stage iterative Fourier transform (IFT) algorithm proposed by Wyrowski [31] for finding a phase-only DOE.

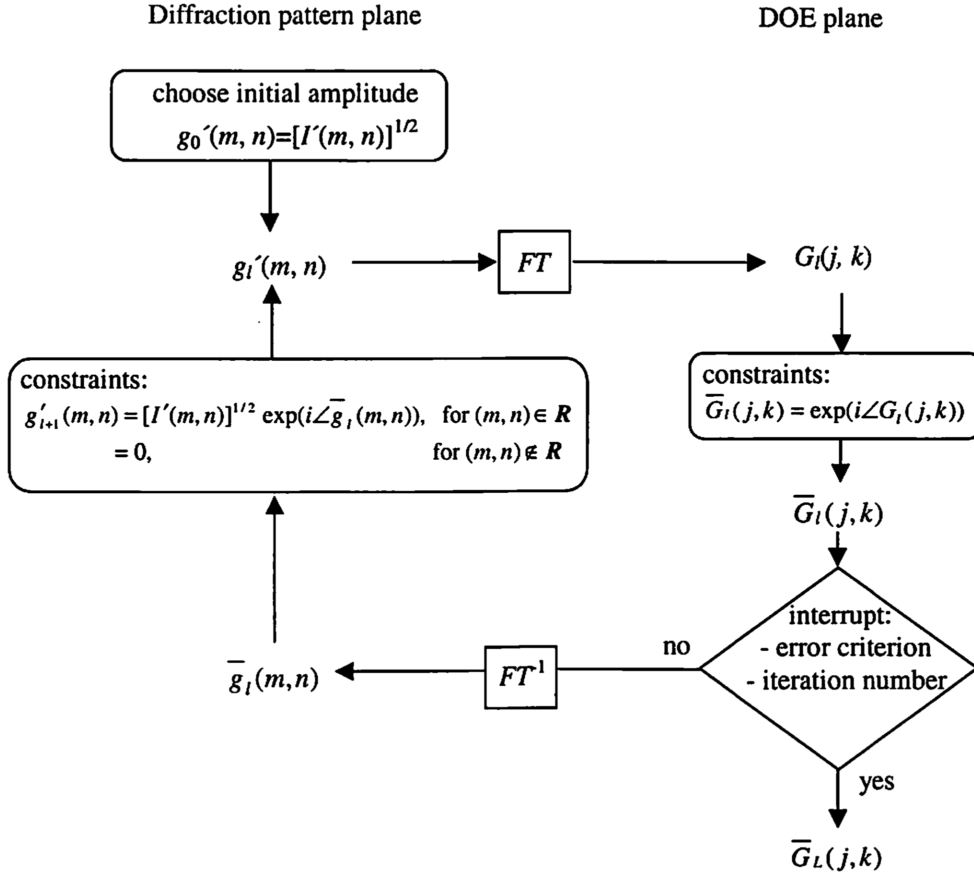


Figure 3-2: The diagram of the first stage in the two-stage iterative Fourier transform (IFT) method.

Figure 3-2 shows the first stage block diagram of the 2-stage IFT algorithm. The initial amplitude is

$$g_0'(m, n)=[I'(m, n)]^{1/2} \tag{3.17}$$

where $I'(m, n)$ is the desired diffraction intensity combined with the reconstruction window function as defined in Eq. (3.5). In the l-th iteration, the DOE elements are derived from the DOE plane constraints

$$\bar{G}_l(j,k) = \exp(i\angle G_l(j,k)), \tag{3.18}$$

where $\angle G_l(j, k)$ denotes the phase of $G_l(j, k)$, which is an element of the Fourier transform of the diffraction amplitude $g_l'(m, n)$. The update of the diffraction amplitude utilizes the phase freedom of the $g_l'(m, n)$. The diffraction plane constraints are:

$$\begin{aligned} g'_{l+1}(m,n) &= [I'(m,n)]^{1/2}\exp(i\angle\overline{g}_l(m,n)), && \text{for } (m,n) \in \boldsymbol{R} \\ &= 0, && \text{for } (m,n) \notin \boldsymbol{R} \end{aligned} \tag{3.19}$$

where $\boldsymbol{R}$ defines the region of signal diffraction orders and $\angle\overline{g}_l(m,n)$ denotes the phase of $\overline{g}_l(m,n)$, which is an element of the inverse Fourier transform of the derived DOE elements $\overline{G}_l(j,k)$. After L iterations, the interrupt condition, which can be either the maximum number of iterations or the threshold of variation in derived results between two iterations, is matched then the second stage algorithm is applied. Figure 3-2 shows the second stage block diagram of the two-stage IFT algorithm. The differences between the first and the second stages are in the constraints of the DOE plane and diffraction plane. The DOE plane constraints in the second stage employ the stepwise quantization [20][31] in addition to resetting the amplitude of the derived $G_l(j, k)$ to unity. The diffraction plane constraints in the second stage utilize both the amplitude freedom and the phase freedom as expressed by

$$\begin{aligned} g'_{l+1}(m,n) &= c_l[I'(m,n)]^{1/2}\exp(i\angle\overline{g}_l(m,n)), && \text{for } (m,n) \in \boldsymbol{R} \\ &= \overline{g}_l(m,n), && \text{for } (m,n) \notin \boldsymbol{R} \end{aligned} \tag{3.20}$$

where c_l is the energy scaling factor.

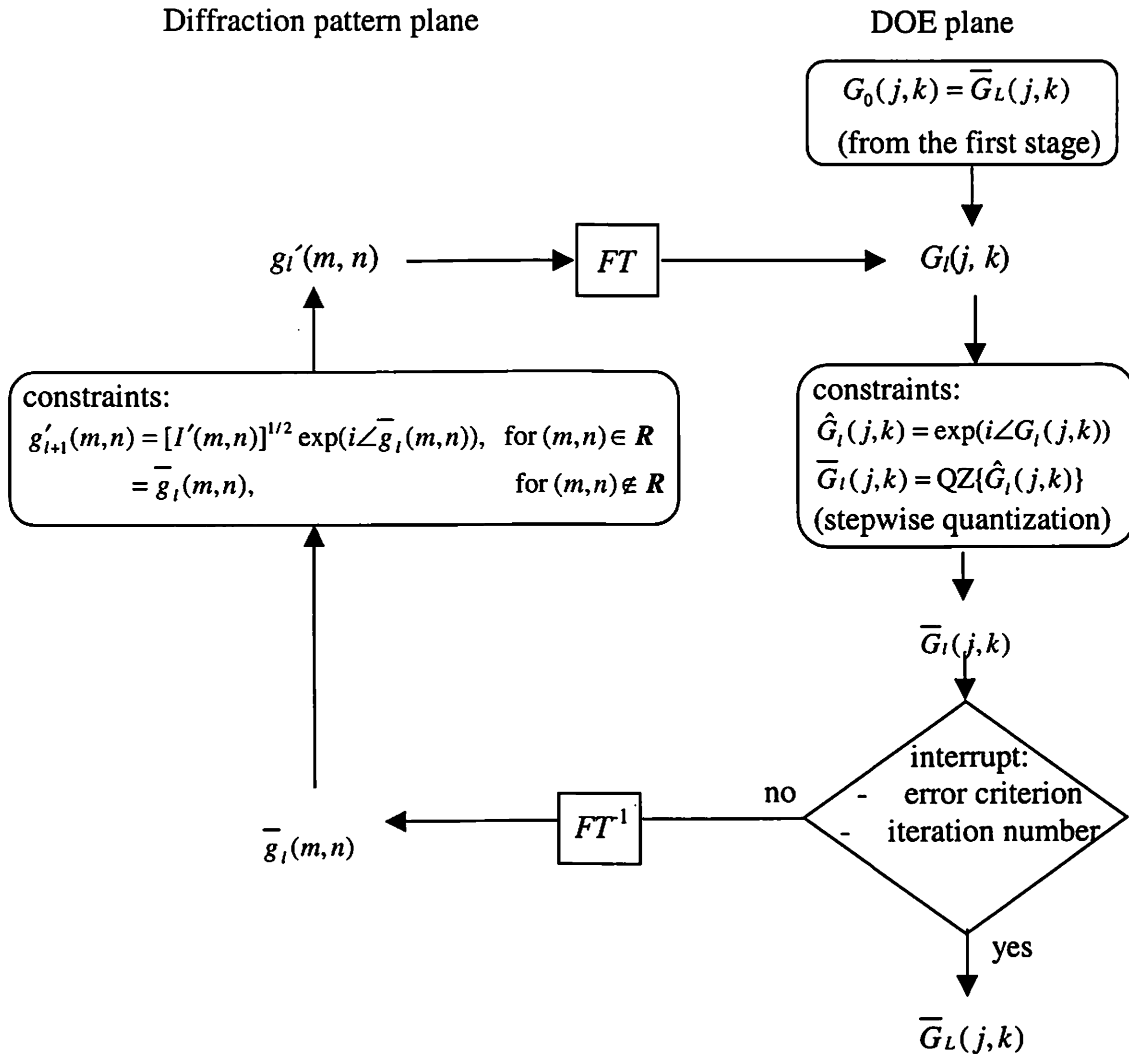


Figure 3-3: The diagram of the second stage in the two-stage iterative Fourier transform method.

This method uses the FFT algorithm, so its computation cost for each iteration is on the order of $MN\log_2(MN)$, or $N^2\log_2N^2$ if $M=N$. Compared to the NLS method, the cost per iteration of the iterative Fourier transform method is obviously lower.

3.4 Performance Evaluation Parameter

In order to evaluate the reconstruction of DOEs, we define five performance parameters, *non-uniformity*, *observation window efficiency*, *grating efficiency*, *signal-to-noise ratio* and overall *quality factor* in addition to the general mean square error (MSE in Eq. (3.3)). For the desired known diffraction pattern **I** and a reconstructed pattern $\mathbf{I}_r=\mathbf{S}_r+\mathbf{N}_r$, the $\mathbf{S}_r$ represents the signal diffraction orders in $\mathbf{I}_r$ with the amplitude of the noise orders set to zero, and the $\mathbf{N}_r$ represent the noise diffraction orders in $\mathbf{I}_r$ with the amplitude of the signal orders set to zero. Unity illumination intensity is assumed in calculating the evaluation parameters. Then, we define

$$\text{Non-uniformity } (U) = (S_{\max} - S_{\min})/(S_{\max} + S_{\min}), \tag{3.21}$$

$$\text{Efficiency in observation window } (\eta_w) = \sum_{m,n} S_r(m,n) / \sum_{m,n} I_r(m,n), \tag{3.22}$$

$$\text{Efficiency of diffraction grating } (\eta_g) = \sum_{m,n} S_r(m,n), \tag{3.23}$$

$$\text{Signal-to-noise ratio } (SNR) = 10 \cdot \log_{10}(S_{\min}/N_{\max}), \tag{3.24}$$

$$\text{quality factor} = w_1 \times (1-U) + w_2 \times \eta_w + w_3 \times \eta_g + w_4 \times SNR, \text{ where } \sum_{i=1}^{4} w_i = 1. \tag{3.25}$$

In Eq. (3.21), (3.22), (3.23) and (3.24), $S_{\max}=\max\{S_r(m, n)\}=S_r(m_{s\max}, n_{s\max})=I_r(m_{s\max}, n_{s\max})$, $S_{\min}=\min\{S_r(m, n) >0\}=S_r(m_{s\min}, n_{s\min})=I_r(m_{s\min}, n_{s\min})$, $N_{\max}=\max\{N_r(m, n)\}=N_r(m_{n\max}, n_{n\max})=I_r(m_{n\max}, n_{n\max})$, where $S_r(m, n)$, N_r(m, n), $I_r(m, n)$ and $I(m, n)$ are the elements of $\mathbf{S}_r$, $\mathbf{N}_r$, $\mathbf{I}_r$ and **I** respectively. An $M\times N$ phase element DOE produces $M\times N$ diffraction orders within its observation window when it is reconstructed. The η_w is the percentage of the intensity within the observation window that goes into the signal orders.

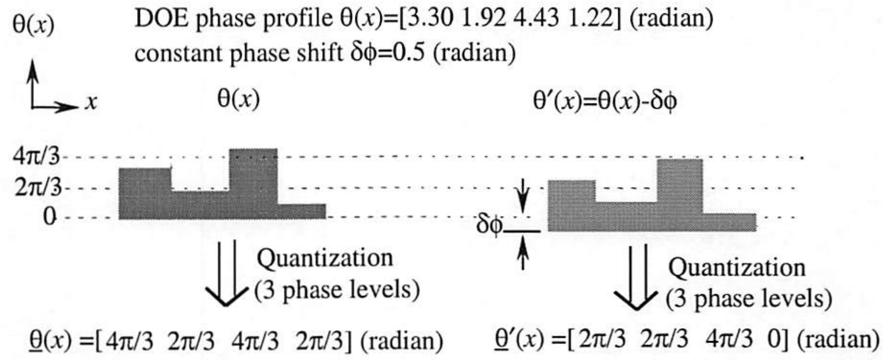
The η_g indicates the percentage of the illumination intensity that goes into the signal orders. The quality factor in Eq. (3.25) is a linear combination of non-uniformity, efficiency and signal-to-noise ratio with different weights, which produces an overall performance measure for the reconstructed pattern. The weight w_1, w_2, w_3 and w_4 can be adjusted to serve various application requirements. An advantage of the quality factor is that it is a single variable for evaluation and optimization during the iterative process.

3.5 Phase Shifting Quantization Scheme

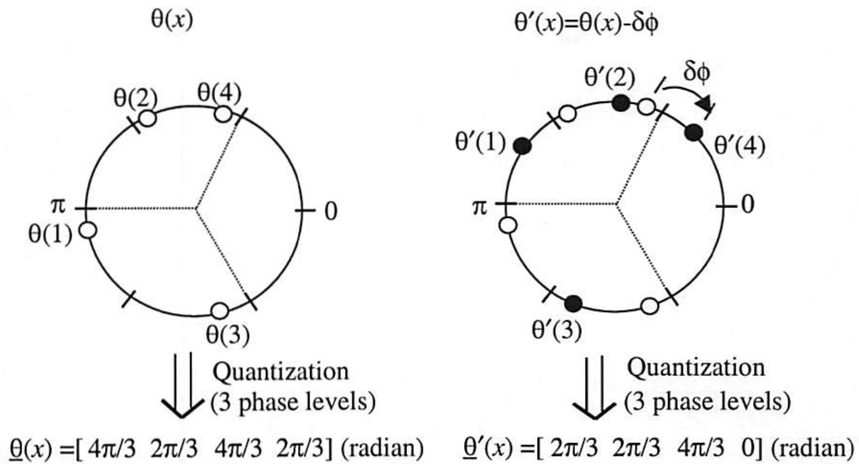
In the physical design of DOEs, all phase elements are quantized into a set of discrete phase levels, such as 0, π, $\pi/2$, $\pi/4 ... \pi/L$, depending on the number of phase levels L to be used in fabrication. The value of L is limited by the complexity of DOE fabrication. Using K VLSI masks in the ion-beam-etching step of DOE fabrication, we obtain 2^K distinct levels [32]. The traditional and simplest way to quantize the computed phase value is just to assign it to the nearest phase level, which we can call *fixed quantization.* However, this technique of phase quantization generally does not give the best reconstruction. Observing that, for a constant phase shift $\delta\phi$ placed on the DOE profile **G**, the reconstructed intensity

$$I_r = \left\| W \times FT^{-1}\{G \times \exp(i\delta\phi)\} \right\|^2 = \left\| W \times FT^{-1}\{G\} \times \exp(i\delta\phi) \right\|^2, \tag{3.26}$$

we know the diffraction intensity is independent of any constant phase shift of the DOE. That is, the diffraction pattern depends only on the relative phase values between the DOE phase elements rather than on their absolute values. Then we are able to apply the phase-shifting quantization scheme described in Figure 3-4.



(a)



(b)

Figure 3-4: Phase shifting effect in quantization (3 phase levels). (a) The constant phase shift $\delta\phi$ results in different quantization pattern. (b) The effect of constant phase shift (rotation) in the phase coordinate.

From Figure 3-4(a), we see that the constant phase shift $\delta\phi=0.5$ (radian) on the DOE phase elements $\theta(x)$ produces a different quantization pattern $\underline{\theta}'(x)$ compared to the original quantization pattern $\underline{\theta}(x)$. Figure 3-4(b) uses the phase coordinate to illustrate the changes of quantization pattern due to the shifted (rotated) phase $\delta\phi$ for the 1×4 phase elements $\theta(x)$. Thus, the quantization patterns can be adjusted by tuning the phase shift parameter $\delta\phi$ within the range $[\pi/L,-\pi/L]$, where L is the number of quantization phase

levels. The procedure of applying the phase shifting quantization is the following: (the derived phase profile is $\phi(x)$)

(1) $\phi_0(x)= \phi(x)$.

(2) $\phi_{l+1}'(x)=[\phi_l(x)-\delta\phi]_{\mathrm{mod}}\, 2\pi$, where $\delta\phi=2\pi/(LN)$, L is the number of discrete phase level and N is the number of grid points.

(3) $\underline{\phi}_{l+1}(x)=QZ[\phi_{l+1}'(x)]$, where QZ is the fixed quantization operator.

(4) Calculate the reconstruction Mean Square Error (MSE) or other evaluation parameters for the quantized phase $\underline{\phi}_{l+1}(x)$.

(5) $\phi_l(x)=\phi_{l+1}'(x)$. If $\phi_l(x)=\phi_0(x)$, then stop; otherwise go to (2).

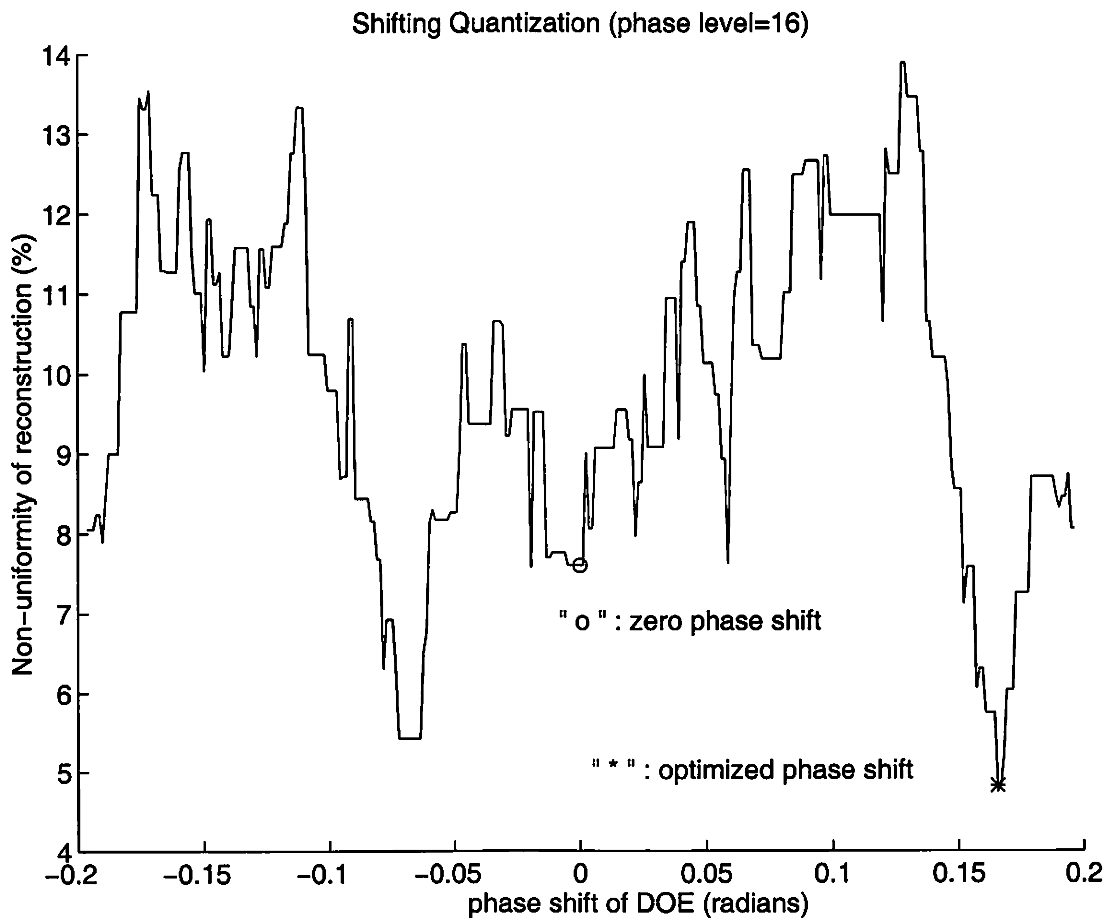


Figure 3-5: Improvement of uniformity by using phase shifting quantization.

Figure 3-5 shows the improvement of the non-uniformity factor as a function of phase shift $\delta\phi$ for calculated DOE phase elements for a 4×4 spot array generator example. In Figure 3-5, the non-uniformity of reconstruction with a phase shift $\delta\phi=0$ is around 7.59% (labeled as 'o') while it is 4.83% for a 0.165 radian constant phase shift applied to the calculated DOE phase elements (labeled as '*'). The number of phase levels L is 16 in the Figure 3-5 simulation.

3.6 Simulation Results

In this section, we compare the reconstruction simulations for a cellular hypercube digital interconnection pattern DOEs which are designed using the two-stage iterative Fourier transform (IFT) method and Nonlinear Least Square (NLS) methods. The five parameters, non-uniformity (U), window efficiency (η_w), grating efficiency (η_g), signal-to-noise ratio (SNR) and quality factor (QF) of Eq. (3.21) and (3.25), are evaluated in each simulated reconstruction.

Figure 3-6 illustrates the design procedure of using the NLS method and phase shifting quantization scheme. In Figure 3-6, the first step is to specify the objective efficiency η_o of the desired diffraction pattern **I**. The definition of η_o is

$$\text{Objective efficiency } (\eta_o) = \sum_{m,n\in R} I(m,n) / \sum_{m,n} I(m,n), \tag{3.27}$$

where $\boldsymbol{R}$ defines the region of signal diffraction orders as in Eq. (3.19) and $I(m, n)$ are the elements of the diffraction pattern **I** described in section 3.4. The purpose of η_o is to reduce the noise order constraints.

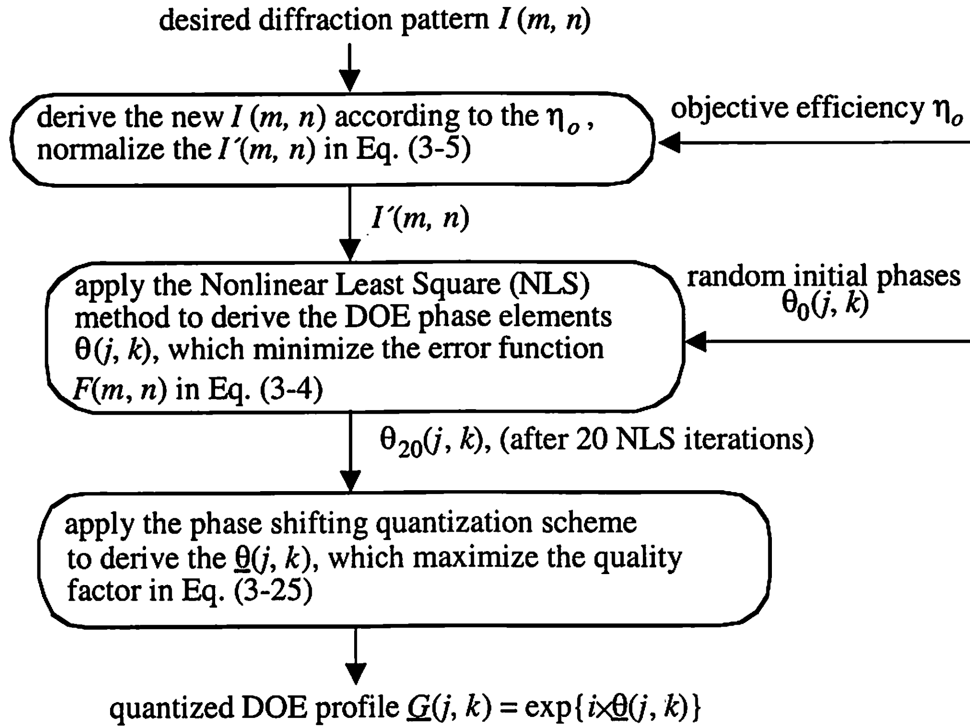


Figure 3-6: The diagram of DOE design using the Nonlinear Least Square (NLS) method and the phase shifting quantization scheme.

For example, if the desired diffraction pattern (normalized) with η_o=100% is

$$\mathbf{I} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0.2 & 0 & 0 \\ 0 & 0.2 & 0.2 & 0.2 & 0 \\ 0 & 0 & 0.2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix},$$

then the diffraction pattern with η_o=90% is

$$\mathbf{I} = \begin{bmatrix} 0.005 & 0.005 & 0.005 & 0.005 & 0.005 \\ 0.005 & 0.005 & 0.18 & 0.005 & 0.005 \\ 0.005 & 0.18 & 0.18 & 0.18 & 0.005 \\ 0.005 & 0.005 & 0.18 & 0.005 & 0.005 \\ 0.005 & 0.005 & 0.005 & 0.005 & 0.005 \end{bmatrix}.$$

Ideally, the objective efficiency η_o should be 100%. However, from simulations, we notice that reducing η_o relaxes the constraints in NLS iterations and results in DOE designs with better *SNR* in trade off for very small reduction of grating efficiency η_g without any distinct effect on the uniformity and the window efficiency η_w. The phase shifting quantization scheme described in section 3.5 is applied after the phases have been iteratively determined using the NLS method. The quality factor (*QF*) with a fixed set of weights is used to determine the optimized phase shifted DOEs during the phase shifting quantization process. For the two-stage IFT method described in section 3.3, the η_o is restricted to be 100% (Eq. (3.19)) in the first stage while the noise orders are preserved during the iterations in the second stage. In fact, because of the amplitude and phase freedom for the noise orders in the second stage, there is no significant improvement on the overall performance (quality factor) for the two-stage IFT algorithm by changing the η_o. In case we want to vary the η_o at the first stage of IFT algorithm, the modified diffraction plane constraints turns to be

$$\begin{aligned} g'_{l+1}(m,n) &= \eta_o [I'(m,n)]^{1/2} \exp(i\angle \overline{g}_l(m,n)), \quad \text{for } (m,n) \in \boldsymbol{R} \\ &= c, \quad \text{for } (m,n) \notin \boldsymbol{R}, \end{aligned} \tag{3.28}$$

where $c=(1-\eta_o)/\{\text{number of noise diffraction orders}\}$.

The target pattern used for simulation is the 16×16 {1, 2, 4} cellular hypercube interconnection pattern [33], which is useful in parallel optical cellular logic processing [34]. The reconstructed pattern is shown in Figure 3-7.

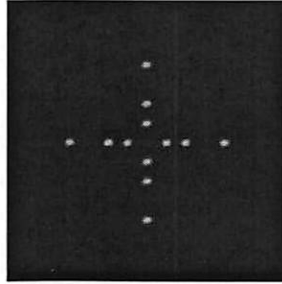


Figure 3-7: The diffraction pattern of {1, 2, 4} cellular hypercube interconnection DOE.

The normalized diffraction intensity matrix for this pattern with η_o=100% is

$$\mathbf{I}=\begin{bmatrix}
0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0\\
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0&0&0&0&0&0&0&0&1&0&0&0&0&0&0&0\\
0&0&0&0&1&0&1&1&0&1&1&0&1&0&0&0\\
0&0&0&0&0&0&0&0&1&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&1&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&1&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0
\end{bmatrix}\times\frac{1}{12}.$$

According to the discussion above, we specify a slightly reduced objective efficiency η_o of 97-99% for the NLS method, while η_o=100% is specified for the two-stage IFT method. The definition of quality factor (*QF*) for this cellular hypercube pattern and both the other two patterns is

$$QF=\frac{5}{7}\times(100-U(\%))+\frac{1}{7}\times\eta_g(\%)+\frac{1}{7}\times SNR(\text{dB}), \tag{3.29}$$

which implies that {0.2% variation in U}={1% variation in η_g}={1dB variation in *SNR*}. We think these weights are reasonable for general-purpose DOE applications and they can be modified for other specific applications. Table 3-1 lists the simulation results.

From Table 3-1, we can see that the DOEs designed using the NLS method have lower non-uniformity, larger signal-to-noise ratio and better quality factor than those designed using the two-stage IFT method when L is greater than 4. For those designs using the NLS method with more than sixteen phase levels (L>16), our results did not improve over the case of L=16 when limited to 20 initial guesses. The similar situation occurs for the L=32 case in the two-stage IFT method when limited to 500 initial guesses. The grating efficiency η_g of the DOE designs using the NLS method is about 1~1.2% lower compared with those using two-stage IFT method because of the reduced objective efficiency η_o (97%) in order to derive better *SNR* (2.3~2.5dB larger). In general, the NLS method produces even better results as the number of discrete phase level L increases.

method	L	U(%)	η_w(%)	η_g(%)	*SNR* (dB)	*QF*	η_o(%)	number of initial guess
Nonlinear Least Square	4	2.92	81.84	67.69	9.66	80.39	98	100
	8	1.16	89.89	77.91	13.51	83.66	99	40
	16	0.25	91.91	81.05	13.81	84.80	97	20
	32	0.25	91.91	81.05	13.81	84.80	97	
	64	0.25	91.91	81.05	13.81	84.80	97	
	C*	0.25	91.91	81.05	13.81	84.80	97	
2-stage Iterative Fourier Transform	4	3.84	82.07	68.42	9.58	79.82	100	500
	8	1.45	89.62	78.06	13.13	83.42	100	
	16	1.04	91.99	81.56	11.29	83.95	100	
	32	0.69	92.56	82.25	11.57	84.34	100	
	64	0.69	92.56	82.25	11.57	84.34	100	
	C*	0.69	92.56	82.25	11.57	84.34	100	

*: C indicates continuous phase

Table 3-1: Simulation results of different methods for cellular hypercube pattern {1,2,4}.

The binary phase case (L=2) is omitted in Table 3-1 because neither the NLS nor IFT algorithms produce a satisfactory result. In fact, the simulated annealing method is generally used to design binary phase DOEs. Because there are only two-phase levels for each phase element in this case, the computation cost of generating a satisfactory result for the simulated annealing method is still acceptable.

Figure 3-8 shows the Mean Square Error (MSE), defined in Eq. (3.3), for the L=16 phase level cellular hypercube {1,2,4} interconnection simulation whose performance parameters are shown in Table 3-1 as a function of the number of floating point operations (flops) for both the NLS and the two-stage IFT methods. The solid line in Figure 3-8 represents the MSE vs. cost curve for the NLS method from 1 to 20 iterations plus the phase shifting quantization process. The dashed line in Figure 3-8 represents the MSE vs. cost curve for the two-stage IFT method with 40 iterations in the first stage and 137 iterations in the second stage including the stepwise quantization process. We clearly see that the DOE designed using the NLS method has lower MSE after a few iterations while the MSE of the design using the two-stage IFT method reaches the sub-optimal point and cannot be reduced by further iterations. For more design examples and details, please refer to the paper in reference [35].

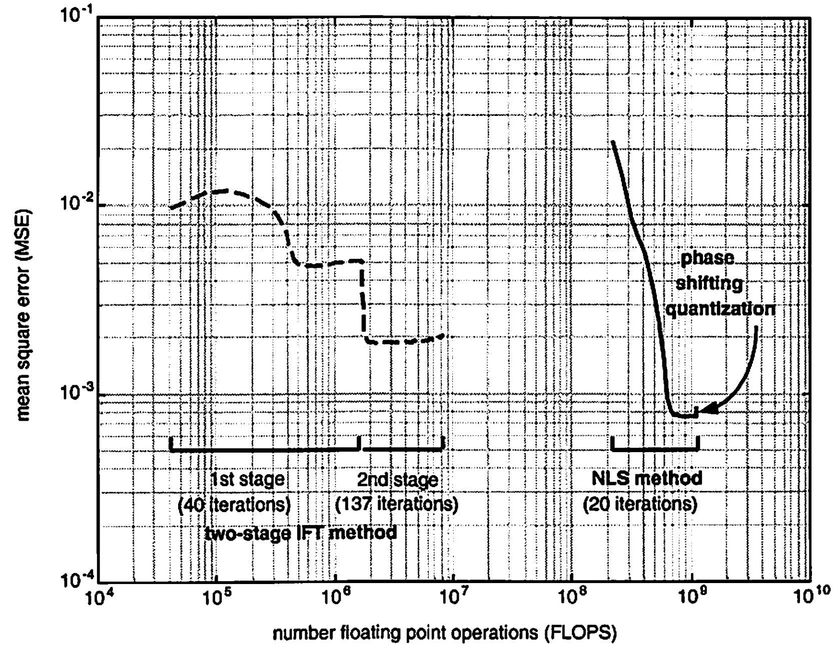


Figure 3-8: Mean Square Error (MSE) versus computation cost (flops) for 16-phase levels cellular hypercube interconnection pattern [1,2,4].

Chapter 4 Design and Analysis of Diffractive Microlenses

Diffractive microlenses have been an attractive alternative of refractive microlenses. They can be fabricated by mask-based lithography processes that result in binary or multiple phase levels elements. These techniques are compatible with VLSI fabrication processes and provide high degree of freedom for the design. However, high diffraction efficiency and high numerical aperture for the diffractive microlenses cannot be simultaneously achieved because of the linewidth limitation in the fabrication processes. As a result, the modified design algorithms [36]-[38], which adaptively vary the number of phase levels in the microlenses, are proposed to improve the diffraction efficiency and the numerical aperture. Further diffraction efficiency considerations are also described in references [39][40]. In this chapter, we develop the analytic forms to define the feasible F/#, numerical aperture and focal length with respect to the specified fabrication linewidth, operation wavelength and physical size of microlenses. We propose a hybrid phase level design method, which is simplified from these adaptively varying phase level methods to be more suitable for the mask etching fabrication processes. We also develop an integrated design program for diffractive optics, which combines the hybrid phase level design algorithm for diffractive microlenses and the iterative design algorithms described in Chapter 3 for the DOEs. This program is able to integrate both the diffractive microlens designs and DOE designs on the same substrate and generate the integrated mask layout files for the vendors to fabricate.

4.1 Design Criteria

From Figure 2-2, we notice that the minimum feature size constraint in VLSI fabrication process limits the available range of the ring period r_P, thus the focal length f of the Fresnel lenses. The relation between the feature size w, lens diameter D, ring period r_P, number of phase levels L, operational wavelength λ, and the focal length f is described in the following.

For the diameter D of a Fresnel lens, we have

$$D = 2r_{Pm}\sqrt{N}\,, \tag{4.1}$$

and

$$N_L \le N < N_L + 1 = N_H\,, \tag{4.2}$$

where r_{Pm} is the minimum feasible ring period, N is a real number, N_L is the maximum integer which is less or equal than N, and N_H is the minimum integer which is larger than N. Then, the given minimum feature size w satisfies

$$r_{pm}(\sqrt{N_H} - \sqrt{N_H - \frac{1}{L}}) < w \le r_{pm}(\sqrt{N_L} - \sqrt{N_L - \frac{1}{L}}\,, \tag{4.3}$$

where L is the number of phase levels. Using a first order approximation to the second square root term, we derive a simpler relation

$$\frac{r_{Pm}}{2L\sqrt{N_H}} < w \le \frac{r_{Pm}}{2L\sqrt{N_L}}\,. \tag{4.4}$$

From Eq. (4.4), the minimum feasible ring period r_{Pm} is in the range

$$2wL\sqrt{N_L} \le r_{Pm} < 2wL\sqrt{N_L + 1}\,, \tag{4.5}$$

while it should also satisfy Eq. (4.1). Since the focal length $f=r_p^2/(2\lambda)$, the derived minimum feasible focal length f_m is in the range

$$\frac{2w^2L^2N_L}{\lambda} < f_m \leq \frac{2w^2L^2(N_L+1)}{\lambda}. \tag{4.6}$$

The minimum feasible F-number $(F/\#)_{min}$, which is defined as f_m/D, can be directly derived from Eq. (4.6).

4.2 Hybrid Phase Level Design Method (Feature Expansion)

In order to further utilize the SBWP (space bandwidth product) and also lower the F-number (F/#) of the diffractive lenses, we use a varying number of phase levels in the diffractive lens design. This design method uses the maximum number of phase levels from the first ring period until the plotted linewidth of the feature decreases below the minimum feature size. Then, it adaptively changes to the next fewer number of phase levels with the expanded line width. This phase level reduction procedure is repeatedly executed until only two phase levels are used or the maximum diameter size is reached.

We have designed several different microlens arrays for the smart pixel systems using the hybrid phase level method. Table 4-1 and Figure 4-1 show one microlens array design we have developed using this method and compared with two other designs using traditional microlens design method.

lenslet array design	F/#	focal length (μm)	lenslet aperture (μm^2)	phase levels	Minimum feature (μm)	diffraction efficiency η_g	array size
1	4.17	884	150×150	16/8/4	1	90.85%	8×8
2	4.17	884	150×150	4	1	81.06%	8×8
3	10.36	2198	150×150	16	1	98.72%	8×8

Table 4-1: Comparison of different microlens array designs.

Table 4-1 shows three diffractive microlens designs and the phase profiles of design 1, 2 and 3 are shown in Figure 4-1(b), (c) and (d), respectively. Figure 4-1(a) shows a continuous phase diffractive microlens with F/#=4.17 and focal length f= 884μm for comparison with the other three discrete phase level designs. For design 1 in Table 4-1, we applied the hybrid method with 16, eight and four phase levels combined. For design 2 and designs 3, we applied the regular diffractive lens design method with four phase levels and 16 phase levels, respectively. In Figure 4-1(b), we see that the number of phase level starts with 16 in the first ring period and, since the linewidth is less than the feature size (1μm) in the second period, an eight phase level design is applied in the following periods. After five ring periods, the linewidth shrinks to less than the feature size again, so a four phase level design is applied for the rest of the lens area. In Figure 4-1(c), the design uses only four phase levels with the same ring-period for comparison of Figure 4-1(b). In Figure 4-1(d), the design uses only 16 phase levels. Because of the linewidth constraint mentioned in the previous section, the minimum ring-period for this design is much larger than the other two designs. From Table 4-1, we see that the regular design method with 16 phase levels (design 3) can only derive F/#>10, while the hybrid method (design 1) is capable of deriving the design with a much lower F/#=4.17 or less.

By using the regular design method with four phase levels (design 2), we also derive the design with F/#=4.17, but with diffraction efficiency η_g=81% (defined in Eq. (3.23)) that is much less than the design using the hybrid method (η_g = 91%). This is because the hybrid phase level design method can extend the feature size limitation and, in another words, better utilize the SBWP of the microlenses.

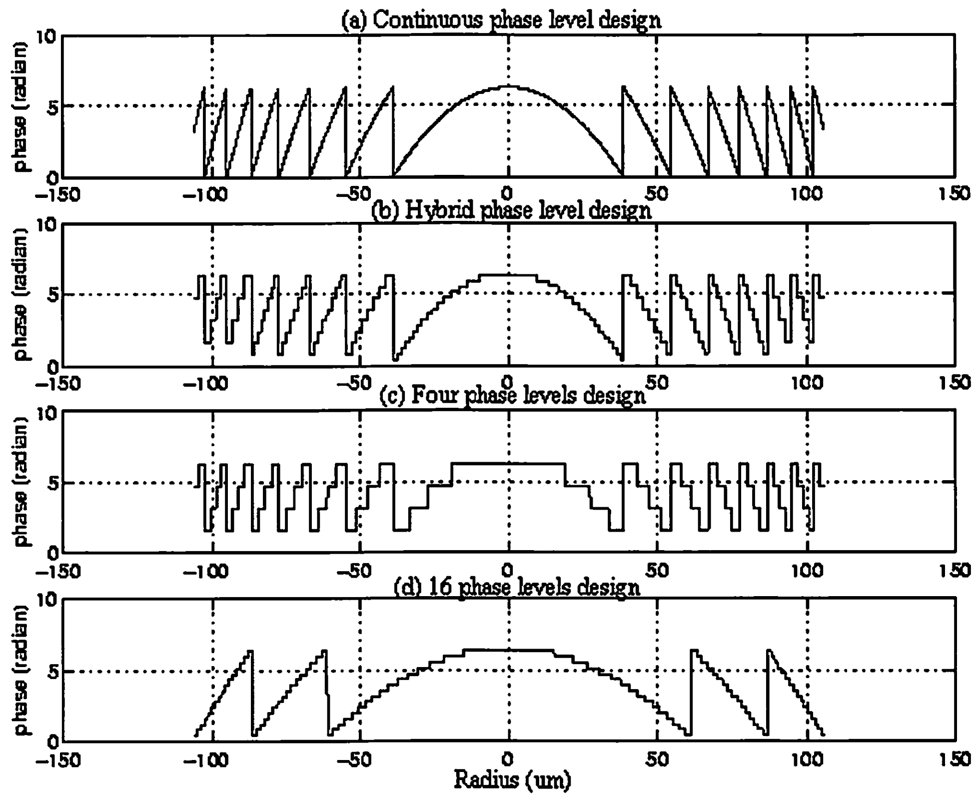


Figure 4-1: (a) Continuous phase profile of diffractive microlens with F/#=4.17 and focal length f=884μm. (b) Phase profile of diffractive microlens design 1 (with hybrid phase level) in Table 4-1. (c) Phase profile of diffractive microlens design 2 in Table 4-1. (d) Phase profile of diffractive microlens design 3 in Table 4-1.

4.3 Integrated Diffractive Optics Design Program

We have developed an integrated design program in MATLAB® to generate both diffractive optical elements and diffractive microlens arrays onto the same substrate. It creates the respective mask files in CIF or GDS format for the vendors to fabricate using lithography etching procedures. The integrated design flowchart is shown in Figure 4-2.

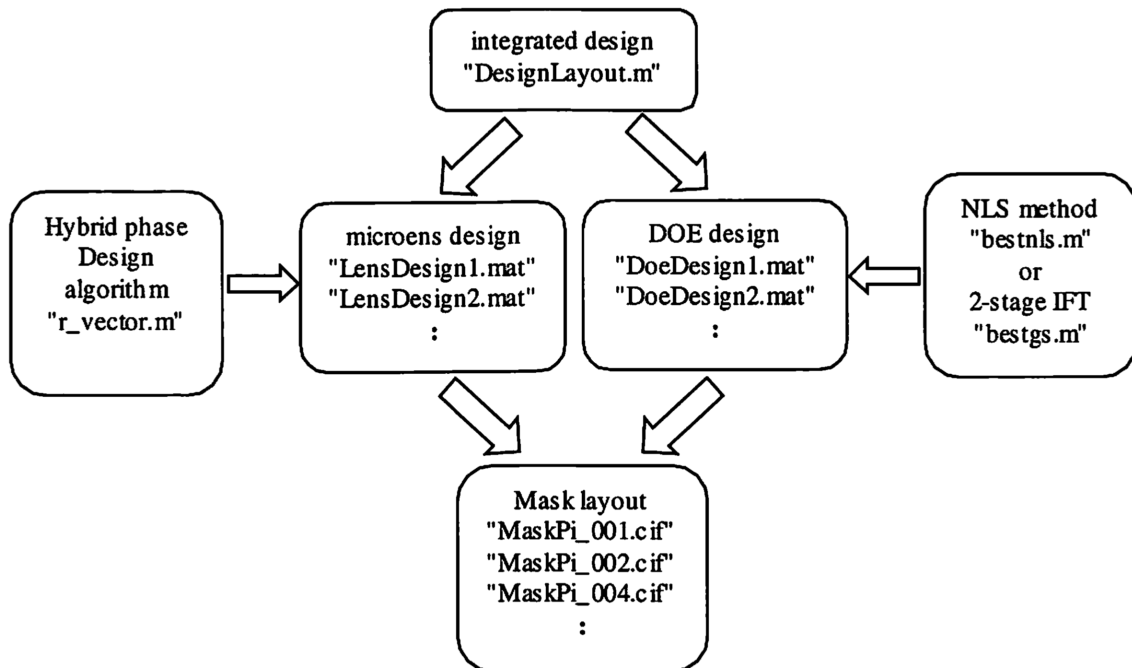


Figure 4-2: Integrated diffractive optics design flowchart.

The integrated program in file "DesignLayout.m" contains two parts of procedures. One part is to generate the DOEs layout and the other part is to generate the layout for diffractive microlens arrays. All the designs with respective parameters are included in the file and specified by the location coordinates for placement on the substrate. The DOE design data are derived from either the nonlinear least square (NLS) design algorithm (file "bestnls.gs") or 2-stage iterative Fourier transform (IFT) method

(file "bestgs.m") described in Chapter 3. The design data for diffractive microlenses are derived using the hybrid phase design algorithm (file "r_vector.m") described in section 4.2. As a result, the integrated program will generate k mask layout files "MaskPi_001, 002, 004...L", if the maximum number of phase levels 2^k are used.

4.4 Decomposition/Synthesis Analysis for Diffractive Lenses

4.4.1 Point Source Interference Representation of Phase-only Diffractive Lenses

In section 2.2, we describe the grating function of an FZP as

$$g(r) = \text{circ}(\frac{r}{r_p\sqrt{P}})\sum_{n=-\infty}^{\infty} A_n \exp(\frac{2\pi i n r^2}{r_p^2}), \tag{4.7}$$

where

$$A_n = \exp(\frac{-i\pi n}{L})\text{sinc}((\frac{n}{L})\delta(n-[mL-1])), \tag{4.8}$$

L is the number of phase levels in FZP and r_P is the ring period as shown in Figure 2-2. Taking each quadratic phase term in Eq. (4.7) as a spherical wavefront from a point source, we get the representation of an FZP as an interference of several point sources [41]-[44]. Observing that A_n's in Eq. (4.8) are close to zero when n is large, consider the use of a finite number of Fourier series terms in Eq. (4.7) to represent the effective grating function of FZP as

$$g(r) = \text{circ}(\frac{r}{r_p\sqrt{P}})\sum_{k=-M_1}^{M_2} A_n \exp(\frac{-i\pi r^2}{\lambda z_n}), \tag{4.9}$$

where

$$A_n = A_{(kL-1)} = \exp(\frac{i\pi}{L})(-1)^k \mathrm{sinc}(k-\frac{1}{L}),\ z_n = \frac{-r_p^2}{2n\lambda} = \frac{-r_p^2}{2\lambda(kL-1)}, \tag{4.10}$$

$n=kL-1$, and $M_1, M_2 \geq 0$.

In Eq. (4.10), we removed all the $A_n=0$ terms, so the index 'n' in Eq. (4.10) equals 'kL-1'. The number of components used to generate the effective FZP in Eq. (4.9) is $M=M_1+M_2+1$. From above discussion, we see that the effective FZP is actually the coherent interference pattern of the wavefront from individual point sources at specific locations with different complex amplitude. The location of k-th point source is just the (kL-1)-th focal plane of FZP. The graphic illustration is in Figure 4-3.

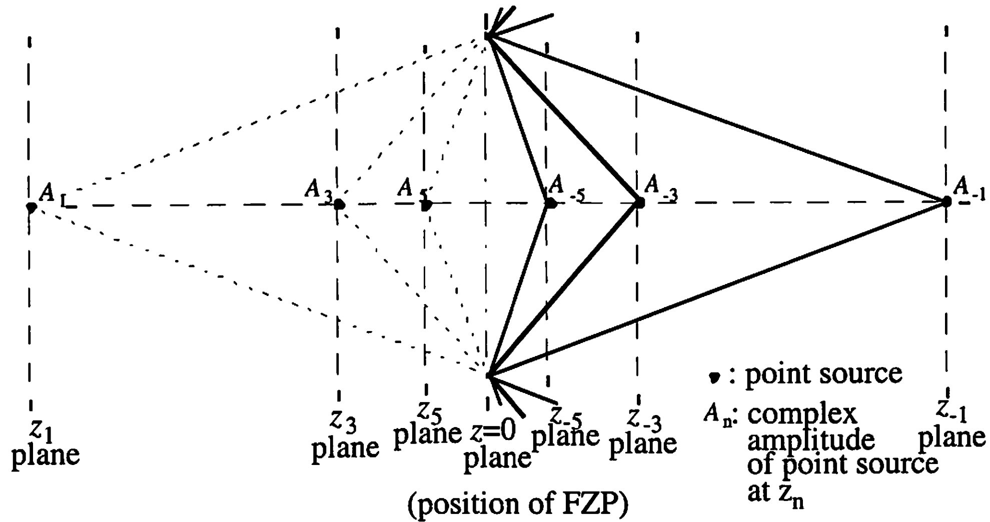


Figure 4-3: Point-sources interference representation of binary phase level (L=2) FZP with the number of synthesis components M=6.

4.4.2 Thin Lenses Decomposition/Synthesis Analysis

In section 4.4.1, we have described that the FZP can be taken as the interfered pattern of infinite number of point sources with different weights located at specific position on the optical axis. However, we can treat Eq. (4.7) from another point of view. The quadratic

phase term in Eq. (4.7) can be viewed as not only the wavefront of a point source but also the phase profile of a thin lens. It means that the phase profile of FZP can be taken as the summation effect of infinite number of thin-lens phase profiles with different weights and focal lengths. Figure 4-4 illustrates this thin-lens decomposition concept.

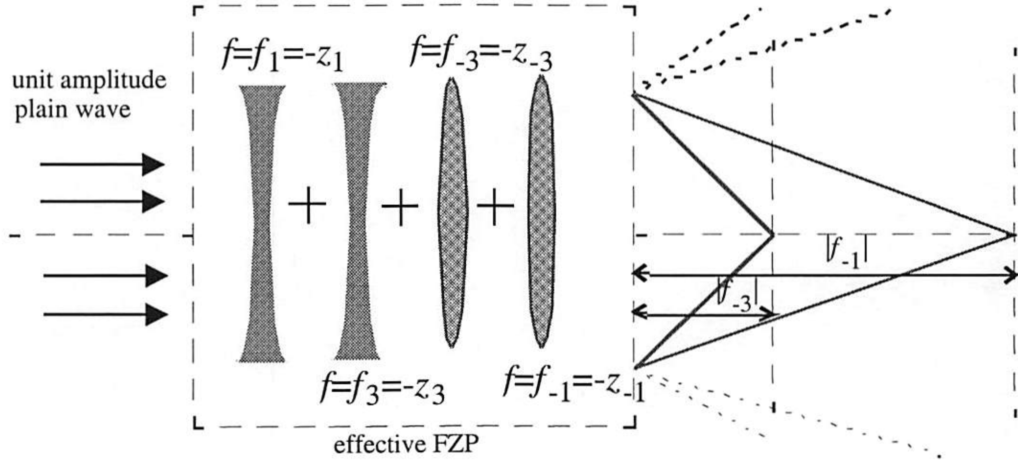


Figure 4-4: Thin-lens decomposition of a binary phase FZP with four components.

Similarly to Eq. (4.9), we can rewrite Eq. (4.7) as

$$g(r) = \mathrm{circ}(\frac{r}{r_p\sqrt{P}}) \sum_{k=-M_1}^{M_2} A_n \exp(\frac{i\pi r^2}{\lambda f_n}), \tag{4.11}$$

where

$$A_n = A_{(kL-1)} = \exp(\frac{i\pi}{L})(-1)^k \mathrm{sinc}(k-\frac{1}{L}),\ f_n = \frac{r_p^2}{2n\lambda} = \frac{r_p^2}{2\lambda(kL-1)}, \tag{4.12}$$

$n=kL$-1, and M_1, $M_2 \geq 0$. In Eq. (4.11), those f_n's less than zero ($n<0$) represent the positive lenses, and those f_n's greater than zero ($n>0$) represent the negative lenses. We also see that the magnitude of f_n in Eq. (4.11) is exactly the magnitude of z_n in Eq. (4.9) but with negative sign. To synthesize the effective FZP, we simply take the summation

of diffraction fields from finite number of thin-lenses' phase profiles, which have respective complex constant amplitude A_n and focal length f_n. In another words, the Fresnel Zone Plate is actually a superposition of individual thin lenses with different constant weights and focal lengths. This concept is useful especially on the calculation of diffraction patterns of FZP with complicated input profile illumination. For example, if we want to calculate the diffraction pattern $U(r', z)$ of FZP for the object U_{obj}, we just need to directly sum up the individual diffraction pattern $G_n(r', z)$ of each decomposed thin-lens as

$$U(r',z) \cong B \cdot FT\{ \sum_{n=-N_1}^{N_2} U_{obj}(r,z=0)A_n \exp(i\pi r^2(\frac{1}{f_n}+\frac{1}{\lambda z}))\}_{f_r=\frac{r'}{\lambda z}} = B\sum_{n=-N_1}^{N_2} G_n(r',z) \tag{4.13}$$

where

$$G_n(r',z) = BFT\{U_{obj}(r,z=0)A_n \exp(i\pi r^2(\frac{1}{f_n}+\frac{1}{\lambda z}))\}_{f_r=\frac{r'}{\lambda z}}. \tag{4.14}$$

The BFT{} in the above equation indicates the Bessel Fourier Transform. If the diffraction pattern $G_n(r', z)$ of each thin-lens is in analytic form, the derivation of $U(r', z)$ is only at the cost of 1-D summation operation.

4.4.3 Synthesis Simulation for Gaussian Beam Illumination on Phase-only Diffractive Lens

In order to demonstrate the advantage of applying Thin Lenses decomposition/synthesis analysis method, we simulate the diffraction pattern of FZP while it is illuminated by the Gaussian beam source at distance z_2 = 40mm with radius r_0 = 100μm before the FZP plane (z=0).

Gaussian beam source : $U_{obj}(r, z = -z_2) = \exp(\frac{-r^2}{r_0^2})$, (4.15)

where $r_0 = 100\mu m$, $z_2 = 40000\mu m$.

Field at front surface of FZP (from Eq.(5-11)) : $\lambda=0.633\mu m$

$$U(r, z = 0) = \frac{1}{i\lambda z_2}\exp(ik(z_2 + \frac{r^2}{2z_2}))FT\{U_{obj}(r, z = -z_2)\exp(\frac{i\pi r^2}{\lambda z_2})\}_{f_r=\frac{r}{\lambda z_2}} . \tag{4.16}$$

$$\text{FZP phase profile} : g(r, z = 0) = \sum_{k=0}^{N(L-1)}\exp(\frac{-i2\pi k}{L})\text{rect}(\frac{r^2 - \frac{kr_p^2}{L} - \frac{r_p^2}{2L}}{\frac{r_p^2}{L}}) , \tag{4.17}$$

where $r_p = 100\mu m$, L=4, N=100 (diameter=$2r_p(N)^{1/2}$ = 2000μm).

Fresnel diffraction pattern at distance z_a :

$$U_{fdp}(r, z = z_a) = D \cdot FT\{U_{obj}(r, z = 0) \cdot g(r)\exp(\frac{i\pi r^2}{\lambda z_a})\}_{f_r=\frac{r}{\lambda z_a}} , \tag{4.18}$$

$$\text{where} \quad D = \frac{1}{i\lambda z_a}\exp(ik(z_a + \frac{r^2}{2z_a})) . \tag{4.19}$$

Fresnel synthesis pattern at distance z_a: (from Eq. (4.9))

$$U_{fsp}(r, z = z_a) = D \cdot FT\{\sum_n A_n \exp(\frac{i\pi r^2}{\lambda f_n})\text{circ}(\frac{r}{r_p\sqrt{N}})U(r, z = 0)\exp(\frac{i\pi r^2}{\lambda z_a})\}_{f_r=\frac{r}{\lambda z_a}} , \tag{4.20}$$

Direct synthesis pattern at distance z_a: (from Eq. (4.13))

$$U_{dsp}(r, z = z_a) = D\sum_n \exp\{-r^2[\frac{\pi s}{\lambda^2 z_a^2(s^2 + T_n^2)}]\}\exp\{-ir^2[\frac{\pi T_n}{\lambda^2 z_a^2(s^2 + T_n^2)} - \frac{\pi}{\lambda z_a}]\} \tag{4.21}$$

$$\text{where } s = [\pi r_0^2(1 + (\frac{z_2}{z_R})^2]^{-1}, \ T_n = \frac{1}{\lambda}\{[z_2(1 + (\frac{z_R}{z_2})^2)]^{-1} - \frac{1}{f_n} + \frac{1}{z_1}\} . \tag{4.22}$$

The diffraction field derived from conventional numerical Fresnel diffraction equation on FZP is in Eq. (4.18), which is called **Fresnel Diffraction Pattern.** The **Fresnel Synthesis Pattern** is derived by applying the Fresnel diffraction equation to a finite number of decomposed thin-lens components of FZP which are then summed to form the diffraction field in Eq. (4.20). The diffraction field derived by direct summation of the already known diffraction patterns (Eq. (4.14)) of each thin-lens component of FZP is described in Eq. (4.21), which is called **Direct Synthesis Pattern.** The difference between the Fresnel Synthesis Pattern and Direct Synthesis Pattern is that the latter is the linear addition result of the explicit diffraction pattern formula, Eq. (4.14), of decomposed thin-lens components at different focal length while the former performs Fresnel diffraction equation on each decomposed components of FZP and then sums up. Therefore, the cost of computing Direct Synthesis Pattern is proportional to the object dimension n, while the cost of computing the Fresnel Synthesis Pattern is on the order of n^2.

In the following simulation, we compare the Fresnel Diffraction Patterns U_{fdp} from Eq. (4.18) and two different synthesis patterns: Fresnel Synthesis Pattern U_{fsp} from Eq. (4.20) and Direct Synthesis Pattern U_{dsp} from Eq. (4.21).

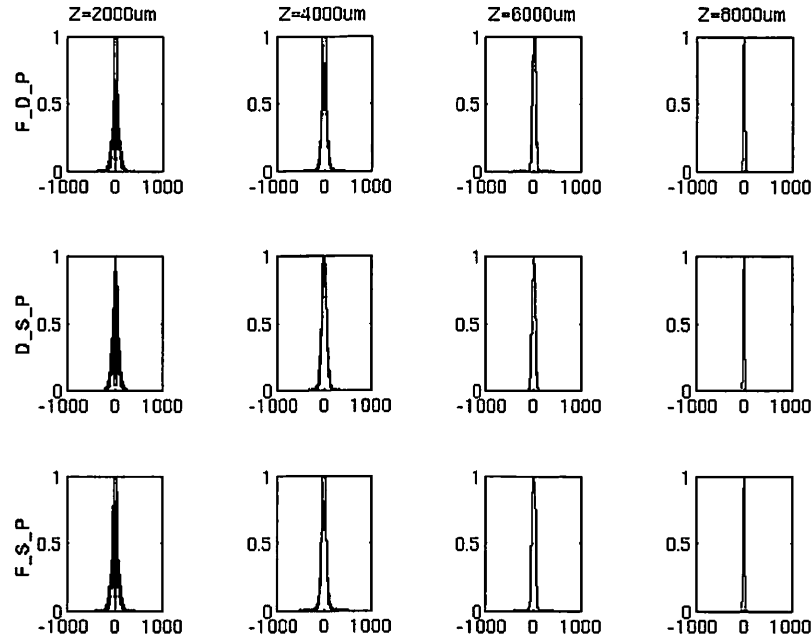


Figure 4-5: Synthesis simulation for propagation distance z=2000μm to 8000μm. F_D_P denotes Fresnel Diffraction Pattern, D_S_P denotes Direct Synthesis Pattern and F_S_P denotes Fresnel Synthesis Pattern.

Figure 4-5 shows the comparison of Fresnel Diffraction Patterns, denoted by F_D_P, Direct Synthesis Patterns, denoted by D_S_P and Fresnel Synthesis Patterns, denoted by F_S_P, at different observation plane. It is observed that the Fresnel Synthesis Pattern is closer to the Fresnel Diffraction Pattern than the Direct Synthesis Pattern. This is because Direct Synthesis Pattern applies the theoretically derived diffraction field formula for a thin-lens, which assumes infinite size of lens aperture, to synthesize the diffraction field of FZP. But, the physical diffraction of FZP occurred with finite size of pupil function as described in Fresnel Diffraction Pattern and Fresnel Synthesis Pattern. However, when the diffracted beam diameter is near the beam waist, the direct synthesis pattern can also yield a very precise result because the phase variation around beam waist is close to zero. Hence, as long as the phase variation of the

diffraction field of FZP is much less than the aperture effect of the FZP pupil function, we can apply Direct Synthesis Pattern to approximate the Fresnel Diffraction Pattern with a lot less computation cost.

Figure 4-6 shows the Mean Square Error (MSE) comparison of the Fresnel Synthesis Patterns and Direct Synthesis Patterns at propagation distance from 2000μm to 24000μm. The MSE is defined as

$$MSE \equiv \{\frac{1}{T}\sum_{i\in T}(I_a(i) - I_s(i))^2\}^{1/2}. \tag{4.23}$$

We can see that the MSE is kept below 0.03 for the Fresnel Synthesis Patterns. This is mainly from the truncation error as finite number of thin-lens components of FZP is used to synthesize the diffraction field. On the other hand, the MSE of Direct Synthesis Pattern is small when the diffraction patterns is observed around the beam waist position and is large when the field is observed away from beam waist position. This is due to the aperture effect mentioned above.

Figure 4-7 compares the beam diameter of derived from these three diffraction fields. Similarly, the beam diameter of Fresnel Synthesis Patterns well follows which of Fresnel Diffraction Pattern and the beam diameter of Direct Synthesis Patterns is close to which of Fresnel Diffraction Pattern only around the beam waist position (z=10000μm).

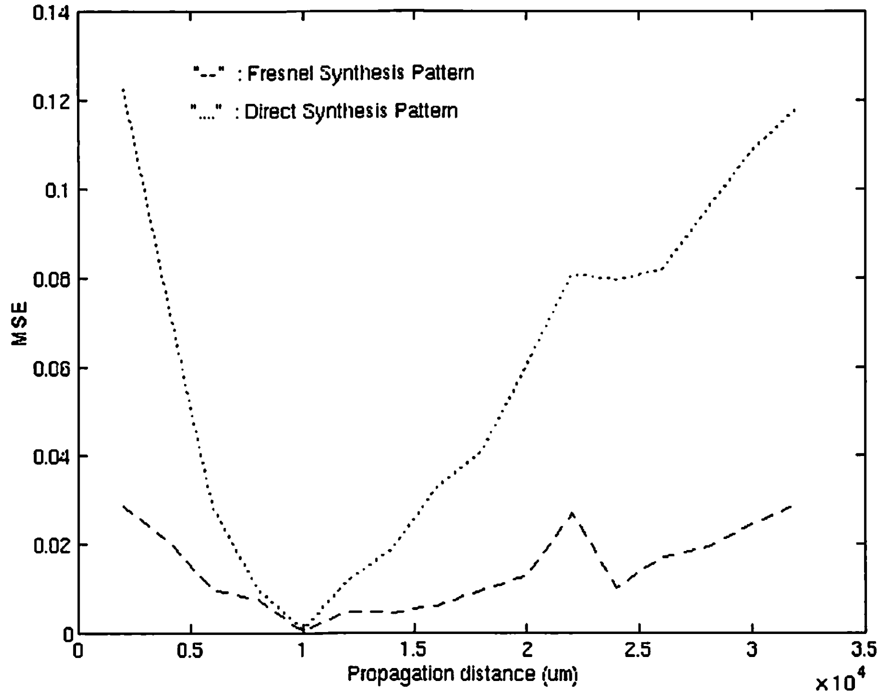


Figure 4-6: MSE comparison of direct synthesis patterns and Fresnel synthesis patterns.

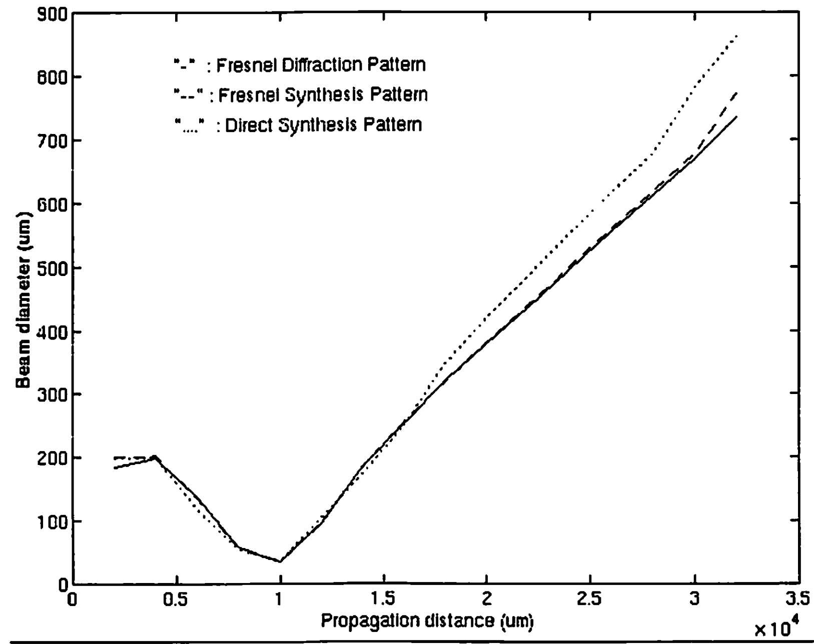


Figure 4-7: Comparison of beam diameter.

simulation	method	computation order	computation time
1	Fresnel diffraction (2-D convolution)	$O(N^4)$	N/A
2	Fresnel diffraction (2-D FFT)	$O(N^2 \log N^2)$	878 sec
3	Fresnel diffraction (1-D BFT)	$\tau \cdot O(N^2)$	330 sec
4	Fresnel Synthesis (1-D BFT)	$\tau \cdot O(N^2)+O(mN^2)$ *3	330 sec
5	Direct Synthesis (1-D linear addition)	$O(mN)$	< 1 sec

*1: Time measurement is taken on HP 9000 machine and N=2000.
*2: BFT=Bessel Fourier Transform. Each call of Bessel function takes time τ.
*3: m is the number of synthesis components, and m=9 in the time measurement.

Table 4-2: Computation cost of FZP diffraction pattern ($N \times N$ pixels circularly symmetric object).

Table 4-2 lists the comparison on computation cost and computation time for three different algorithms mentioned above. For the simulations 1, 2 and 3, the Fresnel diffraction algorithm is used but implemented in different ways [5]. The 1-D BFT Fresnel diffraction method in simulation 3 is used to implement the F_D_P curve Figure 4-5, the Fresnel synthesis method in simulation 4 is used to implement the F_S_P curve in Figure 4-5, and the direct synthesis method in simulation 5 is used to implement the D_S_P curve in Figure 4-5. From Table 4-2, we see that the Fresnel Synthesis method doesn't gain its advantage on the computation cost, while it can synthesize the diffraction pattern with a few components at high accuracy. Hence, the Fresnel Synthesis method mainly contributes to the quality analysis of FZP. On the other hand, the Direct Synthesis method reduces the computation cost a lot in trade off the accuracy. Therefore it is suitable for the quantitative analysis of FZP. However, we should remember that two fundamental assumptions are required in applying Direct Synthesis method:

(1) The aperture of FZP has to be much larger than the spatial resolution of the diffraction field.

(2) The diffraction field of input object with respect to a thin lens is known.

4.4.4 Advantages and Limitations of Thin Lenses Decomposition/Synthesis Analysis

4.4.4.1 Advantage

(1) The decomposition models reduce the complexity of analyzing the FZP

From the discussion above, we know using a few simple components, either point sources or thin lenses can effectively represent the FZP. Hence, instead of directly analyzing the complicated diffraction pattern of FZP, we decompose this diffraction pattern into the summation behavior of individual wavefront generated through the thin lenses, which synthesize the FZP. This superposition synthesis process is linear with respect to the complex amplitude of the wave fronts.

(2) Decomposition method could reduce the computation order

For an input object transmittance, if its thin-lens behavior (diffracted complex field) is known, then we are able to synthesize its FZP diffraction pattern by superimposing the diffracted complex fields with respect to the thin lenses that decompose FZP. By doing so, the computation cost is hugely reduced since the linear addition is much faster to derive than taking the Fourier Transform operation in the numerical Fresnel diffraction equation. In section 4.4.3, I demonstrate the simulation results of applying the thin-lens decomposition method to synthesize the diffraction pattern of FZP, which is illuminated by a Gaussian beam.

4.4.4.2 Limitation

If we have an object transmittance $U_{obj}(r, z=0)$ and the FZP grating function from Eq. (4.9) at z=0 plane, the diffracted complex field at certain plane is derived by using the Fresnel diffraction equation as

$$U(r',z) = B \cdot \{ \frac{J_1(2\pi w)}{\pi w} \otimes BFT[\sum_{n=-\infty}^{\infty} U_{obj}(r, z=0) A_n \exp(i\pi r^2 (\frac{2n}{r_p^2} + \frac{1}{\lambda z}))]_{f_r = \frac{r'}{\lambda z}} \}, \tag{4.24}$$

where BFT denotes the Bessel Fourier transform, $B = \frac{1}{i\lambda z} \exp(\frac{i\pi}{\lambda}(2z + \frac{r^2}{z}))$, J_1 is the Bessel function of first order, $w = \frac{r_p \sqrt{p r'}}{\lambda z}$, and $\otimes$ denotes the convolution operator. We notice that this diffracted complex field is the convolution result of the Fourier transform of FZP's pupil function (aperture), $J_1(2\pi w)/\pi w$, and the diffracted wavefront of FZP. If we try to synthesize this pattern by direct summation of the diffracted complex amplitude $G_n(r', z)$ of each decomposed thin-lenses components by ignoring the convolution effect of finite aperture as described in Eq. (4.21), then we will have an aberration on the synthesized result. Hence, Eq. (4.21) is precise only when the Fourier spectrum of the pupil function, that is $J_1(2\pi w)/\pi$ in Eq. (4.24), is compared negligible to the spatial variation of diffracted wavefront. Otherwise, we have to decompose the FZP without exclusion of the aperture off the Fourier transform, which is shown in Eq. (4.20).

Chapter 5 Testing and Characterization of Diffractive Optical Devices

Investigating the quality of designed and fabricated diffractive optics is very important for evaluating the design algorithms, fabrication processes, and defining the system requirements for optoelectronic smart pixel projects. It reveals the information on device characteristics for system engineers to develop a reliable system with ambient tolerance. In this research, I develop measurement systems to test and characterize the fabricated DOEs and diffractive microlens arrays, which are designed using the methods described in previous chapters. By collecting the testing results, we are able to derive the system parameters, such as power budget, propagation distance, crosstalk and signal-to-noise ratio, to design the smart pixel systems. The devices we have tested include the 4:2:1 weighted fanout DOEs for optical neural network systems, diffractive microlens arrays for SPARCL, SAPIENT, TRANSPAR-MQW and TRANSPAR-VM smart pixel chips, and spot array generators (SAGs) for SPARCL and TRANSPAR-MQW chips. The characterization on mechanical measurement error and various fabrication error sources is also described.

5.1 Measurement System

There are two major ways to investigate the optical beam profile. One is applying the optical interferometer setup system [45][46] to analyze the interfered fringe pattern of the target beam and its coherent reference beam. This interfered pattern reveals the phase

distribution information of the target beam. This type of system is usually used for the measurement of micro-devices thickness, coherent length of a light source or surface profile of an object...etc. The other measurement system is for the direct measurement of power distribution of a beam profile [47][48]. This measurement setup measures the spatial intensity distribution of a beam and its temporal variation. It also shows the beam width (or spot size), which is very useful in many optoelectronic applications, such as laser printing, optical data storage and imaging scanning. Since we are interested in the intensity distribution of the DOE diffraction pattern in this research, we apply the direct measurement system by measuring the reconstructed intensity profile of the fabricated DOEs with charge-coupled devices (CCD).

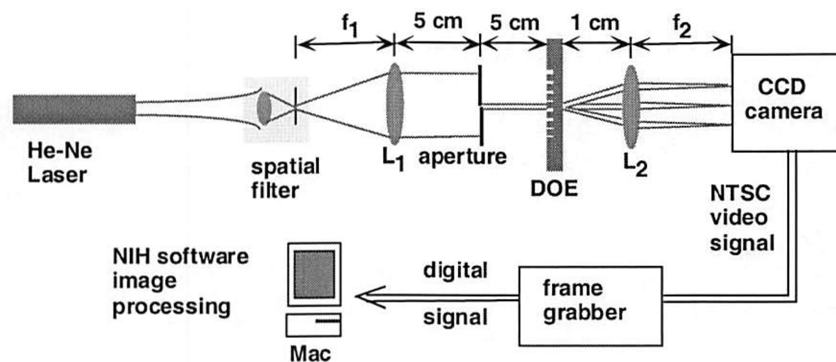


Figure 5-1: Measurement system for DOEs.

Figure 5-1 shows the schematic layout of the test system. This system collimates the laser light with wavelength λ=633nm from the 15μm pinhole spatial filter into a coherent plane wave that illuminates the subject DOE. The system images the resulting diffraction intensity pattern into a 510×492 pixel CCD detector array having a pixel size of 17.3μm×13.4μm, digitizes the pattern into an eight bit signal and stores it in a computer for subsequent processing. We have written a program to calculate the energy

of each diffraction order. These energy levels are compared with the energy levels in the original DOE computer design. A similar measurement setup shown in Figure 5-2 is used for diffractive microlens array testing. This system is used to measure the uniformity and efficiency of the focused spot arrays generated from microlenses.

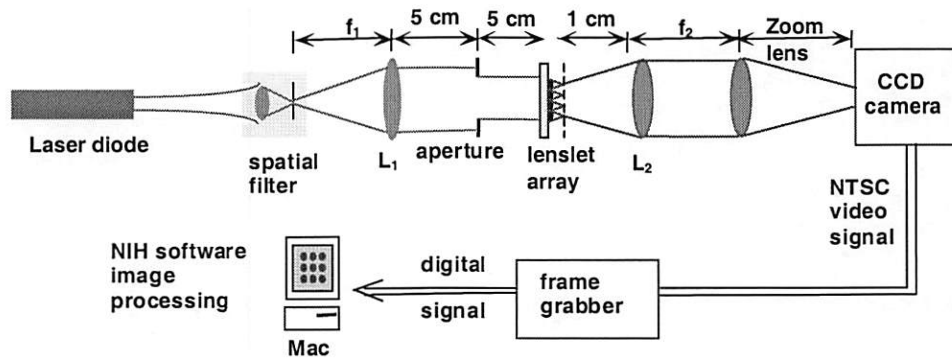


Figure 5-2: Measurement system for diffractive microlens array.

We have fabricated the DOEs and microlens arrays using various design methods with different feature sizes and aperture sizes. We have also used various mask making vendors and processing steps. With the systems shown in Figure 5-1 and Figure 5-2, we experimentally measured and compared the fabricated diffractive optics. In order to characterize both the digital and the analog weighed fanout DOEs, we defined five parameters, including *Group Non-Uniformity* (GNU), *Average Percentage Error* (APE), *Average Group Error* (AGE), *efficiency* and *signal-to-noise ratio* (SNR), to evaluate the DOE reconstruction patterns. Among these five parameters, the GNU and efficiency parameters are also used for the microlens evaluation.

5.2 Evaluation Parameter fo r Analog/Digital DOEs

As an illustration of the reconstruction evaluation, we describe the definitions and calculations of all evaluation parameters for the example DOE designed as in Figure 5-3.

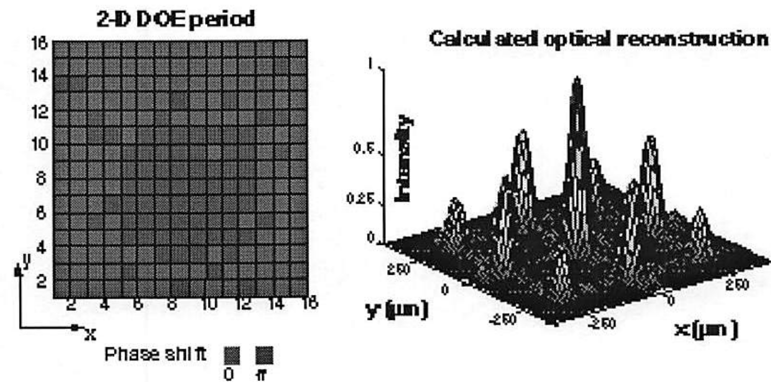


Figure 5-3: (a) 16×16 binary phase elements in one period of a 4:2:1 analog weighted DOE. (b) Simulated reconstruction pattern for the design in (a).

Figure 5-3 shows the design and reconstruction simulation of a 4:2:1 analog weighted DOE, which is useful in the optical neural network systems [49]. The experimentally observed diffraction pattern of this DOE is shown in Figure 5-4. In this DOE, the theoretical intensity of spot 1 should be twice the intensity of spots 2 through 5 (group 0.5) and four times that of spots 6 through 9 (group 0.25).

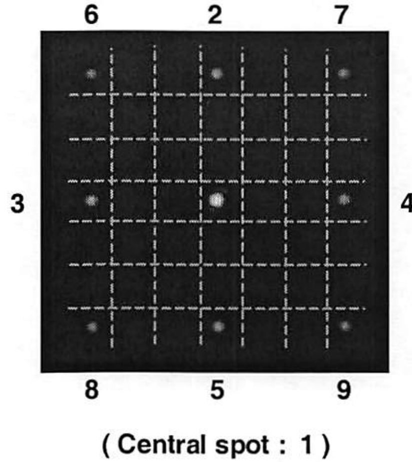


Figure 5-4: Actual measured reconstruction of 4:2:1 weighted fanout DOE. The numbers 1 through 9 are labels for each of the diffracted output orders.

The five parameters described below are applied to the observed pattern in Figure 5-3 to evaluate the reconstruction performance.

5.2.1 Average Percentage Error (APE)

The *Average Percentage Error* (APE) indicates the average percentage error of signal diffraction orders between the observed pattern and the ideal pattern. The definition of APE is

$$APE = \frac{1}{N}\sum_{i=1}^{N}\left|\frac{I_d(i) - \lambda_{opt} I_o(i)}{I_d(i)}\right| \times 100\% , \tag{5.1}$$

where $I_d(i)$ is the i-th signal order of the ideal pattern, $I_o(i)$ is the i-th signal order of the observed pattern, N is the total number of signal orders in the diffraction pattern and λ_{opt} is the normalization factor. In order to have the APE measurement meaningful, the measured diffraction pattern has to be normalized by λ_{opt} to the same bias level as the

ideal pattern. The normalization factor λ_{opt} is derived by minimizing the value of APE to reduce the error caused by the bias intensity level. The derivation of λ_{opt} is using the steepest decent iteration algorithm [50] as

Step 1: $\lambda_0 = I_d(0)/I_o(0)$

$$\text{Step 2: } d\lambda_k = -\alpha \frac{\partial}{\partial \lambda} APE = \alpha \sum_{i=1}^{N} \{ \text{sign}(\frac{I_d(i) - \lambda_k I_o(i)}{I_d(i)})(\frac{I_o(i)}{I_d(i)}) \}, \quad (5.2)$$

where α is the step factor and sign(·) indicates the sign function.

Step 3: $\lambda_{k+1} = \lambda_k + d\lambda_k$

Step 4: repeat step 2 and step 3 till $|(d\lambda_k)/(\lambda_k)| <$ threshold.

In some cases, we want to exclude the zero order effect. Thus, we also define the *Non-Zero order Average Percentage Error* (*NZAPE*) in a similar sense by

$$NZAPE = \frac{1}{N-1} \sum_{i=1}^{N-1} \left| \frac{I_d(i) - \lambda_{opt} I_o(i)}{I_d(i)} \right| \times 100\% . \quad (5.3)$$

Figure 5-5(a) shows the ideal 4:2:1 relative signal intensity level of DOE reconstruction and Figure 5-5(b) shows the respective relative intensity level of the observed pattern in Figure 5-4. By using the definition of Eq. (5.1) and Eq. (5.3), we calculate the *APE* of the pattern in Figure 5-5(b) to be 7.54% and its *NZAPE* is 6.26%.

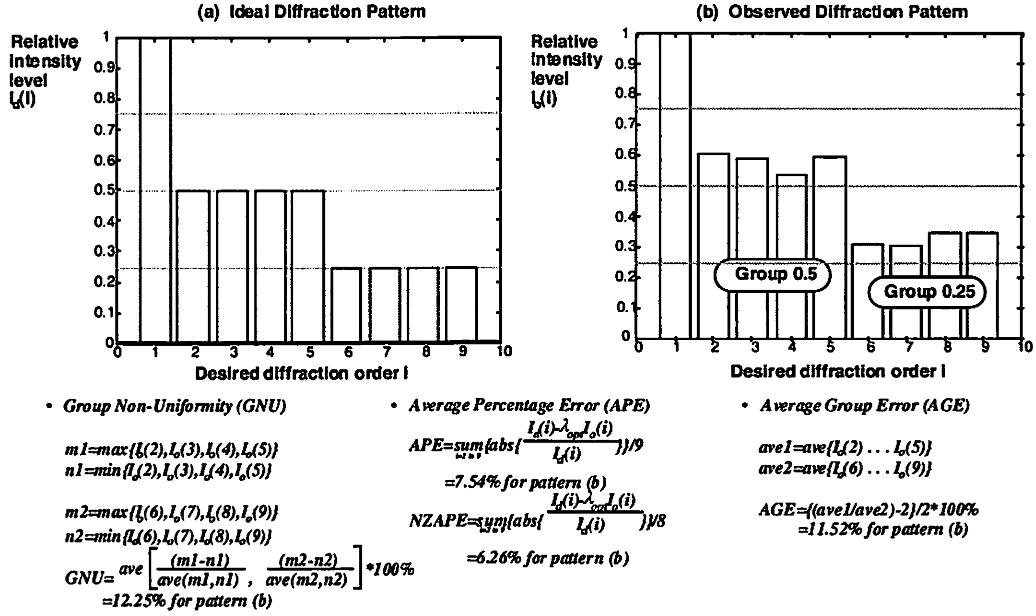


Figure 5-5: (a) Intensity spectrum of the 4:2:1 analog weighted DOEs. (b) Intensity spectrum of the observed diffraction pattern in Figure 5-4. The values of the parameters *GNU*, *APE*, *AGE* are evaluated for the spectrum in (b).

5.2.2 Group Non-uniformity (GNU)

The *Group Non-Uniformity* (*GNU*) reveals the average quality of uniformity within the groups. The "group" refers to those signal orders with the same intensity level in design. The definition of *GNU* is

$$GNU = \frac{1}{M}\sum_{k=1}^{M} U_k , \tag{5.4}$$

where M is the total number of groups, U_k is the non-uniformity of the k-th group defined as

$$U_k = \left(\frac{max_k - min_k}{ave_k}\right) \times 100\% . \tag{5.5}$$

The max_k, min_k and ave_k in Eq. (5.5) are the maximum, minimum, and average intensity values of the signal diffraction orders in group k. Note that there must be at least two or more diffraction orders to form a group in order to make non-uniformity meaningful. To derive the *GNU* for the pattern in Figure 5-5(b), we assign group 0.5 to be the first group and group 0.25 to be the second group, then calculate U_1=10.02%, U_2=14.48% and *GNU*=12.25%.

5.2.3 Average Group Error (AGE)

The Average Group Error (AGE) gives the variation of the average energy ratio between groups. The definition of AGE is

$$AGE = \frac{1}{L}\sum_{j=1}^{L} E_j , \tag{5.6}$$

where L is the total number of pairs of groups, that is

$$L = \begin{pmatrix} M \\ 2 \end{pmatrix} = \frac{M!}{2!(M-2)!}, \tag{5.7}$$

M is the number of groups. The E_j in Eq. (5.6) is the error of the energy ratio for the j-th pair of groups, including group a and group b, which is defined as

$$E_j = \left| \frac{(ave_a / ave_b) - R_j}{R_j} \right| \times 100\% . \tag{5.8}$$

The ave_a, ave_b are as defined in Eq. (5.5) and R_j is the ideal intensity ratio between group a and group b in the j-th pair of groups.

For the pattern in Figure 5-5(b), there is only one pair of groups, which are group 0.5 and group 0.25. According to Eq. (5.6), (5.7) and (5.8), we derive the $AGE=E_1=11.58\%$ by knowing $R_1=0.5/0.25=2$, $ave_{0.5}=0.58$, and $ave_{0.25}=0.328$.

5.2.4 Signal to Noise Ratio (SNR)

The *Signal to Noise Ratio* (*SNR*), which is also defined in Eq. (3.24), measures the quality of noise immunity in the reconstructed pattern of DOE. This parameter is evaluated in dB scale. The *SNR* is defined by

$$SNR = 10 \times \log_{10}\{\frac{\min(I_{signal})}{\max(I_{noise})}\}, \tag{5.9}$$

where $\min(I_{signal})$ is defined as the minimum intensity value of signal diffraction orders and $\max(I_{noise})$ as the maximum intensity value of noise diffraction orders. For the observed pattern in Figure 5-4, in which the noise diffraction orders are not shown, the calculated *SNR* is 7.07dB.

5.2.5 Efficiency

As mentioned in section 3.4, we define two parameters

1) Efficiency in observation window (η_w)=$(\sum I_{signal})/(\sum I_{noise} + \sum I_{signal})$

2) Efficiency of diffraction grating (η_g)=$\sum I_{signal}$

used to evaluate the diffraction efficiency. The first definition represents the optical power efficiency in the observation window. The second definition reveals the

diffraction efficiency of the grating. For the pattern in Figure 5-4, the calculated efficiency in observation window η_w is 85.2%.

5.3 Testing Results

5.3.1 Tested DOEs

In the optical neural network system, the DOE is used to provide analog weighted interconnections. For this purpose, we designed and tested three different patterns of DOE with the same nine weighed fanouts but in different locations. Figure 5-6 shows the experimental reconstructions of these three variations.

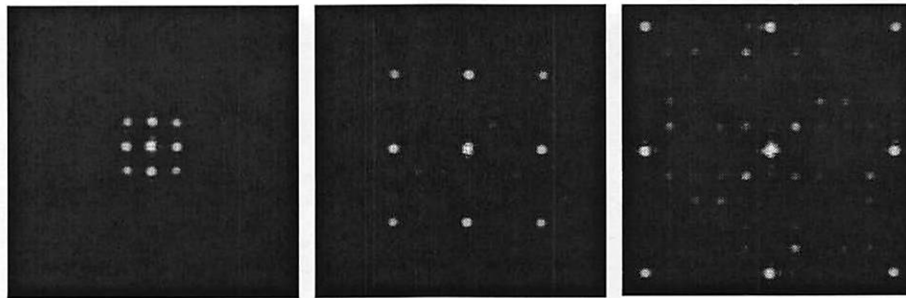


Figure 5-6: 4:2:1 analog weighted fanout DOEs with different interconnection locations. (a) Q1 diffraction pattern (b) Q3 diffraction pattern (c) Q5 diffraction pattern.

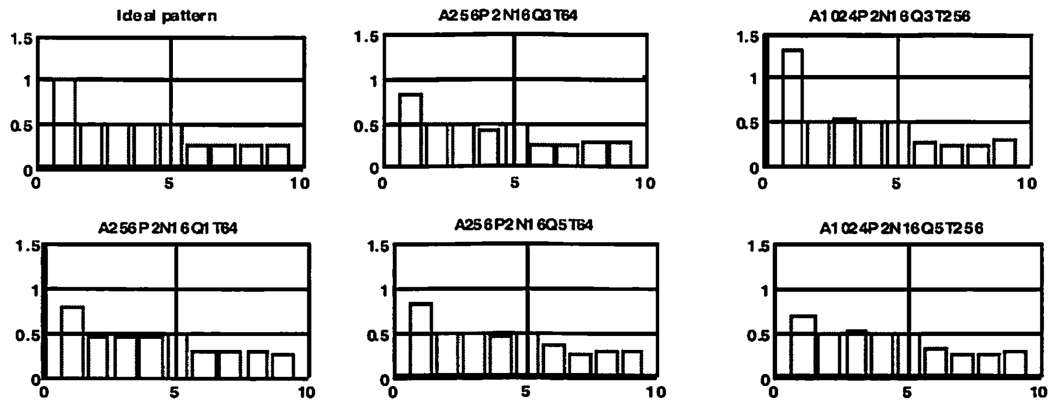
Applying the spot ordering in Figure 5-4, we see that in Figure 5-6, spot 1 is always the zero diffraction order and spots 2 to 9 locate at the first diffraction order for the Q1 pattern (Figure 5-6(a)), the third diffraction order for the Q3 pattern (Figure 5-6(b)) and the fifth diffraction order for the Q5 pattern (Figure 5-6(c)), along both x and y directions. The reason for generating the Q1, Q2 and Q3 diffraction patterns is for

cross talk analysis [51], which is beyond the discussion here. As described in the beginning of section 5.2 and as shown in Figure 5-3, each diffraction pattern theoretically has the highest intensity level in spot 1, which is twice the intensity of spots 2 through 5 (group 0.5) and four times that of spots 6 through 9 (group 0.25). All of the fabricated DOEs discussed in this chapter have 16×16 binary phase level elements in one period and are designed with a simulated annealing algorithm [52]. The masks of DOE are manufactured by two different vendors in various feature sizes and are subsequently used in the ion-beam etching process using USC's facilities to fabricate the DOEs with different size apertures.

5.3.2 DOE Measurement Comparison

Figure 5-7 shows the measurement results of five selected DOEs made by the mask from one of the two vendors. The name of the DOEs in Figure 5-7 indicates the aperture size (letter 'A'), the designed pattern (letter 'Q'), the number of phase elements in one period (letter 'N') and the period size (letter 'T'). All the size values are in units of microns along both the x and y directions. The feature size is derived from dividing the period size by the number of the phase elements. For example, the first DOE in Figure 5-7 is 'A1024Q3N16T256', which indicates that its aperture size is 1024μm, its design pattern is Q3, the number of phase elements is 16 and the period size is 256μm. Hence, we find its feature size to be 256/16=16μm. Applying the parameters described in section 5.2, we obtain a quantitative evaluation of the fabricated DOE. Typically, for all the DOEs we fabricated, the *APE* is from 7.5% to 19.2%, the *NZAPE* is from 5.3% to 15.7%, the *GNU*

is from 3.2% to 24.2%, the *AGE* is from 4.6% to 28.8%, the *SNR* is from 1.7dB to 12.1dB and the *Efficiency* is from 53% to 94%.



	APE	NZAPE	GNU	AGE	SNR	Efficiency
A1024P2N16Q3T256	10.37%	10.06%	11.37%	4.62%	6.41dB	70.53%
A1024P2N16Q5T256	10.01%	8.87%	13.62%	13.03%	1.72dB	56.38%
A256P2N16Q1T64	11.59%	10.45%	13.68%	17.77%	10.89dB	94.11%
A256P2N16Q3T64	7.54%	6.22%	12.25%	11.52%	7.07dB	85.19%
A256P2N16Q5T64	10.10%	8.81%	15.01%	15.84%	2.18dB	60.47%

A: aperture size
P: phase level
N: number of features
Q: DOE parameter
T: period size

Figure 5-7: Measurement comparison of various fabricated 4:2:1 analog weighted fanout DOEs.

5.3.3 Diffractive Microlens Array Testing

The tested microlens arrays, as listed in Table 5-1, are designed and fabricated using two different methods. The top three designs use the hybrid phase level method, which is described in Chapter 4, and fabricated with a mask etching lithography procedure. The other four designs use a gray scale phase profile, which is written by laser writer onto the polymer surface upon the glass substrate. The lithography etching method provides sharp edge features and more accurate phase values, but is constrained to the maximum number of quantization phase levels allowed. For the designs in Table 5-1, the maximum number

of phase levels allowed is eight because of the mask alignment tolerance. In general, this method is more repeatable and generates the designs with better uniformity. The gray scale method provides more degrees of freedom for the diffractive optics design in terms of the number of phase levels used. It also generates designs with higher optical power efficiency. However, the Gaussian profile of the writing laser beam in the laser pattern generator for this process decreases the accuracy in the phase features and also produces smoothing of the sharp transitions between the phase elements. These lenslet arrays are used in the SPARCL, SAPIENT, TRANSPAR and TRANSPAR-VM (VCSEL-MSM) smart pixel systems, which are described in Chapter 6.

Lenslet array	Focal length	F/#	Lenslet period	Phase level	Non-uniformity	Efficiency	Application
2×2	1554	1.74	625×625	8/4/2	6.53%	84.86%	Testing
10×20	986	7.06	125×62.5	8/4	19.15%	86.69%	SPARCL
10×20	312	3.53	125×62.5	8/4	36.82%	80.34%	SPARCL
8×8	2015	5.7	250×250	256	18.48%	97.69%	VCSEL
10×20	2795	20	125×62.5	256	28.78%	97.92%	TRANSPAR
8×8	1500	6	176×176	256	31.84%	99.74%	VCSEL-MSM
3×3	2043	5	1140×450	256	5.43%	96.83%	SAPIENT

Dimension unit: μm

Table 5-1: Design and testing comparison for fabricated diffractive microlens arrays.

5.4 Characterization

There are two key factors that cause measured reconstruction errors. The first is the measurement error in our system, including mechanical alignment, random vibration,

aberrations, quantization error in the digitizer, and the reduced fill factor of CCD imaging elements [53]. The second is fabrication controlled effects such as etch depth variation, feature shrinkage effects in the masking and etching steps, and multiple surface reflections. The DOE pattern discussed in section 5.2 is used to illustrate those fabrication effects.

5.4.1 Mechanical Measurement Error

Mechanical measurement error resulting from hardware imperfection usually limits the measurement precision. Another source of mechanical error is the inevitable random vibration of the measuring environment. The mechanical alignment error can be kept small but is also hard to eliminate. Lens aberration effects can be reduced through the use of optical system design software, such as OSLO®, which allows us to choose the appropriate achromatic doublet or triplet lenses for the system. The effect of these three measurement errors are relatively small compared to errors in intensity level measurement due to quantization error in the digitizer and the fill factor effect of the CCD imaging array. For the eight-bit digitizer used in our system, the intensity level of one pixel is quantized on a scale from 0 to 255. The quantization error for a quantized value is within half of the quantization accuracy, which ranges from -0.5 to +0.5. Thus, for the calculated average intensity I_{ave} of one spot (diffraction order), the maximum quantization error percentage is

$$E_{Q,\max} = \pm 0.5 / I_{ave} \times 100\% . \tag{5.10}$$

The reduced fill factor effect is illustrated in Figure 5-8, which shows that only a partial area of an imaging pixel is active in the detection of light (gray zone in Figure 5-8). The remaining part of the pixel is used as storage and for shifting the detected signal.

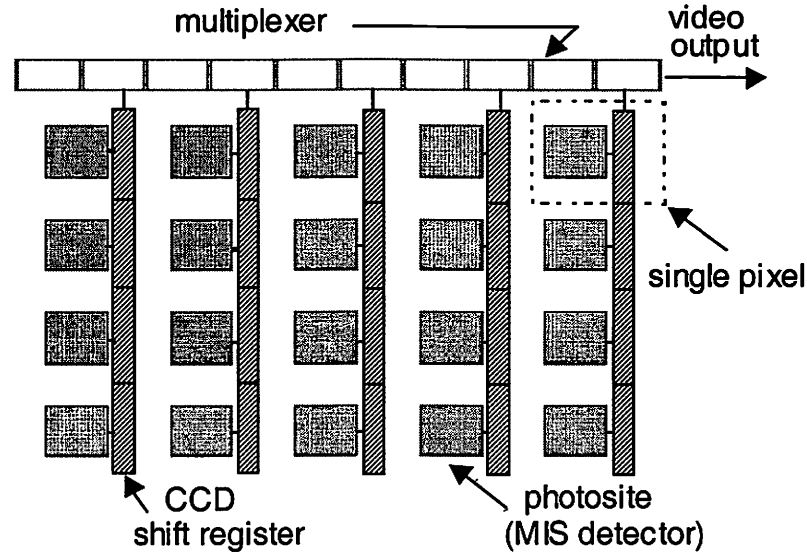


Figure 5-8: Charge Coupled Devices (CCD) array configuration.

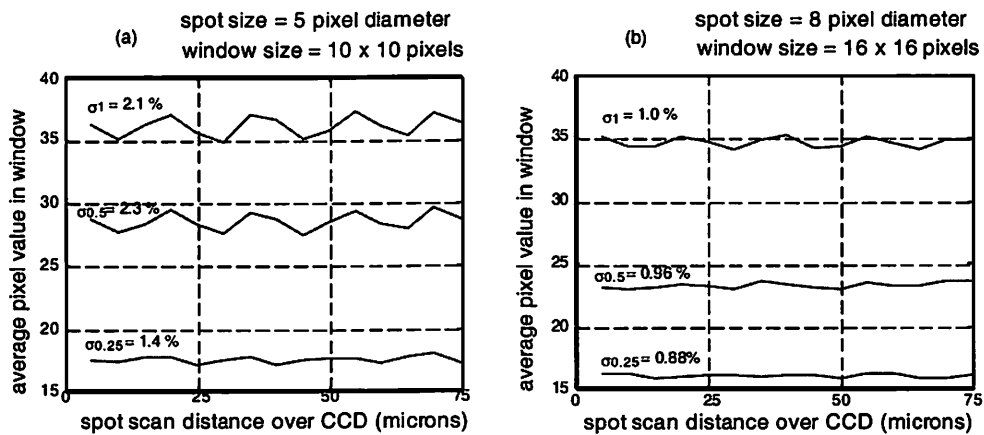


Figure 5-9: Intensity variation of the laser beam spot with (a) spot size = 5×5 pixels, measurement window size = 10×10 pixels and (b) spot size = 8×8 pixels, measurement window size = 16×16 pixels, scanned over 75μm distance along x direction on the CCD camera.

Figure 5-9 plots the variation of the intensity of one laser beam spot as we move the CCD camera along x (or y) direction for 5μm at a time. We see that the fluctuation is periodic, with period around 15μm, which is approximately the size of single CCD image pixel (17.3μm×13.4μm). Figure 5-9(a) is the result for a spot with a diameter of 5 pixels (~75μm), and Figure 5-9(b) shows the result for a spot with an 8 pixel diameter (~120μm). The σ_1, $\sigma_{0.5}$ and $\sigma_{0.25}$ in Figure 5-9 are the standard deviations of the measured intensity moving along one direction for the zero diffraction order spot, group 0.5 spots and group 0.25 spots of the observed DOE reconstruction respectively. There are three observations from Figure 5-9:

(1) We easily see that the smaller spot, which covers less CCD pixels, has more severe variation (larger standard deviation σ) due to the more serious reduced fill factor effect of CCD imaging pixel.

(2) The reduced fill factor error is proportional to the illumination power, because the greater the intensity of the light on the CCD pixel, the more power lost on the inactive detection area.

(3) When the intensity value of a spot is low, the quantization error E_Q becomes the dominant error other than the reduced fill factor effect. This is why the $\sigma_{0.25}$ in Figure 5-9(b) is not clearly periodic.

Therefore, the combined mechanical measurement error E_M is represented as

$$E_M = \max\{E_Q, \sigma\}, \tag{5.11}$$

where E_Q is the quantization error, which is less than the $E_{Q,\,max}$ in Eq. (5.10), and σ is the empirical standard deviation of the beam spot's intensity value resulting from the reduced fill factor effect of CCD imaging element.

5.4.2 Internal Reflection

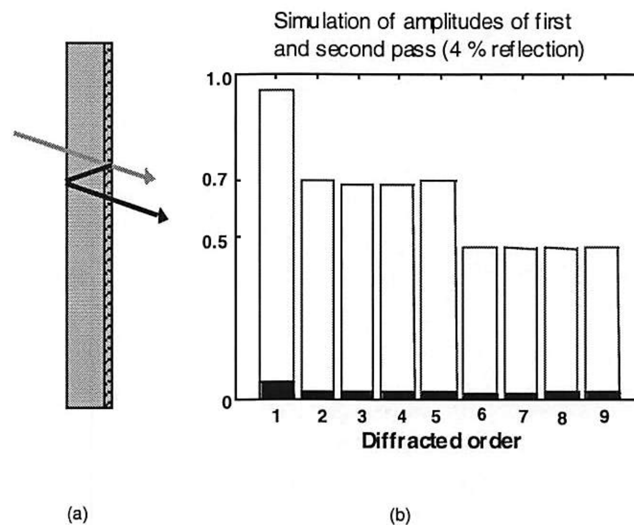


Figure 5-10: (a) Internal reflection illustration between the DOE surfaces. (b) Absolute amplitude comparison of the diffraction spectrum for the first pass reconstruction and the second pass reconstruction.

Figure 5-10(a) illustrates the internal reflection problem in DOE reconstruction. The gray arrow indicates the beam which goes through the DOE surface on the first pass and the black arrow indicates the primary internal reflected beam which goes through the DOE surface on the second pass. Figure 5-10(b) shows the relative proportion of amplitude for the first pass beam and the second pass beam. From Figure 5-10, we know that the internal reflection beam has some coherent phase destruction effect on the uniformity of the DOE reconstruction pattern. In order to reduce the internal reflection

effect, we coated the DOE with an anti-reflection (AR) layer and measured the diffraction pattern before and after AR coating.

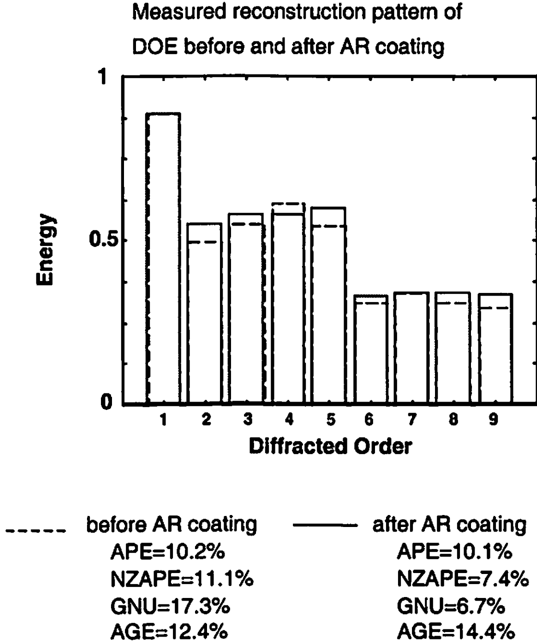


Figure 5-11: Measurement comparison for the DOE before AR coating (dashed line) and the DOE after AR coating (solid line).

Figure 5-11 shows the measured result before and after AR coating for the DOE with 256μm aperture, 4μm feature size, 64μm period, and Q1 pattern. We see that the *GNU* has been reduced over 10% and the *NZAPE* is also reduced. However, the *APE* incorporated with zero order is not improved since the zero order intensity offset mainly results from the etch depth variation and feature shrinkage error.

5.4.3 Feature Shrinkage Effect

In the physical DOE fabrication process, the shape of the fabricated elements is not perfectly rectangular and the sidewalls may have a finite slope. The exact shape depends on the fabrication method used [32][54]. Figure 5-12 shows the possible phase relief profile of a fabricated DOE. We see that the slope of the side walls of the etched valley in Figure 5-12(b) is not perfectly sharp, which results in the changes of the effective etched (π phase) area and the unetched (0 phase) area compared to the designed profile in Figure 5-12(a).

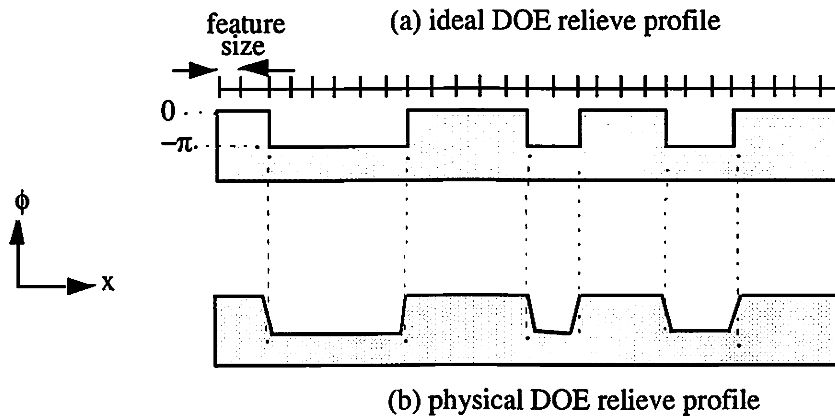


Figure 5-12: DOE phase relief profile. (a) Ideal relief profile. (b) Physical relief profile with etching error.

In addition, the mask fabrication is also not perfect, leading to round corners, non-ideal connections and shrunk/extended feature area as shown in Figure 5-13.

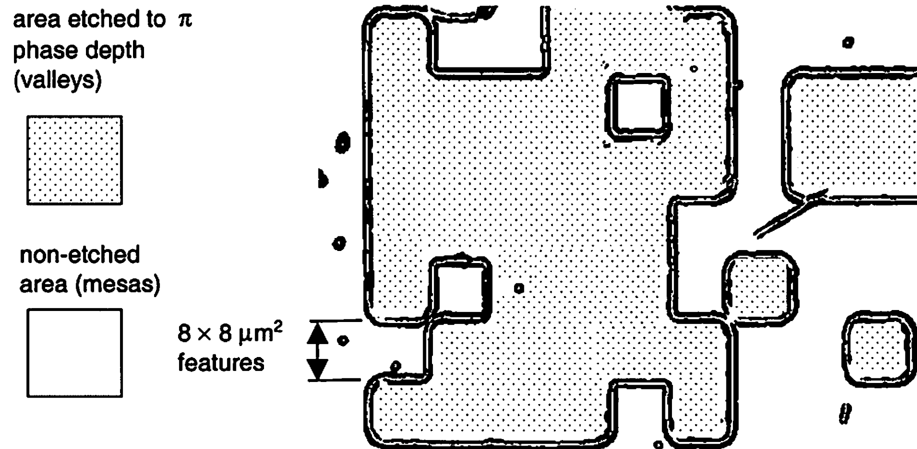


Figure 5-13: Feature shrinkage effect from the imperfection of ion-beam etching mask.

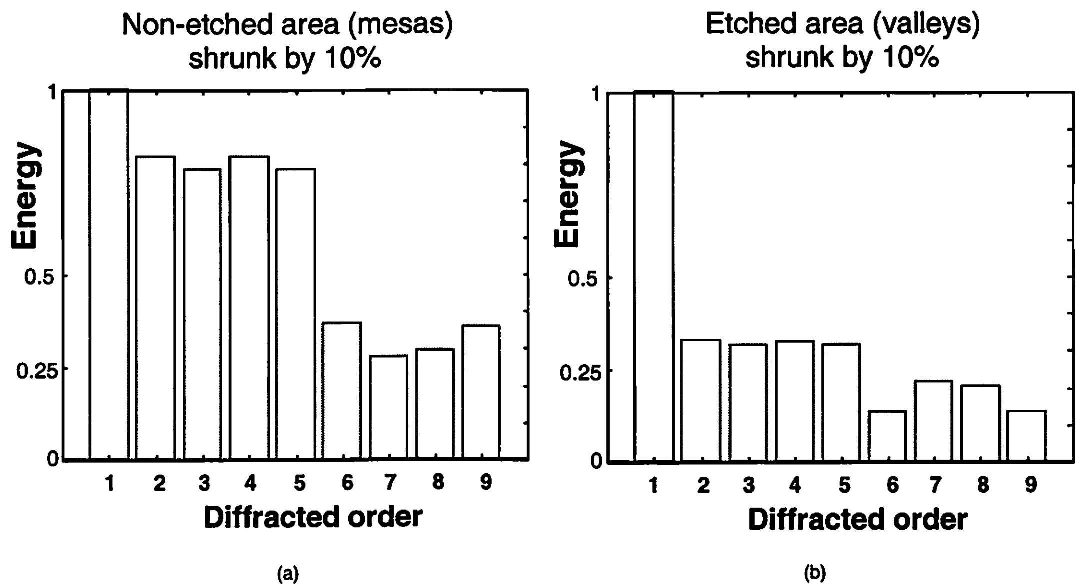


Figure 5-14: Simulation of the diffraction spectrum for DOEs whose features have shrunken. (a) The non-etched area (mesas) of the DOE is shrunk by 10%. (b) The etched area (valleys) of the DOE is shrunk by 10%.

Figure 5-14 shows the reconstruction simulations of 10% feature shrinkage effect, which is similar to some observed patterns in Figure 5-7. In those reconstruction patterns, the worst intensity level degradation occurs in the zero order.

5.4.4 Etch Depth Variation

Any errors in the etch depth in DOE fabrication causes a variation of phase delay in reconstruction. The relationship between phase delay and etch depth in a binary phase DOE is

$$\phi = \frac{2\pi d(n-1)}{\lambda}, \tag{5.12}$$

where ϕ is the optical phase delay, d is the etch depth, λ is the operation wavelength and n is the index of refraction of the DOE material. The worst etch depth precision Δd for the ion beam etching machine used to fabricate our DOEs is around 0.02μm. This means that at the wavelength of operation λ=633nm and n=1.5 (fused silica), the worst phase variation percentage $\Delta\phi/\phi$ is 3.1% for the binary phase DOE with designed d=λ=633nm. From simulations, we have observed that the 3% variation in etch depth does not cause much significant degradation on the DOE reconstruction. However, when the etch depth error is larger than 5%, changes in the zero order reconstruction power are significant. Figure 5-15 shows the reconstruction spectrum of a DOE having 10% etch depth error in which the group uniformity remains almost unchanged, but the variation of zero order intensity is severe. The zero order intensity levels in Figure 5-15(a) and (b) are both normalized to unity for comparison. The 10% etch depth error assumed in Figure 5-15(b)

is for the case of extremely low precision fabrication environment. In general, the etch depth error is kept below 5% for the ion-beam etching process.

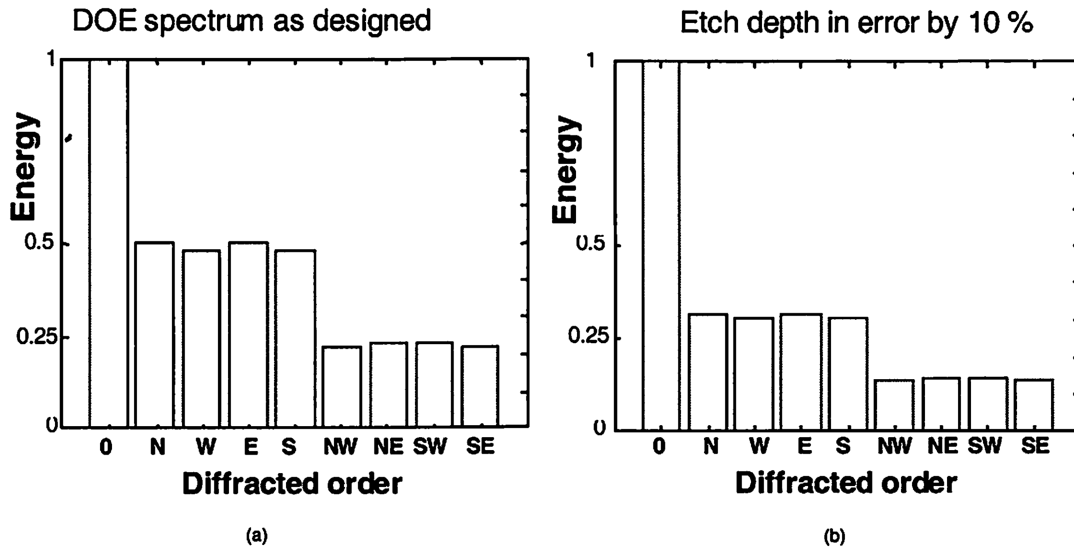


Figure 5-15: Simulation on etch depth variation. (a) Designed DOE spectrum. (b) DOE spectrum with 10% etch depth variation (worst case).

Figure 5-15 suggests a way to correct the incorrect zero order diffraction power due to feature shrinkage effects. Since changing the etch depth influences mostly the intensity level of the zero order and doesn't destroy the uniformity of other diffraction orders, we could use the re-calculated etch depth to fabricate the DOEs instead of the theoretical etch depth value derived from Eq. (5.12). After the error measurement on the zero order power of a fabricated DOE, we are able to calculate the corrected etch depth to compensate for the feature shrinkage effects on the next fabrication batch of the same DOE design.

Chapter 6 Smart Pixel Systems Using Free Space Digital Optics

6.1 General Layout for High Throughput Smart Pixel System

To take the advantage of high space-bandwidth product of optics, the free-space digital optical (FSDO) technologies have become an attractive platform for high throughput interconnection systems. Along with fast growing progress in optoelectronic (OE) device development and mature VLSI lithography technology, the OE-VLSI smart pixel system provides a feasible and powerful solution to the data demanding information processing world. Basically, the smart pixel module consists of a two-dimensional array of electronic logic elements, drive and receive electronics, optical sources, optical detectors and integrated micro-optics for imaging.

Figure 6-1 shows a typical layout for the smart pixel system. Each smart pixel node interfaces the optical parallel data packet (OPDP) and electronic communication to the hosts. The schematic representation in Figure 6-1 shows smart pixels with receivers on one side and transmitters on the other side, even though nearly all smart pixel systems have receivers and transmitters on the same side. By integrating highly parallel optical devices with high speed electronic circuits, the smart pixel system has an aggregate capacity of up to 100's Gb/s or even Tb/s data throughput [3]. For example, by scaling up the TRANSPAR-MQW (described in section 6.4) chip to 2×2 cm^2, the size of smart pixel array is scaled up to 40×80 pixels and the aggregate data throughput is 0.96 Tb/s at 300MHz channel rate.

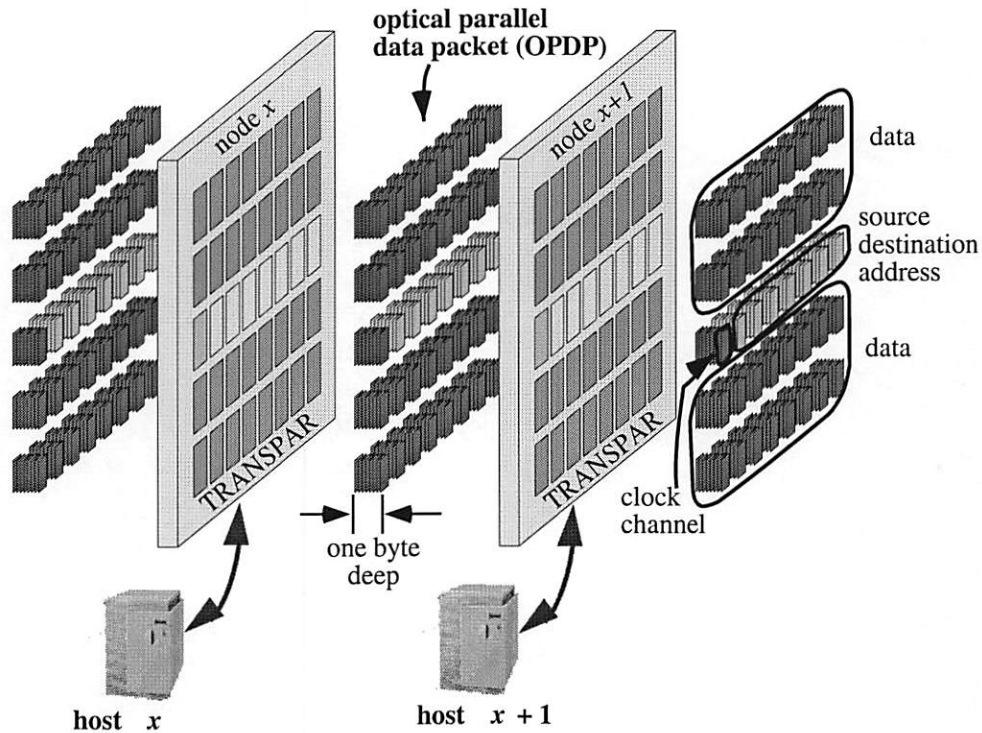


Figure 6-1: High throughput optoelectronic smart pixel system layout.

As described in section 2.3, there are two main integration principles for OE-VLSI systems, monolithic integration and hybrid integration. There are two types of optical light source: (1) passive devices, such as modulators; and (2) active devices, like the LEDs and VCSELs. In the past few years, we have designed and developed several smart pixel systems for networking and information processing applications using various integration technologies and optoelectronic devices. We describe the design details of these smart pixel systems in the following sections.

6.2 Smart Pixel Array Cellular Logic Processor: SPARCL

In order to provide high bandwidth for data transfer and data processing, we designed a Smart Pixel Array Cellular Logic Processor (SPARCL) through the DARPA sponsored CO-OP program at George Mason University. The SPARCL chip was first fabricated through MOSIS foundry service on the 0.8μm CMOS then the AlGaAs/GaAs MQW p-i-n structures were bonded onto it by Bell-Lab./Lucent Technologies. The SPARCL system is a single instruction multiple data-stream (SIMD) machine, which provides the image or parallel-data processing with cellular logic. With multiple chips SPARCL system, we are able to perform the 2D parallel data pipelining processing using free-space digital optical interconnects that attempts to overcome the electronic I/O bottleneck. The multistage SPARCL system is shown in Figure 6-2.

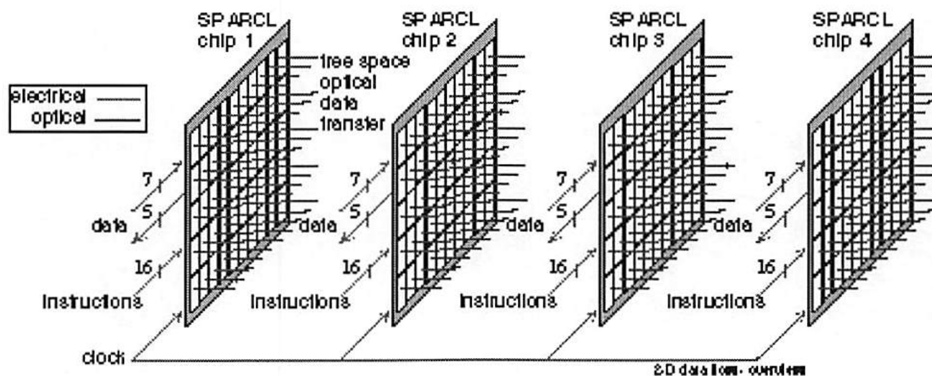


Figure 6-2: Free space 2D optical data transfer in a multiple chip SPARCL system.

6.2.1 SPARCL Chip Design

In each SPARCL chip, there are 5×10 mesh-connected smart pixels. Each pixel consists of one modulator pair (two MQW diodes), one detector pair (two MQW diodes), three bit memory, and three logic functions (complement, union and dilation) circuitry. With

these logic functions, each SPARCL pixel is a 1-bit processor for binary image processing and each SPARCL chip is a processing node for binary image algebra. The detailed design and algorithm implementations are described in the reference [55].

6.2.2 Optical System Setup and Simulation

In order to generate an external source array for the MQW modulators in the SPARCL chip, we designed the 5×20 spot array generator (SAG) DOEs using the 2-stage IFT design algorithm described in Chapter 3 and had them fabricated through the Honeywell foundry service. For the five copies of the 5×20 spot array generator DOE we received from the Honeywell foundry, we tested the non-uniformity (Eq. 3-21), the signal-to-noise ratio (SNR in Eq. 3-24) and the efficiency in the observation window η_w (Eq. 3-22). We also tested the same DOEs after they were anti-reflection (AR) coated and compared the results in Table 6-1. From Table 6-1, we see that the AR coated DOE's have, in average, 8% higher efficiency, 2 dB higher *SNR*, and 4% better uniformity. However, in the dual rail MQW smart pixel applications, the more important parameter for the spot array generator is the pairwise non-uniformity U_p, which measures the non-uniformity of each dual rail pair. Among the five fabricated DOE copies, the best pairwise non-uniformity U_p is 0.0%, the worst U_p is 18.7%, and the average U_p is 5.5%.

5×20 SAG	AR or N/A	Non-uniformity	SNR	Efficiency η_w
DOE1	AR	36.44%	11.61 dB	97.59%
	N/A	41.79%	8.12 dB	90.10%
DOE2	AR	23.13%	12.04 dB	95.64%
	N/A	25.32%	10.17 dB	85.78%
DOE3	AR	30.47%	11.23 dB	95.05%

DOE3	N/A	33.12%	9.18 dB	88.12%
DOE4	AR	26.77%	9.74 dB	94.55%
	N/A	31.49%	9.07 dB	86.85%
DOE5	AR	24.73%	12.00 dB	95.02%
	N/A	28.50%	8.64 dB	86.44%

Table 6-1: Comparison of 5×20 spot array generator DOEs for SPARCL.

Figure 6-3 shows the reconstructed 5×20 spot array illuminating the SPARCL chip and acting as a source array for the MQW modulator diodes. Each pair of spots forms a dual-rail modulated signal. Upon the stored 1-bit electrical data in the memory of a smart pixel, the bias voltages across the two MQW diodes in a dual-rail pair are different, which results in the different absorption rate for these two diodes. In this way, we can define the logic '1' and '0' according to the contrast ratio of the reflected dual-rail beam.

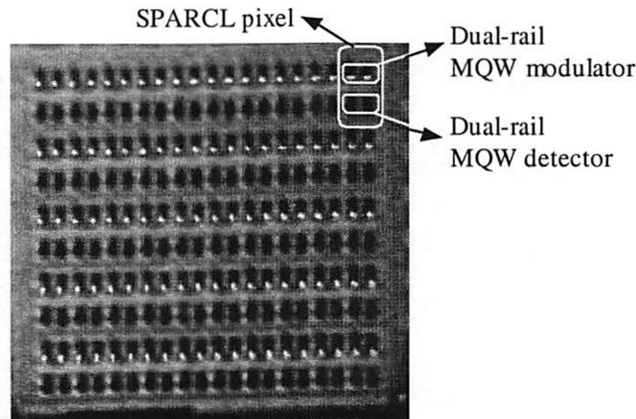


Figure 6-3: 5×20 spot array illuminating the MQW diodes on the SPARCL chip.

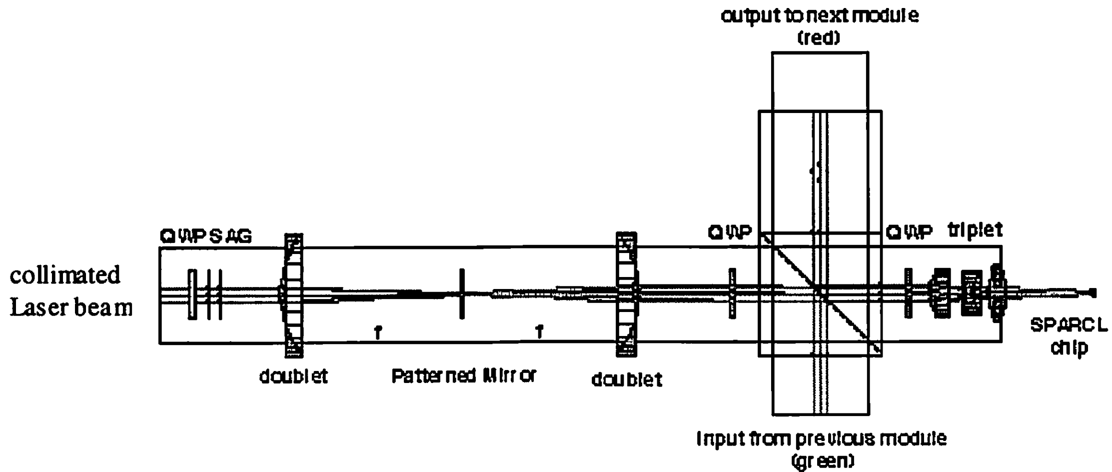


Figure 6-4: Ray tracing simulation showing the optical interconnection module between two SPARCL chips in the multi-chip SPARCL system.

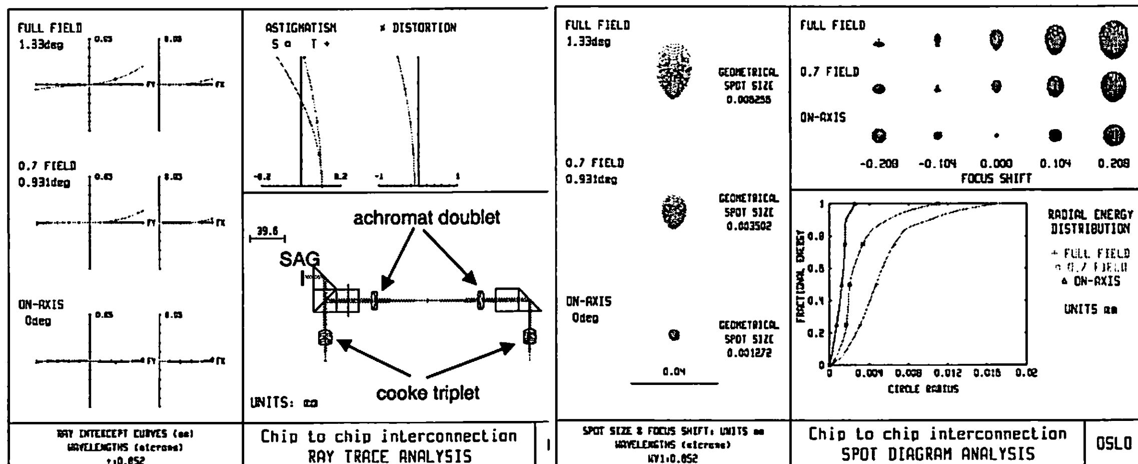


Figure 6-5: Ray tracing simulation showing the aberration effect and spot size variation on various filed of view in the chip to chip interconnection SPARCL system.

The optical setup for the chip-to-chip interconnection in the SPARCL system is shown in Figure 6-4. The collimated external laser beam illuminates the Spot Array Generator (SAG) to generate a 5×20 spot array onto the MQW modulator array of SPARCL chip. The reflected 2-D spot array (readout beam) propagates through the Quarter Wave Plates (QWP) and Polarization Beam Splitters (PBS) onto the MQW

detector array of the next stage SPARCL chip. Figure 6-5 shows the optical quality simulation generated by OSLO®, which illustrates the astigmatism, distortion and coma aberration for the optical system. The worst case spot size is 6μm, which occurs on the corner of the spot array.

6.2.3 SPARCL Application Systems

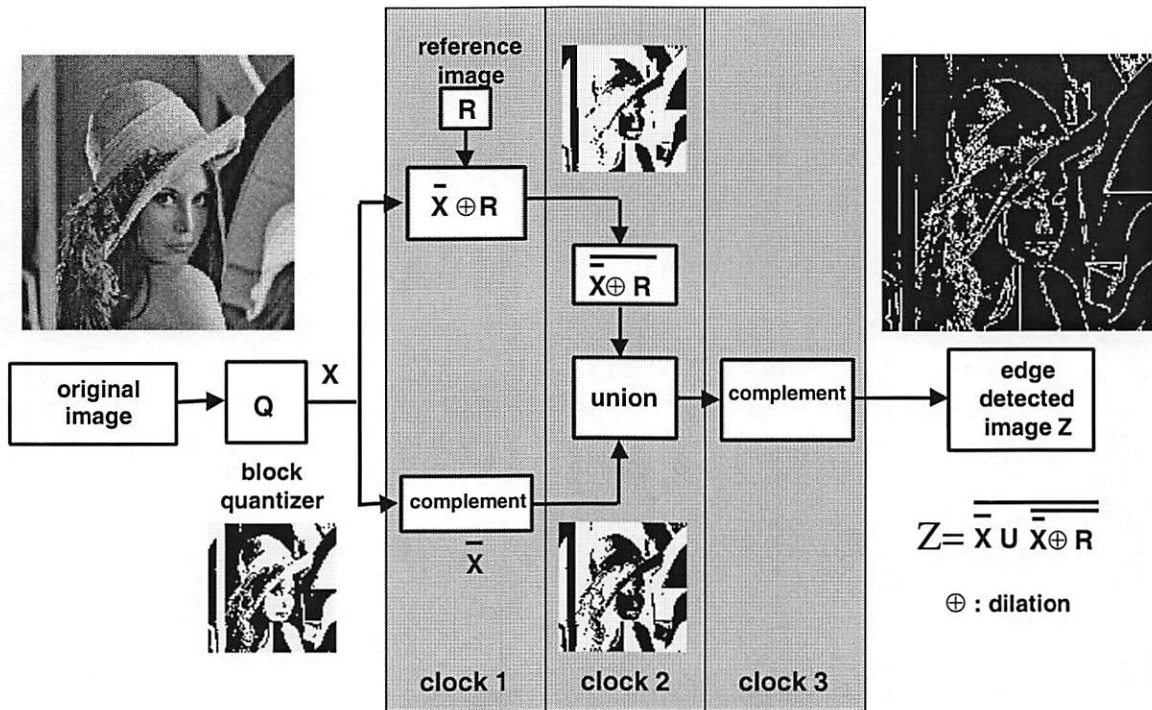


Figure 6-6: Edge detection processing of the SPARCL chip.

We have experimentally tested the functionality of the SPARCL chip in the laboratory, including the image edge detection, noise removal, and binary image algebra operations. Figure 6-6 shows the image edge detection operation of the SPARCL chip in three clock cycles. More testing results are shown in the paper [55] submitted to Applied Optics.

6.3 Smart Pixel Array Network Interface: SAPIENT

In contrast to the flip-chip bonding smart pixel integration technology used for the SPARCL chip in section 6.2, the SAPIENT (smart pixel for network interface) chip [56] monolithically integrates LEDs and optical-field-effect transistor (OPFET) detectors with GaAs circuitry. The SAPIENT chip is fabricated through the NCIPT's OPTOCHIP program at MIT. The GaAs electronic circuitry and the detectors are fabricated through MOSIS standard Vitesse 0.6μm process. The LED's were integrated into the GaAs circuitry by MIT [57] using a low temperature growth process, which is called the Epitaxy-on-Electronic (EoE) technology.

6.3.1 SAPIENT Chip Design

The SAPIENT chip contains a 3×3 array of smart pixels along with control and address detection circuitry. This 9-bit packet consists of 2 bits of address header and 7 bits payload. Figure 6-7 shows the SAPIENT layout and a photograph of the fabricated chip. The chip size is 2×1 mm^2. Figure 6-8 shows the layout and photograph of single pixel in the SAPIENT chip. Figure 6-9 shows the complete logic function of single smart pixel. Each pixel contains one LED, one OPFET detector, one 1-to-2 multiplexer, three 2-to-1 demultiplexers, and two 1-bit memories. One memory, the optical buffer, is dedicated to transferring data onto the optical network. The other memory, the electrical buffer, is dedicated to transferring data into and out of the node processor. There are three control signals generated from the address detection and control modules within the SAPIENT

chip: (1) *add packet* moves the data packet from the electrical buffer onto the optical network, (2) *drop packet* moves data from the optical network into the electrical buffer, and (3) *address match* signifies that the address contained in the optical data packet matches the processor node address and moves detected data into the electrical buffer if the buffer is free. The address detection and control modules also signal the node processor when a data packet has been transmitted onto the optical network and when a packet with matching address has arrived with two acknowledge signals: *ack_send* and *ack_drop*. Figure 6-10 shows the schematic design and part of the input/output truth table for the address detection and control modules. The *send_packet* and *load/unload* signals of the control modules are externally controlled by the node processor.

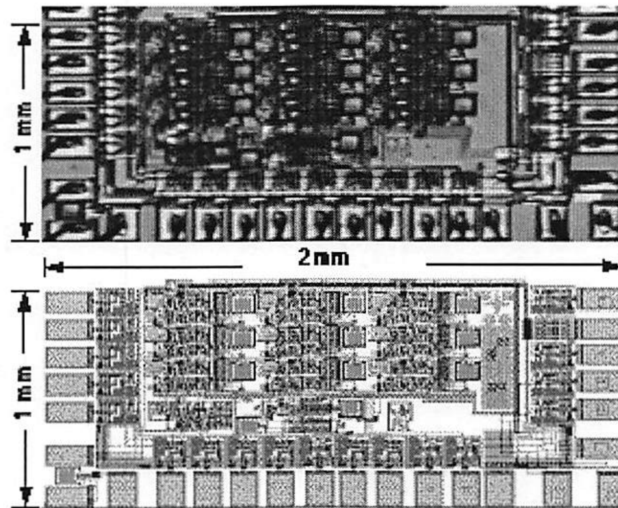


Figure 6-7: SAPIENT chip photo and layout.

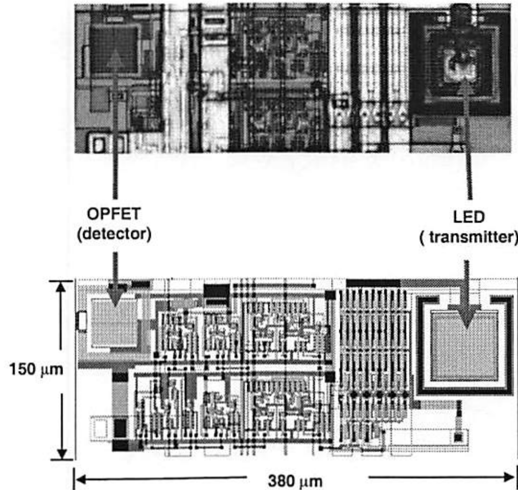


Figure 6-8: The photo and layout of a single smart pixel on the SAPIENT chip.

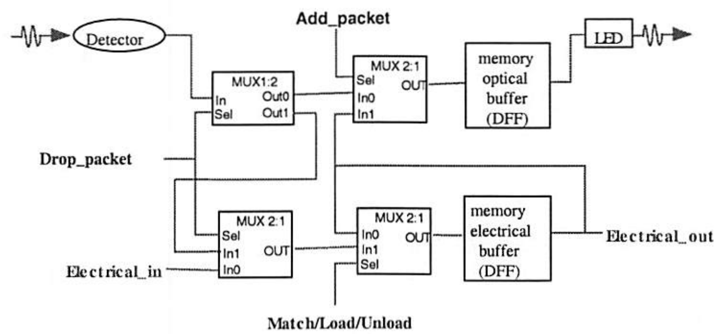
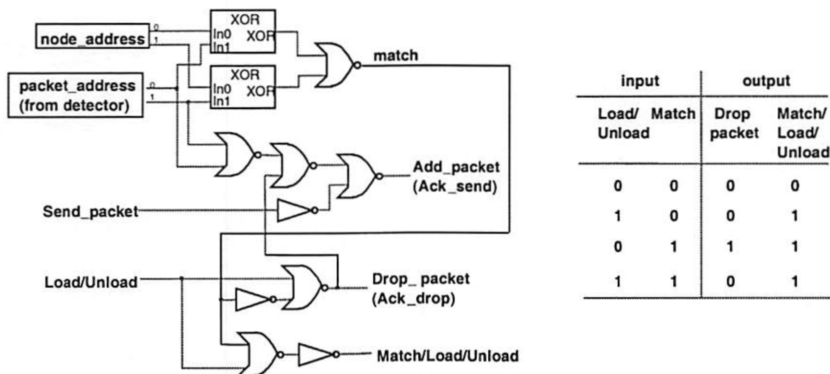


Figure 6-9: Gate level logic diagram for a single smart pixel on the SAPIENT chip.



input		output	
Load/ Unload	Match	Drop packet	Match/ Load/ Unload
0	0	0	0
1	0	0	1
0	1	1	1
1	1	0	1

Figure 6-10: Gate level logic diagram and truth table for the SAPIENT control unit.

Figure 6-11 shows the design flow chart for the SAPIENT chip. At the top of the design flow, system application and functionality are first defined and then transferred into a Register Transfer Level (RTL) design. The B^2Logic tool is used to generate the

schematic design and simulate the logic functions. The physical layout, including floorplanning, placement, routing, design rule checking (DRC) and circuit extraction, is done in the MAGIC tool. The standard cells used in the layout are generated by VHDL codes and synthesized by the EPOCH tool. Finally, the extracted layout netlist is simulated using IRSIM at the logic level and HSPICE at the transistor level to verify the correctness of the design.

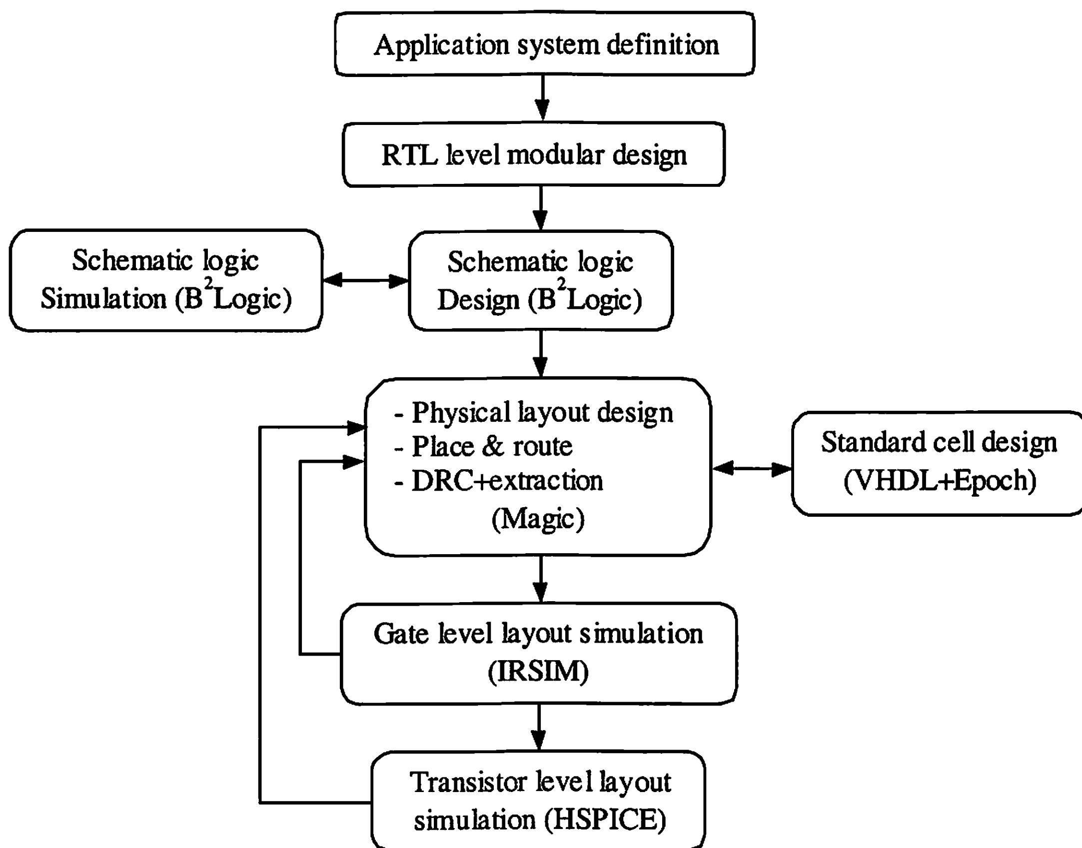


Figure 6-11: Design flowchart for the SAPIENT chip.

6.3.2 SAPIENT Network Architecture

Figure 6-12 is a schematic of three nodes of the SAPIENT ring-connected parallel data packet network. The 2-D parallel data packets transfer from node to node through free-

space propagation. Similar to the Fiber Distributed Digital Interface (FDDI) architecture, this system provides a shared ring-connected link for all nodes in the network. In the SAPIENT network, 2-D parallel packets are synchronously transported from one chip to the next chip in one clock cycle. The network routing control is contained in the interface chip, which is capable of recognizing address bits embedded in the optical data packet. The main advantage of the SAPIENT network system is the shared 2-D parallel data link and a packet is sent and received in fully parallel manner, which provides a much higher network throughput. Using Free Space Digital Optics (FSDO), the multi-node SAPIENT network system can be integrated as a compact switching network module for the LAN applications.

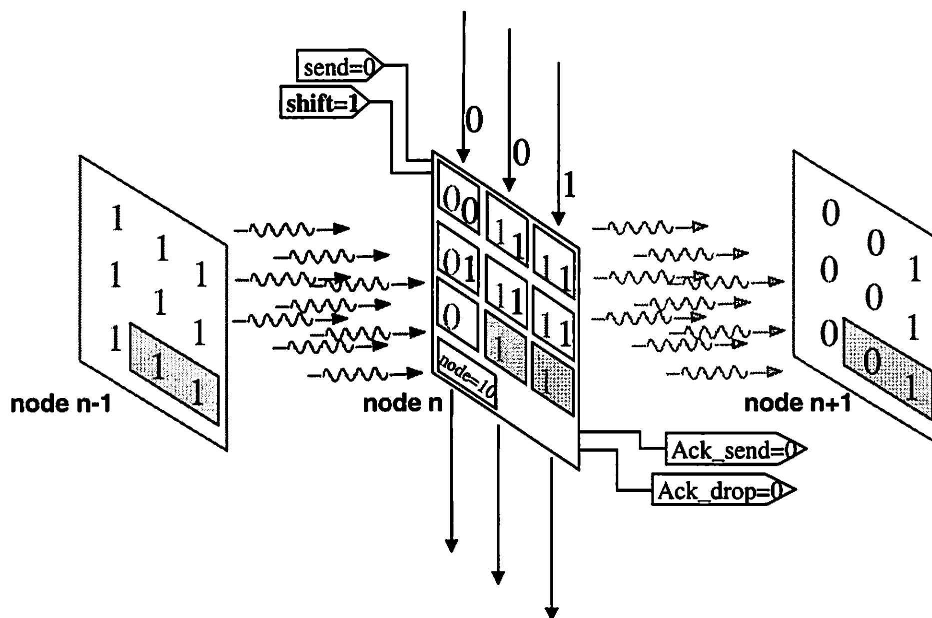


Figure 6-12: Smart Pixel Array Network Interface (SAPIENT) for 2D parallel data packet network system.

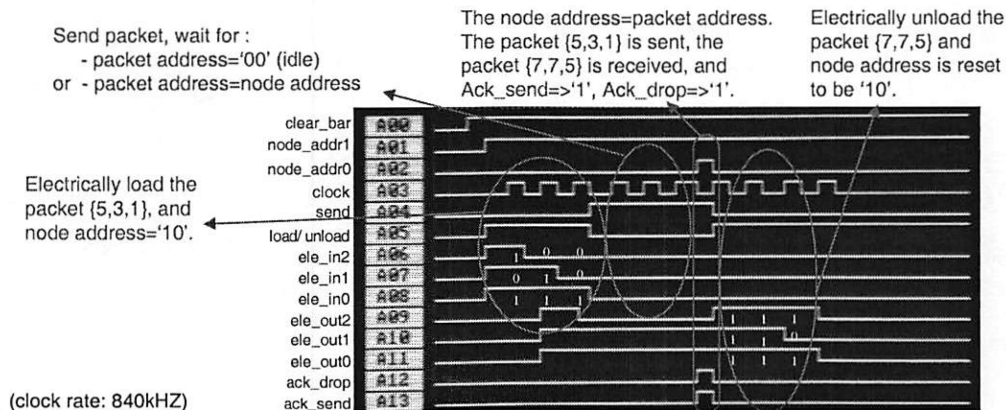
As shown in Figure 6-12, each SAPIENT chip is capable of column-parallel loading of electrical data from the node processor into the chip and column-parallel

unloading of optical packets to be dropped from the chip to the node processor. Each SAPIENT pixel contains a one-bit electrical buffer and a one-bit optical buffer, which provide the intermediate buffering between the incoming optical packet and the electrical loaded packet. A time slot with no data (i.e. an idle packet on the network) is indicated by an optical packet address of "00". When a node has electrical data to transmit, it loads the packet in column-parallel fashion from the top edge of the chip, then stores the packet in the optical buffer and waits for an idle time slot to transmit through the LED array. An optical packet is dropped into the interface chip from the network when the address bits of the optical packet match the node address specified in the chip. This dropped packet is first stored in the electrical buffer, then electrically unloaded to the node processor. When the chip has a loaded electrical packet waiting to send and an incoming optical packet contains the address bits matched to the node address, the SAPIENT chip is able to swap a waiting-to-send electrical packet with an incoming optical packet in the same clock cycle. In this way, it avoids the eternal waiting deadlock situation on the network. The address detection circuitry is built on chip to check the address bits of the optical packet in real time.

6.3.3 SAPIENT Testing Results and System Demonstration

We have been successfully tested the SAPIENT chip electrically and optically. To illustrate the full operation of the SAPIENT chip, Figure 6-13(a) shows experimental results from testing the packet swapping operation as observed on the signal analyzer and Figure 6-13(b) shows the packet flow in a three node SAPIENT system. We concentrate on node *n* in the middle, whose address is fixed at "11". The packet swapping operation

consists of four steps: (1) the electrical *packet loading* stage, (2) the *waiting to send* stage, (3) the *swapping* of optical packet and electrical packet stage, and (4) the dropped *packet unloading* stage. In the first stage, an electrical data packet {7,3,1} is loaded into the chip in three clock cycles and the destination node address is set to "10". During the second stage, the electrical packet is waiting for an idle time slot in network, in which the address bits of the detected optical packet are "00", or waiting for an optical packet contains an address matched to the node address "11". In the third stage, we change the node address from "10" to "11" and, in the same time, an optical packet {7,7,5} whose address equals "11" is detected. Hence, the electrical packet {7,3,1} stored in the optical buffer is transmitted onto the optical network and the optical packet {7,7,5} is dropped into the electrical buffer in the same clock cycle. This packet swapping operation is performed as an data exchange between the optical buffer and electrical buffer. In the fourth stage, the dropped packet {7,7,5} is electrically unloaded to the node processor.



(a)

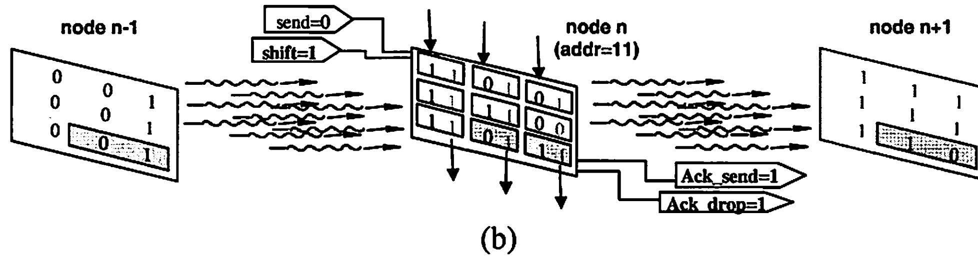
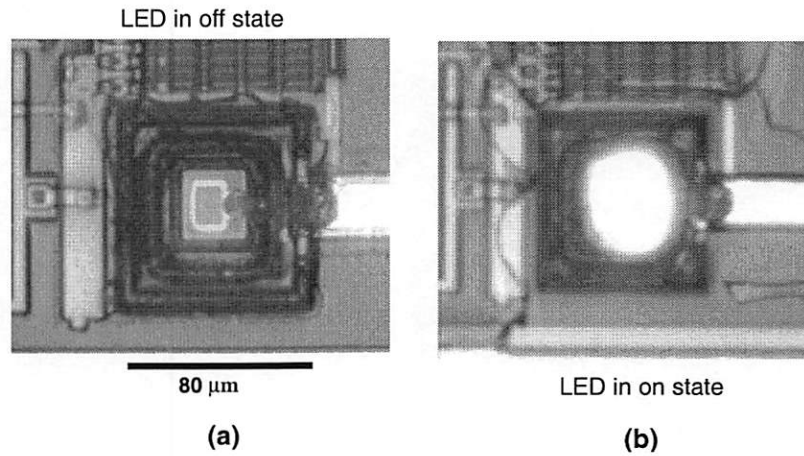


Figure 6-13: (a) Experimental demonstration for the packet swapping operation of SAPIENT chip. (b) Packet flow illustration for the third stage of packet swapping operation described in (a).

Figure 6-14(a) and (b) show the LED of SAPIENT pixel in OFF state and ON state respectively. Figure 6-14(c) plots the optical power emitted from LEDs in the SAPIENT chips versus the LEDs' driving current. The peak emission spectrum is at 873 nm and the average radiated power is 0.2 μW/mA for the LEDs. From Figure 6-14(c), we see the threshold current of LEDs is 2.5 mA. The low power efficiency of LED is due to the difficulty of growing high performance optical sources under low temperature fabrication environment. Figure 6-15(a) shows the optical turn-on power versus switching frequency for the OPFET detector and Figure 6-15(b) shows the detected signal at 200 KHz with 10 μW illumination power. The DC turn-on power is 0.18 μW and the detector sensitivity is 25 A/W at 40×40 μm^2 detector window size. The switching bandwidth of OPFET detector has been limited to 200 KHz. Because of the concern of power loss from one chip to the next chip in the network, we choose the more sensitive OPFET detector in stead of the higher speed Metal-Semiconductor-Metal (MSM) detector. It results in sacrificing the switching bandwidth of the system. On the other hand, the electrical operation of the SAPIENT chip has been tested over 200 MHz and the electrical power consumption is measured 600 mW at 200 MHz.



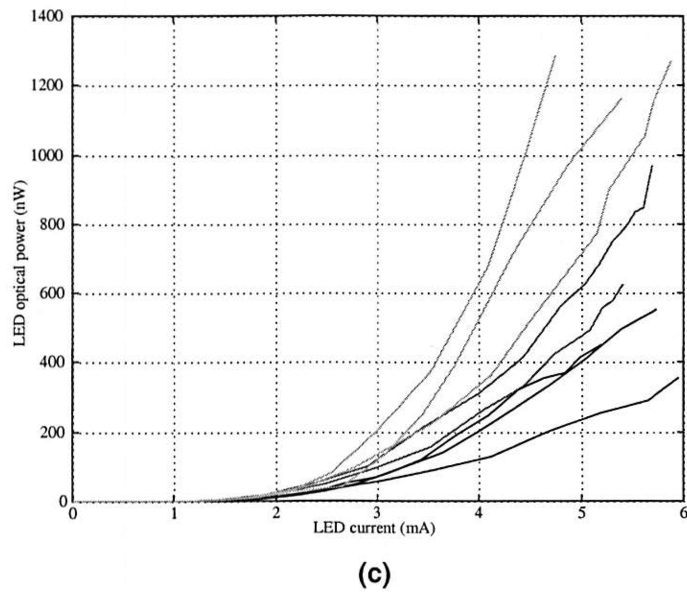


Figure 6-14: (a) LED in OFF state. (b) LED in ON state. (c) Optical power vs. driving current for LEDs.

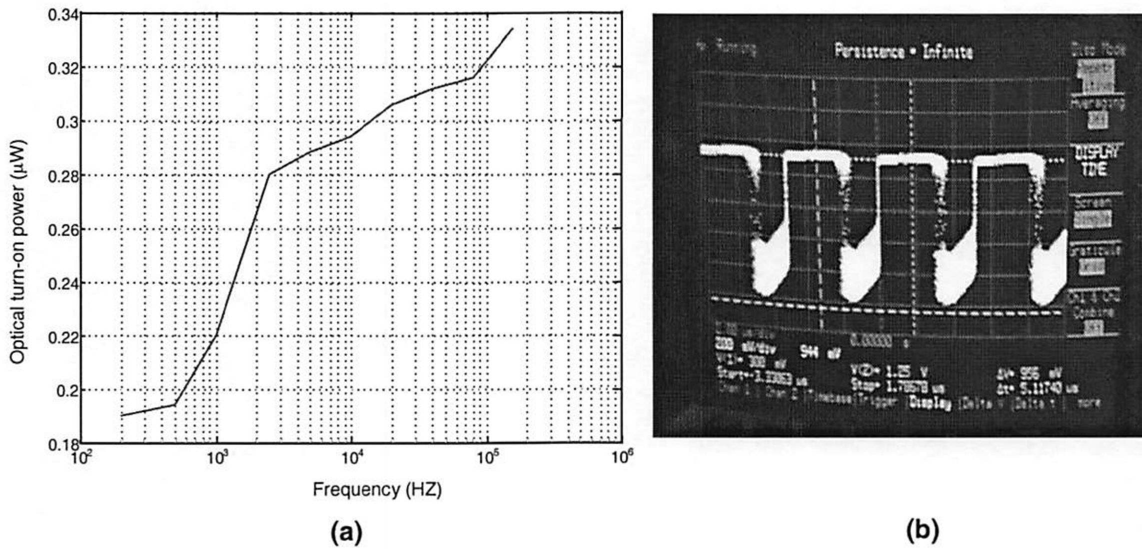


Figure 6-15: (a) Optical turn-on power vs. switching frequency for OPFET detector. (b) Detected signal from OPFET switching at 200KHz.

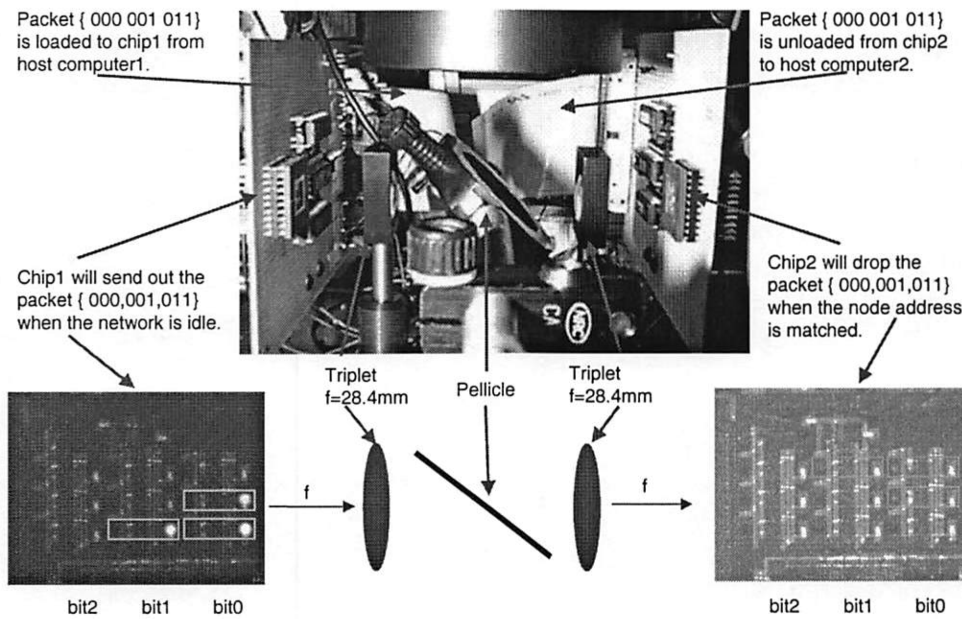


Figure 6-16: System demonstration for chip-to-chip interconnection using two SAPIENT nodes.

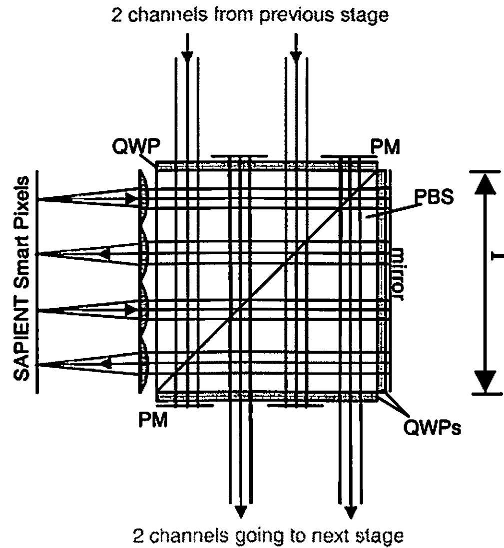


Figure 6-17: Optical module for the PE array in SAPIENT chip.

Figure 6-16 demonstrates the optical system setup for a two-chip test communication network. The optical data packet {0,1,3} is transmitted from chip 1, propagated through an imaging system, and then successfully detected by chip 2. In this system, the emitting power of LED is 2 μW, the OPFET sensitivity at 100 KHz is 0.3 μW and the power loss of the imaging system is over 20 dB because of the wide beam divergent angle of LEDs. In order to successfully perform the packet transmission between the chips using this image system, we have to raise the background illumination power to keep the detector barely below the threshold. Then the imaging spots of the LED array from the first chip will have enough power to turn on the detector array on the second chip. To improve the power efficiency of the image system, we design a compact optical module, which combines the microlens array, polarization beam splitter (PBS), pattern mirrors (PM), reflective mirror and quarter wave plates (QWP). Each SAPIENT chip is integrated with an optical module to provide the duplex parallel optical links to

the network. The optical module is designed to reduce the alignment error of each node in the optical network and increase the optical transmission power efficiency by using high numerical aperture diffractive microlens array. This design is also applicable to other non-polarized active sources, like VCSEL array, in the network system. By using VCSEL array as the emitting sources, we can further reduce the power loss of the network system. Figure 6-17 shows the schematic design of the optical module. The designed and fabricated 3×3 diffractive microlens array with focal length f=2.043mm and F/#=5 is shown in Figure 6-18. Figure 6-19 shows the network system consists of four SAPIENT chips integrated with optical modules.

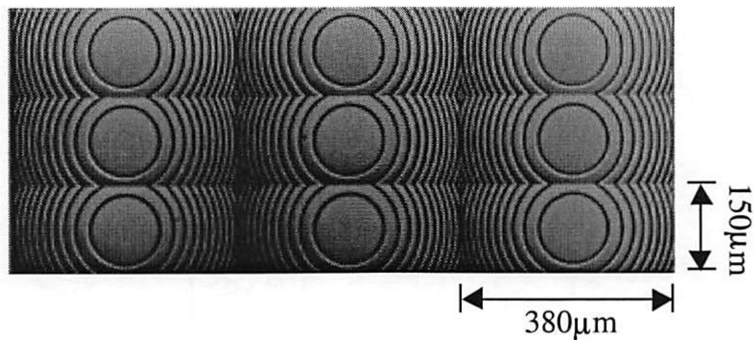


Figure 6-18: 3×3 diffractive microlens array for the SAPIENT chip.

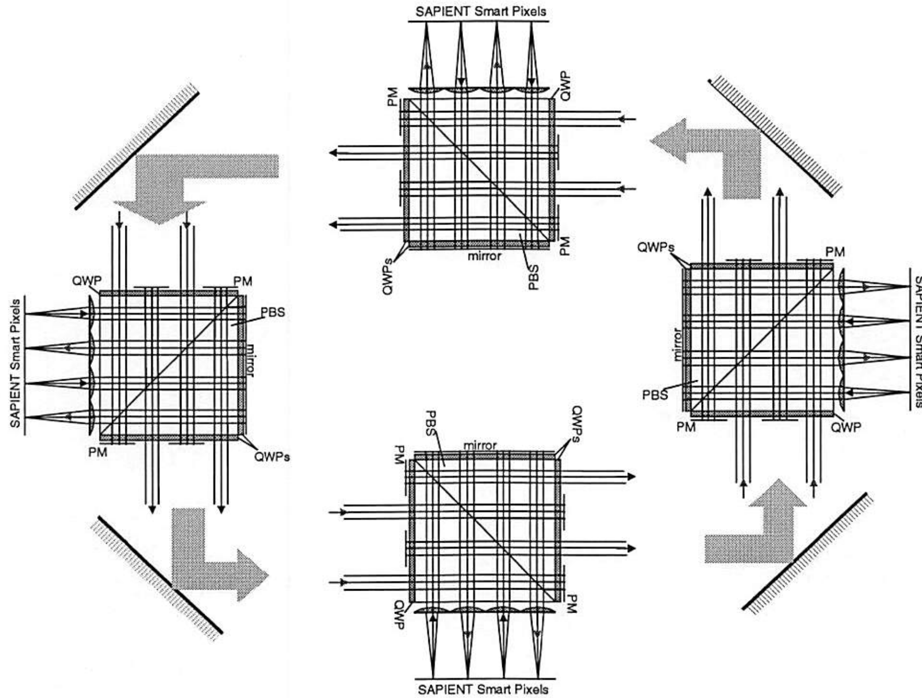


Figure 6-19: Scalable multi-node SAPIENT network system (four node system is shown).

In the 2-D parallel data network, all data bits are transmitted, propagated and detected in parallel. Because only two address bits are available in this version of SAPIENT chip, at most three nodes can be built in the ring-connected SAPIENT network system (address "00" is reserved for idle network). Along with advances in fabrication technology, the SAPIENT smart pixel array can be easily scaled up to 30×60 array on a 2×2 cm^2 die area and the SAPIENT system can be scaled up to (2^N-1) node system with N bit address. However, the proper scaling size of a network system should be a compromise between the issues of network throughput, clock skew, packet overhead ratio and network latency.

6.4 Translucent Smart Pixel Array Processor: TRANSPAR

TRANSlucent Smart Pixel Array (TRANSPAR) is a novel smart pixel chip with applications in very high throughput networks and in single-instruction–multiple-data (SIMD) parallel signal processing. The TRANSPAR architecture and smart pixel chip is designed to optimize two functions: (1) network interface for 3-D data packet transfer between computing nodes using a carrier-sense-multiple-access/collision-detection (CSMA/CD) protocol; and (2) high-throughput SIMD-type processing of 2-D data fields. The detailed TRANSPAR chip and system designs are described in the following section and also in reference [58]-[61].

6.4.1 TRANSPAR Chip Design

We are exploring two different fabrication technologies for TRANSPAR: self-electro-optic effect (SEED) GaAs multiple quantum well (MQW) modulators (referred to as TRANSPAR-MQW); or VCSEL-MSM technology (referred to as TRANSPAR-VM). The TRANSPAR-MQW chip is fabricated by Lucent Technologies through the DARPA/CO-OP foundry program. The TRANSPAR-MQW chip contains a 4×8 array of identical replicated smart pixel elements in a 2mm×2mm chip. Figure 6-20 shows the TRANSPAR-MQW chip layout, which also contains 3-bit destination address pixels, 3-bit source address pixels, one optical clock pixel, internal clock generator, finite state machine module and CSMA/CD control unit.

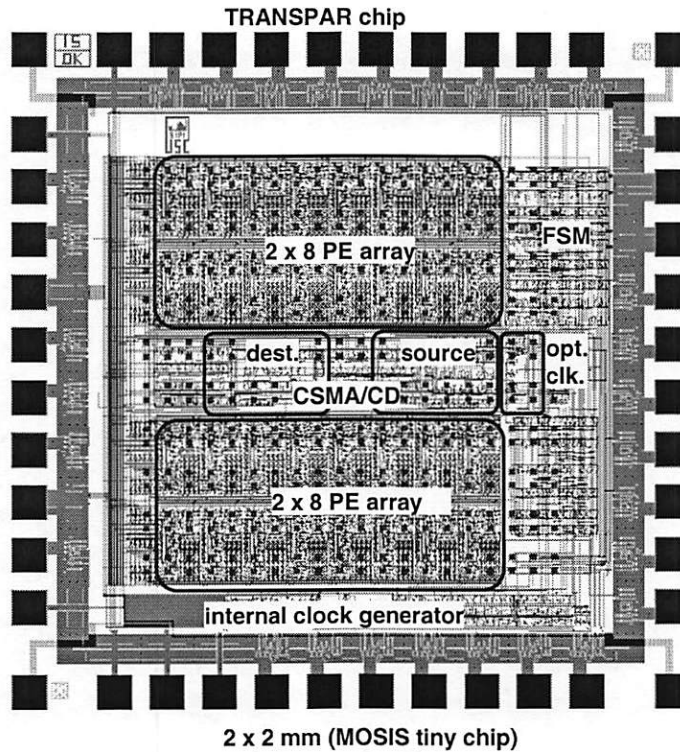


Figure 6-20: TRANSPAR-MQW chip layout.

Each smart pixel element (550 transistors/pixel) contains a 32 bit memory, 8 bit FIFO, one-bit ALU, three register, a one-bit optical transmitter and a one-bit optical receiver, and four GaAs multiple quantum well (MQW) modulators flip-chip, which are bonded to 0.5 micron CMOS. The pixel photo and layout are shown in Figure 6-21.

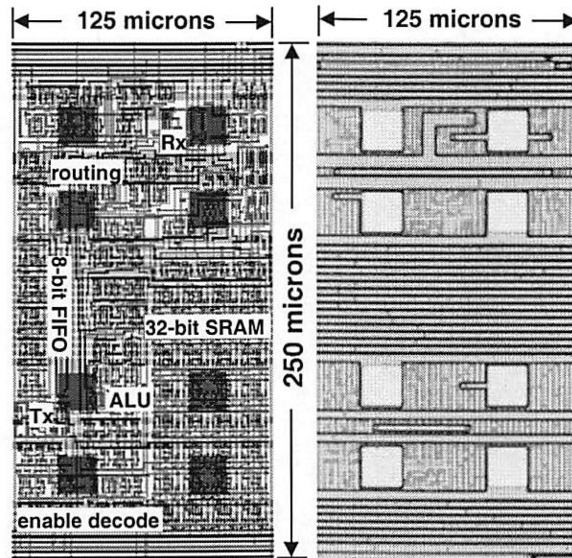


Figure 6-21: Smart pixel photo and layout for TRANSPAR-MQW chip.

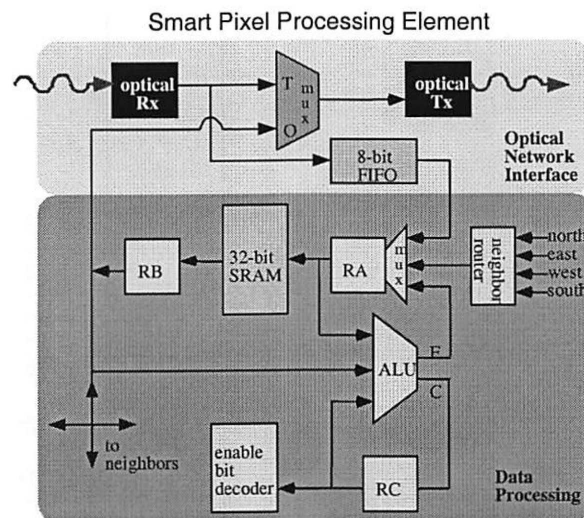


Figure 6-22: Schematic diagram of TRANSPAR-MQW smart pixel.

Figure 6-22 shows the schematic diagram of TRANSPAR-MQW smart pixel. The upper half portion of the diagram illustrates the translucent optical network interface. When the chip is in 'transparent' mode, which means it is only a listener in the network, the received optical signal is directly sent to the transmitter and transmitted optically with less than 1ns delay. When the chip is in 'opaque' mode, the chip is optically transmitting

the data stored in its memory. Any incoming optical signal is blocked out during the transmission. The lower half portion of the diagram shows the logic circuitry, which is capable of performing any logic function and one bit addition operation.

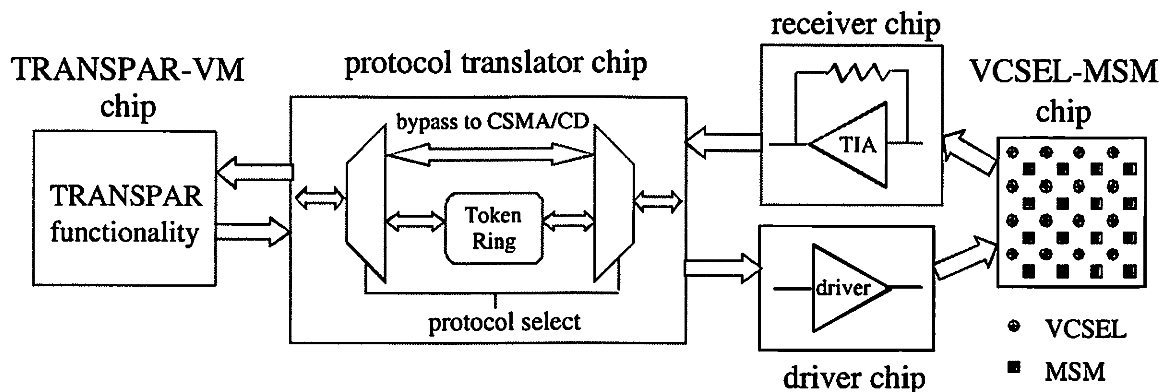


Figure 6-23: Schematic layout of TRANSPAR-VM system.

The other technology uses a separate optoelectronic input-output chip containing VCSEL source array and MSM detector array. This program is also a DARPA sponsored CO-OP foundry operated by GMU. The TRANSPAR-VM system shown in Figure 6-23 consists of a VCSEL-MSM chip, VCSEL driver chip, MSM receiver chip, protocol translation chip and TRANSPAR function chip. Honeywell will supply the VCSEL-MSM chip, which contains interlaced 4×4 VCSEL devices and 4×4 MSM detectors at 250μm×250μm grid. The CO-OP program provides the driver chip. The other three chips are designed by us and fabricated through MOSIS using 1.2μm AMI CMOS process. In addition to the CSMA/CD function of TRANSPAR chip, the protocol translation chip provides an option for implementing the token ring network protocol. The TRANSPAR-VM node can also be programmed as a bypass/exchange switching stage for a multistage interconnection network. There is one control signal for each pair of horizontal adjacent pixels to determine if the pixel is in bypass or exchange mode.

The receiver chip design is optimized for: (1) low crosstalk from the high-current VCSEL drivers (1-10 mA) to the low current MSM outputs (10-20 μA); (2) wide bandwidth operation (100 Mb/s), with no oscillations; (3) high transimpedance gain (50 kΩ); and (4) ability to operate in a PCB environment, with a large input capacitance, 1-10 pF. The HSPICE simulation of TRANSPAR-VM chip operations is shown in Figure 6-24. This simulation demonstrates the operations of loading status register, loading memory pointer, data routing, memory clearing, 'and' logic on two single bit data, packet receiving, FIFO to memory transfer, packet sending and collision detection. Only four selected I/O signals are shown in Figure 6-24.

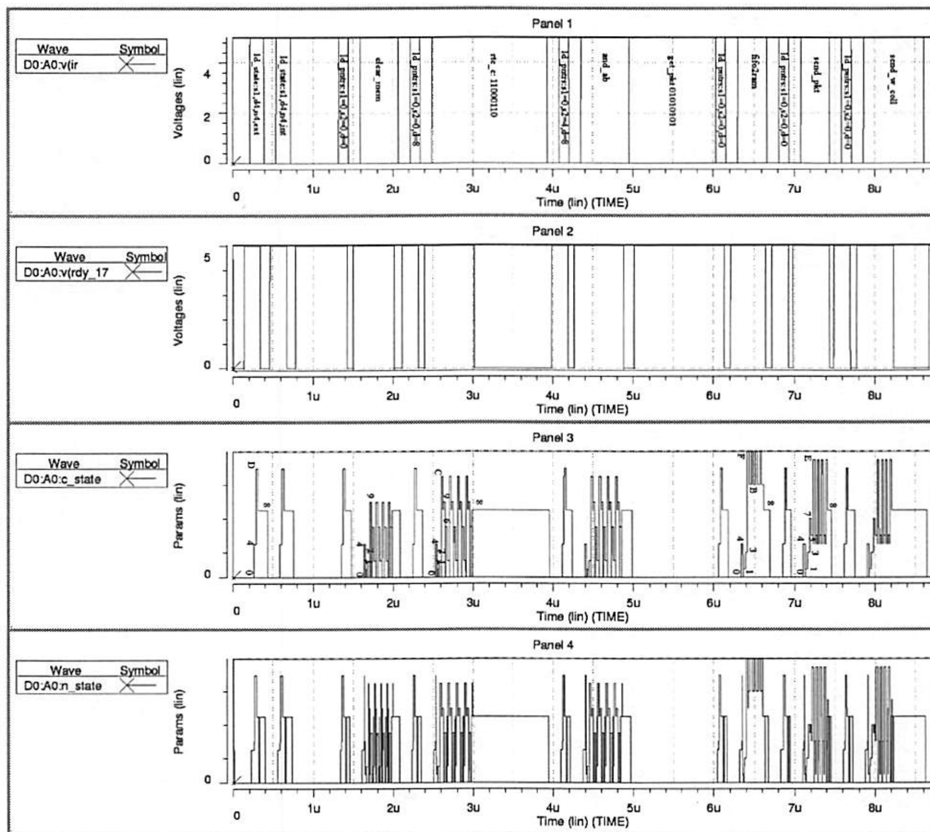


Figure 6-24: TRANSPAR-VM functional simulation.

The design flows for the TRANSPAR-MQW and TRANSPAR-VM chips are shown in Figure 6-25 and Figure 6-26 respectively. As the design flow of SAPIENT chip, the system application and functionality are first defined for the TRASNPAR-MQW chip. The VHDL behavior models for the functional modules, such as CSMA/CD network protocol, finite state machine, address recognition, pad muxing and FIFO control, are then generated and simulated at schematic logic level. The simulated modules are synthesized using EPOCH tool. Because of the physical size of the TRANSPAR-MQW pixel is defined at 250×125 μm^2 for the flip-chip bonding process, the smart pixel circuitry has to be manually designed and laid out. Both synthesized modules and manually designed smart pixels are integrated into the same design layout. The floorplanning, global routing, DRC and layout extraction for the entire chip are then performed in MAGIC tool. Finally the extracted layout netlist is simulated using IRSIM at the logic level and HSPICE at the transistor level to verify the correctness of the design.

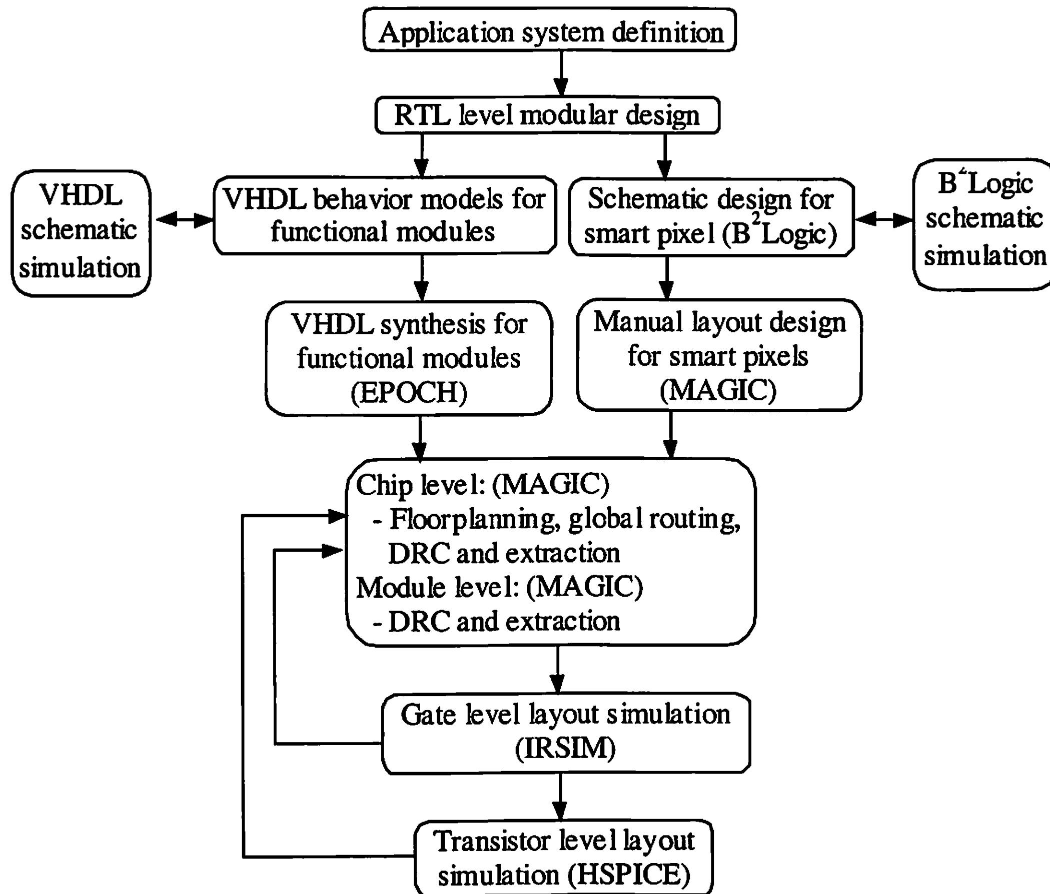


Figure 6-25: Design flow for the TRANSPAR-MQW chip.

On the other hand, the TRANSPAR-VM chip has no physical size limitation on the pixels because the optical devices for the smart pixels are on the VCSEL-MSM chip provided by Honeywell. Thus, the design flow is much simpler than the TRANSPAR-MQW chip. All the modules and smart pixels are designed using VHDL models and synthesized using EPOCH tool. The rest of the design process is basically the same as the TRASNPAR-MQW chip.

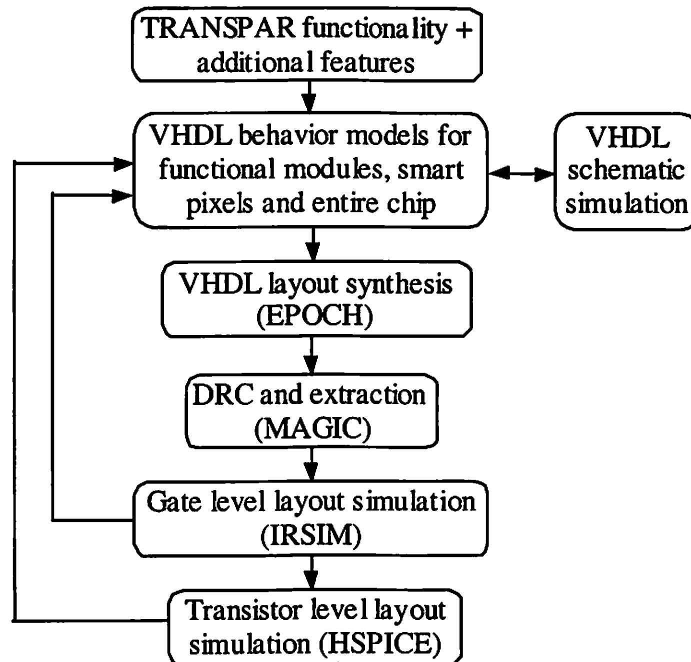


Figure 6-26: Design flow for the TRANSPAR-VM chip.

6.4.2 TRANSPAR Network System

The TRANSPAR nodes are physically arranged as a ring network shown in Figure 6-27. Host processors communicate using TRANSPAR nodes configured in a ring with uni-directional data propagation. The TRANSPAR CSMA/CD protocol is derived from the Ethernet standard and is extended to operate over ring networks that pass spatially parallel packets. Once transmitted from a source TRANSPAR node, an Optical Parallel Data Packet (OPDP) travels through the entire ring, *optically* propagating in free space between nodes and *electrically* propagating on the VLSI plane within nodes. Each OPDP is a 3-D structure packet, which contains 4×8×8 bits payload, 3-bit source address, 3-bit destination address and one optical clock channel. All TRANSPAR nodes detect the OPDP and compare its destination address with their own address, downloading on a

match. The latency per node consists of the time required for optical detection, electrical propagation through a few gates, optical transmission, and free space optical propagation time between nodes. The TRANSPAR latency is less than 1ns per node and 6ns for the entire network.

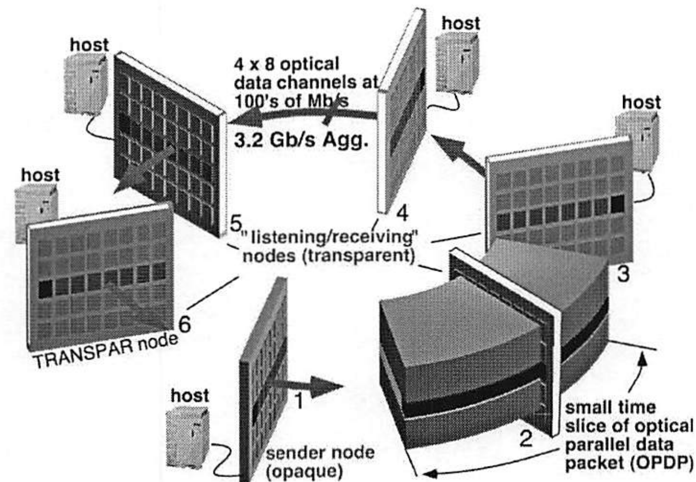


Figure 6-27: Ring connected TRANSPAR network system.

The CSMA/CD protocol control module consists of several functions, including carrier sensing, collision detection, source and destination address recognition, optical clock detection and FIFO control. *Carrier sense*: Before a node transmits a new packet, it listens to the network to determine if the network contains a propagating OPDP. If the network is busy, the node waits until the network is available. The TRANSPAR senses the carrier by detecting the 3 bit-wide source address in parallel. It considers the all-zero source address as an empty packet. If any of these bits are high, the carrier sense signal becomes high. *Collision detection*: A collision occurs when two or more nodes try to transmit data at the same time. Because of the finite propagation delay time between nodes, it could happen that two or more nodes sense the channel to be idle and begin sending data. When a collision occurs, all collision packets are garbled. The nodes reset

and re-transmit the packets after a random length of time. All nodes detect the collision, and therefore no network global reset signals are necessary. *Optical clock pixel*: The OPDP contains one optical clock channel that is synchronized with the data. The optical clock pixel has three states - idle, send and match. When idle, the pixel is transparent and retransmits the optical clock from the previous node to the next node. When in the state of "send", it sends out an optical clock defined by the on-chip clock. The state of "match" means that there is an address match. In this case, the optical clock pixel routes the detected optical clock signal to the FIFO control module.

Figure 6-28 illustrates the collision detection and elimination procedure for the TRANSPAR network. At time=0ns, node 1 starts to send a packet to node 3. At time=10ns, node 3 successfully receives the packet from node 1 and node 5 starts to send a packet to node 2. At time=20ns, node 1 and node 5 both detect the changing of source address in the received packet and realizes that a collision has happened, then transmits the collision packet with source address '111' to all nodes in the network. After the end of collision packet, the node 1 and node 5 send out the clean-up packet, which contains all zero signals, to circularly clean up the network.

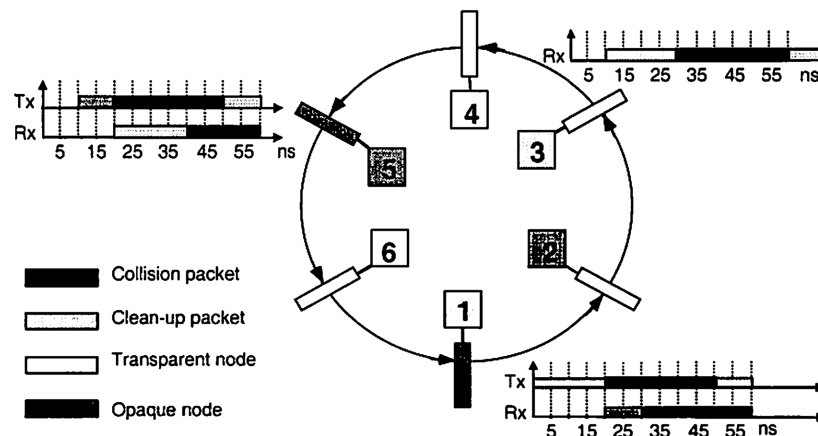


Figure 6-28: Collision detection example for the TRANSPAR network.

In addition to the CSMA/CD function of TRANSPAR chip, the protocol translation chip in TRANSPAR-VM system provides an option for implementing the token ring network protocol in case of noise coupling between the signals lines for VCSEL and MSM arrays. The TRANSPAR-VM node can also be programmed as a bypass/exchange switching stage for a multi-stage interconnection network. By properly setting the bypass/exchange control signals in the multi-stage TRANSPAR-VM network, all the pixels in the first stage node are fully connected to the pixels in the last stage node and the interconnection routes are dynamically programmable.

6.4.3 TRANSPAR Pipelining System Applications

For SIMD computation, each TRANSPAR chip contains an array of mesh-connected processing elements (PE's) implemented by the smart pixels. The PE design is a classic SIMD processor, containing an Arithmetic Logic Unit for performing add, subtract and Boolean operations on bits stored in the 32 bit-SRAM within the PE or on bits within neighboring PE's. A 2-D data field enters and leaves the 2-D PE array either electrically through the edge of the array in a 1-D row parallel format (shifted into the array via the mesh network) or optically directly into 2-D array of PE's via the optical detectors integrated into the PE's. By cascading multiple stages of TRANSPAR node as the structure shown in Figure 6-1, the TRNASPAR pipelining system performs very high throughput and very fast parallel processing of 2-D data fields, such as required in image/video processing or packet header recognition and routing. Figure 6-29 shows the example of the standard MPEG encoder schematic. The pipelining TRANSPAR system

is suitable for the most computation intensive part of the MPEG codec operation, which includes the picture block matching and motion prediction modules.

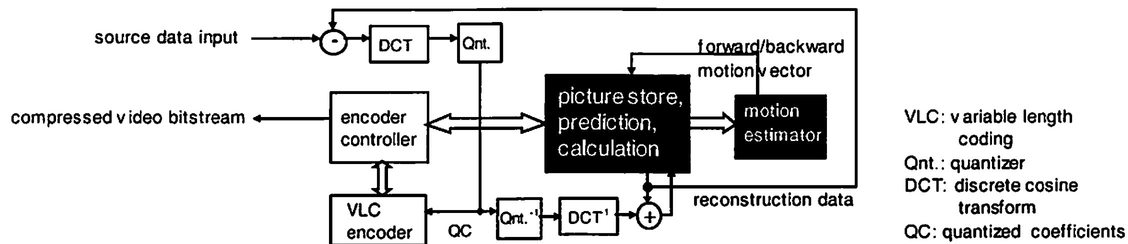


Figure 6-29: MPEG encoder schematic diagram.

6.4.4 VCSEL vs. Modulator

The selection of transmitting devices in the smart pixel system is always a dilemma. However, as the threshold current of VCSELs continues to decrease and its power efficiency continues to improve, the advantage of integrating VCSEL devices with CMOS circuitry becomes more obvious. We make some comparison for the TRANSPAR-MQW and TRANSPAR-VM systems on the following issues: (1) *Power* - The threshold current of VCSEL device for the TRANSPAR-VM is in the range of 3-6mA. At 10mA driving current, the VCSEL optical emission power is greater than 1mW and the forward voltage drop is 2V, which results in 20mW power consumption and 5% power efficiency for each device. For the dual-rail MQW modulator, at 4V and 9V bias voltage, the reflectivity is 76% and 26%, respectively [62]. In our lab experiment, the dual-rail modulator requires at least 1~2μW beam power difference to operate correctly. That is, in the ideal condition of 0W and 2μW beam illumination, the electrical power consumption for the dual-rail MQW device is less than 0.7μW. (2) *Bandwidth* - The small signal bandwidth of VCSEL is over 9GHz and the rise time of MSM detector is

measured at 133ps. The switching bandwidth of MQW modulator is measured up to 1GHz. Both TRANSPAR-MQW and TRANSPAR-VM chips operate at 850nm wavelength. (3) *Contrast ratio* - For the VCSEL based system, the relative optical power level of VCSEL at ON and OFF state is extremely high. On the contrary, the contrast ratio for the dual-rail MQW device is only 3:1 or less.

6.4.5 Optical system

The optical system for the TRANSPAR-VM node is more compact than the TRANSPAR-MQW chip because of the active light source, VCSEL array [63]. The optical module described in Figure 6-17 can also be used for the TRANSPAR-VM system. The interlaced microlens array for the VCSEL-MSM chip with F/#=6 and focal length f=1.5mm is designed using the hybrid phase level algorithm described in Chapter 4. The central part of this microlens array is shown in Figure 6-30. This microlens array is integrated with each TRANSPAR-VM node to provide bi-directional communication at 99% optical power efficiency, which is measured and list in Table 5-1. The optical system design for interconnecting four TRANSPAR-MQW nodes requires larger space and can be setup on a 12" square baseplate. The Laser diodes (LD), spot array generators (SAG) and other optical components are used for the TRANSPAR-MQW chips to provide the external light sources for the readout of modulators, which is shown in Figure 6-31. The SAG grating is designed using Nonlinear Least Square (NLS) method described in Chapter 3, which generates very uniform, high diffraction efficiency and high signal-to-noise ratio spot array as shown in Figure 6-32. This SAG grating contains

48×12 periods and each period consists of 20×80 phase elements. The feature size of each phase element is 5.1 μm and eight discrete phase levels are used in the SAG design.

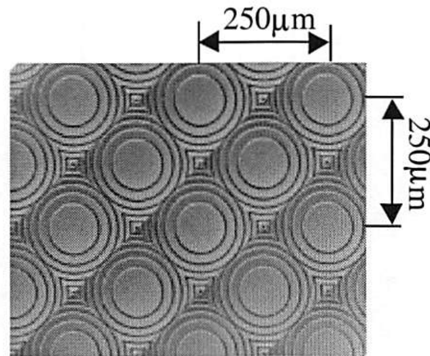


Figure 6-30: Partial view of the interlaced microlens array for VCSEL-MSM chip.

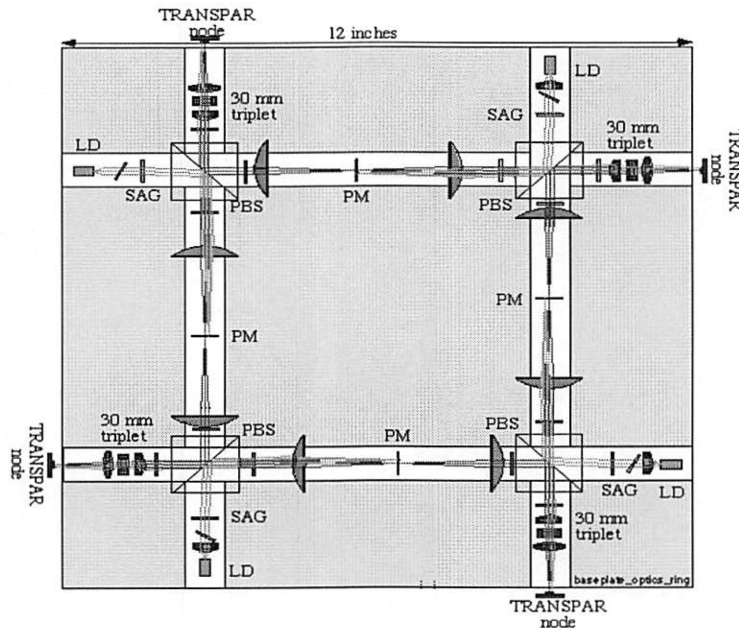


Figure 6-31: Optical system setup for four TRANSPAR-MQW nodes.

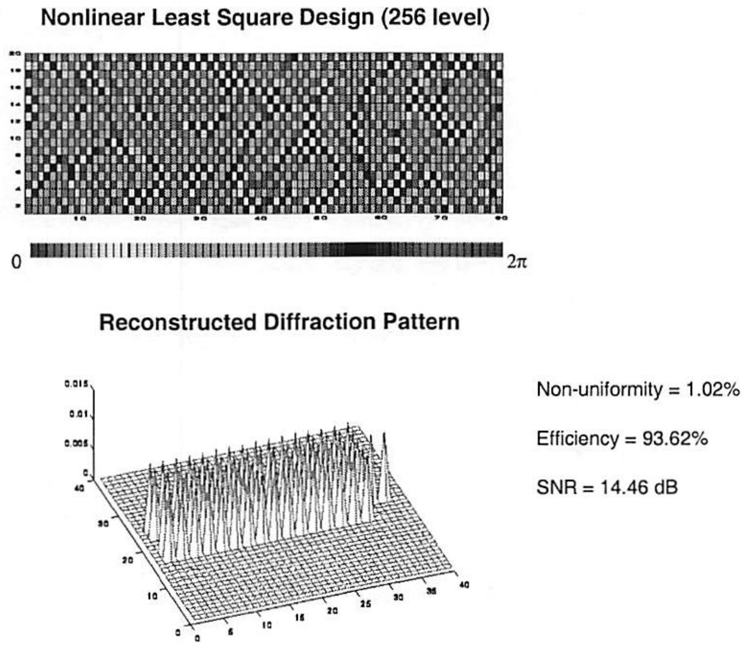


Figure 6-32: Spot Array Generator design and reconstruction pattern.

Chapter 7 Discussion and Conclusions

The efforts of this research work can be classified into four major areas:

- **Device level design**

- *Optical device design*: For the phase-only DOE design, I developed a nonlinear least square method to design the DOEs with lower non-uniformity and higher signal-to-noise ratio at the cost of minor efficiency reduction compared to the two-stage iterative Fourier transform method. The phase shifting quantization scheme optimizes the phase quantization level for the DOE phase elements. To design diffractive microlenses, I applied the hybrid phase level method to adaptively reduce the phase levels to further utilize the limited space bandwidth product (SBWP) of the microlenses due to the feature size constraint in fabrication. By using this method, I design the diffractive microlens arrays with higher numerical aperture and efficiency for smart pixel systems. I developed computer programs that integrate both DOE design algorithms and diffractive microlenses design methods to generate all the diffractive optics designs on the same substrate and create mask layout files for the vendor to fabricate. I also developed a thin-lens decomposition/synthesis model for the phase-only Fresnel zone plate to simplify its diffraction analysis and reduce the computation cost.

- *Electronic device design*: I incorporate in the smart pixel network interface (SAPIENT) chip design using monolithic GaAs optoelectronic integrated circuitry (OEIC) technology and in the translucent smart pixel arrays (TRANSPAR) design using CMOS/SEED flip-chip bonding technology and VCSEL-MSM technology.

I'm also involved in the design simulation of SAPIENT, TRANSPAR and cellular logic processor (SPARCL) chips.

- **Device level testing**

- *Optical device testing*: For the fabricated diffractive optics, including the spot array generators, cellular hypercube interconnection DOEs, weighted fanout DOEs and diffractive microlens arrays, I set up the testing system to measure the diffraction patterns. I also defined the evaluation parameters, which are applicable to both digital and analog fanout DOEs and microlenses. From the measurement data, I characterize the measurement error and the fabrication error for those DOEs and propose the modified fabrication process to improve the zero order reconstruction power.
- *Electronic device testing*: Full electronic and optical function testing for the SAPIENT chip.

- **System level design**

- *Optical system design*: Applying the OSLO® ray tracing software, I design and simulate the optical system for the SPARCL chip. I also design the multi-chip network system for the SAPIENT nodes.
- *Electronic system design*: Develop the electronic buffer board for the SAPIENT chip to interface with host computer.

- **System integration and testing**

For the smart pixel parallel data network interface (SAPIENT) chip, I develop the integrated system using macro-optical devices to test and demonstrate the chip-to-chip communication network functions. This SAPIENT chip is capable of loading/unloading

the electrical data and parallel transmitting/receiving the optical data with built-in address recognition and network control circuitry. To improve the optical power efficiency, system size and alignment tolerance, I also design and fabricate the diffractive microlens array for the SAPIENT optical module. The translucent smart pixel array (TRANSPAR) chip is primary for the 3D parallel data packet network using CSMA/CD protocol. This chip also provides the SIMD data operation functionality for image and video processing. For the MQW modulator version of TRANSPAR chip (TRANSPAR-MQW), a 5×16 spot array generator is integrated for data modulation and read-out using the optical system design similar to the SPARCL chip. For the VCSEL-MSM version of TRANSPAR chip (TRANSPAR-VM), an interlaced 8×8 microlens array is integrated for optical beam collimating using the optical module design similar to the SAPIENT chip. This chip provides an option of using the token-ring network protocol instead of CSMA/CD protocol. The bypass/exchange switching function is also incorporated in the TRANSPAR-VM chip for the multi-stage interconnection network application.

Chapter 8 Future Extensions

The study described in this dissertation has suggested many potential topics for future development. Some of them are summarized below in two categories:

(1) Diffractive Optics Design, Fabrication and Testing

- Apply the nonlinear least square (NLS) method and phase shifting quantization scheme to design various kinds of DOE patterns (digital and analog) for various applications. In particular, the NLS method can generate the global optimized phase matrix design, but the number of quantized phase levels usually limits the DOE performance. It means that the DOE designed using NLS method can be the optimal design when the fabrication technology improves to the precision of gray scale level.
- The maximum matrix size of DOEs designed using the NLS method is limited by the computer's processing power. There may be other numerical optimization algorithms besides the NLS method suitable to design the DOEs of similar or better performance with much less computation cost.
- Develop the algorithm to calculate the required etch depth in fabrication to compensate the intensity offset resulted from the feature shrinkage effect. With the corrected etch depth, the reconstructed diffraction power in the zero order of DOEs can be reset to the designed value.
- Apply the developed hybrid phase microlens design program to fabricate the microlens array for various system applications. There are two major methods to integrate microlens with the optoelectronic system: The first is monolithic integration, which fabricates the lenslet array on the other side of the substrate to provide better

alignment [64]. The other is the hybrid integration, which attaches the fabricated lenslet array onto the different substrate with the advantage of no extra device fabrication step needed.

(2) Smart Pixel System Design, Integration and Testing

- Along with rapid improvements in VLSI fabrication resolution, a smart pixel chip having 10^4 individual pixels on-chip design at Giga Hertz clock can push the available data throughput to over 100Tb/s. The smart pixel chips described in the dissertation are all scalable to utilize the full space-bandwidth-product that the future fabrication industry can provide.
- The smart pixel system integrated with VCSELs has become more advantageous over the other emitting devices because of its high power efficiency, low divergent angle and much improved low threshold. The TRANSPAR-VM system can be modified in the future to a system-on-chip design rather than the board level chipset design at current.
- With the aid of mixed signal design technique, the future smart pixel system may incorporate both the digital logic and the analog circuit to interface the optoelectronic I/O devices and extend the chip functionality. The analog circuit may include the amplifier, switched capacitor filter, phase lock loop, analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuits.
- Due to the highly parallel data flow in the smart pixel chip, the fully functional test has become a more difficult job. In the future design, we may want to put some built-in-self-testing (BIST) modules or bit-error-rate (BER) testing modules on chip to reduce the testing cost.

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