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Optoelectronic-VLSI System Integration For Digital Information Processing

by

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Dedication

To my parents

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Abstract

Optoelectronic-VLSI systems can provide high-bandwidth multimedia applications and real-time parallel processing using the complementary properties of electronics and optics. Optics has many advantages in high-speed data transfer including inherent low crosstalk and low power, while electronics is more suitable for logic functions and integrated circuitry. In this research, we present designs and demonstrations of optoelectronic-VLSI systems based on two different approaches: a modular integration, and a monolithic integration. Both approaches deal with the optimal integration of optoelectronic devices for high-speed, high-throughput network communications and data processing.

We have designed and tested a modular optoelectronic-VLSI system called Translucent Smart Pixel Array (Transpar). The system includes a field-programmable gate array (FPGA), a transimpedance amplifier (TIA) receiver, and an interlaced array of 4×4 vertical-cavity surface-emitting lasers (VCSELs) and metal-semiconductor-metal (MSM) detectors. The FPGA allows for reconfigurable networks and processors, thus Transpar can implement dynamic novel network protocols. The components are mounted on a printed circuit board (PCB) for testing of various optical interconnection techniques. Bulk lenses, diffractive optical elements (DOEs) and fiber image guides (FIGs) were tested and compared as interconnection techniques for the Transpar system. A detailed wave-propagation simulation for the FIGs is presented and compared with

experimental results. The effect of optical crosstalk and minimization of the overall power dissipation are also considered.

One technique for the monolithic integration of mixed-signal integrated circuits with optoelectronics is Ultra-thin Silicon-on-Sapphire (UTSi) technology. UTSI has low parasitic capacitance and enables different optical and electrical components to be integrated with ordinary complementary metal-oxide semiconductor (CMOS) circuits using standard fabrication processes. It is well suited for low-cost and high-performance optical data communication systems. The sapphire substrate of UTSi is highly transparent to the propagation of light from VCSELs and simplifies the packaging. We have designed and tested four different UTSi chips for evaluation and testing of integration of optoelectronic components. These chips contain VCSEL drivers, receiver circuitry, clock generators, frequency dividers, and voltage controlled oscillators. Flip-chip bonding is used to combine VCSEL and detector arrays with the UTSi CMOS circuits. The architecture and system performance of each chip is tested and discussed.

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Abbreviations

ASG	acid-soluble glass
BPM	beam propagation method
CSMA/CD	carrier-sense multiple access/collision detection
CDR	clock/data recovery
CMOS	complimentary metal-oxide-semiconductor
COOP	Consortium for Optical and Optoelectronic Technologies in Computing
CTE	coefficient of thermal expansion
DAQ	data acquisition
DOEs	diffractive optical elements
DFF	double flip-flop
EDA	electronic design automation
EEPROM	electrically erasable programmable read-only memory
ESD	electrostatic discharge
FIGs	fiber image guides
FPGA	field-programmable gate array
HDTV	high definition television
ISI	intersymbol interference
JOP	Joint Optoelectronics Project
LSB	least significant bit

LED	light-emitting diode
LANs	local area networks
LNA	low noise amplifier
LSB	least significant bit
LVDS	low-voltage differential signals
MCMs	multichip modules
MIM	metal-insulator-metal
MSM	metal-semiconductor-metal
MMICs	monolithic microwave integrated circuits
OIF	Optical Internetworking Forum
OPDPs	optical parallel data packets
PLL	phase-locked loop
PD	photodetector
PBS	polarizing beam splitter
PE	processing-element
PRBS	pseudo-random bit steam
PCB	printed circuit board
SEEDs	self-electrooptic effect devices
SOC	system-on-chip
SOI	silicon-on-insulator
TBC	transparent boundary conditions
TDM	time-division multiplexing

TIA	transimpedance amplifier
Transpar	Translucent Smart Pixel Array
TR	token ring
TSPC	true single-phase clock
UTSi	Ultra-Thin Silicon-on-Sapphire
VCSELs	vertical-cavity surface-emitting lasers
VLSI	very large scale integration
VSR	very short reach
VR	virtual reality
VCO	voltage-controlled oscillator
WDM	wavelength division multiplexing

Chapter 1

Introduction

1.1 Motivation and Objective

The demands for high bandwidth and high-speed data processing are always increasing in modern information society. During the last decades, processor clock speeds have increased according to Moore's law [23] and the bandwidth of long haul communication systems have exploded with the advent of fiber optics. Recent multimedia applications such as high definition television (HDTV), virtual reality (VR), real-time image/video processing, and media immersion require more intensive signal processing and bandwidth [43]. For these reasons we expect that the need for more bandwidth and faster data processing will continue in the future.

In high-bandwidth telecommunications, optics has been extensively used and is increasing its role in networks over shorter distances, such as 10 km or less [55]. Optical interconnections in local area networks (LANs) that interconnect routers and other transport equipment are now being developed using links at over 10 Gbps using multiple parallel fiber optic channels [7]. Recently the Optical Internetworking Forum (OIF) has announced the use of 1×4 parallel optical transceiver for very short reach (VSR) intra-office interface [50]. This enables the use of optical interconnects down to the range of 2 m communication distance.

Figure 1-1 summarizes the possible use of optical interconnects for various distance scales. In long distance optical communication systems the information is carried by single-mode fibers using 1.55 μm wavelength. Expanding the spectral bandwidth using wavelength division multiplexing (WDM) increases the capacity enormously. Short distance optical interconnects, such as chip-to-chip, board-to-board, and backplane interconnections are based on waveguides on a substrate, free-space, or multi-mode fiber arrays with 850 nm laser sources [51], [53]. The information bandwidth can be expanded by increasing the number of spatial channels in two-dimension (2D) or one-dimension (1D).

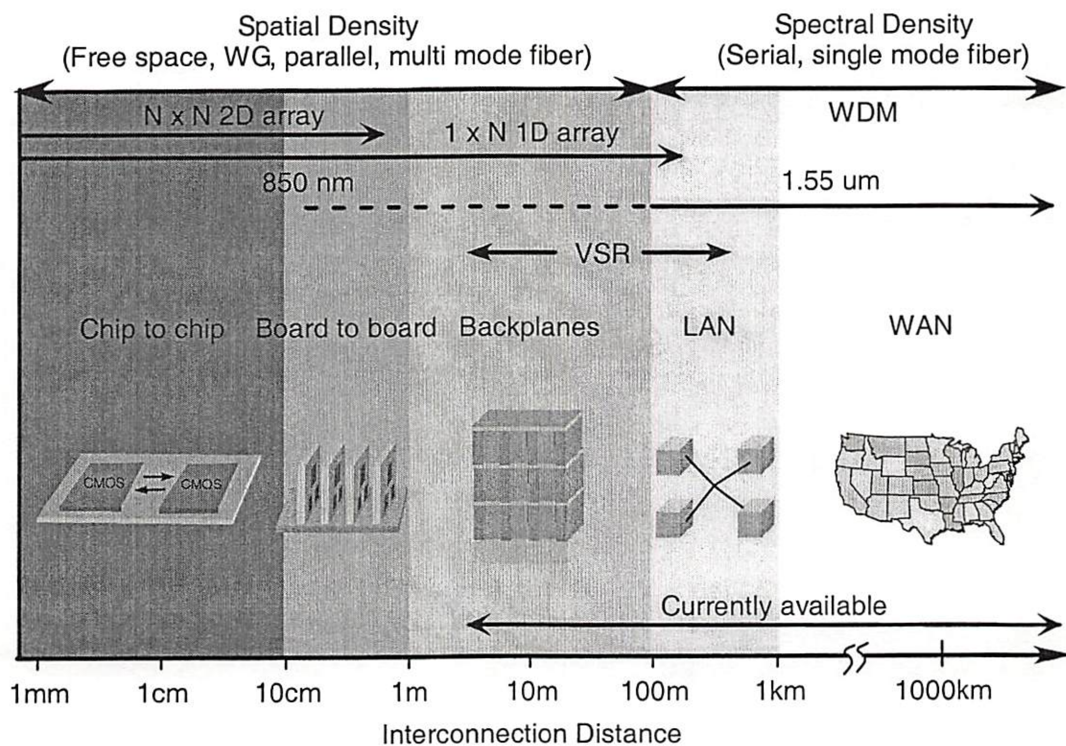


Figure 1-1. Optical interconnection hierarchy as a function of distance.

Despite the success in long-haul communications and its emergence in LANs and VSR, optical interconnects in short-range communications are not well developed. The use of optics in short distance is quite different from long distance telecommunication systems from device and module fabrication to system integration and packaging [66]. In short distance data communication the optical input/output (I/O) has to be directly connected to silicon based electronic chips and this is still a challenge [31], [39], [45]. However, we need to push the limits of optical interconnects to short-range distances because the scaling limit of copper-based electrical interconnects soon will be reached [23].

Electronics has had a key role in digital logic, integrated circuitry, switching and storing data. Also, cost-effective complimentary metal-oxide-semiconductor (CMOS) processing will be a driving force for electronics in future digital information systems [24]. Many argue that Moore's law will soon face its limit in system performance and that performance improvements will likely come from new architectures, new materials, and new technologies. One limit is the I/O bottleneck. The bandwidth of electrical interconnections between chips or boards limits future information capacity. One solution is replacing electrical interconnections with optical interconnections that have attractive advantages for transmitting high-density 2D or 1D array data at low power, low crosstalk, and low latency. Moreover the recent development of vertical-cavity surface-emitting lasers (VCSELs) arrays has increased the flexibility of optical I/O arrays by providing optical sources with relatively low power consumption, high data rates, and the possibility of integration with electronics [37], [38].

Integrating optics to electronic systems faces many technical challenges. The key challenge is the introduction of optical devices based on III-V materials to silicon-based very large scale integration (VLSI) electronics. In addition high-energy photons are not efficiently converted to low-energy electrons. The idea of optical interconnects to VLSI electronics was first proposed by Goodman, *et al* in 1984 [10]. Since then many groups have been trying to integrate optics to VLSI using various methods, such as quantum-well devices [30], or VCSEL arrays [52], but cost effective solutions have not been found yet.

The goal of this research is the development of a new optoelectronic-VLSI technology for integrating optical interconnects to VLSI CMOS to relieve the interconnection bottleneck by optimizing the complementary properties of electronics and optics. In this technology 2D or 1D optics is used to transfer information to and from arrays of optoelectronic units with electrical processing between the optical I/Os.

1.2 Contributions of the Research

In this research we describe optoelectronic interconnections for two different types of optoelectronic-VLSI systems. The first is a modular system called Translucent Smart Pixel Array (Transpar) [4], [34]. Transpar is an optoelectronic system that can perform high efficiency parallel data processing through smart pixel arrays on 2D data structures such as images and video. In this modular system, the optical and electrical components are individually tested and combined to optimize the system performance. The other

approach uses electrical components monolithically integrated on CMOS circuitry with optical I/O arrays that are flip-chip bonded to the CMOS. For the monolithic integration of the digital and analog circuitry we used a silicon-on-insulator (SOI) technology called Ultra-Thin Silicon-on-Sapphire (UTSi) that has been developed by Peregrine Semiconductor Corp. [2], [33]. This process is being developed to meet the cost and performance requirements of future integrated system-on-chip (SOC) solutions for high performance communication systems. We also investigate different optical interconnection methods such as fiber image guides (FIGs), and free-space optical interconnections based on refractive lenses and diffractive lenses. The modeling of FIGs is presented for the waveguide simulations. Details on the contributions are given as follows:

(1) *A modular approach for optical interconnects: Transpar.*

We present a modular approach for optoelectronic-VLSI system called Transpar. Transpar uses different optical and electrical components mounted on printed circuit board (PCB). Each component can be optimized to perform high speed, low noise optical interconnections. We present the characteristics of each component and discuss the optimization of the modular system. Experimental results are also presented.

(2) *Optical interconnection system based on free-space.*

Optical data packets can be transmitted and received via interconnection systems implemented with free space or fiber arrays. We present optical interconnection

methods based on free-space with bulk refractive lenses and diffractive optical elements (DOEs). We show that refractive lenses have much better optical coupling efficiency but their bulky size is a problem in packaging and alignment. DOEs offer the advantage of a small volume advantage and possible integration with VCSEL arrays. We discuss different pros and cons in free-space optical interconnection systems for Transpar and UTSi based systems. The system optimization in terms of power loss and packaging is also discussed.

(3) *Fiber image guides (FIGs) interconnection.*

FIGs can offer 2D parallel data transmission without any other optical elements and are a convenient way to interconnect optical receiver array and transmitter arrays. We introduce a FIG based optical interconnection system and explore methods to minimize optical loss and crosstalk.

(4) *FIGs modeling and simulations.*

The propagations of light in FIGs are modeled, simulated compared with experimental measurements. We first model appropriate laser modes for VCSELs and the hexagonal array FIG structure. The modeling and simulations are done using the RSoft BeamPROP package. We analyze the simulation results and compare with experiments.

(5) *An integrated approach for optical interconnects: UTSi.*

UTSi is an integrated approach for an optoelectronic-VLSI system. Electrical components are monolithically integrated on Si-based CMOS circuitry and optical I/O arrays are flip-chip bonded to the CMOS. We have designed and tested four different UTSi chips. Each UTSi chip has different devices, functions, and sub-systems. We demonstrate different testbeds based on each different function. Different PCBs are also designed to perform high-speed test plans.

1.3 Organization of the Dissertation

The remainder of this dissertation is organized as follows.

- Chapter 2 reviews the background of optical interconnects. We discuss the need for optical interconnection systems in multi-giga rate date transfer. The design issues in integration of optoelectronic components and its network implementations are also discussed.
- Chapter 3 introduces a modular approach for optical interconnects. The idea of Transpar and the network applications are presented. We introduce the use of field programmable gate arrays (FPGAs) for the system logic and VCSEL/MSM arrays for the optical I/O.
- Chapter 4 presents the demonstrator system based on Transpar and shows details of the components and the implementation. The test results are also presented and discussed.

- Chapter 5 introduces interconnection methods between optical I/O arrays. Free space optical interconnections based on bulk refractive lenses and diffractive optical elements are presented. We discuss the optical power profile, coupling efficiency and their influence on the system design.
- Chapter 6 explores the interconnection methods using FIGs. We examine the optimization of the power profile and optical I/O coupling to minimize power loss and crosstalk.
- Chapter 7 describes FIGs modeling and simulations. We discuss and compare the test results.
- Chapter 8 presents an integrated interconnection approach based on UTSi and we discuss the design issues and network applications.
- Chapter 9 presents different designs of UTSi based systems and evaluates the performance and the system implementations.
- Chapter 10 concludes on the results of the research and discusses possible future work.

Chapter 2

Optical Interconnects for Electronic Systems

Silicon-based CMOS VLSI has been the industry standard and will continue to be the mainstream technology in digital electronic devices and systems. However the bandwidth of the data communication I/O between electronic processing modules is reaching a limit. In recent years, optical interconnects have been introduced as a solution for the I/O bottleneck, and the development of optoelectronic devices such as dense VCSEL and detector arrays, and flip chip-bonding technology have accelerated the use of optical interconnects in digital electronic systems [46], [58], [66].

In this chapter we discuss the advantages of optical interconnects over electrical interconnects and discuss the design issues of optoelectronic integration with Si-based electronic systems.

2.1 Advantages of Optical Interconnects over Electrical Interconnects

Optical systems are used extensively in long-haul communication systems. Long-distance electrical communication links have limitations in bandwidth, impedance matching, power budget, and signal delay (skew) while optical links overcome many of these electrical limitations. The basic reason for the advantage comes from the high energy, high frequency nature of photons. Compared to electronics, optics has no

frequency dependent loss and crosstalk, low loss over a long distance, low skew, and no need for impedance matching. In addition, the ability to use many different colors (wavelengths) in WDM gives more than 100 TBps bandwidth over a single fiber [48]. Therefore optical networks have been dominant in long-haul communication systems. However the use of optical interconnects in short distance data communication systems is very immature because short distance data communication has different characteristics from long-haul communication systems.

Table 2-1 summarizes the differences between telecommunications and data communications. Currently, data communication applications generally use conventional coaxial cable for short distances at data rates up to 622 Mbits/sec (OC-12). When the rate reaches over 1 Gbit/sec, optical solutions look attractive [35].

	Data communications	Telecommunications
Distance	Short (< 300m)	Long (> km)
Fiber	Multimode	Single mode
Wavelength	Short (0.85 μm)	Long (1.3 or 1.55 μm)
Typical data rate	1~ 10 Gbps	10 ~ 100 Gbps
Electrical interface	Directly from ASIC	Serial/de-serial
Volume/price	High/low	Low/high

Table 2-1. Comparisons of data communications and telecommunications.

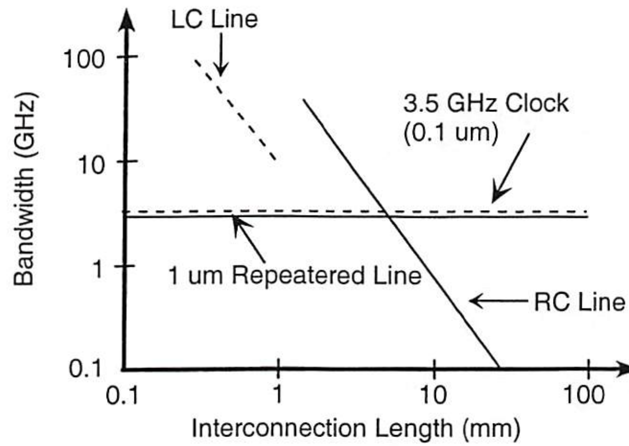
In current digital electronic systems, electrical interconnects have not yet reached their limits for typical applications, and cost effective optical interconnects are not yet available. It is expected that future system performance will be limited by I/O bandwidth soon and cost-effective optical interconnects may be required.

The bandwidth capacity for the electrical interconnects is limited by aspect ratio defined as

$$B \cong B_0 \frac{A}{l^2} \text{bits/s}, \tag{2-1}$$

where A is the cross-section area of the line, l is the line length (A/l^2 is dimensionless) and the prefactor B_0 is ~ 10^{15} for unrepeatered inductive-capacitive (LC) lines, ~ 10^{16} for resistive-capacitive (RC) lines, ~ 10^{17} for equalized LC lines [47]. These limits are relatively independent of the details of the design of the line.

Figure 2-1 shows a simple modeling of the bandwidth and delay effects of Cu-based electrical interconnections [45]. The modeling for RLC lines and repeatered lines is based on 0.25-μm technology and the 3.5 GHz clock line is based on future 0.1-μm technology. We also assume that the repeatered line is ideal and it simply attenuates all frequencies below the clock frequency to have the same loss as the clock frequency signal. From this discussion we see if the interconnection length is over 1 cm, the limitations of bandwidth and delay severely limit the 3.5 GHz clock-based system. Even with repeater amplifiers in the lines, the limitation of the delay is apparent over 1 cm [Fig 2-1 (b)]. Compared to these results, optical interconnects have no length-dependent limitation of bandwidth and the delay over the distance is much smaller than that of electrical interconnection.



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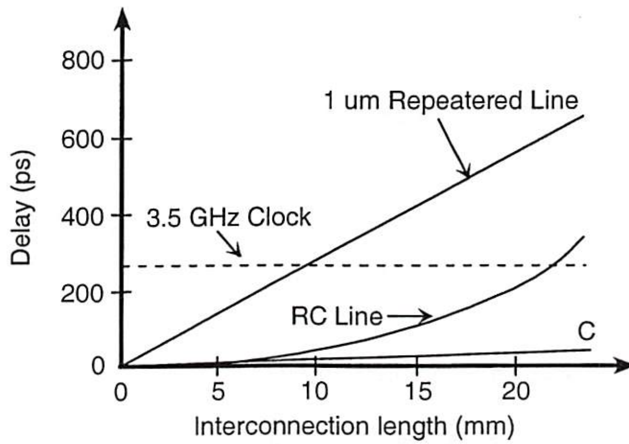


(b)

Figure 2-1. Copper interconnection with 1 μm × 1 μm cross-section as a function of interconnection length [45]. LC and RC lines are with 1 μm unrepeatered lines. The bandwidth of the repeatered line is with amplifiers to maintain a maximum bandwidth. On-chip clock rate is 3.5 GHz for 0.1 μm technology. (a) Bandwidth of copper interconnect; (b) Delay of copper interconnect, the line labeled C for the case of optics.

Another advantage of optical interconnects is the energy efficiency over the transmission distance [44]. A comparison of the energy required to send one bit shows optical interconnections can be more energy efficient than electrical interconnects for distance over 1 mm [Fig 2-2]. This calculation is based on 10 × 10 μm^2 optical modulators, 1.5 eV photon energy, and 1 V electrical signal swing. Ii is also shown that smaller optical devices offer lower communication energies. Other groups show similar results and find that the on-chip energy requirements of one-to-one optical interconnect up to 2 cm are generally less than 50 pJ/bit transmitted, while electrical interconnects require on the order of several hundred picojoules [71]. From these results we can conclude that optical interconnects have advantages in power efficiency, bandwidth, and delay over distances of more than 1 mm.

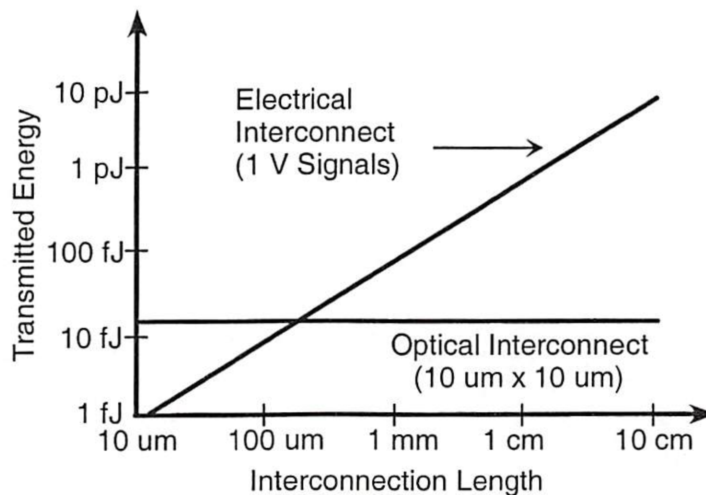


Figure 2-2. A comparison of typical optical and electrical communication energies: the actual crossover point is system dependent [44].

In addition to the advantages above, optical interconnects are capable of dense 2-dimensional data processing without any crosstalk. While long-haul optical interconnects using WDM, use parallel spectral channels, short distance data communication increase the overall data rate at low cost by using parallel data channels. This is made possible due to the absence of electromagnetic crosstalk. Recently developed 2D VCSEL arrays are now available at relatively low cost. The ultimate density of optical interconnects is still an open issue that will affect the practical distance of the interconnections. The limit on the density of optical interconnects to chips is likely the power dissipation in the receiver and transmitter circuits.

2.2 Optical Interconnects to Silicon CMOS: Design Issues

2.2.1 Strategy

Optical devices are based on GaAs materials that have different lattice structures from Silicon. For this reason, it is very difficult to integrate optical I/O to silicon substrates and there are many approaches to integrated Si-GaAs technology to date. As a practical approach, a hybrid integration technology such as flip-chip bonding can be used. Several techniques for integration and system optimizations are described in Refs. [15], [27], [36], [64].

In the integration of optical transceivers to electric circuitry, the system power budget must be considered and optimized [70]. This is also one criterion for selecting appropriate optical sources and detectors. Low power lasers with threshold current

below 1 mA are essential and photodetector amplification must be very low power. In addition, transmitter and receiver circuits must not consume too much power. Integration of optoelectronic devices is a possible solution to reducing power consumption in the optimized systems.

Clock distribution strategy is also an important factor in system integration and optimization. Optical signals have no lower delay than electronic circuitry, but the optical transmitters and receivers in the system induce delay and can introduce excessive jitter and signal skew in the system. To avoid delay the circuitry for optical transceivers should have the same or fewer numbers of stages than their electrical counter parts.

Another consideration in integration is that optical transmitter and detector arrays need to be aligned to the optical signals and the tolerance of the misalignment must be considered. In the case when the optical components are directly attached to the chips this problem has to be considered with the system packaging. The packaging is an essential part of the design and implementation of an optical interconnection system and the system designers have to consider the final packaging at the beginning of the design for system optimization.

Generally, compared to electrical interconnection systems, optical interconnects gives two design benefits. The difficulty of impedance matching and wave reflections can easily be avoided. The inductance of the electrical connections to the chip that can give substantial voltage errors is not present in optical interconnections. In clock distribution, since optics have a very high frequency and the modulation frequency is

negligible compared to the carrier frequency, the optics itself does not have to be redesigned as the clock speed is increased.

2.2.2 Component Requirements and Designs

Optical Transmitter Array

Optical transmitter arrays are an essential part of optics-based communication systems. Transmitters for high-speed optical communications require sources with high modulation bandwidth and high power at low threshold currents, small divergence angle, and cost-effective array capabilities. There are three different basic kinds of transmitters on the market for optical interconnection systems: quantum-well modulators, light-emitting diodes (LEDs), and VCSELs.

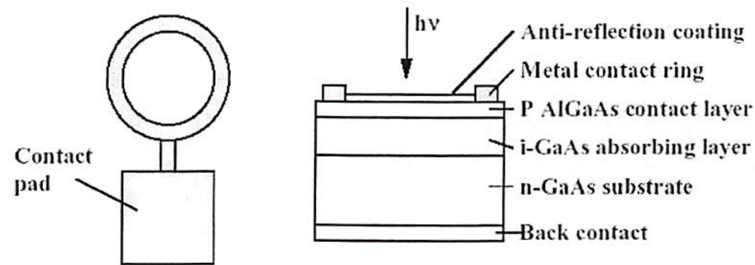
One type of quantum-well modulator is also called self-electrooptic effect devices (SEEDs) [46]. The modulators can be made in large arrays that can be flip-chip bonded onto VLSI chips. The performance of quantum-well modulators has proven good enough to allow demonstrations of large optically interconnection systems [30], but they require an external laser source, so that the optical system can be more complicated than in the case of active sources.

LEDs are relatively easier to manufacture at low cost than other devices. However, LEDs have limited speed response, low optical efficiency, and high divergence angle, therefore they are not generally used as the optical source for dense optical interconnects.

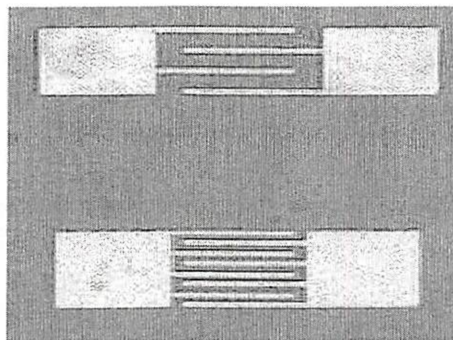
The use of VCSEL arrays has held promise as low-cost optical sources for optical array interconnections. Since VCSEL light is emitted perpendicular to the substrate, VCSEL arrays are more appropriate for 2D parallel optical interconnection systems. However there are drawbacks with current VCSELs. First, VCSELs have relatively high threshold current with a turn-on delay in the emission of light from the laser that depends on the previous data pattern. Second, VCSELs have different spatial optical modes and polarization at different current; and third, it requires high power supply voltages. Since future supply voltage of Si-CMOS likely to be under 1 V, the current high power supply voltages (~ 2 V) need to be lower. Despite these drawbacks, VCSELs are commonly used for short distance interconnections with 850 nm wavelength and research continues on single mode, low power, longer wavelength (> 1300 nm) or even tunable VCSEL arrays for local area optical interconnections [3].

Photodetector (PD) Array

Favorable characteristics for a photodetector are low capacitance, short transit time, high responsivity (high sensitivity), and low dark current (low shot noise). The basic PD types are commonly used in optoelectronic-integrated devices. One is the PIN diode and the other is metal-semiconductor-metal (MSM) detector. These are shown in Fig. 2-2. The PIN diode produces a photocurrent that flows mostly vertically across the *i* region shown in Fig. 2-2 (a). The PIN diodes offer very good quantum efficiency up to 85 % with low noise.



(a) PIN diode



(b) MSM detector

Figure 2-2. Two most common photodetector types.

The MSM detector has photosensitive region consists of the interdigitated metal electrodes and produces a mostly lateral photocurrent flow as shown in Fig. 2-2 (b). The electrode geometry provides the MSM photodetector with a very low intrinsic capacitance, and thus the possibility of extremely high-speed devices. The MSM detectors have been also used in a number of microwave photonic applications because their compatibility for integration with field-effect-transistor devices in optically controlled monolithic microwave integrated circuits (MMICs) [62]. One drawback to use of MSMs is the low quantum efficiencies, typically in the range of 25 % to 40 %.

Receiver Circuitry

Receivers are an essential part of optoelectronic circuit design. Laser drive currents and other electronic I/O specification limit the degree of freedom in the design of electronic circuitry for optical interconnects. A low noise and high sensitivity receiver is necessary for reliable optical data processing in the system [15], [59], [61].

The optical receiver consists of an optical detector and a high gain, low noise transimpedance amplifier (TIA) that converts the low photocurrent to a large voltage variation with very short rise and fall times. Since typical input currents are in the range of 1 ~ 100 μA and the typical output voltages are 1 ~ 2.5 V, the transimpedance gain of the receiver amplifier must exceed 25 kΩ. With such a large-gain stage, the receiver designer has to be careful about the danger of oscillations, and should leave sufficient design margins to avoid them.

Small detector capacitance leads to larger voltage swings for a given photocurrent, which leads to better noise immunity and fewer gain stages. Also it allows the use of small, low-power dissipation transistors in the input stage. Therefore the capacitance of the photodetector and its connection to the receiver circuits should be as small as possible.

The noise, gain, and bandwidth of the TIA directly impact the sensitivity and speed of the overall system. The clock and data recovery functions must provide a high speed, tolerate long runs, and satisfy stringent jitter and bandwidth requirements [57].

Chapter 3

A Modular Testbed for Optical Interconnects

3.1 Transpar

We have developed and built an optical interconnection testbed system called Transpar [4]. Transpar is configured as a high throughput photonic bus or ring network that transfers digital data using three-dimensional optical parallel data packets (OPDPs) propagating in free-space [16] or fiber image guides (FIGs) among nodes [18], [19]. It can provide high information capacity with digital interconnections and networks with three-dimensional (3D) optical data packets (2D spatial and 1D time) as in Fig. 3-1. Spatially parallel channels provide low latency for high-speed data transfers at the on-chip clock rate. Each node can serve as a high-throughput single-instruction-multiple-data (SIMD) parallel pipeline signal-processing node; with an internal arithmetic logic unit (ALU) and internal local mesh connections at each pixel.

Each 2D spatial channel is created by a smart-pixel array (SPA) [38]. By utilizing many spatial parallel channels Transpar can achieve high throughput, low latency communication between nodes. Each network node has three main components that are combined on a printed-circuit board (PCB). One is a Honeywell VCSEL/MSM smart pixel that is supplied by the DARPA-sponsored foundry project operated by the

Consortium for Optical and Optoelectronic Technologies in Computing (COOP) program at George Mason University.

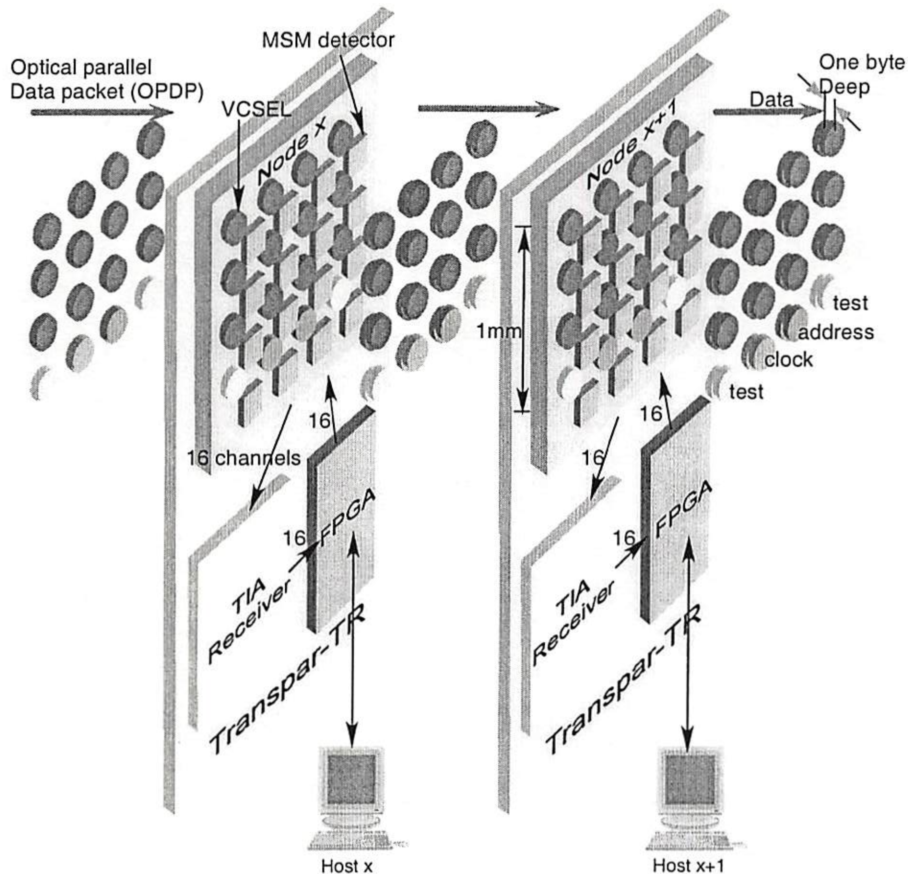


Figure 3-1. Two Transpar nodes and free-space optical packets flowing from left to right between them.

The VCSEL/MSM arrays are two-dimensional arrays of optical input and output devices. The second chip is a field-programmable gate array (FPGA) that allows the flexible implementation of specific architectures without having to design custom chips

[65], [67]. The FPGA in Transpar is an Altera EPF10K100EQC 208-pin enhanced embedded programmable logic device from the FLEX10KE family. The third chip is a TIA receiver that amplifies the detected optical signals to electrical logic signals. We have designed four different TIA detector amplifiers and fabricated them through the MOSIS foundry. One of the drivers has been chosen for the best performance. We will discuss these components more in the next chapter.

FPGAs provide structural emulation at logic level and to mimic arbitrary logic level circuits. The FPGA can be programmed to implement different network logic such as: token-ring network, carrier-sense multiple access/collision detection (CSMA/CD), or other experimental protocols. Another advantage of the FPGA is that it can directly drive the VCSEL array. Its output voltage can be chosen to 2.5 V but it is limited to a drive frequency of 250 MHz for the FLEX10KE. For parallel processing, the Transpar node can operate as a mesh-connected SIMD processing-element (PE) array with electrical I/Os via FPGA or optical I/Os via 2D MSM detector or VCSEL array. The ALU performs add, subtract and other Boolean logic operations on bits that are stored in the local SRAM. The prototype system is able to perform very fast parallel processing of 2D data array, such as those required on image/video processing.

The logic design, design compilation, verification, timing analysis, and the programming of Transpar can be performed in Altera electronic design automation (EDA) tool, MAX+PLUS II.

For the optical interconnections between Transpar nodes we have investigated diffractive and refractive free-space optics, and FIGs for guided-wave interconnections.

Free-space interconnection systems have been studied in the past and demonstrated the usefulness and advantages of optical systems over electronic-only systems. However, bulk lenses and the difficulty of alignment of diffractive and refractive components might be obstacles to constructing practical systems. Diffractive optical elements (DOEs) or FIGs may be one of the key technologies to avoid packaging problems. DOEs are of comparable size to VCSEL arrays and could be monolithically integrated with VCSEL at low cost [42]. In comparison, FIGs are easy to set up and offer relatively flexible packaging and spatial parallelism that is easily realized.

3.2 Transpar Token-Ring Network

Transpar uses a particular network protocol called Transpar-token-ring (Transpar-TR) [16], [72]. Transpar-TR is a high throughput photonic ring network that transfers digital data using three-dimensional OPDPs propagating in free-space or waveguided medium among nodes. The number of nodes (*N*) in Transpar-TR is always an even number and each has an optoelectronic interface for an electronic host or server as shown in Fig. 3-2. *N/2* optical parallel data packets are transmitted simultaneously around the *N* node ring using a slotted protocol that avoids the possibility of collisions. To avoid crosstalk, the Transpar-TR protocol does not allow the simultaneous use of VCSEL transmitters and MSM receivers.

In designing Transpar-TR, we have been concerned with potential electrical crosstalk between the closely spaced VCSELs and MSM-detectors at each node. The

VCSELs have mA drive signals that are three orders of magnitude greater than the μA signals generated by the MSM detectors. Similarly, optical crosstalk may also be a problem due to the divergence of the neighbor beams or unwanted reflections in the imaging system.

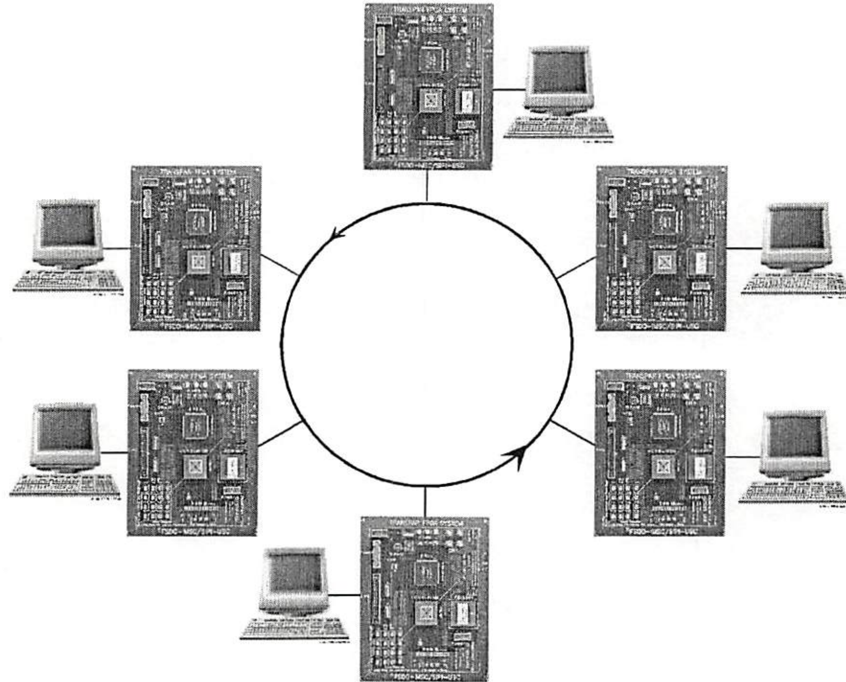


Figure 3-2. Transpar token-ring network.

In anticipation of crosstalk problems between VCSEL and MSM signals, several protocols have been evaluated and implemented. In the CSMA/CD protocol, each node simultaneously "listens" and "talks" to the network, requiring simultaneous operation of the VCSEL sources and MSM detectors. We have developed a novel slotted token-ring protocol for an N node (N even) Transpar-TR that is designed for collision free, high

throughput network operation and which also avoid simultaneous VCSEL/MSM operation. Hence, crosstalk problems are eliminated. In this scheme, each node waits for a 'ready to receive' signal from the next node before transmitting an optical packet. In contrast to the CSMA/CD protocol, packets are received, buffered and re-transmitted at each node as they traverse the network. Using this technique, the handshaking protocol allows packets from alternate network nodes to occupy the network concurrently. Thus $N/2$ nodes transmit simultaneously. A transmit queue and a receive queue serve as a bridge between the ultra fast optical network and relatively low speed of the electrical smart pixel array processors to minimize packet loss. Due to the parallel transmission of address and data packets, the processing latency is reduced compared to traditional serial token-ring networks. The CMOS SRAM process utilized in the Altera FLEX10KE FPGA devices can be rapidly reprogrammed. This suggests the possibility of implementing other novel OPDP protocols that can be dynamically reconfigured (to CSMA/CD or ATM, for example) depending on traffic level and other parameters.

Figure 3-3 shows a block diagram with details of the FPGA logic functions at each node. As shown in Fig. 3-1, a detected incoming packet includes twelve detected payload channels, an address channel, and an optical clock channel. The double lines with arrows at the top left in Fig. 3-3 show twelve incoming payload (data) signals derived from optical inputs through the MSM detectors. The double lines at the top right are twelve transmitted signals that drive optical VCSEL outputs. The detected optical clock input at the left is generated by the previous (transmitting) node and is used to clock in the data and the node addresses. Incoming data is loaded into the node buffer at

the top. The ready to receive signal from the previous node goes to logic level "1" when the node is receiving an input.

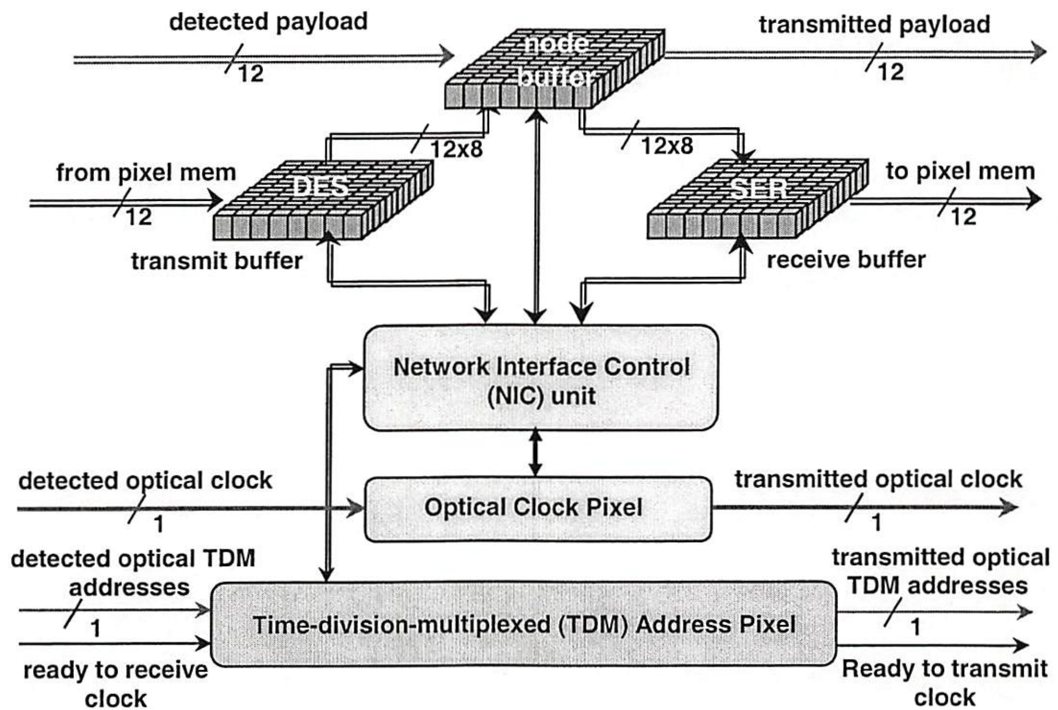


Figure 3-3. Block diagram of Transpar TR logic functions.

The detected optical clock signal at a node comes from a local clock at the previous node, and its frequency can be different from the local clock frequency at other nodes. The slowest clock must be able to transmit an 8-bit deep 3D OPDP packet within the token time controlled by the ready-to-receive signal. To account for variations in the optical delay and minimize the bit error rate, the optical transmitted clock at each node is

delayed by 1/2 period so that the rising edge of each clock samples data in the middle of a bit time slot.

The address pixel reads the detected source and destination addresses, which are transmitted serially in one eight-bit byte, and sends them to the network interface control (NIC) unit (at the center of Fig. 3-3) where a comparison with the fixed node address are performed. The NIC is also responsible for global timing, optical clock generation, add/drop, retransmission, etc. The transmit buffer is a twelve channel deserializer, and the receive buffer is a twelve channel serializer. They perform packet adding and dropping in parallel with minimum delay and communicate with local pixel memory in serial for simplicity. The node buffers reshape the detected signal and limit noise accumulation or recirculation around the ring. In an advanced version of Transpar-TR, the transmit and receive buffers are twelve 8-bit long queues that are 7-bits deep (rather than 1-bit deep). These larger buffers perform even better to match the high-data rate of the optical ring network with the relatively slower host electronics. The 2D (3×4) electrical data fields are transferred to and from the electronic host processor in Fig. 3-1 through the edge of the array in a 1D row-parallel format via a mesh network into twelve pixel memories (not shown). The pixel memories are connected to the transmit and receive buffers. The host processor controls these operations via the NIC unit and monitors the status of the OPDP packet network.

The Transpar-TR protocol is designed such that if the destination address of the incoming packet matches the node address, the packet is removed from the network and drops into the receive buffer. The oldest packet in the transmit buffer is added to the

network. If no address match occurs, the traffic on the ring has higher priority and continues to circulate around the ring to the next node. A newly generated packet is injected by a node into the network only if its ready to transmit time slot is or becomes empty. In case of packet add or drop contention, the new packet along with earlier ones, if any, are then queued in the transmitting queue. Any dropped (received) packets are queued in the receive buffer and moved to local pixel memories in sequence.

We describe now the test of a reconfigurable-Transpar system that specifically implements the Transpar-TR network protocol and host interface. In this test, two Transpar-TR nodes are set up with electrical inputs applied to emulate its operation in the optical token-ring network environment described. A data generator attached to the first node generates signal that would originate from the Honeywell MSM detectors. The VCSEL drive signal output of the first node is electrically connected to the detector input of the second node.

Figure 3-4 shows a test example of the communication between these two Transpar-TR nodes [16]. At the top are the Ready-to-Receive signal for node 1 (Ready2Rx1) and its complement (Ready2Rx2) for node 2. The top set of receive-transmit labels refers to node 1 and the bottom to node 2. Here the time interval for receive and transmit is 400 ns. When the Ready2Rx1 is high, node 1 receives incoming data (Rxd Data 1) and address data (Rxd Address 1) at the clock rate transmitted by the previous node (Rxd Clock 1). In the first 400 ns period shown, there is no address match, so at the next available transmit interval, node 1 retransmits the data and address to node 2 at its own local clock rate. In this example, as before, there is no address

match at node 2 so it again retransmits the data and address at its own local clock rate to the next node.

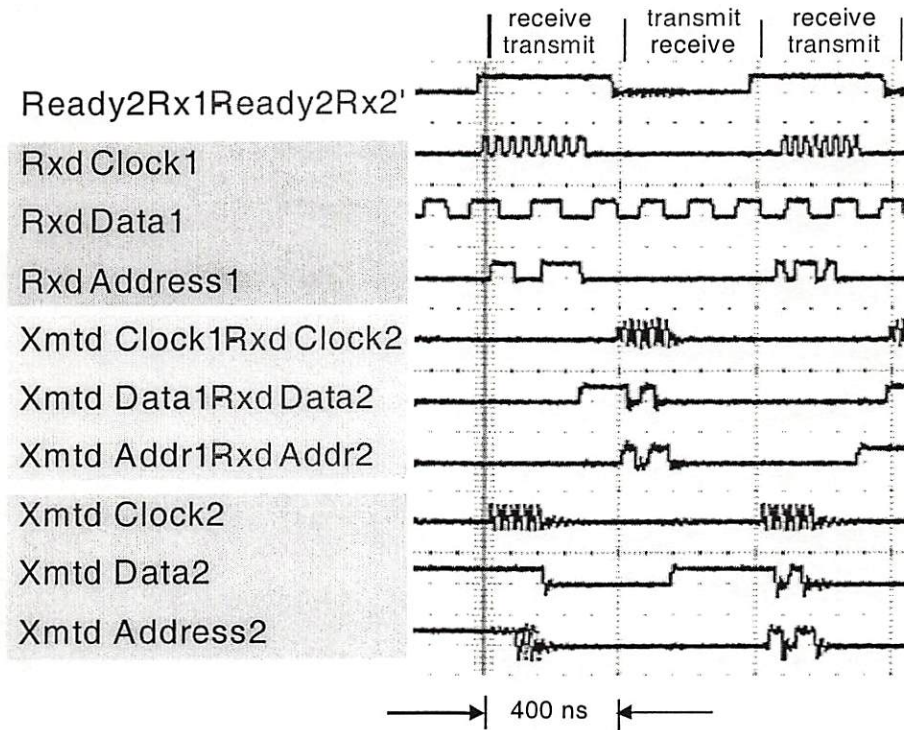


Figure 3-4. Two Transpar packet communications.

Chapter 4

Transpar Modular System Components and Experimental Setup

4.1 Printed Circuit Board (PCB)

A printed circuit board (PCB) is used to test circuit components and interconnect them electrically. We have designed a PCB to test the Transpar system in which the components can be individually characterized for the optimal operating parameters and system integration. The PCB is four layers and made with conventional FR-4 materials. The physical size of the board is 15 cm × 20 cm as shown in Fig. 4-1. The PCB includes basically three major components: a FPGA chip for system logic, VCSEL/MSM chip for optical I/O, and a receiver chip for amplification of detected optical signals. These components are well positioned on the board to reduce crosstalk and power noise. We will discuss the details of these components in the next sections.

Other on-board components include surface mount decoupling capacitors, potentiometers, SMA connectors, SRAM, and pin connectors. The capacitors are designed to minimize switching noise on the power supply lines for high-speed operation. 16 separate potentiometers are to control the output optical power of the VCSELs individually. Two different power inputs are for the FPGA and receiver. A

32-bit SRAM chip is included to store data from the FPGA. Four SMA connectors are included to monitor high-speed data outputs. A 68-pin connector is on board for the data acquisition (DAQ) and 32 digital I/O lines are used. Ribbon cables are used to read and apply all 16 channels with data-in and data-out simultaneously and a 34-pin connector is mounted. A host computer can be connected to DAQ and monitor the data input and output.

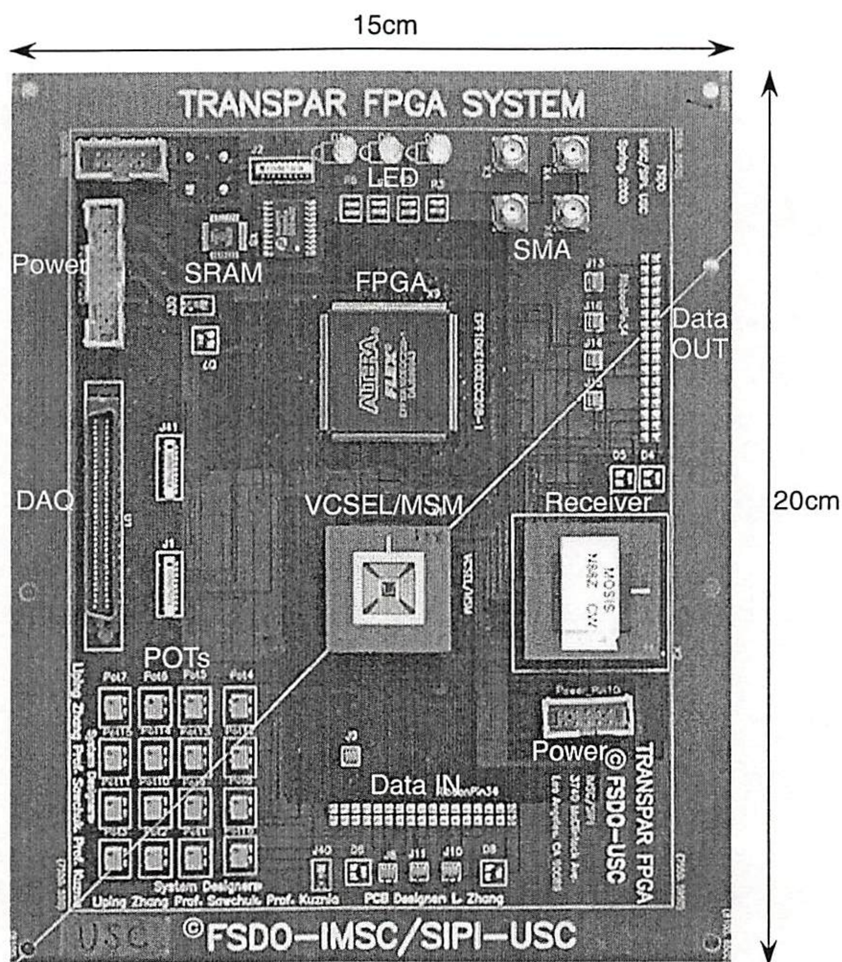


Figure 4-1. Transpar PCB.

4.2 VCSELs and MSM Detectors

Optical transmitters and receivers are the vital components in optical data communication. The requirements of optical transmitters are low power dissipation, high wall-plug efficiency (defined as the optical output relative to the electrical power), and stable operation with temperate change. In addition, the output power characteristics must be fairly uniform with spatial extent. VCSELs are one of the few light sources that satisfy the requirements and becoming widely available for high speed, short distance data communication systems. VCSELs have many advantages such as: low manufacturing costs, enhanced reliability, low threshold currents, low power consumption, high speed performance, circularly symmetric optical output and high density 2D array capability. 850nm VCSEL technology is accepted by the data communication industry [7]. The recent advent of VCSEL technology with longer and tunable wavelengths will soon be valuable in the telecommunication industry [3].

The desirable characteristics of photodiodes are low capacitance, short transit time, and high responsivity. Two different types of photodetectors are commonly used: MSM detector and PIN diode. We use MSM photodetector that is optimized at 850 nm wavelengths for Transpar system. PIN diode arrays are used for UTSi chips and are discussed later. The MSM photodetector is composed of back-to-back Schottky diodes that use an interdigitated metal electrode configuration on top of an active light absorption layer (GaAs). The interdigitated design minimizes parasitic resistance. The two adjacent metal electrodes are connected to upper or lower electrodes, respectively.

When biased during operation, either of the two electrodes could be chosen as cathode or anode. To manufacture the array of VCSELs and MSM detectors, the MSM is fabricated on a 1.5 μm epilayer of undoped GaAs grown on top of the VCSEL structure and the undoped GaAs layer is selectively removed from the regions where the active VCSELs are located [38].

We have chosen Honeywell VCSEL chip that was obtained through the George Mason University COOP program. The chip has 4 × 4 array of VCSELs with interleaved MSM photodetector arrays. The physical properties of VCSELs and MSM detectors are summarized in Table 4-1 and a cross-section of the Honeywell VCSEL/MSM detector is shown in Fig 4-2. Figure 4-3 shows the interleaved VCSEL/MSM array layout.

VCSEL		MSM detector	
Operating wavelength	850 μm	Responsivity	0.25 mA/mW
Beam divergent angle	15°	Dark current	< 1 μA@ 5 V
Optical power	>1 mW@ 10 mA	Bias voltage	> 0.22 V
Optical window size	15 μm	Detector size	75 μm x 75 μm
Threshold current	4 mA	Capacitance	< 0.5 pF
Pitch	250 μm	Pitch	250 μm

Table 4-1. Honeywell VCSEL/MSM characteristics.

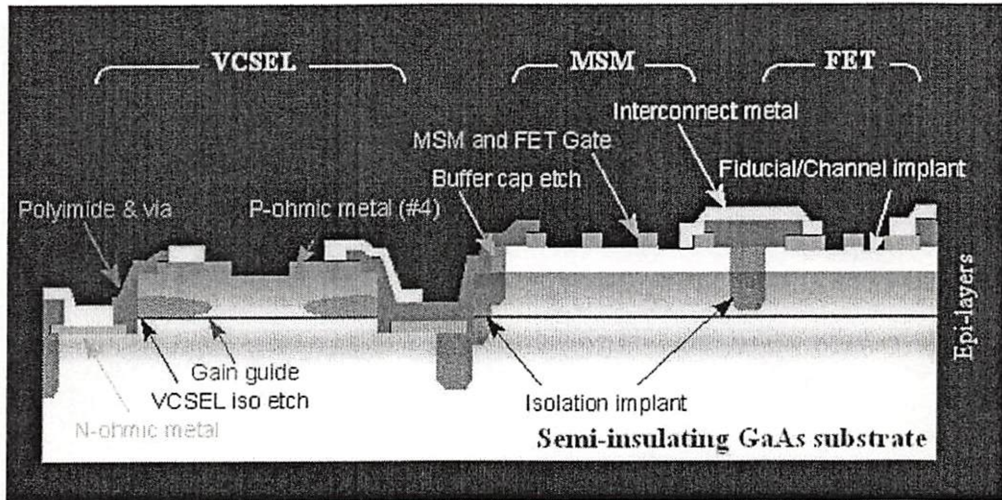


Figure 4-2. Cross-sectional view of Honeywell VCSEL/MSM chip.

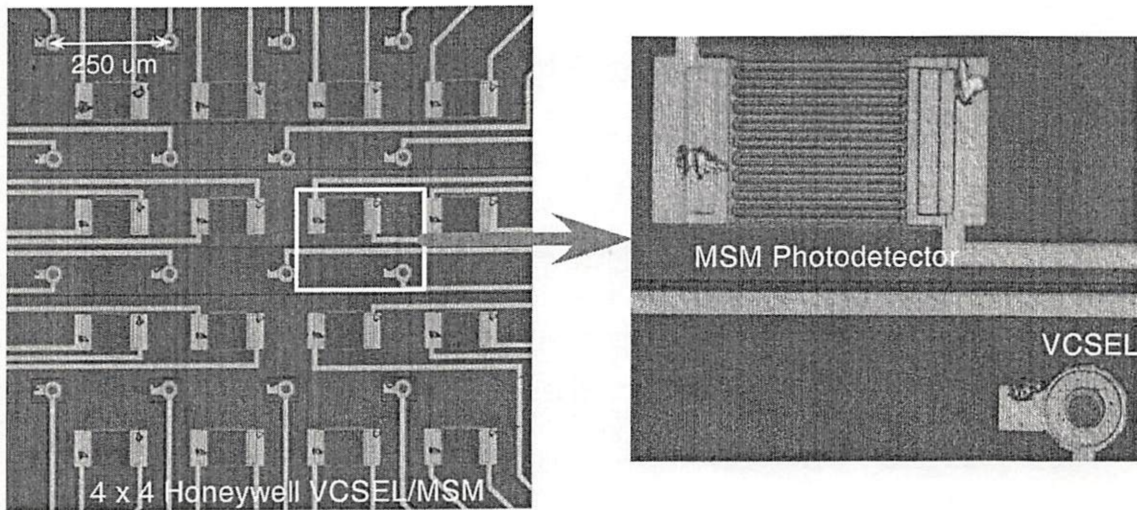


Figure 4-3. 4 × 4 array of Honeywell VCSEL/MSM photodetector array.

4.3 VCSEL Measurements

The Honeywell VCSEL output power as a function of current and voltage is shown in Fig. 4-4. We found experimentally that the impedance, output power, mode structure and frequency response of each VCSEL are closely interrelated and set the operation output power of the VCSEL to a minimum of 0.7 mW to a maximum of 1.3 mW for the highest frequency response (100 MHz). Higher power may also increase the effect of optical crosstalk to the neighbor detectors, thus it is important to determine an optimum optical power range. Crosstalk also can be produced by the reflection of VCSEL beams from the MSM detectors. To reduce these effects one might use anti-refection coated lenses.

The VCSEL output beam diameter δ can be calculated by

$$\delta = 2d \tan\frac{\theta}{2} + a, \tag{4-1}$$

where d is distance between VCSEL and detector, θ is VCSEL divergence angle (measured between its $1/e^2$ profile), and a is the aperture diameter. The divergence angle of the Honeywell VCSEL is 15° and the aperture diameter is 15 μm. This equation indicates that the distance between VCSEL and detector should be controlled to get the proper VCSEL output beam diameter. For example, δ should be less than the detector pitch that is 250 μm and the distance d should be less than 0.9 mm without any optical elements. However longer interconnection can be realized using optical elements for beam collimating and focusing in practical optical interconnection systems.

The impedance of each VCSEL is dependent on the drive frequency, and therefore the VCSEL output power depends on the modulation frequency. To adjust for these different output characteristics, Transpar includes on-board potentiometers that vary the series resistance of each VCSEL from 1 Ω to 100 Ω. The potentiometers can be controlled individually to get uniform optical power for 16 different VCSELs.

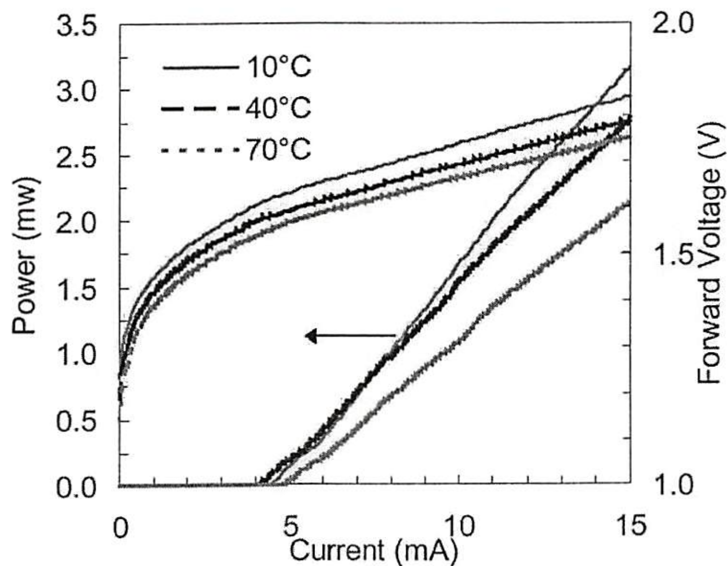


Figure 4-4. Honeywell VCSEL output power performance [69].

4.4 Transimpedance Amplifier (TIA) Receivers

A low-noise, high-sensitivity receiver is essential for reliable transmission of optical data. The optical receiver consists of a photodetector, which converts the incoming optical power into electrical current, followed by a high-gain, low noise TIA that converts the small photocurrent to a large voltage swing. The Transpar system uses

a TIA receiver array that receives sixteen parallel signals in the form of currents from the MSM photodetectors on the Honeywell VCSEL/MSM array chip and converts them into 16 parallel digital CMOS signals for input into the FPGA chip. The TIA chip is intended for use with MSM detectors to convert photodetected current signals into 5 V CMOS compatible signals. The TIA chip was designed by Bogdan Hoanca, fabricated by MOSIS using the AMI 1.2 μm process and is packaged in a 108 pin 12 × 12 PGA package. It also includes an array of 16 receivers for the detection of 16 parallel channels. The TIA is designed to meet the following specifications: low adjacent-channel crosstalk between small MSM signals (~ 10 μA), stable and wide bandwidth operation (100 Mbps), high transimpedance gain (> 50 kΩ), and ability to operate in a printed circuit board environment with large parasitic capacitance.

In order to find the optimal solution, the TIA receiver chip contained four distinct receiver designs. Through testing we found the best receiver design (shown in Fig. 4-5) that meets the above requirements. This design uses a preamplifier stage with multistage feedback to achieve high gain, followed by another gain stage and the digital output. The receiver chip is placed on a PCB as close as possible to the MSM chip and electrical connections should be made as short as possible between the output pins of the MSMs and chip and the receiver input pins. We have used a large number of separate power supply pins to ensure good separation between the analog and the digital domains on chip. To reduce the number of power supplies required, some of the pins can be connected together on the PCB, or even better at the power supply.

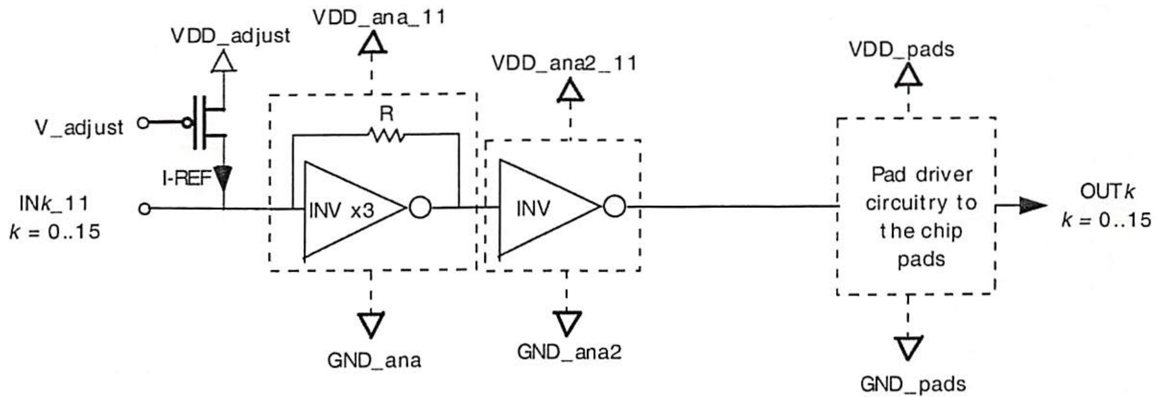


Figure 4-5. Block diagram of the TIA used in our experiments.

4.5 Field Programmable Gate Array (FPGA)

One limitation in optoelectronic systems is the need to design custom optoelectronic integrated circuits for each different application. This limitation can be addressed by merging a FPGA. FPGA is a device that can implement reconfigurable hardware and rapidly adapt to changing requirements and was emerged as a new technology for the implementation of digital logic circuits during the mid 1980's. FPGAs with optical I/O can have their functionality specified in the field by means of downloading a control-bit steam and can be used in a wide range of application, such as optical signal processing, optical image processing, and optical interconnects [67].

For Transpar, the design of the FPGA was synthesized from VHDL using the Maxplus II software package. The device operates at up to 250 MHz and has multi-volt I/O pins that can drive or be driven by 2.5 V, 3.3 V, or 5.0 V devices. We selected 2.5 V output in order to drive the VCSELs and found the FPGA can directly drive about 10

mA input current to the VCSELs [Fig. 4-6], so that the VCSEL output optical power can be about 1 mW.

To implement Transpar-TR, the FPGAs are programmed to implement a spatially parallel packet of a token-ring protocol. Our test system used an Altera EPF10K100EQC to drive 16 VCSELs in parallel. In Flex 10KE Devices 100 K of 250 K gates typically can be used, 50 K RAM and 250 MHz I/O. Also they have independent internal logic V_{CC} and I/O V_{CC} to allow direct drive of VCSELs. In testing the optical inputs and outputs of Transpar we use a 15-bit pseudo random string that is generated by the FPGA to drive the VCSELs on the Transpar board.

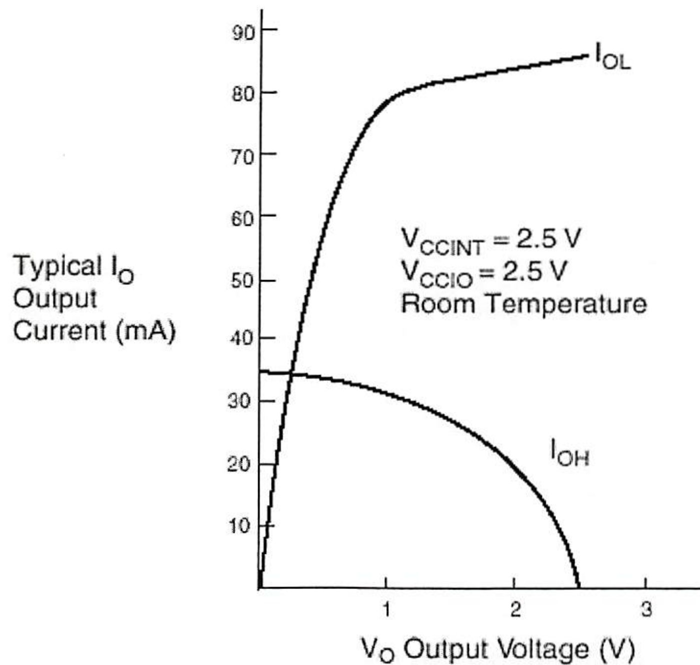


Figure 4-6. FPGA operation voltage and its current output.

4.6. Power Setup

We need six separate power supplies for receiver array and MSM detector array. We supply 0.35 V for MSM bias; 4.93 V for V_{PAD} (power for output pins); 4.95 V for $V_{dd\text{-}ana}$ (power for the first stage amplifier); 5.06 V for $V_{dd\text{-}ana2}$ (power for the second stage amplifier); 4.91 V for $V_{dd\text{-}adjust}$ (power for the threshold adjusting circuitry); 3.68V for adjust (threshold adjustment input).

The FPGA utilizes two independent voltages: V_{CCINT} = 2.5 V for internal logic and V_{CCIO} = 2.5 V for input and output operations. Since the FPGA is digital, there is an acceptable range of adjustment available on V_{CCIO}. Therefore, we can tune the VCSEL drive voltage to suit our optical link requirements. For Honeywell VCSELs, we found that V_{CCIO} = 2.5 V results in a VCSEL drive current of 10 mA and optical power of 1 mW. We supply 3.3 V for the Altera EPC2 that can store configuration data for SRAM-based FLEX device. Table 4-2 summarizes the power supplies for the Transpar system.

Power	Voltage	Power	Voltage
FPGA V_{CCIO}	2.5 V	Oscillator	5 V
FPGA V_{CCINT}	2.5 V	MSM bias	0.2 ~ 0.4 V
EPC V_{CC}	3.3 V	Receiver bias	~ 5 V
Pull-up resistors	5 V	Threshold adjustment	3 V

Table 4-2. Power setup for the Transpar system.

Chapter 5

Free Space Optical Interconnection Systems

5.1 Introduction

In this chapter we will present free-space optical interconnection systems using bulk refractive macrolenses and DOEs. Free-space interconnects have no waveguide medium such as fiber or polymers in the optical path and the interconnection efficiency is relatively high in short-distance optical interconnections. They can offer high bandwidth but poor tolerance to misalignment. The problem of misalignment is related to the link distance, and channel density, and these factors must be addressed in the system point of view.

Comparing DOEs and macrolenses, DOEs have shorter link distance because of the diffraction limit while macrolenses offer maximum link distance with high efficiency but are aberration-limited [14]. DOE performance strongly depends on the wavelength and is mostly used for single wavelength applications. DOEs also can be combined with refractive lens to correct for the chromatic aberration. The choice of which types of lens depends on the system and the parameters. In the packaging point of view DOEs have advantages because of their small volume and the possibility of directly integrating them with light source arrays for beam collimating and focusing. The basic setup for interconnections with DOEs and refractive lenses is shown in Fig. 5-1.

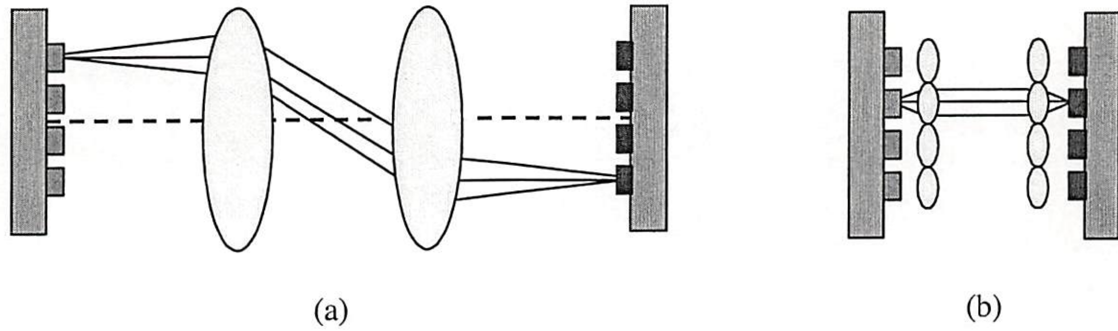


Figure 5-1 Free-space optical interconnection using (a) macrolenses, (b) DOEs.

A refractive lens is characterized by a refractive index $n(\lambda)$ and the two-lens radii c_1 and c_2. The focal length f_r of a refractive lens is

$$f_r(\lambda) = \frac{1}{n(\lambda)-1}\left(\frac{1}{c_1 - c_2}\right). \tag{5-1}$$

For the case of rotationally symmetric DOE lens, at an arbitrary position (x, y) the phase function can be described by

$$\Phi(x, y) = 2\pi(a_2 r^2 + a_4 r^4 + \ldots), \tag{5-2}$$

where r is the radial coordinate in the plane of the diffractive lens. The optical power of the diffractive lens in the mth diffraction order is then given by

$$\frac{1}{f_0} = -2a_2\lambda_0 m, \tag{5-3}$$

where λ_0 is the design wavelength and f_0 is the design focal length. Then the focal length of a diffractive lens is

$$f_d(\lambda) = f_0 \frac{\lambda_0}{\lambda}. \tag{5-4}$$

The dispersion of a refractive lens can be described by the Abbe number v_r, defined as,

$$v_r = \frac{n(\lambda_1) - 1}{n(\lambda_2) - n(\lambda_3)}. \tag{5-5}$$

In the case of diffractive lens, the Abbe number becomes

$$v_d = \frac{\lambda_1}{\lambda_2 - \lambda_3}, \tag{5-6}$$

where $\lambda_3 > \lambda_1 > \lambda_2$. From these Abbe numbers we can calculate the dispersion and a small Abbe number corresponds to a strong dispersion. For longer wavelengths (λ = 600 ~ 1000 nm), the dispersion of a DOE is typically about 20 times higher than the dispersion of refractive lenses [14]. In order to test the relative performance of diffractive lenses, we set up two different systems described in the next sections.

5.2 Free Space Optical interconnection Experiment Setup: Refractive Lens

Our first interconnection test system uses free space interconnects based on bulk lenses with focal length f = 60 mm. The experimental setup is shown in Fig. 5-2 and Fig. 5-3. Two identical boards were manufactured and set up on *xyz* stages. The distance between two boards is 24 cm. To generate experimental data we used either an FPGA or Tektronix data generator. We measured the optical power output just after the VCSEL source array and just before the detector array. We found that 91 % of the VCSEL power arrives at the detector arrays. The divergence angle of each VCSEL

beam was measured at 15° for $1/e^2$ intensity profile as expected. We used 2 cm diameter Melles Griot doublet lenses with 6 cm focal length and an F/# of 3 to make sure we capture most of the optical power from the VCSELs. These lenses have anti-reflection coating and less than 0.4 % reflectivity at 850 nm.

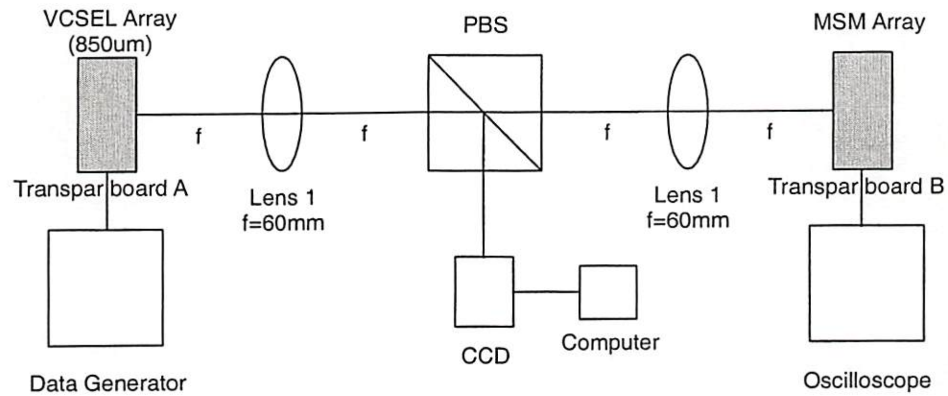


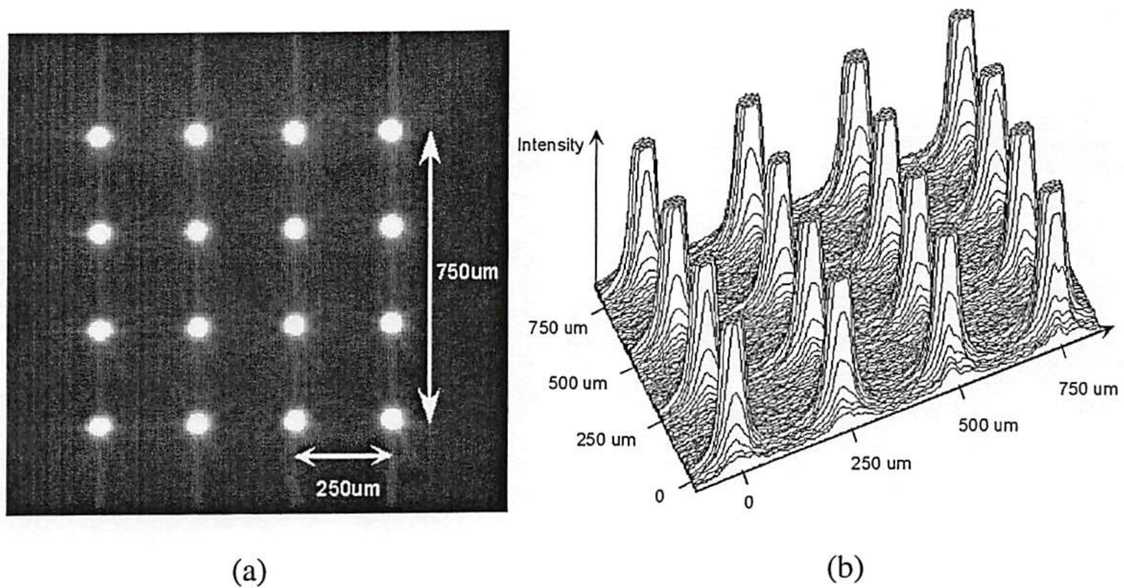
Figure 5-2. Setup for free space interconnection using bulk lenses.

Figure 5-3. Picture of free-space optical interconnection experiment setup.

5.3 Optical Alignment

We align the optical system making sure that the four middle VCSEL beams out of 16 VCSELs hit the center of the corresponding middle detectors, and that the optical axis is on the center of the detector arrays. This is done using CCD camera observing the system through a polarizing beam splitter (PBS) as shown in Fig. 5-3. The beams from the VCSEL arrays are detected as an image at the detector arrays. To match the inversion of the imaging system and the interlaced detector arrays, the receiver board is rotated at 90° compared to the transmitter board.

The optical power of the VCSEL is set to 0.8 mW ~ 1 mW on the detectors and the range of the applied voltage for the Transpar board (Transpar board A in Figs. 5-2, 5-3) is 2.5 V to 2.7 V. To compensate for the non-uniformity of the VCSEL output we adjusted 16 on-board potentiometers to get uniform optical power outputs. The adjustment range is variable from 1 Ω to 100 Ω. We carefully adjusted the output beam uniformity as monitored by a CCD camera and measured the power change by a computer program, NIH Image. The optical power outputs from the VCSEL array have a roughly uniform intensity at the detector plane as shown in Fig. 5-4.



(a) (b)

Figure 5-4. 4 × 4 VCSEL output power uniformity. (a) CCD output, (b) the output profile.

5.4 Test Results

We used a Tektronix DG2020A data generator to modulate 16 VCSELs simultaneously. We measured the output of the TIA receiver and obtained an eye diagram as shown in Fig. 5-5 where signal 1 is the ground and signal 2 and 3 are the eye diagrams of two different detector outputs with different pseudo-random patterns generated by DG2020A. The eye diagram shows the system is operating at 100 Mbps and the open eyes indicate wideband operation with low noise and intersymbol interference (ISI). When we increase the modulation frequency over 100 Mbps we observed the eyes started to close and they closed completely at 120 Mbps.

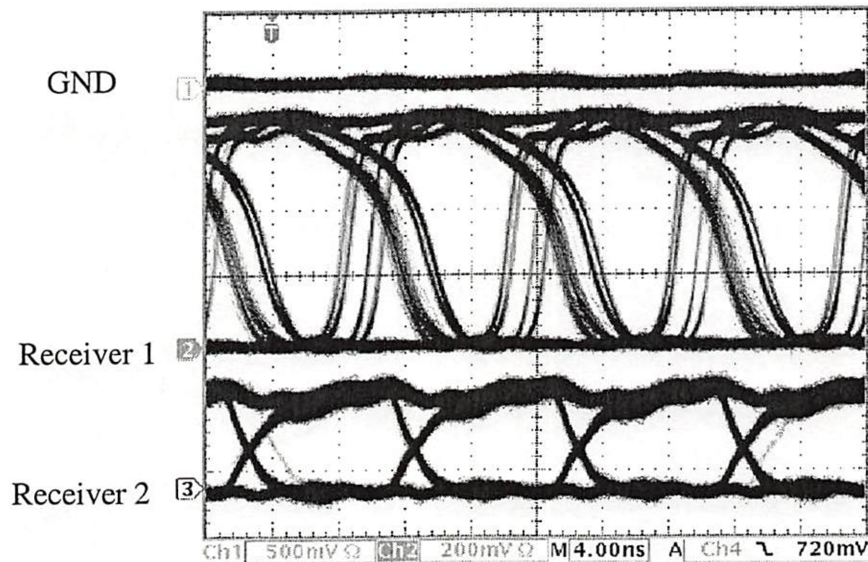


Figure 5-5. Eye diagrams at 100 Mbps.

5.5 Diffractive Optical Elements (DOEs)

DOEs are one of the key elements for beam steering in free-space optical interconnections and can offer an important role in optically interconnected multichip modules (MCMs) and other optoelectronic devices [14]. DOEs generally have much less weight and occupy less volume than their refractive or reflective counterparts. One limitation of DOEs is that because they are based on diffraction; they are highly dispersive and best used with optical systems using monochromatic or narrowband light. DOEs can be fabricated by microelectronic lithography technology, and hence have a great potential for low cost, high yield, and mass production applications. Optical systems with DOEs may offer advantages over bulk refractive optics in terms of cost and

packaging. DOEs can also be directly integrated with VCSELs for beam collimating and focusing [42].

We have designed four different 8×8 DOEs that have manufactured by Digital Optics Corporation through the Joint Optoelectronics Project (JOP). The four different types of DOEs, A, B, C, and D have different focal lengths which are 407 μm, 500 μm, 672 μm and 831 μm each. The physical size of each DOE is 1.416 cm × 1.416 cm and the aperture is 177 μm × 177 μm. The diagonal distance between each DOE is 250 μm ($\sqrt{2} \times 177$ μm), which is equal to the pitch of the Honeywell VCSEL/MSM array. The coupling efficiencies that are defined as the ratio of output optical power over input optical power are A: 68 %, B: 57 %, C: 40 %, D: 34 %. Four different DOEs are on a single transparent substrate. Through various tests on the coupling efficiency we chose type A DOE for the best performance in our experiments. Figure 5-6 (a) shows a Scanning Electron Microscope (SEM) picture of type A DOE (a) and CCD picture of a type B DOE (b).

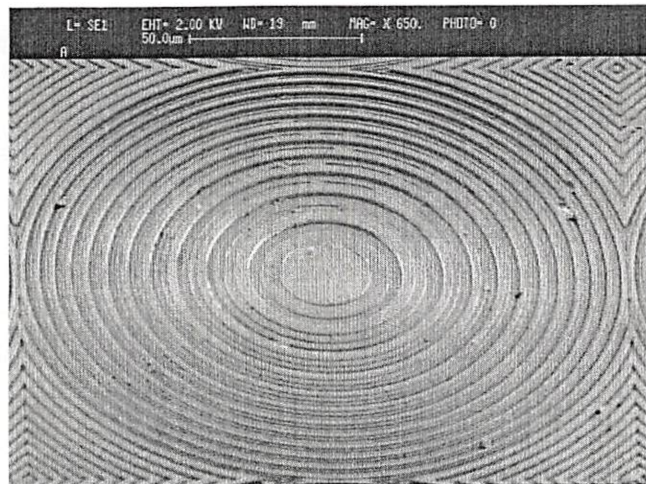
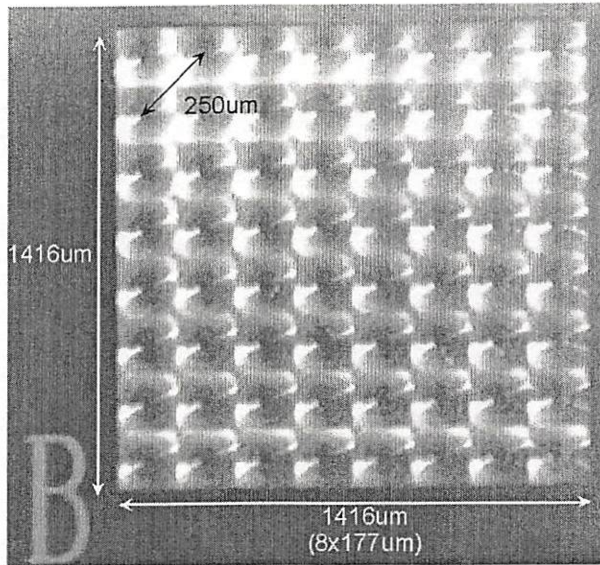


Figure 5-6. DOE. (a) SEM picture of type A DOE.



(b)

Figure 5-6 (cont.). (b) 8 × 8 array of type B DOE.

Figure 5-7 shows the DOE experiment setup. We attach DOE type A to a VCSEL/MSM chip using epoxy and used a *xyz* stage to get the correct distance between DOEs and VCSELs. The applied voltage was 2.50 V at all 16 VCSELs. The total applied current was 20.54 mA and the corresponding total optical power was 6.01 mW summed over all 16 VCSELs. First we observed the *x* and *y* position through CCD camera.

Figure 5-8 (a) shows that the VCSEL beams have uniformly distributed intensity over each DOE, which means that the DOEs and VCSELs are aligned. We then adjusted the *z* position to collimate the beams on the detectors. Through a CCD camera that is set on constant sensitivity, we observed the beam profile change and determined the focal length position [Fig. 5-8 (b)].

The maximum distance between DOEs is determined by L that is defined by

$$L = \frac{2\pi\omega_a^2}{\lambda} \tag{5-7}$$

where ω_a is the beam-waist radius in air (about 43 μm with f = 407 μm DOE). Substituting these values in Eq. 5-7 give the maximum distance for the interconnection using DOEs is at approximately 1.4 cm.

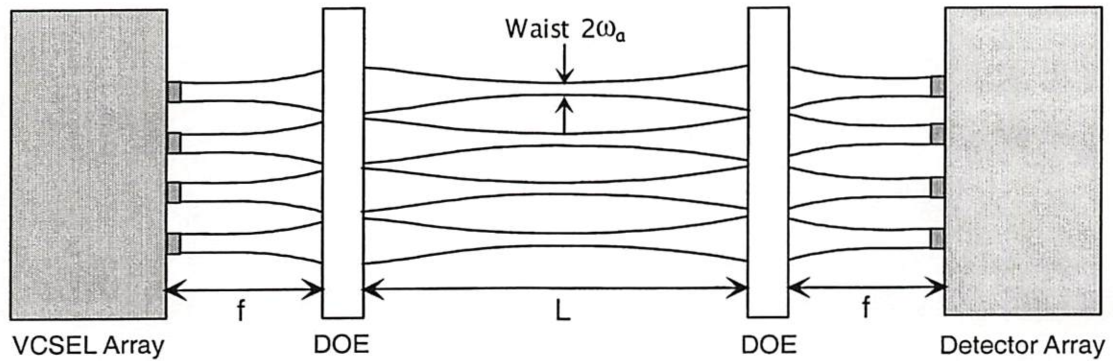


Figure 5-7. Interconnection setup using DOEs.

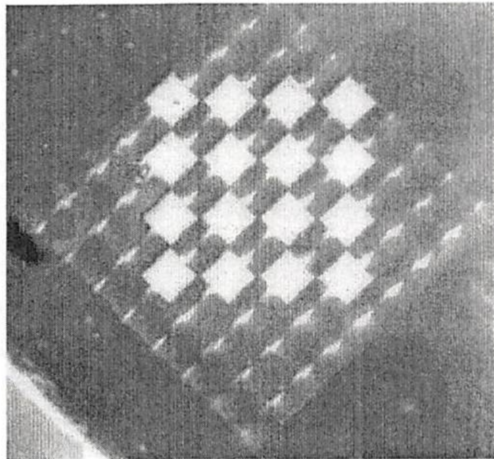
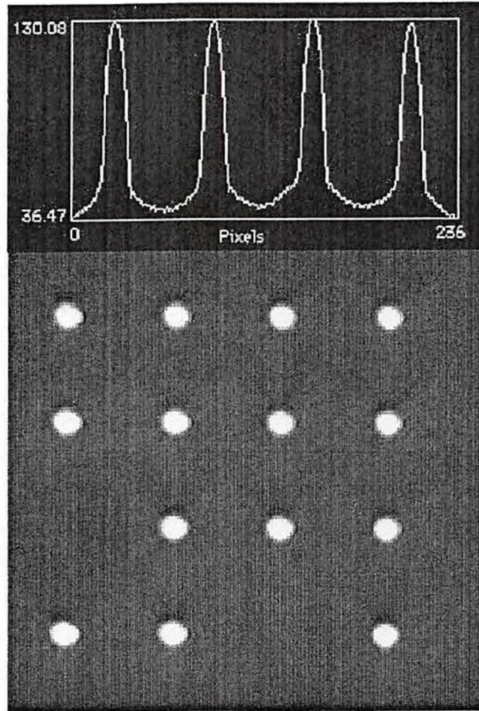


Figure 5.8. DOE and VCSEL alignment. (a) The VCSEL beams after passing through the DOEs.



(b)

Figure 5.8 (cont.). (b) Collimated VCSEL beam and the intensity profile for the first row of the VCSEL array.

Since the DOEs are small and have a short focal length it is very difficult to perform *x*-*y*-*z* alignment of the DOEs with the VCSEL array. We did this adjustment of DOEs on VCSEL chip by observing the output beam's power and size. The experimental setup for the measurement is shown in Fig. 5-9. Figure 5-10 shows the optical power and the beam shapes with distance between VCSELs and DOEs. For the experiment we use the type A DOE that has focal length f = 407 μm. To observe the

output beam through DOE array we used another lens with $f = 6$ cm that is focused on the DOE array with CCD camera.

The output optical power is measured as a function of distance d between VCSELs and DOEs as shown in Fig. 5-9. Figure 5-10 shows that the measured power reaches a maximum at approximately 405 μm, which is close to the focal length of type A DOE. The pictures of the output beams in Fig. 5-10 are taken with CCD camera. They show that the size of the VCSEL becomes smaller as the distance increases. This occurs because the output power is getting weaker and spreading out as the distance d gets longer. In the range of 400 μm to 415 μm the beam size changes only slightly with distance. This occurs because the beam waist changes slowly near the focal length. Also, the uniform circular shape of the output beam shows the correct x-y position on VCSEL array.

From these experiments we conclude that we can align the DOE with the VCSELs using a CCD camera based on the output power profile and the beam size. Near the focal length the output power is a maximum and the beam size changes little with distance. After performing this alignment, the DOE are packaged to the VCSEL chip using epoxy.

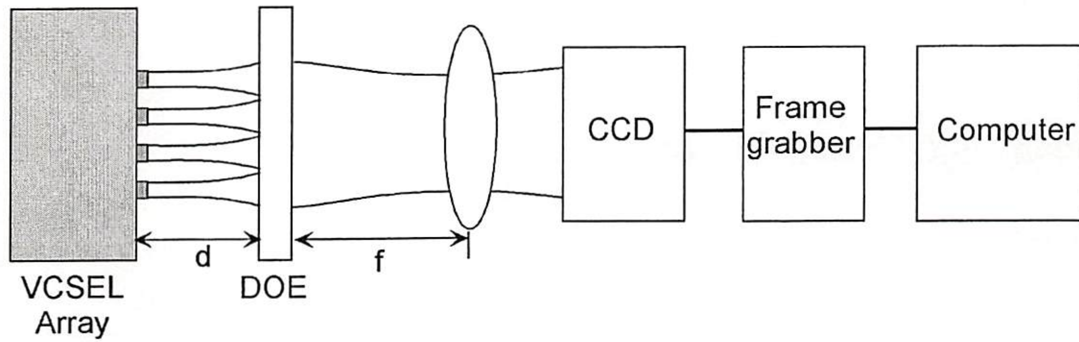


Figure 5-9. Experimental setup for Fig. 5-10.

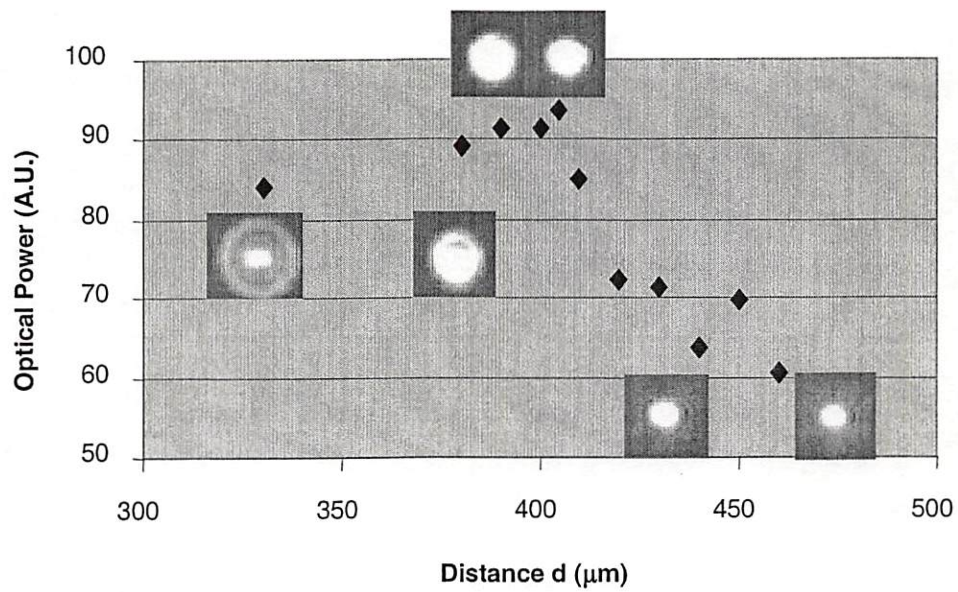


Figure 5-10. Power and VCSEL changes along z-direction.

Chapter 6

Fiber Image Guides (FIGs)

6.1 FIGs

In this chapter we discuss the use of fiber image guides (FIGs) to transfer 2D optical data packets as an alternative to free-space interconnections. Free-space optical interconnects are very useful for short-distance 2D parallel interconnects but they are not suitable for multi-channel interconnects for long-distance (over 1 m) because of the beam spreading and the difficulty of alignment. FIGs are a tightly packed array of thousands of optical fibers, and are capable of 2D parallel image transmission with more flexible alignment and packaging than free-space alternatives [1], [5], [28], [41]. Figure 6-1 shows one example of the use of FIGs.

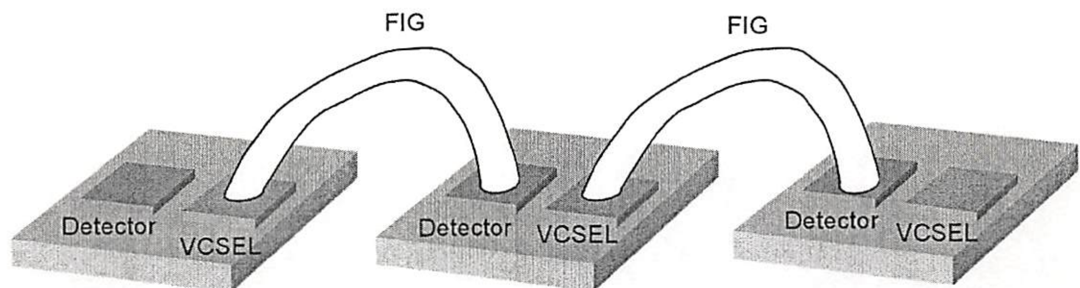


Figure 6-1. FIG interconnects.

The process for making FIGs is based on the acid-soluble glass (ASG) technology [6]. Individual fibers of the FIGs are fabricated using a rod-in-tube method. In this technique, a solid core glass is surrounded by a cladding tube to create the individual waveguide structure. The cladding is then surrounded by a second tube ASG. This glass system is drawn down into a single monofiber that is stacked into a hexagonal array. This array is further drawn down into a multirod. A second stacking and drawing operation follows to create a multi-multi-rod. Throughout these draws the glasses maintain their shape, preserve the core-cladding boundaries, and reduce any manufacturing variance in the original monofiber. Prior to placing the bundles in an acid bath the ends of each bundle are encased in wax. The acid dissolves the ASG in the middle of the bundles, whereas the wax protects the ASG at the ends. After the wax is removed the central part of each fiber is free to flex. Figure 6-2 shows the detailed structure of the FIG at end points where the background material (ASG) fills the space between the cladding.

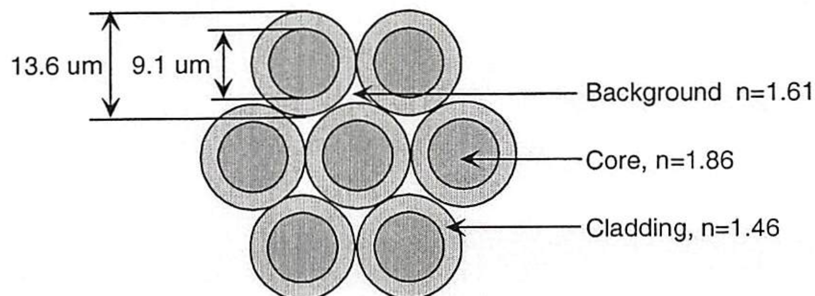


Figure 6-2. FIGs structure.

Figure 6-3 shows the construction of typical FIGs. The FIGs we used in the experiment are produced at Schott Optovance, Inc. Their density is order of 10^4 /mm^2 and each core fiber is a step index multi-mode fiber. The FIGs used in our experiment consist of 15,379 core fibers, each with a 9.1 μm core diameter and 13.6 μm pitch. The numerical aperture (NA) is 1.0 and the attenuation level is less than 0.4 dB/m in the wavelength range from 700 nm ~ 1100 nm [68]. The optical attenuation with lower NA is less; it is 0.1 dB/m with a 0.25 NA FIGs. At the end point of the FIGs the background material has index of refraction 1.61. As mentioned earlier, the ASG is removed from most of the FIG length except the end points that have 2.5 cm length. The properties of FIGs used in our experiments are summarized in Table 6-1.

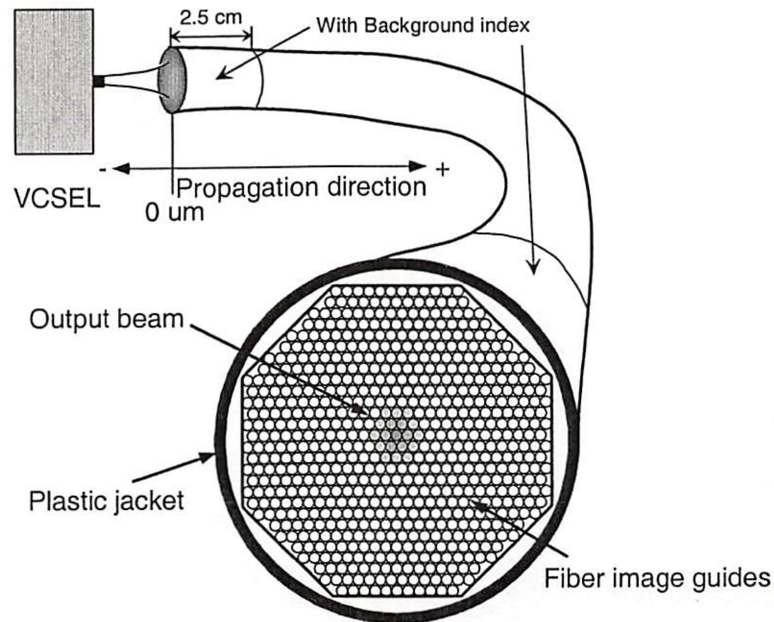


Figure 6-3. FIGs.

FIG diameter	1.64 mm
Center-to-center spacing	13.6 μm
Core diameter	9.1 μm
Numerical aperture	1.0
Attenuation	< 0.4 dB/m
Lengths	0.3 m
Bandwidth	> 1 GHz
Indices of refraction	Core: 1.86 Background (ASG): 1.61 Clad: 1.46

Table 6-1. Characteristics of Schott FIGs.

The individual fiber elements of the FIG have beam characteristics that can be calculated by the normalized frequency V defined as

$$V = \frac{2\pi a}{\lambda} NA = \frac{2\pi a}{\lambda} \sqrt{n_1^2 - n_2^2}, \tag{6-1}$$

where a is the fiber radius, λ is the free-space wavelength, n_1 is the core refractive index, and n_2 is the cladding refractive index. For the Schott FIGs, we have a = 9.1 μm, λ = 0.85 μm, n_1 = 1.86, n_2 =1.46, and a NA of 1. These parameters result in a V number of 77. This high V number implies that most of the optical power in the waveguide propagation is carried in the core [49].

6.2 FIG Experiments

The experimental setup is shown in Figs. 6-4 and 6-5. We interconnect two test boards by mounting each end of the FIGs close to a VCSEL array and a detector array. We mounted two Transpar boards and FIGs on *xyz* stages so that we could perform the experiments in many flexible alignment situations. When we mount the FIGs, we use conventional fiber connector to fix the ends using epoxy for convenience of optical alignments. We make sure that end face of FIG is parallel to VCSEL-MSM plane and VCSEL-MSM device is entirely contained in the FIG aperture. Compared to the free-space system, it is not necessary to rotate or shift the boards physically in the FIG system because the adjustment is easily done by moving the ends of the FIGs at each.

The distance between each VCSEL/detector and FIGs is critical in terms of optical power and beam collimation. There are three different distance variables in our setup. The distance between the top of the VCSELs and the input end of the FIG is given by d_{in}; the distance between the output end of the FIG and the detector is d_{out}; and the distance along the length of the FIG from the input end is given by d_{FIG} as shown in Fig. 6-5.

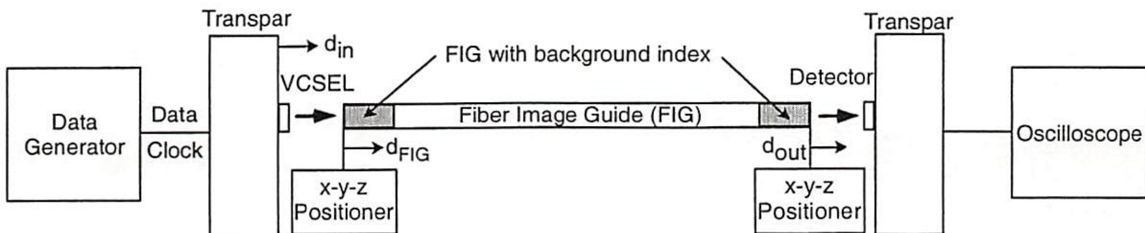


Figure 6-4. FIGs experimental setup.

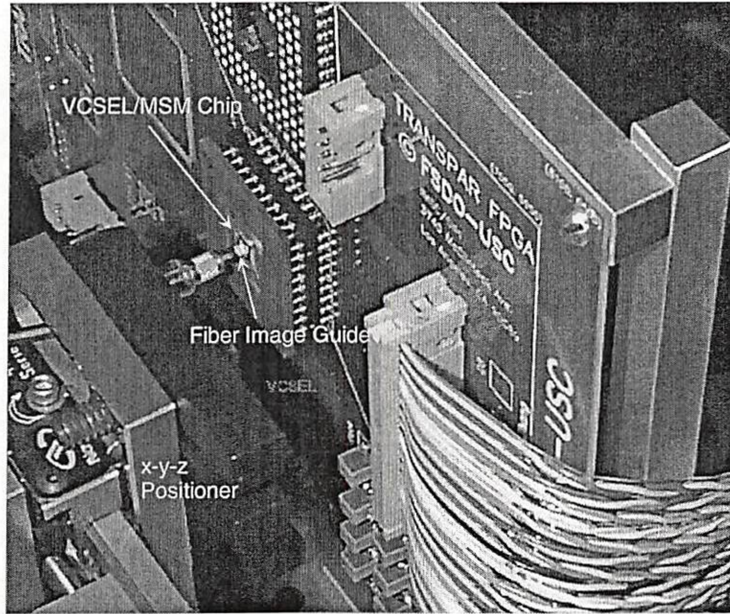


Figure 6-5. Picture of FIGs setup on Transpar.

Figure 6-6 is a photo of the output plane of the FIG with d_{in} ~ 0. It clearly shows details of the VCSEL/MSM array and the light output of all 16 VCSELs. We first measured the optical power as a function of d_{out} distance for d_{in} ~ 0 as shown in Fig. 6-7. In this experiments the FIG was moved into nearly touch the VCSEL array. This measurement was taken by activating one VCSEL, and recording the FIG output power for every 100 μm distance (d_{out}). In this case the optical power decreases slowly as d_{out} increases.

However, the output power decreases rapidly as d_{in} increases. For example we get only 13 % of VCSEL original output power when we measure it through 0.3 m FIGs at 2.5 V, 10 MHz with coupling distance d_{in} = 100 μm. This result implies that the optical

power loss occurs much between VCSELs and FIGs. We will investigate the optical profile along d_{in} in the next Section.

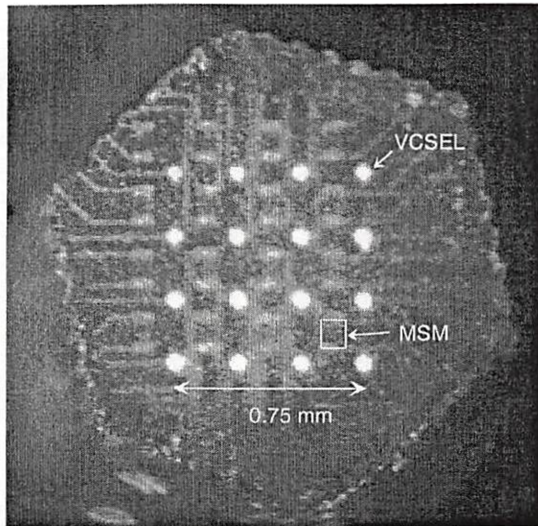


Figure 6-6. FIG output image of Honeywell VCSEL-MSM chip.

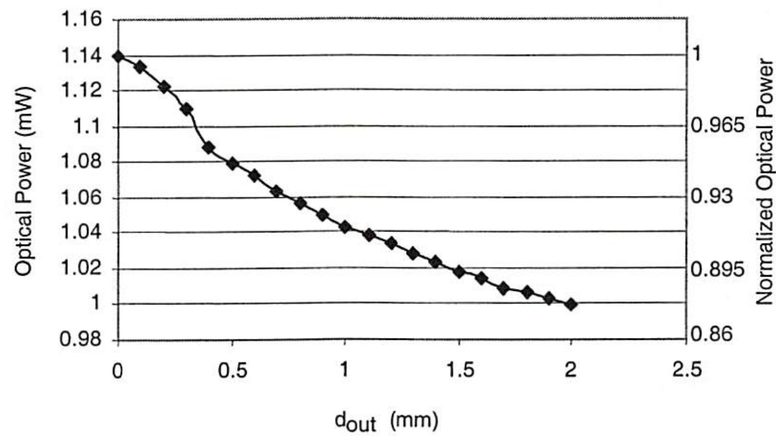


Figure 6-7. Optical power output through 0.3 m FIGs at various d_{out} for $d_{in} = 0$.

To optimize the interconnection efficiency it is important to match the optical spot size to the detector size. The MSM detector size is about 75 μm × 75 μm, so we need the optical spot size to be less than 75 μm diameter. We observed the spot using CCD camera directly from the output of FIGs [Fig. 6-8]. The output spot size is well defined and about less than 75 μm diameter when the coupling distance is less than 100 μm.

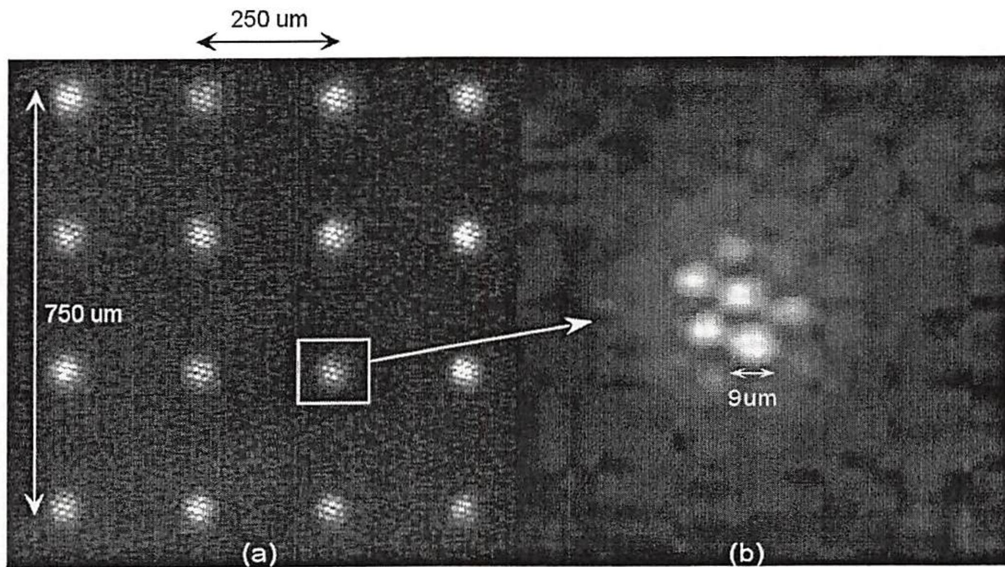


Figure 6-8. (a) 4 x 4 VCSEL guided image output of 0.3 m FIGs for $d_{in} = 0$, (b) a close-up image of one of the VCSELs.

The maximum distance without significant power loss (less than 10 %) on the detector array can be calculated from

$$d_{\max} = \frac{\delta - a}{2\tan\frac{\theta}{2}}, \tag{6-2}$$

where d_{max} is the maximum distance between FIGs and detector (shown in Fig. 6-9), θ is VCSEL divergence angle, and a is the output VCSEL beam diameter. When d_{in} = 0 μm the output beam size of VCSEL through the FIGs is about 36 μm (= a), θ = 15°, and δ = 75 μm (the detector size), then Eq. 6-2 gives the maximum distance d_{max} ~ 148 μm.

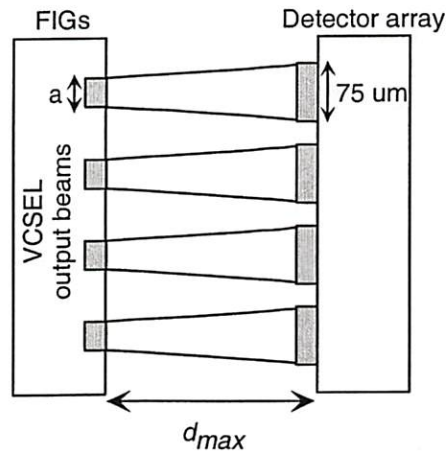


Figure 6-9. The maximum distance between FIGs and detectors.

6.3 VCSEL Output Uniformity

In an optical transmission or interconnection system it is highly desirable to obtain a uniform power distribution on the detectors. This power uniformity allows the receiver arrays to have a common decision level and eliminates the need to adjust each individual VCSEL channel. Since FIGs transfer images through array of fibers, the optical output and effective attenuation may vary depending on the launch position of

VCSEL light into the fiber. In this section we discuss the variation of VCSEL output power as a function of the launch positions.

We performed propagation tests for two different alignment positions as shown in Fig. 6-10. Figure 6-10 (a) shows the VCSEL launch position located at the core fiber center and Fig. 6-10 (b) is the background center position (both marked with ×). The optical input tends to spread out with propagation, and is distributed over several core fibers. The output also depends on launch position, producing different optical power outputs at the receiving ends, and different effective insertion losses. In general, the field coupled into cladding area is diffused and attenuated, and gives relatively low power output compared to power is conveyed mostly through adjacent core fibers.

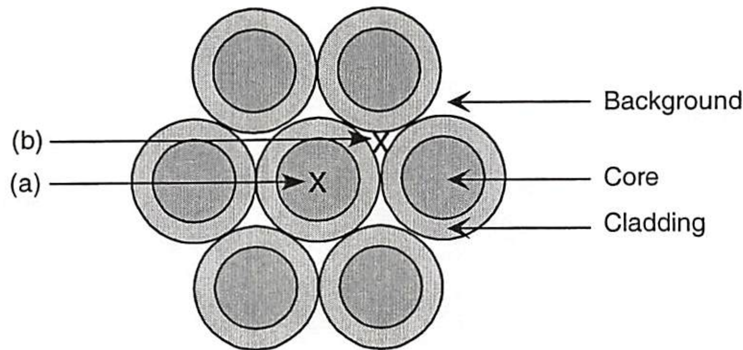


Figure 6-10. Launch positions (a) core center position, (b) background center position.

Because the VCSELs have a divergence angle that is 15°, shorter distances produce smaller beam size, thus the coupling distance d_{in} between VCSEL array and the FIGs is an important factor. Figure 6-11 shows different output beam profiles as a

function of d_{in} for two different VCSEL positions, (a) and (b) with 1.6 V applied voltage on the VCSEL. The pictures are taken at the receiving end of the FIG with $d_{out} \sim 0$. From these measurements we conclude that the input beam size and its position are critical to get a uniform output power.

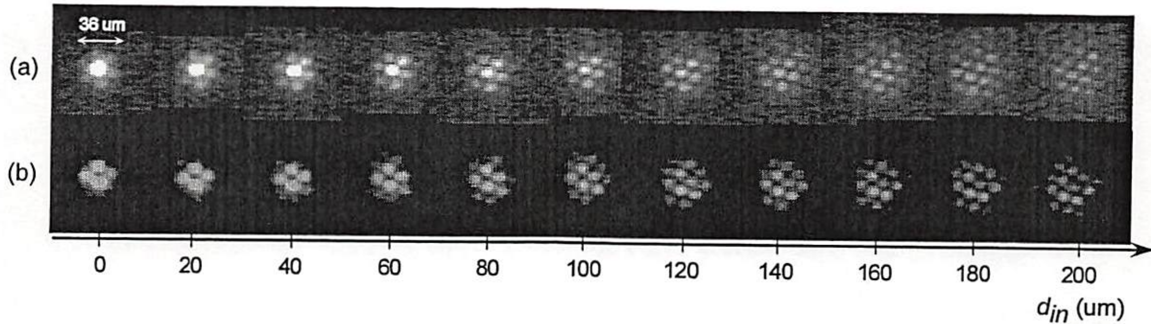


Figure 6-11. VCSEL output as a function of different d_{in}. The top row is for launch position (a) core, and the bottom row is for launch position (b), background center launch position.

6.4 Test Results

We have measured the optical power coupling as a function of distance between the FIGs and VCSELs, d_{in}. In these experiments, we measured the output power at the end of 0.3 m FIGs with $d_{out} \sim 0$ using a Newport optical power meter Model 835 and detector Model 818-SL. The bias voltages are 2.5 V for VCSELs. The optical power output results are shown in Fig. 6-12. The pictures of the FIGs output in Fig. 6-12 were taken for a coupling distance d_{in} of 50 μm. The core center launch position gives a much

larger power output than for the background center case when $d_{in} < 50$ μm. The optical power detector has active area 1 cm^2 and the area covers the whole area of the FIGs. More accurate measurement may need a detector that has a comparable active area with the output beam size.

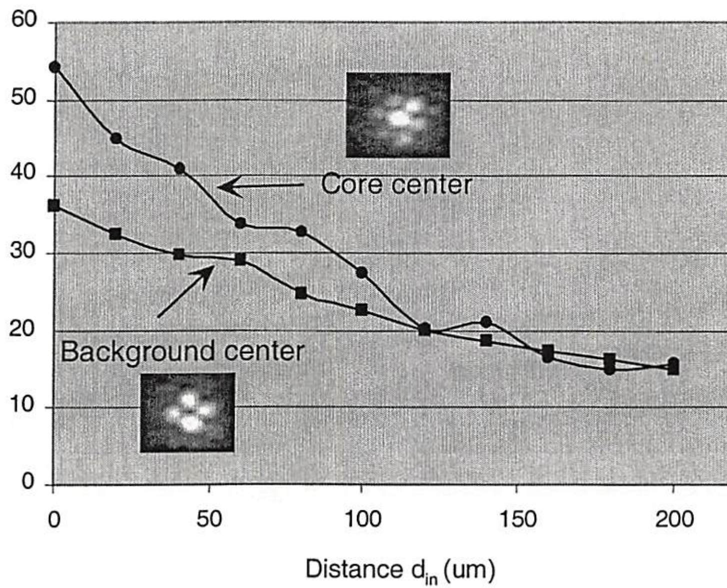
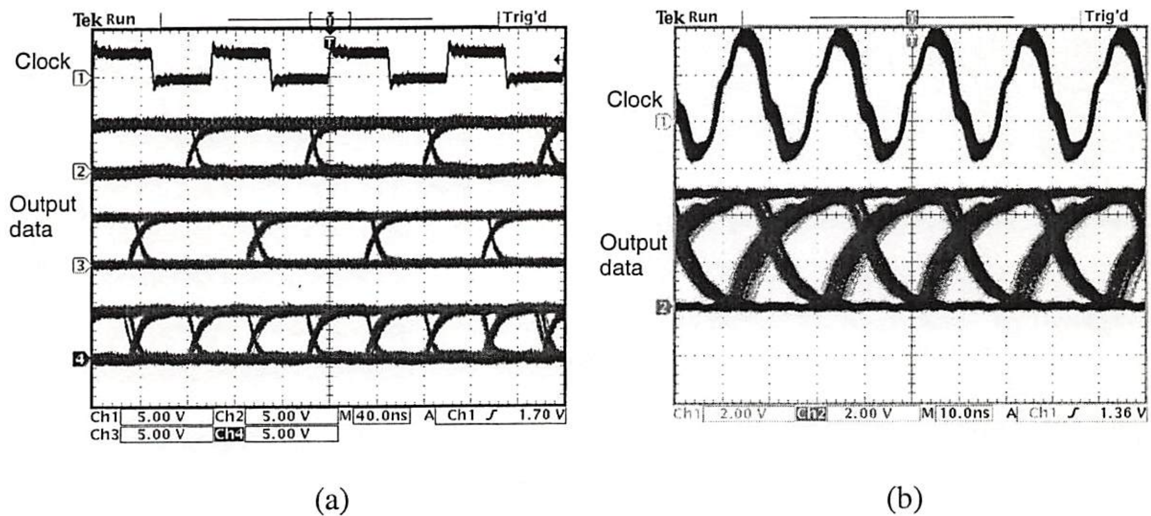


Figure 6-12. Optical power output through 0.3 m FIGs with various d_{in}.

When the distance d_{in} is over 100 μm the output power difference is negligible. With 15° VCSEL divergence angle the beam diameter at d_{in} = 100 μm is 41 μm from Eq. 4-1. This means that the diameter of the beam is entering the FIG covers many core fibers, thus the launch position no longer affects the output power.

6.5 Interconnect Performance

We interconnected two Transpars using the FIG as shown in Figs.6-4 and 6-5. For the operating conditions we used the same conditions with the free-space optical interconnection as discussed in Chapter 5 and the VCSEL array bias was 2.5 V and produced 13 mA output current. The distance between FIGs and Transpar was d_{in} = 50 μm and d_{out} = 0 μm. The eye diagrams in Figure 6-13 (a) shows simultaneous Transpar receiver outputs of three different MSM detectors at low crosstalk and Fig. 6-12 (b) shows that the system is operating at up to 50 Mbps. The open eyes indicate wideband operation with low noise and intersymbol interference through the FIGs.



(a) (b)

Figure 6-13. Eye diagrams of FIG output (a) at 10 Mbps, (b) 50 Mbps.

Chapter 7

FIG Modeling and Simulation

7.1 Introduction

There are several critical problems that arise in optical interconnection systems using FIGs. First, the coupling distance between the optical sources the FIGs must be optimized so that source signals are transmitted without significant power loss. In one application, 2D array of VCSELs can transmit laser beams to a 2D array of detectors through FIGs. Each VCSEL beam has a Gaussian far-field pattern that spreads out with distance. With a long coupling distance d_{in} from VCSEL to FIGs, the transmitted power will decrease and the beams from adjacent VCSELs will overlap, causing crosstalk at the detector array.

Second, the insertion loss caused by different VCSEL beam launch positions on FIGs should be minimized. While the first problem is depends on z direction distance (the propagation direction of the laser); the second problem is caused by the x-y directional alignment. Since FIGs consist of core fibers, and cladding, and background material, the beam launched into the cladding or background may cause a significant propagation loss.

We investigate these problems by computer simulation using BeamPROP software by RSoft. The BeamPROP simulations are based on the beam propagation method

(BPM) described in the Appendix. BPM is a widely used propagation technique for modeling integrated photonic and fiber optic devices. It is conceptually simple, very efficient and can be applied to a complicated geometrical structure.

7.2 Simulation Limitations

In the simulations, the limitations come from the assumptions that are based on the BPM [60]. The limitations are following,

(1) Paraxial approximation of the Helmholtz equation. This implies that the divergence angle of the propagation beam should be small. To minimize the limitation we will use a laser has 15° divergence angle with 300 μm propagation length in the simulation. For the bigger divergence angle, the limitation can be more accurate using Pade approximations [13].

(2) Polarization effects are ignored from the scalar field assumption. In the FIG interconnection the polarization effects are negligible, but several vector beam propagation techniques can be used to overcome the limitation [21].

(3) Backward reflections are ignored. The model does not account for backward reflection that may occur in the interfaces between fiber and optical source or detector. Various bi-directional BPM techniques have been developed to address this issue [56].

7.3 Simulation Setup

7.3.1 Fiber Array

The properties of the fiber core and cladding for the simulations are summarized in Table 7.1.

Center-to-center spacing	13.6 um
Core diameter	9.1 μm
Fiber array length	200 μm
Indices of refraction	Core: 1.86 Clad: 1.46 Background: 1.61

Table 7-1. FIGs simulation parameters.

We assume that the fibers have a uniform step-index core profile of 1.86 and that the cladding index is constant at 1.46. The background between core and cladding is filled with index of 1.61. The fiber array with the indices of refraction is shown in Fig. 6-2. The ratio of the core area to the total cross-sectional area of each FIG is 41 %. For computational simplicity we assume a 7×7 hexagonal array of fiber in our FIG model.

7.3.2 Calculation Parameters

The computational core of the program is based on a finite difference beam propagation method [9], [60]. This method uses finite difference methods to solve the well-known parabolic or paraxial approximation of the Helmholtz equation (see Appendix). In addition, the program also uses full transparent boundary conditions (TBC) [12]. The basic approach of TBC is to assume that the field near the boundary behaves as an outgoing plane wave, with characteristics (amplitude, direction) that are dynamically determined via a heuristic algorithm that is a part of the BPM program.

The plane wave assumption allows the field at the boundary point to be related to the adjacent interior point, thus completing the set of equations. The condition makes the effect of the boundary position irrelevant, and attempts to be more efficient and more accurate. The location of the boundary is fixed which is the boundary of each fiber. Since polarization effects are not important in the setup, these effects are ignored in the simulations.

We have chosen an initial choice of the wavenumber, k_{ext} $(=\frac{2\pi}{\lambda})$. In addition, we set the wave number variable so that we get the divergence effect inside the fiber array. While higher Pade order improves the accuracy at large angles (over 90°), large index difference, and when large ranges of propagation constants are involved (e.g. multimode devices), we will use 0th-order Pade approximation since the divergence angle of the laser is 15°. We have chosen the calculation steps $\delta x = 0.02$ μm, $\delta y = 0.02$ μm, $\delta z = 0.2$

μm. The choice of the step size is critical for the computation time and accuracy. Since the fields along the z-axis change slowly compared to the fields along the x or y-axes, we have chosen ten times more fine steps for x and y propagation. The calculation parameters are summarized in Table 7-2. The x, y, z directions in the simulations are defined in Fig. 7-1.

Numerical scheme	BPM
Boundary condition	Full TCB
Boundary location	Fixed
Reference k	k_{ext}
k angle	Variable
Laser wavelength	850 nm
Computing step size	δx = 0.02 μm, δy = 0.02 μm, δz =0.2 μm

Table 7-2. Calculation parameters.

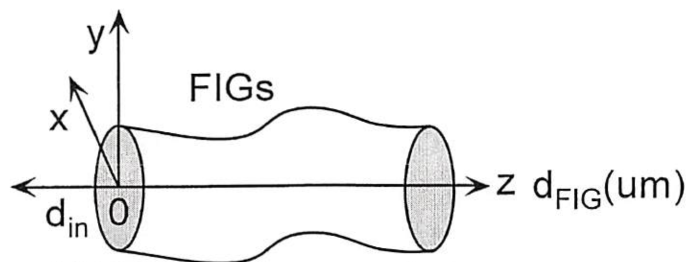


Figure 7-1. x, y, z directions in FIG simulation.

7.3.3 Launching Laser

In the simulation, the wavelength of the laser is set at 850 nm with 15° of divergence angle, which are the wavelength and the angle of the Honeywell VCSEL/MAM array for the experiments. We model the far-field distribution as Gaussian. In the near field, the VCSEL has a multimode structure and a Gaussian-based model is not appropriate. In the multimode simulation we launch a multimode field and calculate the modes from 0 through 2 for m and n = 1 of the LP_{mn} fiber mode. It is reported for VCSELs that the number of modes is less than four for drive current less than 20 mA in various aperture sizes [20]. Therefore it is reasonable to assume that the major modes are LP_{01}, LP_{11}, and LP_{21} in the simulations. Figure 7-2 shows these three modes. The phase is assumed to be uniformly distributed from 0 to 2π and is modeled by a pseudo-random number that does not vary from run to run. The input power is in arbitrary units so we choose a power level that shows the best graphical display of the data.

We have run simulations using several different alignment positions of the VCSEL with respect to the individual core fibers in the FIGs. First we launch a laser beam into the FIGs beginning at the d_{in} = 0 position and over a sequence of steps up to d_{in} = 100 μm. The other critical alignment is x, y positions of the VCSEL to simulate two extreme cases. In one extreme is that the beam is located at the center of the core and at the other it is at the center of the background materials. We will discuss the differences in the next Section.

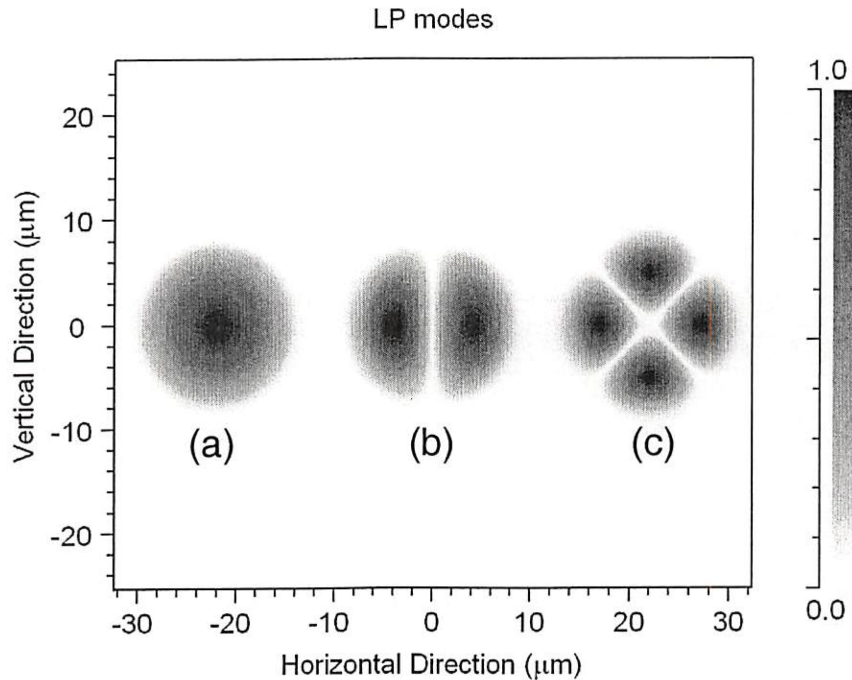


Figure 7-2. Different laser modes (a) LP_{01}, (b) LP_{11}, (c) LP_{21}.

7.4 Results and Discussions

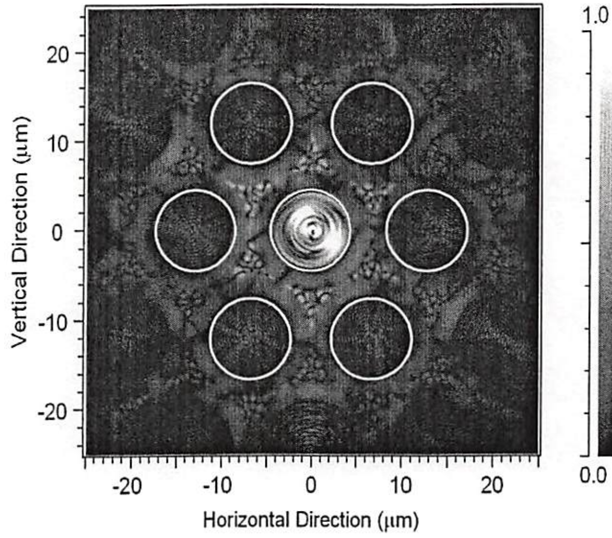
7.4.1 Waveguides in Fiber Arrays

We used two different extreme cases of x-y launch positions for the beams entering the FIGs, shown as × in Fig. 6-10. In this figure launch position (a) is a launch at the core center and position (b) is a launch at the background material, equidistant from the cladding of three neighbor core fibers. Labeling the coordinate system, the (x, y) coordinate of (b) position is $x = 6.8$ μm, $y = 5.9$ μm and position (a) as $x = 0$, $y = 0$. There are three variables along z-positions, d_{in}, d_{FIG}, and d_{out} that are specified in Fig. 6-

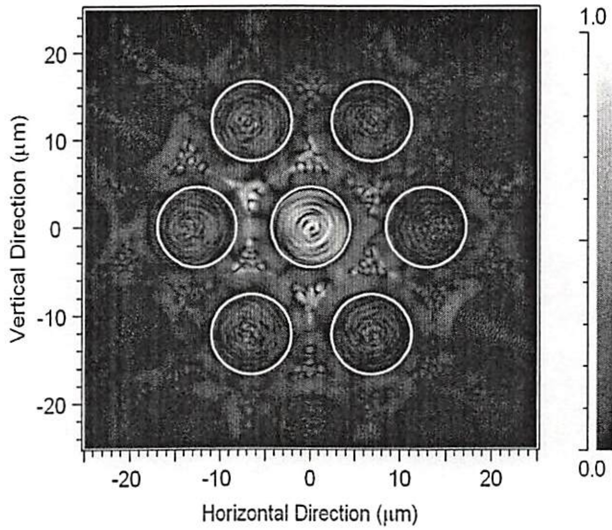
4. In the simulations we focus on the optical power profiles as a function of d_{FIG} value up to 200 μm and d_{in} value from 0 to 100 μm. The simulations for x-y field distributions are shown in Fig. 7-3. The locations of the core fibers are marked with white-lined circles. The output fields are shown at d_{FIG} = 0 μm for Fig. 7-3 (a) and (c), d_{FIG} = 200 μm for Fig. 7-3 (b) and (d).

7.4.2 Launch at Center of Fiber Core

Figure 7-3 (a) shows the field output when laser is launched at the center of a core fiber with d_{in} = 0. The field output shows that the field is confined well at the core fiber and waveguided through the core fibers. The beam width of the laser at d_{in} = 0 is 15 μm that is larger than the core fiber pitch of 13.6 μm but the intensity of the fields at the outside of the core fibers is very low through the propagation. This means the core fiber is the main propagation path for the waveguides, as we have seen in the experiments as shown in Fig. 6-11. The output images in Fig. 6-11 have larger beam diameter than that of simulations because they are measured after a much larger propagation distance of 0.3 m.

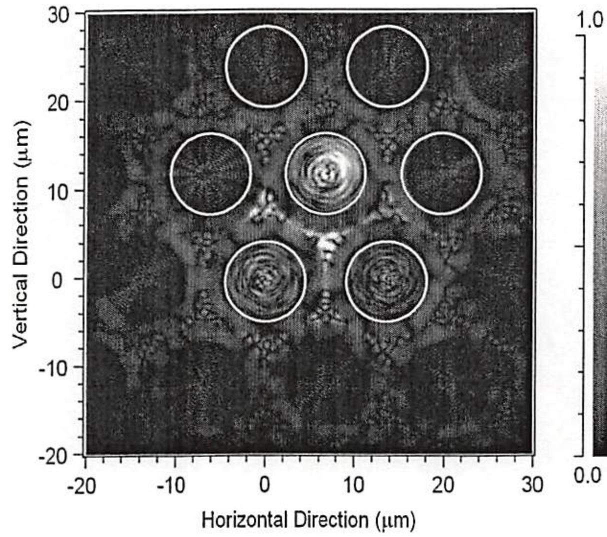


(a) $x = 0$ μm, $y = 0$ μm, $d_{in} = 0$ μm.

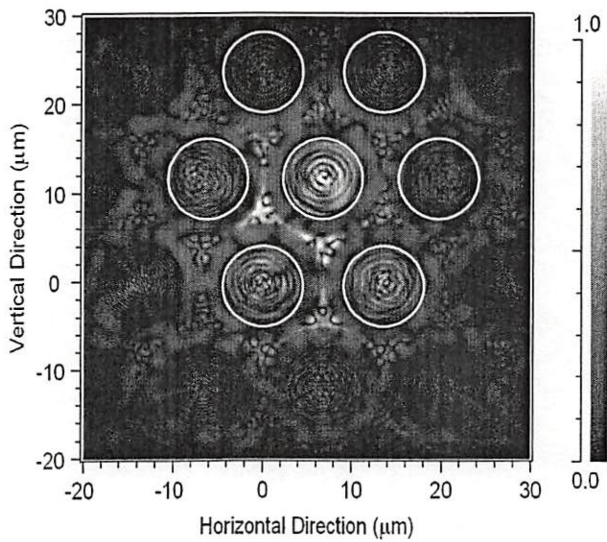


(b) $x = 0$ μm, $y = 0$ μm, $d_{in} = 100$ μm.

Figure 7-3. Transverse field profile outputs. Laser launched at the center of the core with (a) $d_{FIG} = 0$ μm, (b) $d_{FIG} = 200$ μm.



(c) $x = 6.8$ μm, $y = 5.9$ μm, $d_{in} = 0$ μm.



(d) $x = 6.8$ μm, $y = 5.9$ μm, $d_{in} = 100$ μm.

Figure 7-3 (cont.). Launched at the center of the background with (c) $d_{FIG} = 0$ μm, (d) $d_{FIG} = 200$ μm.

When the laser launches with a larger d_{in} distance, more neighbor core fibers are involved in the propagation. Figure 7-3 (b) shows results for the launch distance d_{in} of 100 μm from the FIGs and the fields at the cladding are stronger that will not be waveguided. This means it will have much output power loss when d_{in} is increased. The field intensity in the cladding decreases fast and the fields in the neighbor core fibers get stronger at 100-μm propagation distances. However some of the field intensity remains in the background area through a propagation distance of at least 100 μm because the refractive index of cladding is less than the refractive index of the background.

7.4.3 Launch at Center of Background

Figure 7-3 (c) and (d) show that the neighbor core fibers are the waveguide medium when laser is launched at the center of the background. This simulations show very similar results with the experiment as shown in Section 6-3. Figure 6-11 (a) shows that the seven core fibers are primarily responsible for propagation for the case of core center launch position corresponding to (a) and (b) of Fig. 7-3. The launch in the background material equidistant from the adjacent core fiber is shown in Fig. 7-3 (c) and (d). The simulations show the neighbor four core fibers have much higher field intensity than other cores or claddings. In the experiments four core fibers are waveguided as shown in Fig. 6-11 (b) for less than d_{in} = 100 μm and in Fig. 7-3 (c) and (d). From this simulation result we can conclude that more core fibers are involved in the waveguide

propagations for the case of core center launch. This result is also related to the optical power outputs. We discuss details of the optical power loss in the next Section.

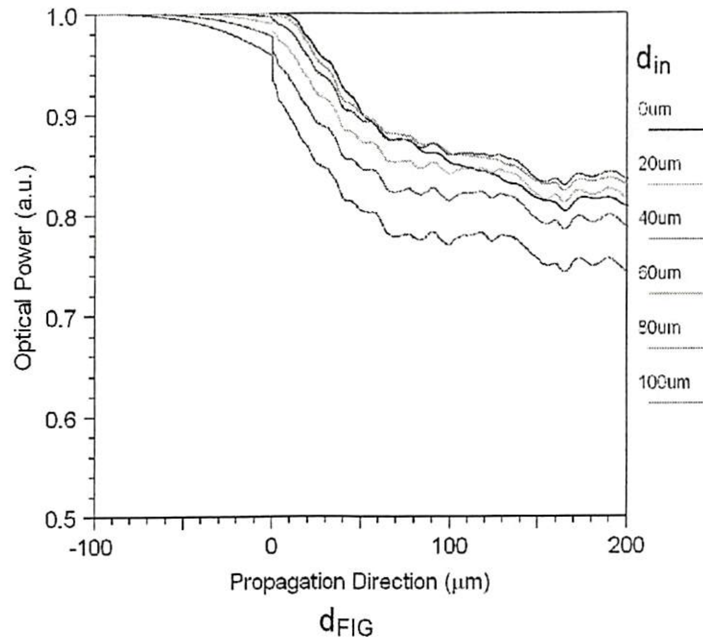
7.4.4 Optical Output Power

In the simulations the optical power is calculated by integrating the power in the calculated field at the current z position over the waveguide cross section. The normalized power is calculated by

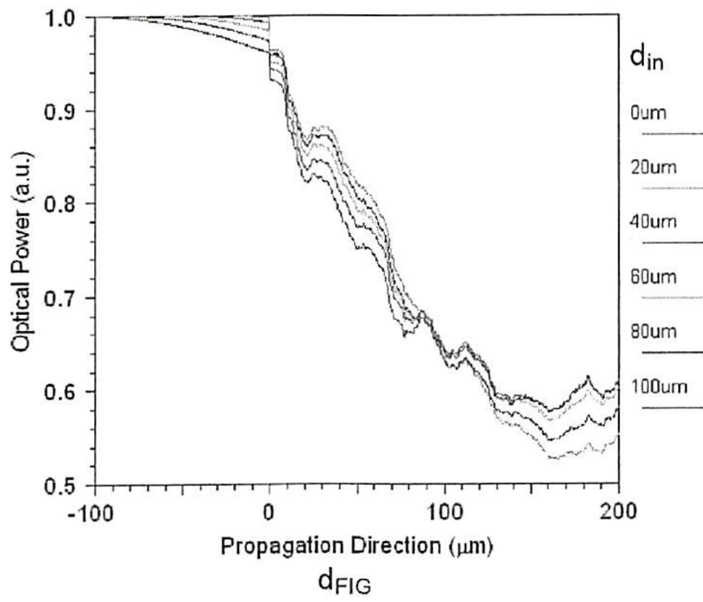
$$\frac{P_M}{P_0} = \frac{\left| \iint_A (\phi_z \cdot \phi_M^*) dxdy \right|^2}{\iint_A |\phi_M|^2 dxdx \cdot \iint_A |\phi_0|^2 dxdx} \tag{7-1}$$

where A is the area of the simulation domain cross-section, ϕ_z is the propagation field along z, ϕ_M is the monitor field during the waveguide propagation, and ϕ_0 is the launch field for normalization.

The power monitor path is defined as the middle seven core fibers and their claddings. In this case the field in the background material will not be counted in the optical power output. This seems reasonable since only core fibers are responsible for waveguides. Before the laser hits the surface of FIGs the power is defined as the power within the radius containing all six fibers (core and cladding) adjacent to the center launch fiber. This radius is 20.4 μm. The simulation results for optical power loss along the propagation direction are shown in Fig 7-4.



(a)



(b)

Figure 7-4. Optical power profile along the propagation axis z. Laser launched at (a) the center of core fiber; (b) the center of the background.

Before the incident laser beam hits the FIGs the power decreases slightly (to 96 % of the incident power after 100-μm propagation) because we monitor the power only within the 20.4 μm radius. Then the optical power decreases to about 3 ~ 4 % at d_{FIG} =0 [Fig. 7-4 (a) and (b)]. When d_{FIG} is increased up to 100 μm for the core launch case and about 150 μm for cladding case, the output power goes down abruptly. The power changes with distance along the propagation axis occur slowly after about 150 μm.

Interestingly when d_{in} =0, the core fiber does not suffer much power loss, while the cladding center case has the largest loss near d_{FIG} =0. This indicates that much more optical power is scattered away to the cladding and the scattering effect is stronger when the laser enters at the cladding center. The results show the power output difference clearly between different launch cases. For the core launch case the output powers at d_{FIG} = 200 μm are more than 80 % of the incident power except for d_{in} = 100 μm when the cladding case is about 60 % of the incident power at d_{FIG} = 200 μm.

For example, when d_{in} = 0 μm the output power ratio (power output of core center case/ power output of cladding center case) is about 1.4, meaning that the output power of the core launch case is about 140 % of the cladding launch case. This number is very close to the experiment. In the experiments the ratio for the output power ratio at d_{in} = 0 μm is 1.49 (see Fig 6-12). For d_{in} = 0 μm, the ratio for the experiments is 1.21 and the simulation shows about 1.25. The comparison of the simulation result and the experiment result are shown in Fig. 7-5. In Fig. 7-5 the power ratio is defined by $P_{core}/P_{background}$ where P_{core} is the optical power output at core center launch case and $P_{background}$ is the optical power output at background launch case.

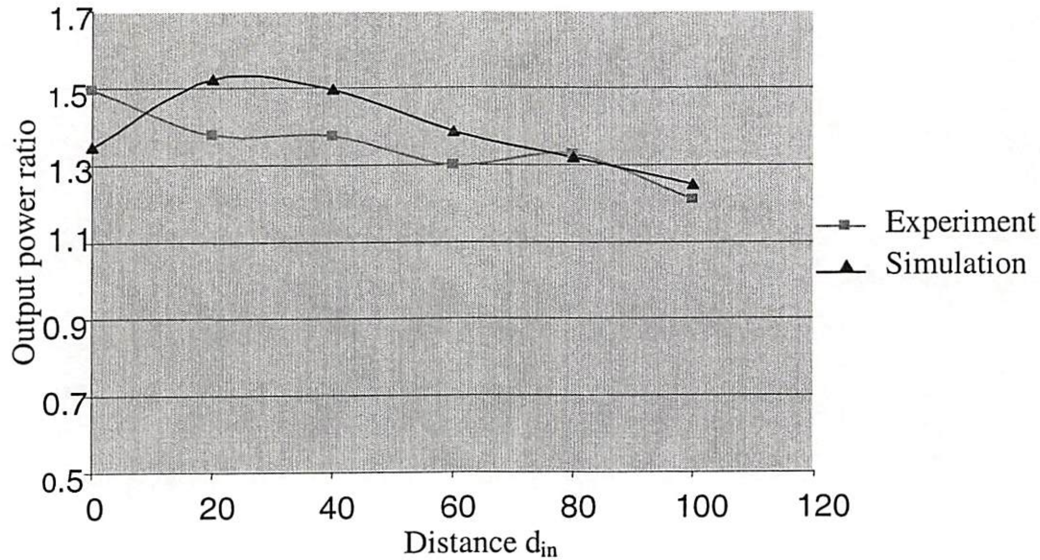
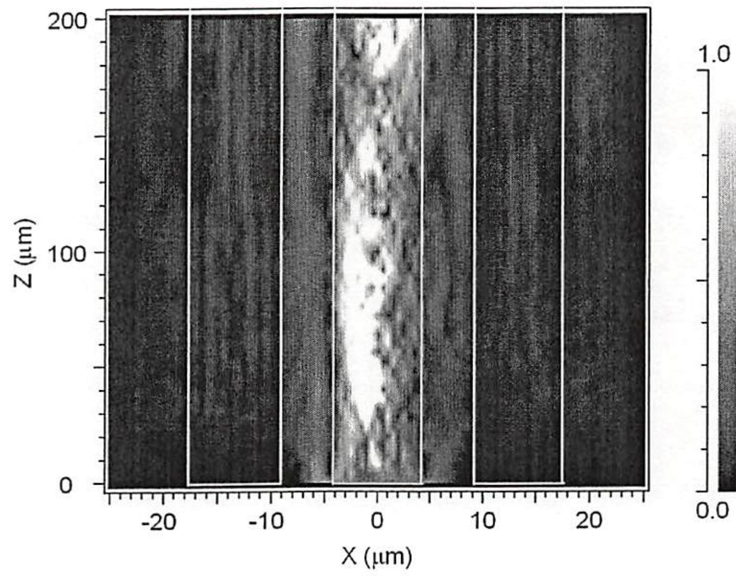


Figure 7-5. Optical power comparison of experiment and simulation along d_{in}.

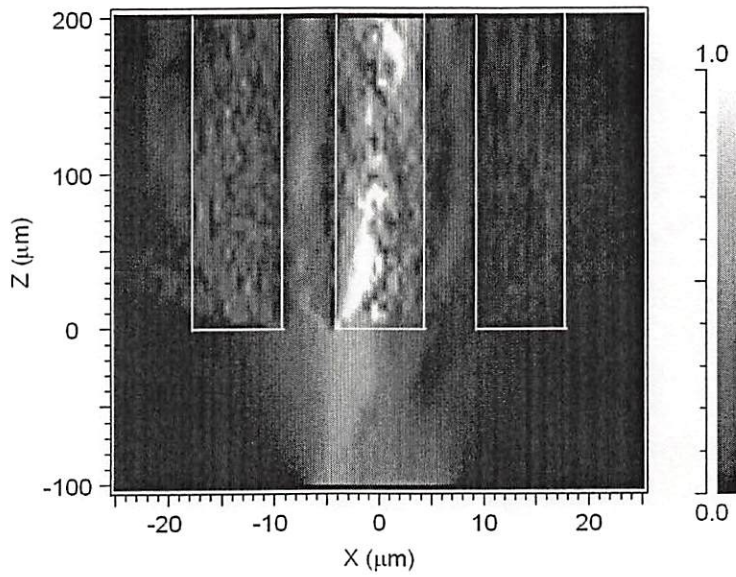
Figure 7-6 shows the wave propagation profiles along z-axis when d_{in} = 0 μm and d_{in} =100 μm for different launch positions. Figure 7-6 (a) and (b) is for the core launch case and Fig. 7-6 (c) and (d) is the background center launch case. The x-y launch positions are x = 0 μm and y = 0 μm for (a) and (b), and x = 5.9 μm and y = 6.8 μm for (b) and (c). The simulation results show field $|E|$ output rather than power output. We choose this because the field distribution shows the distribution inside fibers more clearly than the power distribution. The fiber structures are shown with the white lines in the figures. Their ends are positioned at d_{FIG} = 0 μm and d_{FIG} = 200 μm. From these simulations, again it is clearly shown that the highest intensity of the beam is at the core center launch case.

The field at claddings decreases fast and the field at core fibers remains at almost the same intensity through the propagation. Comparing Fig. 7-6 (b) and (c), even when

the laser is launched with d_{in} = 0 as in (c) the field profile at the core is much weaker than the case of (b) which has d_{in} = 100. Instead the fields in the neighbor core fibers that are marked as lines in (b) have a higher intensity than the neighbor core fibers in (c). The beams launched into the background center form as high-angle spreading leaky modes and thus, the power leaks into the neighbor core fibers. Therefore the field intensity is dramatically decreased along the z direction and spreads out to the neighbor core fibers.

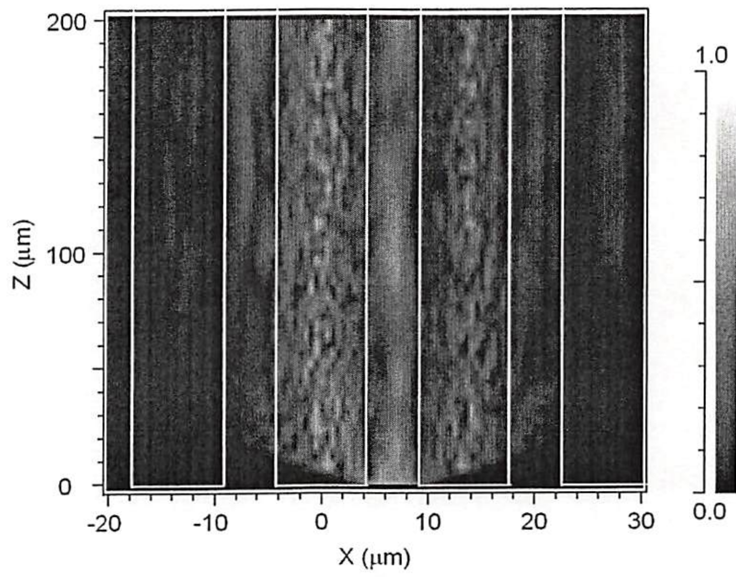


(a) $x = 0$ μm, $y = 0$ μm, $d_{in} = 0$ μm.

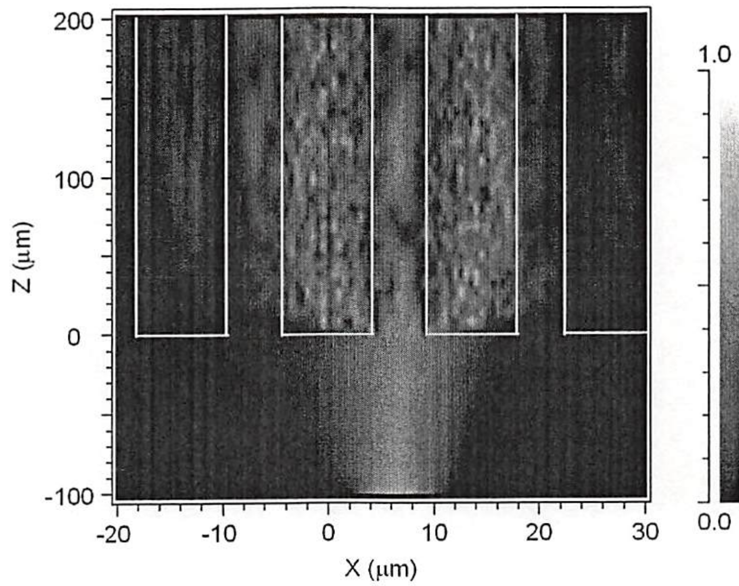


(b) $x = 0$ μm, $y = 0$ μm, $d_{in} = 100$ μm.

Figure 7-6. Simulation outputs for $d_{FIG} = 200$ μm. Laser launched at the center of core with (a) $d_{in} = 0$ μm, (b) $d_{in} = 100$ μm.



(c) $x = 6.8$ μm, $y = 5.9$ μm, $d_{in} = 100$ μm.



(d) $x = 6.8$ μm, $y = 5.9$ μm, $d_{in} = 100$ μm.

Figure 7-6 (cont.). Laser launched at the center of the background with (c) $d_{in} = 0$ μm, (d) $d_{in} = 100$ μm

Chapter 8

An Integrated Approach for Optical Interconnects: UTSi

8.1 Integration of Optical Interconnects to Silicon

The integration of optoelectronic devices with electronic circuits and systems has recently been used in many applications in optical networks and communication systems and will be an essential technology in future high bandwidth data and communication systems. The driving forces of integration are circuit speed, cost, power consumption, reliability, and simplified manufacturing.

The main obstacle in integration is the material incompatibility of optoelectronic III-V materials and silicon. Optical devices such as VCSELs and detectors are based on GaAs, which has different lattice size, performance, and processing with silicon; therefore Si-based VLSI devices provide a poor environment for the optical devices. CMOS can deliver the needed bandwidth to the optoelectronic interface while at the same time effectively bridging to the lower bandwidth density of conventional electronics. In fact, low-cost 0.5 μm CMOS has been shown to be capable of providing a multiplexed 55-Gb/s/cm interface [40].

One could dream that the entire system including CMOS circuitry, laser source, waveguides, and receiver could be fabricated in a single material substrate. However, a cost effective solution for the material incompatibility of optoelectronic III-V materials

and Si has not been found and full integration with the highest optimal performance may not be achieved in the near future.

One solution is hybrid integration where the optical devices are grown separately from the Si electronic circuitry and the optical devices are bonded to the circuitry using a various bonding technologies. These techniques avoid the material incompatibility of Si and GaAs. These include flip-chip bonding, epitaxial lift-off and subsequent contact bonding, and the creation of a physical cavity atop the silicon circuitry and flowing-in optical materials such as liquid crystals [54]. The advantage of this hybrid integration is that the optical parts and the electrical parts can be individually tested and optimized.

8.2 Flip-chip Bonding Technology

Flip-chip bonding technology is one of the most popular techniques to integrate Si-based circuitry with GaAs-based optical I/O. It enables high frequency operation and cuts down on assembly time and cost while increasing yield and optimizing heat flow.

In flip-chip bonding technology, the bonding pads are incorporated into both the compound semiconductor optical devices as well as the silicon circuitry and then associated pads are brought into contact and a mechanical solder bond can be used. Because the optical devices are inverted during the flip-chip bonding process, either the substrate must be transparent (e.g. UTSi) or a bottom-emitting VCSEL could be used (see Figure 8-1). The flip-chip bonding eliminates the wire-bond inductance between driving/receiving circuits and the optical devices that become a problem at data rates over 3 Gbps [30].

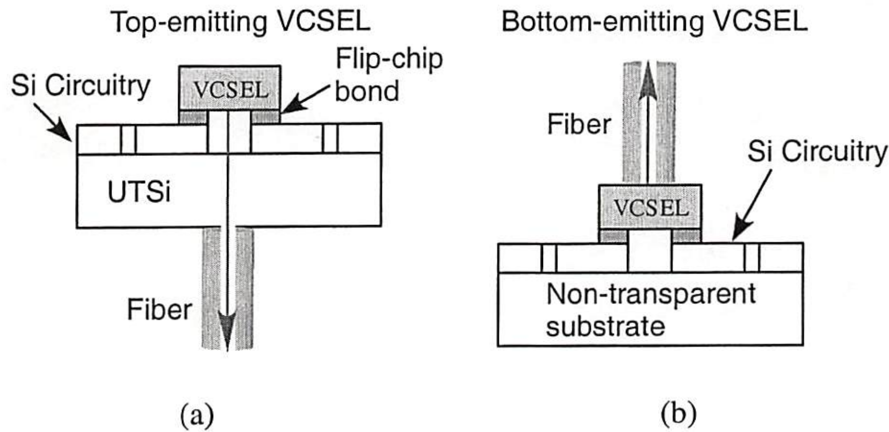


Figure 8-1. Two different flip-chip bonding types: (a) Top-emitting VCSEL with UTSi, (b) Bottom-emitting VCSEL with regular CMOS substrate.

As with monolithic integration, both passive modulators and active emitters can be integrated using this method. The flip-chip bonding of a 16 × 16 VCSEL array [29], and a photodetector array [11] to CMOS VLSI circuits has recently been reported with high-speed bandwidth.

In flip-chip bonding solder balls are first placed on each chip attachment pad. The chip is then turned face down onto the chip or the PCB and directly reflow-soldered in place. The electrical properties of flip-chip bonding are ideal because the bonding lengths are very small, and so all parasitics associated with packaging are minimized [26]. However, flip-chip technology has mechanical and thermal limitations. There is little mechanical compliance between chips or chip and PCB except for the limited springiness of the solder balls themselves. Also the thermal coefficient of expansion between the materials must match extremely closely.

8.3 Silicon-on-Insulator (SOI)

Recently silicon-on-insulator (SOI) has been emerged as a mainstream technology for deep sub-micron VLSI [32], [63]. In traditional bulk CMOS devices, P type or N type MOS transistors are isolated from the well layer. In contrast, SOI-CMOS devices are separated into a Si supporting substrate, which is an insulator, and each element is completely isolated. This isolation enables reduced parasitic and absence of latch-up, enabling high-speed operation at low power in SOI circuits. SOI CMOS has been identified as a possible method for increasing the performance of CMOS that is predicted by Moore's law [Figure 8-2]. It has been shown that SOI CMOS offers a 20-35 % performance gain over bulk CMOS [63]. SOI had not been suitable as a substrate for mainstream application until recent years, because of the SOI material quality, device design, and the steady progress in bulk CMOS performance through scaling.

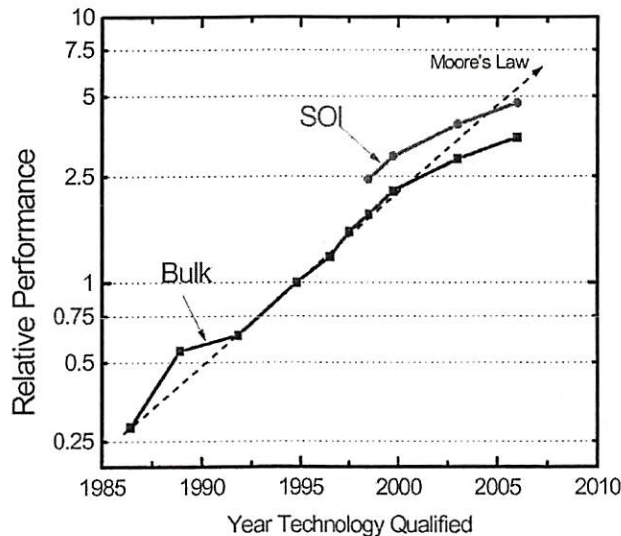


Figure 8-2. Benefits of SOI in Moore's law [22].

Some of the benefits of SOI are its low power, and increased tolerance to errors caused by cosmic rays and background radioaction. The reasons for increased SOI performance are elimination of area junction capacitance and elimination of the body effect in bulk CMOS technology. SOI circuits can operate at low voltage with the same performance as a bulk CMOS at high technology. The benefits of SOI offer a new platform for the deep sub-micrometer CMOS process and produce gigabit–per-second optoelectronic circuits at low noise [25].

One of the distinctive issues in SOI technology is the floating body effect. MOS transistors are formed as electrically isolated islands of silicon on the insulating substrate. This results in undesirable floating effects. The floating body effects reduce analog gain, degrade linearity and induce 1/f noise overshoot.

8.4 Ultra-Thin Silicon-on-Sapphire (UTSi) Technology

UTSi is a SOI Technology, which fabricates CMOS circuits on a silicon-on-sapphire wafer. The circuitry contains a thin layer of silicon (~100 nm) on the top of 250 μm-sapphire layers. The substrate resistance is 10^{16} ohm-cm, which is 14 orders of magnitude higher than the standard bulk CMOS substrate. The isolating substrate has two key advantages over conventional bulk CMOS. It eliminates the substrate leakage that typically results in crosstalk, and reduces parasitic capacitance to the substrate, providing more efficient circuitry. UTSi comparisons with a conventional bulk CMOS process are shown in Fig. 8-3.

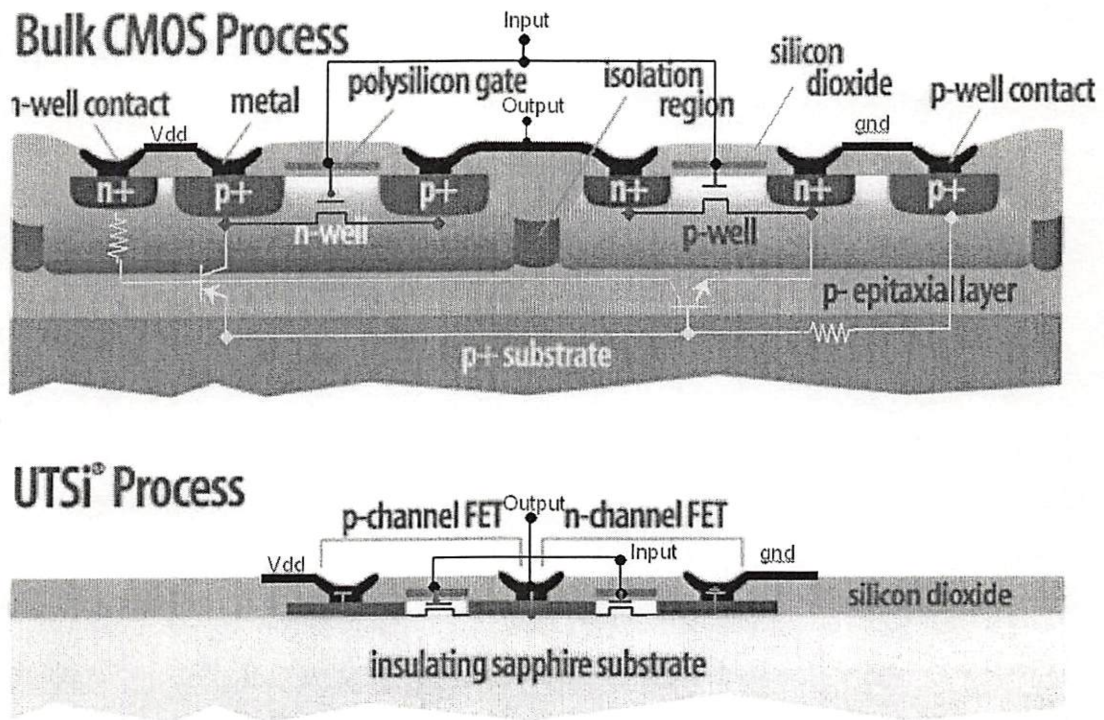
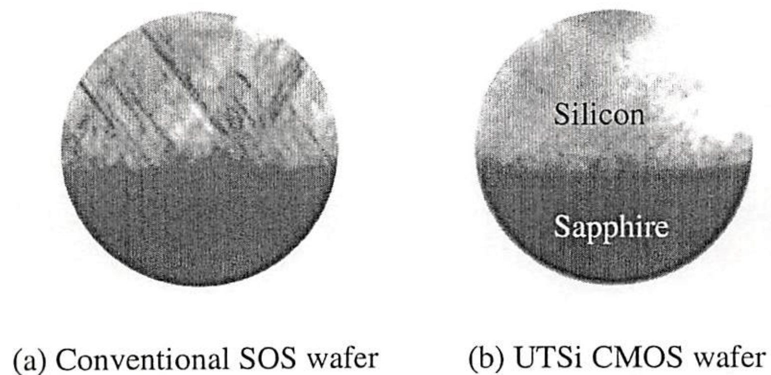


Figure 8-3. Cross-section of bulk CMOS and UTSi process.

UTSi process also eliminates the defects in SOI process as shown in Fig 8-4 and results in high quality and high yield wafers of UTSi on an insulating sapphire substrate. These properties of UTSi allow for dense integration of circuits requiring high isolation.



(a) Conventional SOS wafer (b) UTSi CMOS wafer

Figure 8-4. Cross sectional view of wafers [33].

UTSi CMOS technology is the first SOI process that is capable of delivering RF CMOS production in high volume. It has been developed to provide the cost and performance requirements of future integrated system-on-chip solution for wireless communication systems and it has potential applications for low power system-on-chip solutions.

In photonic circuits it is necessary to integrate multiple channels of transmitters and receivers and other analog circuitry with digital functions. UTSi technology enables the integration of different mixed signal components and is well suited for low-cost optical data communication systems.

8.4.1 Sapphire (Al_2O_3) Physical Properties

The physical properties of sapphire are:

1. Coefficient of thermal expansion (CTE) of sapphire, which is almost matches with GaAs. CTE of Sapphire is 5.3 ppm/C, GaAs is 5.7 ppm/C, and Si is 3.8 ppm/C.
2. It is optically almost transparent. The transmittance data is shown for sapphire in Fig.8-5.
3. It is mechanically strong. Hardness is 9 on Moh scale.
4. Good thermal conductor and electrical insulator, reducing parasitic, substrate coupling.
5. Refractive index ~ 1.76.

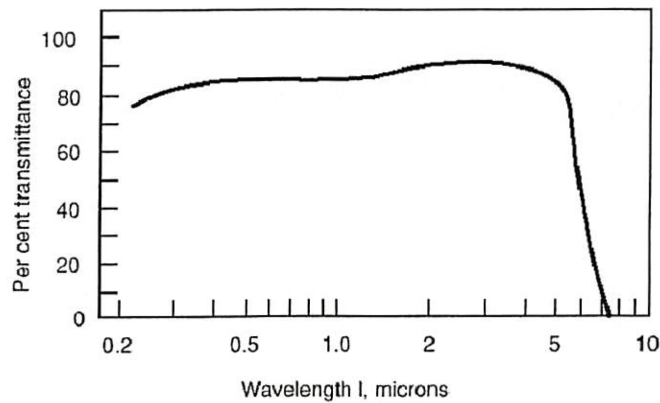


Figure 8-5. Transmittance data of 1 cm thickness sapphire [2].

8.4.2 UTSi Advantages

Some potential UTSi advantages include:

1. Monolithic integration of RF analog and digital circuits.

2. Reducing parasitic capacitance between channels, UTSi operates at high-performance datacom rates over 3 Gbps good isolation between channels (e.g., receivers and drivers).

3. The transparent substrate has packaging advantages such as direct VCSEL beam output through the substrates.

4. It offers an excellent high frequency performance.

5. UTSi has standard process with fewer masking steps, which is available through MOSIS. UTSi has currently 0.5 μm process and it is scalable to 0.1 μm. It has also a standard CAD tool interface.

6. Superior functional integration: analog, digital, electrically erasable programmable read-only memory (EEPROM) memory intimately integrated on single chip. The availability of EEPROM devices, integrated with the drivers and logic circuitry, provides another cost reduction by reducing board level complexity. Very high quality passive devices (inductors, capacitors).

7. Low power consumption than bulk CMOS, SiGe &GaAs.

8. Radiation hard (space applications).

9. Multilevel threshold transistors that give the circuit designer added flexibility to increase performance and reduce power consumption.

8.5 Optoelectronic Integration on UTSi

Since UTSi has many advantages on high-speed devices and enables the integration of mixed signal circuitry it has been investigated for optoelectronic applications in recent years. The main issues are: (1) integration of 2-D VCSEL/PIN arrays, (2) integration of monolithic receiver and PIN diode arrays, and (3) optical packaging with multimode and single mode fiber arrays. UTSi as an SOI technology has benefits for the monolithic integration of receivers and PIN diode arrays. The transparent substrate can transmit laser light through sapphire and enables flip-chip bonding of top emitting VCSEL/PIN arrays. Figure 8-6 shows 1×4 Emcore PIN arrays that have been Au thermo-compression flip-chip bonded to the UTSi circuitry. It shows that the PIN active areas exposed through the substrate and that optical signals can be

detected. The circuitry on sapphire substrate is not transparent and can be seen on the top of PIN array.

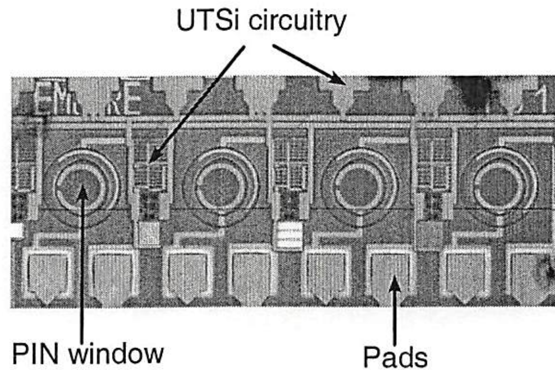


Figure 8-6. Flip-chip bonded 1 × 4 Emcore PIN array. Picture is taken through UTSi substrate.

It is possible to package UTSi with fibers by direct attachment of the fiber array to the transparent substrate. This is an advantage in packaging because no other waveguide paths on the chip are required. Figure 8-7 shows one example of direct attachment of fiber arrays. 100 nm-thickness silicon circuitry is on the substrate, while VCSEL and PIN arrays are flip-chipped on the Si. There is no Si layer in the optical path under the transceiver array. A fiber array is used for light transmission without any beam focusing elements. The fiber array can be 1 × 4 or 1 × 12 and the direction of the attachment could be parallel to the substrate or 90° when FIGs are used. The coupling optical power from transceiver to the fiber array is reported about 3 dBm [33].

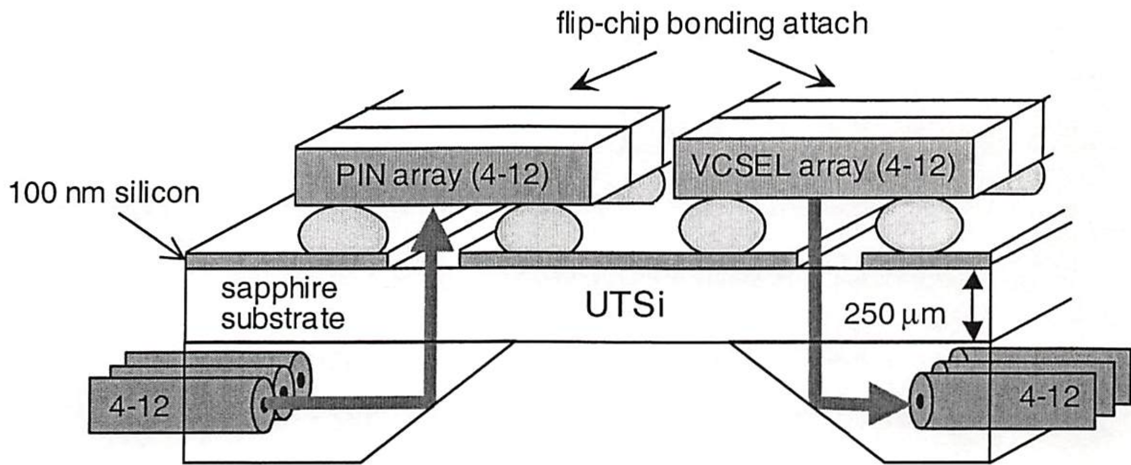


Figure 8-7. Flip-chip bonded UTSi.

Chapter 9

System Design and Testing of UTSi CMOS

9.1 UTSi CMOS System Design

UTSI CMOS is one candidate technology capable of realizing the integration of optoelectronic systems with Si-based CMOS. In this chapter we describe the design and testing of different UTSi chips with various circuitry and system functions for optical signal processing and networks.

Four different UTSi chips have been fabricated. Their circuits were designed, modeled and simulated mainly by Liping Zhang [17], [73]. The chips are named as 2000 UTSi #1, 2000 UTSi #2, 2001 UTSi #1, 2001 UTSi #2. All four chips are based on 0.5 μm Peregrine UTSi technology. Two 2000 chips are designed in the UTSi FA process and the two 2001 chips are designed in the UTSi FC process. Both FA and FC technologies have fully depleted devices, 100 μm Si thickness and multi-threshold transistors. However, the FC process has metal-insulator-metal (MIM) capacitors and thick metal-3 (M3) with looser design rules than the FA process M3.

The UTSi chips are fabricated in MOSIS through the COOP foundry runs at George Mason University (2000) and at the University of Southern California (2001). Each chip contains different circuitry and sub-systems for optical receivers, VCSEL

drivers, pseudo-random bit steam (PRBS) generators, and other test circuitry needed for optical signal processing and networks. Table 9-1 summarizes the descriptions of these chips.

	2000 UTSi chip #1	2000 UTSi chip #2	2001 UTSi chip #1	2001 UTSi chip #2
CMOS standard cells	Dynamic threshold INV, NAND, AND, OR, NOR, XOR, MUX, True single phase clock (TSPC), Double flip-flop (DFF), Static DFF, Double edge triggered DFF			
Pad cells	I/O pads, VDD pads, GND pads, bare pads, ESD protected pads			
LVDS standard cells	INV, OR, XOR, MUX, DFF, differential amplifier, comparator, output buffer			
Digital circuits	2047-pattern TSPC PRBS	4×4 Time-division multiplexing (TDM) switch	TSPC, DFF based PRBS, Double-edge triggered DFF-based 2047-pattern PRBS	Frequency divider
Mixed, analog circuits	1×4 low noise amplifier (LNA) transceiver arrays, ring oscillator	1×4 array receiver, 1×4 VCSEL driver	9 PIN photoreceivers, Quadratic-phase LC-VCO, Mixer, Baluns	1×4 VCSEL drivers, PLL-based clock/data regenerator (CDR), Full-balanced differential LC-VCO

Table 9-1. Summary of 2000 and 2001 UTSi chips.

The circuit design and full custom physical layout were carried out in Cadence EDA tools. The chips are carefully designed to perform high frequency optical signal processing at low power and low noise for optical interconnection and communication systems. One important design issue in SOI is electrostatic discharge (ESD) protection due to the insulating substrate. For ESD protection, two ESD rings are designed for each chip. One is designed for the analog circuit and the other is for digital use. There are

five different types of I/O-cells that are input pad, output pad, V_{dd} pad, GND pad, and bare pad, with bonding pads and diodes are powered by the ring. Only the bare pads connecting optical detector and VCSEL arrays do not have ESD for high-speed operation. Additional diodes are also designed and attached to the ring for ESD protection.

9.2 UTSi 2000 Chip #1

UTSi 2000 chip #1 contains a high-speed four-channel VCSEL driver and TIA receiver array, pseudo-random bit steam (PRBS) generators, and a voltage-controlled oscillator (VCO). The block diagram of chip #1 is shown in Fig 9-1. A multiplexor (Mux 1) selects either the TIA receiver decision circuit output or a PRBS output. The PRBS output is selected from one of two 11-bit PRBS by another multiplexor (Mux 2). One PRBS (PRBS1) is based on a true single-phase clock (TSPC) D-flip-flop, which directly interfaces with the GHz frequency clock output from the voltage-controlled oscillator. The other PRBS (PRBS2) is based on a static D-flip-flop and is clocked by an external clock. The 2.5-volt CMOS output of the multiplexor feeds into the VCSEL driver input, which can drive external VCSELs to emit digital optical signals.

The chip has been fabricated in the Peregrine 0.5 μm CMOS UTSi FA process, and the chip photograph is shown in Fig. 9-2. There are two ESD rings, and the analog front-end and digital smart pixel self-testing circuits use separate power supplies to reduce noise. Furthermore, each transceiver has its own power lines.

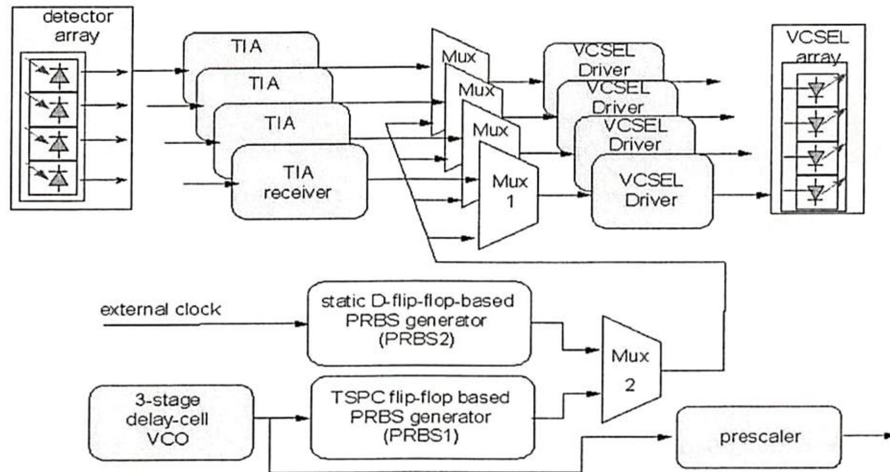


Figure 9-1. Block diagram of UTSi 2000 chip #1.

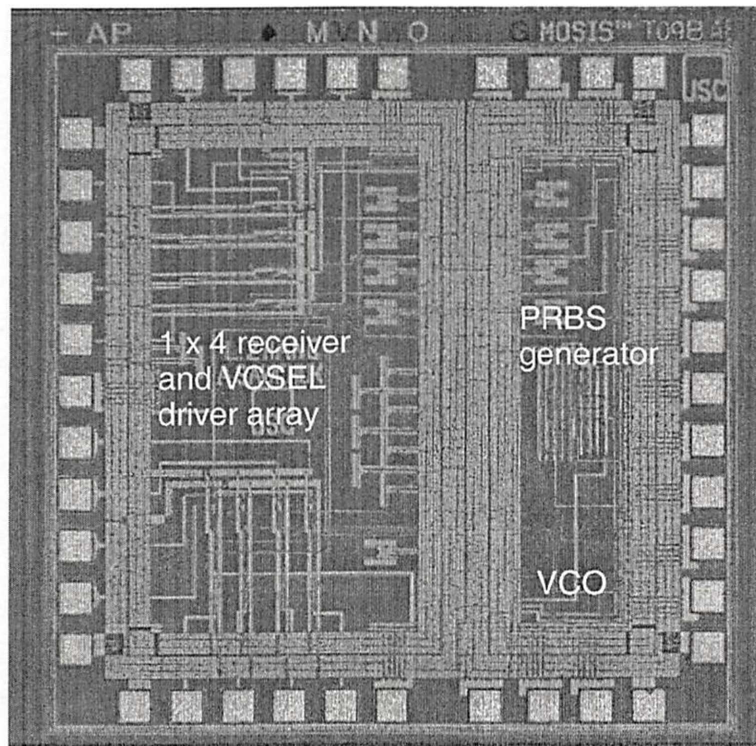
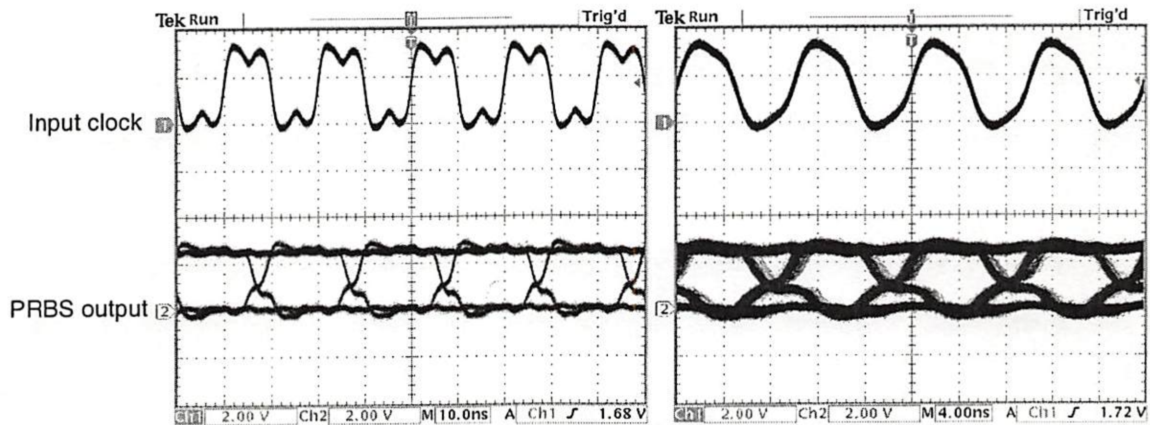


Figure 9-2. Picture of UTSi 2000 chip #1.

9.2.1 Testing of UTSi 2000 chip #1

For testing, the chip is packaged in an LCC 52 package through MOSIS and used in a PLCC 52 pin socket. This packaging is for the convenience of initial testing and is not intended for high-speed environments. The V_{dd} of 2.5 V is applied to four different pads. Ground (GND) is also applied to four different GND pads. First we tested the 11-bit PRBS generator with external clock input. For the selection of the PRBS output, the Mux 2 in Fig 9-1 set to 1. The applied clock is 10 MHz to 100 MHz and the outputs of PRBS were well observed to have open eyes. A Tektronix DG2020A is used as an external clock through the experiments. The test results are shown in Fig 9-3.



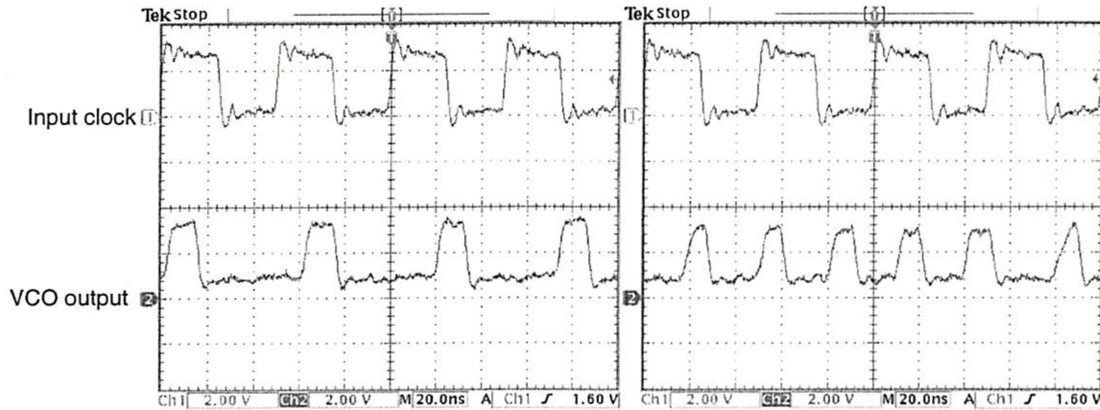
(a) 50 Mbps output (b) 100 Mbps output

Figure 9-3. PRBS outputs of UTSi 2000 chip #1.

The VCO part of the chip was also tested in the package. The change of the frequency is observed through the change of the applied voltage and the output of one-

eight of the VCO frequency after the divide by eight prescaler. The results are shown in Fig 9-4. The frequency of the VCO outputs changes with the applied voltages.

The TIA receiver array was tested with dummy photodetector (PD) inputs. To simulate the low PIN output we simulated the PD output by a voltage source of 2.5 V with a 50 kΩ resistor. This produces an output current of 50 μA that directly feeds the TIA receiver array. The receiver outputs are shown in Fig 9-5.



(a) 1 V input. (b) 2.5 V input.

Figure 9-4. VCO outputs of UTSi 2000 chip #1 with 40 Mbps inputs.

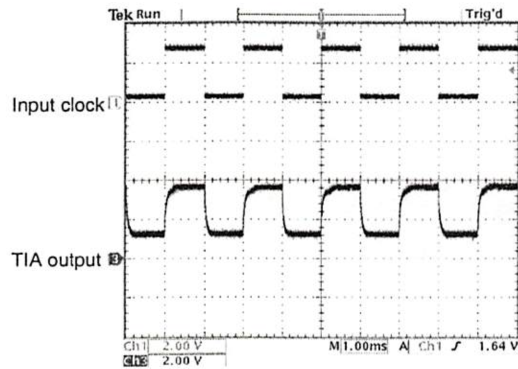


Figure 9-5. TIA receiver output of UTSi 2000 chip #1 with 1 Kbps input.

9.3 UTSi 2000 chip #2

UTSi 2000 chip #2 contains four channel time-division multiplexing (TDM) switches, four channel VCSEL drivers, and receiver arrays. The 4 × 4 TDM switches incorporating optical receivers and VCSEL arrays are for a packet switch with broadcasting capability [8]. The block diagram for chip #2 is shown in Fig. 9-6.

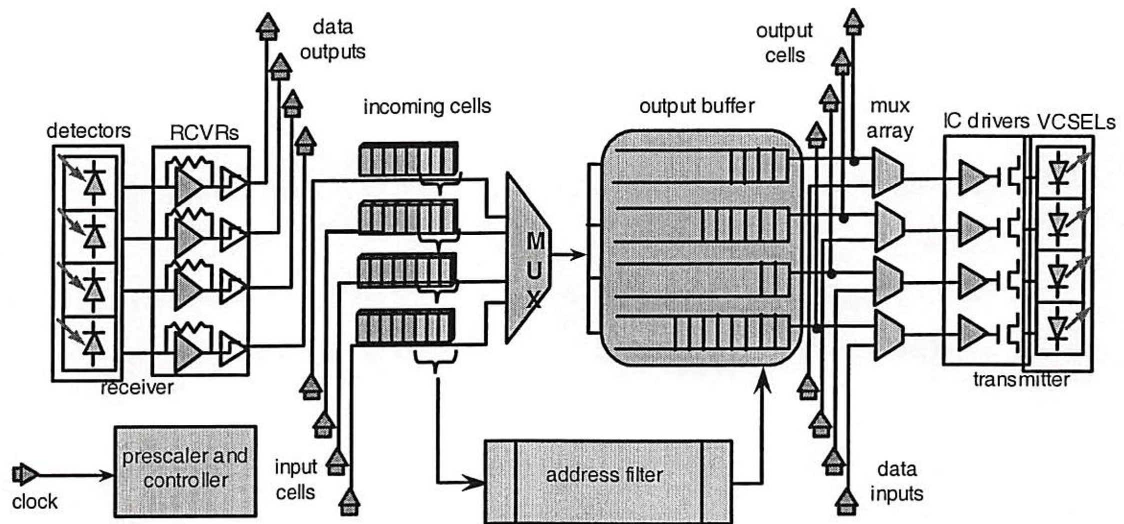


Figure 9-6. Block diagram of UTSi 2000 chip #2.

Inside the chip, four on-chip clocks enable the sequential transmission of the input channels from the receiver array. Each input packet has 8 bits, with the least significant bit (LSB) representing the destination address, the 3rd LSB indicating broadcast, and the remaining bits for the payload. The incoming data packets for each input channel are sampled and sequentially streamed into a single data channel via the multiplexor. The

headers of the packets drop into the address filter and are decoded. The multiplexed data packets are then transmitted to the targeted output channel, or broadcast to all the channels, depending on its header. The output packets can be transmitted electrically through the pads or optically through the VCSEL arrays.

We also designed a 1×4 receiver array with its corresponding electrical output pads. By connecting the receiver array output pads to the inputs of the TDM switch, we obtain a 4×4 electrical switching module having optical inputs and outputs without off-chip high-speed electrical signals.

In addition to the optical inputs and outputs, the chip also has electrical outputs from the TIA receivers, and electrical inputs to the VCSEL drivers. The outputs of the TDMA switch are multiplexed with the electrical inputs to the VCSEL drivers and thus the switch has an option for optical transmission.

A picture of UTSi 2000 chip #2 is shown in Fig 9-7. The bare pads on the left side are optical I/Os. Connected to the upper-left four pads are the transmitter array and receiver array associated with the lower left four pads. The receiver and transmitter arrays share one ESD ring, and the 4×4 TDM switch is confined inside the other ESD ring to the right. This gives a cleaner power supply for the analog front-end receiver and analog back-end VCSEL driver array. In addition, decoupling capacitors are attached to both rings to reduce the switching noise generated from the electrical switch.

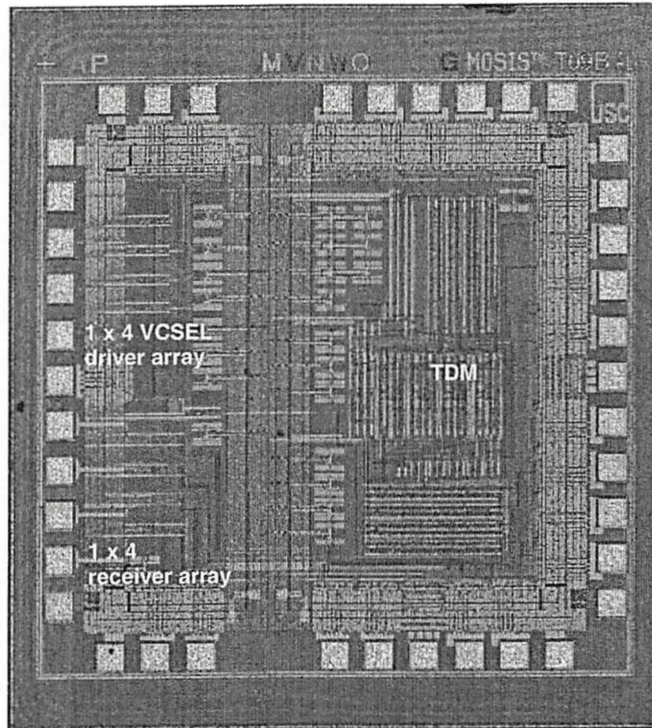


Figure 9-7. Picture of UTSi 2000 chip #2.

9.3.1 Testing of UTSi 2000 Chip #2

UTSi 2000 chip #2 is packaged in a DIP 40 package, through MOSIS. For testing we designed a PCB that is shown in Fig. 9-8 with the chip. The chip is able to drive the VCSEL array and can amplify the detected signals. We mounted Honeywell 4 × 4 VCSEL/MSM array to provide VCSEL outputs the 4 × 4 TDM switch. The applied voltages are 2.5 V for both digital circuits (V_{DD}) and analog circuits (V_{CC}). For simulating PD current we used the external data generator DG 2020A, and applied voltage of 2.5 V with a 50 kΩ resistor. This produces an output current of 50 μA. The

test results are shown in Fig 9-9. From this results we conclude the receiver array is able to amplify the input signals and well observed the open eyes at 15 Mbps.

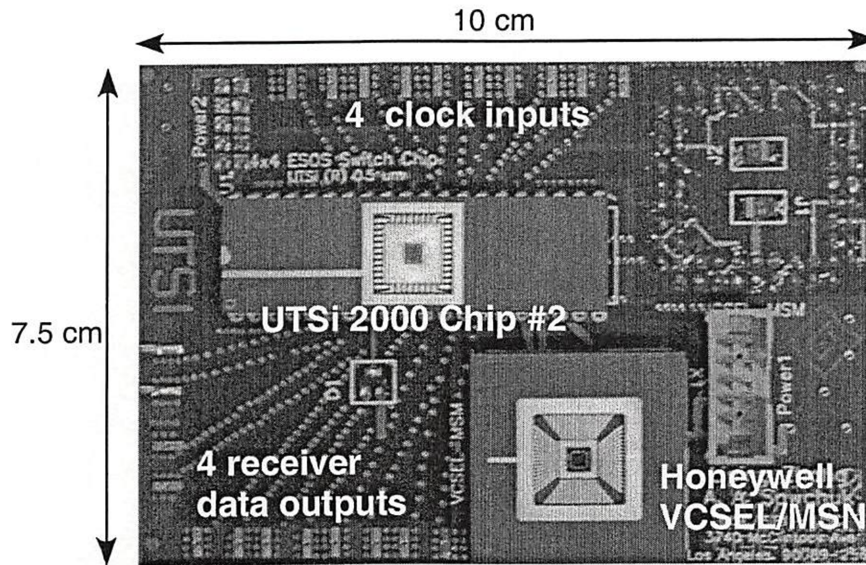
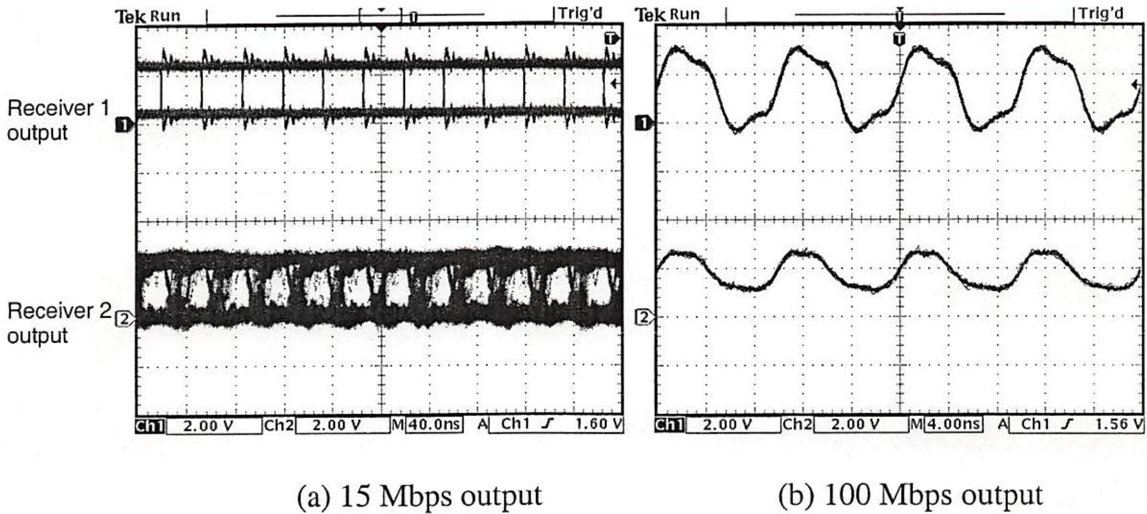


Figure 9-8. UTSi 2000 chip # 2 and Honeywell VCSEL array mounted on a PCB.



(a) 15 Mbps output

(b) 100 Mbps output

Figure 9-9. UTSi 2000 #2 chip receiver outputs.

9.4 UTSi 2001 Chip #1

The block diagram of this chip is shown in Fig 9-10 and Fig 9-11 shows the picture of the chip. One of the most important components in this chip are three different types of optical receiver arrays that are intended for flip-chip bonding to 1×4 Emcore PIN detector arrays. These receiver designs are labeled A, X, and Y in Fig. 9-10. Receiver A is a single-ended transimpedance amplifier with a second-order negative resistance feedback network for high gain and bandwidth as shown in Fig. 9-12. Another design receiver X and Y has low voltage differential signal (LVDS) multi-GHz outputs as shown in Fig. 9-13. An optically clocked 2047-pattern PRBS generator based on TSPC D-flip-flops are included for built-in high frequency self-testing. Eight optical amplifiers have inputs from novel PIN photodiodes labeled a1, ..., a4 and b1, ..., b4 to test monolithic optical receiver designs.

On the left top in Fig. 9-11 are 9 monolithic UTSi PIN photodiodes with integrated receivers. The right corner side is a mixer with two baluns, and a single-ended to differential converter for better noise suppression. A double-edge triggered D-flip-flop based 2047-pattern PRBS generator is next to it. The chip also contains a quadrature-phase inductance-capacitance LC VCO that is located in the bottom half of the chip, as required by single-sideband communication systems.

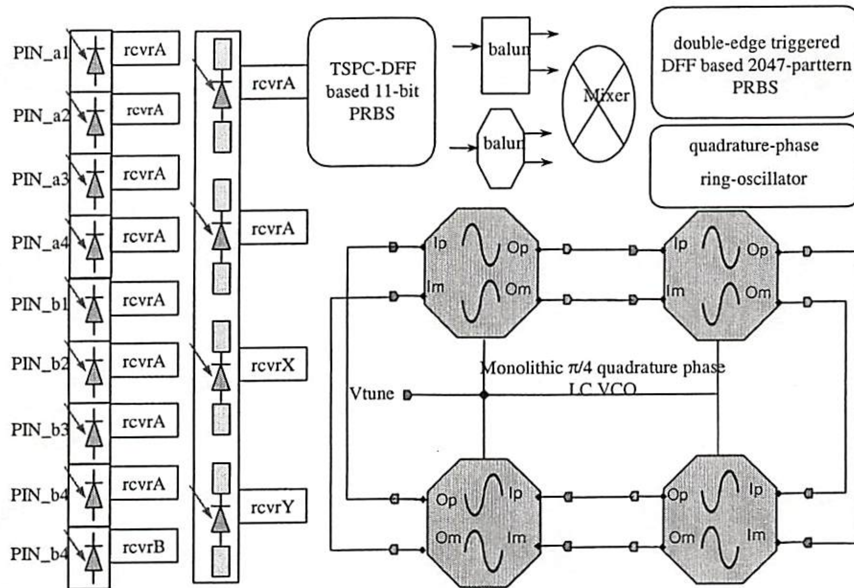


Figure 9-10. Block diagram of UTSi 2001 chip #1.

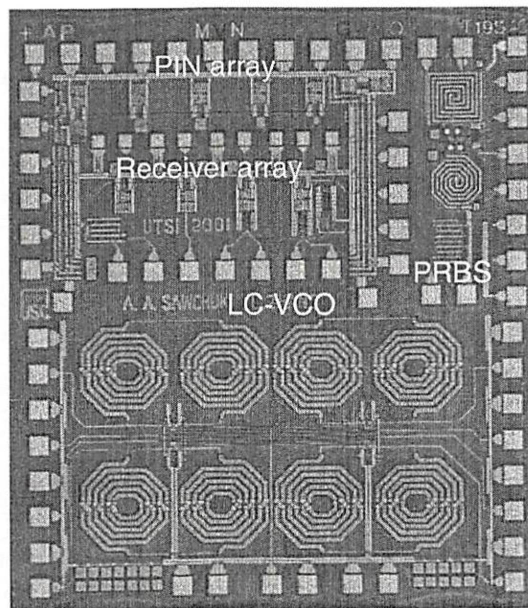


Figure 9-11. Picture of UTSi 2001 chip #1.

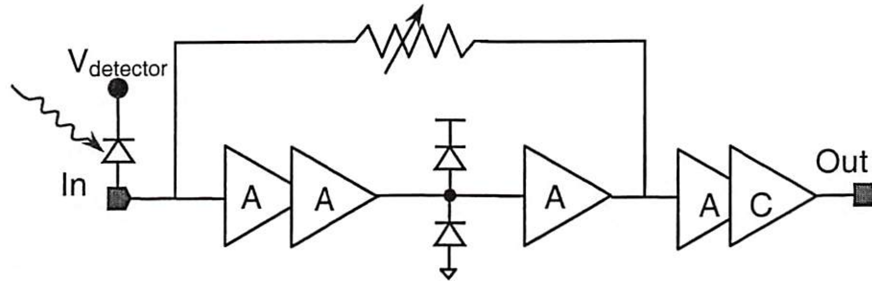


Figure 9-12. Receiver A: a novel single-ended optical receiver with 2nd-order tunable resistance feedback.

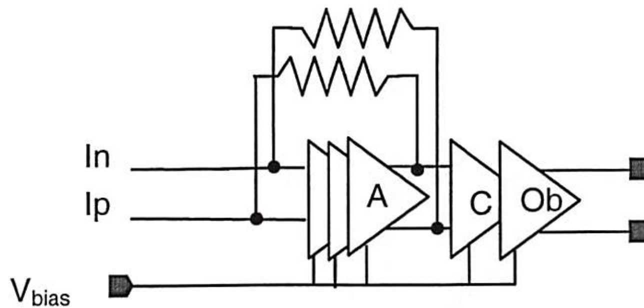


Figure 9-13. Receiver X and Y: an optical receiver design with LVDS outputs.

The VCO design uses novel inductors that was developed using traveling wave superposition and circuit theorems. It cascades an even number of differential oscillator cells as a daisy chain and cross connects one of them to form a ring. The coupling of directly connected pairs of cells makes the next stage in-phase, while the coupling of cross-connected pairs of cells makes the next stage anti-phase. This varactor-based $\pi/4$ quadrature VCO has simulated phase-noise of less than -110 dB at 1 MHz offset

frequency from a ~5 GHz carrier, with less than 3 mW power consumption at nominal 3-V voltage supply. The outputs are 3 V peak-to-peak signals that are enough for mixers to operate in linear region or to drive current mode or low voltage differential logic.

9.4.1 Testing of UTSi 2001 Chip #1

One of the important components of UTSi 2001 chip #1 is receiver array for PIN diodes. The chip can receive the optical current from the detector array and can amplify the signal. An Emcore 1 × 4 PIN diode array was flip chipped on the top surface of the chip. This work was done by Peregrine Semiconductor Corp. The typical specifications of the Emcore 1 × 4 PIN array are summarized in Table 9-2.

Data rate	3.125 GHz
Responsivity	0.5 mA/mW
Active area diameter	70 μm
Crosstalk attenuation	40 dB
Rise/fall time	32/75 ps
Reflectivity	1 %
Capacitance	0.4 pF

Table 9-2. Emcore 1 × 4 PIN array properties.

Figure 9-14 shows the flip-chipped PIN array on UTSi 2001 chip #1 and four PIN apertures are clearly seen through the substrate. We have packaged UTSi 2001 chip #1 in two different ways. For low-speed tests, the chip is wirebonded in a Kyocera 44-pin JLCC as shown in Fig. 9-15 (a) and uses a PLCC socket for the pin connections. For high-speed tests we designed a PCB made of FR4 material with controlled-impedance copper wiring. The bare die is mounted with epoxy and wirebonded directly to pads on the PCB [Fig 9-15 (b)]. The middle part of the PCB is a hole for optical path. The receiver output is shown in Fig 9-16. We measured four different receiver outputs, receiver 1 (design A), 2 (design A), 3 (design X), 4 (design Y) and observed clean eye diagrams at receivers 1, 3, and 4. For the case of receiver 2 we couldn't get clean eye diagram at over 10 Mbps because of noise. However, other receiver outputs indicate the receiver array operates over 10 Mbps with the package.

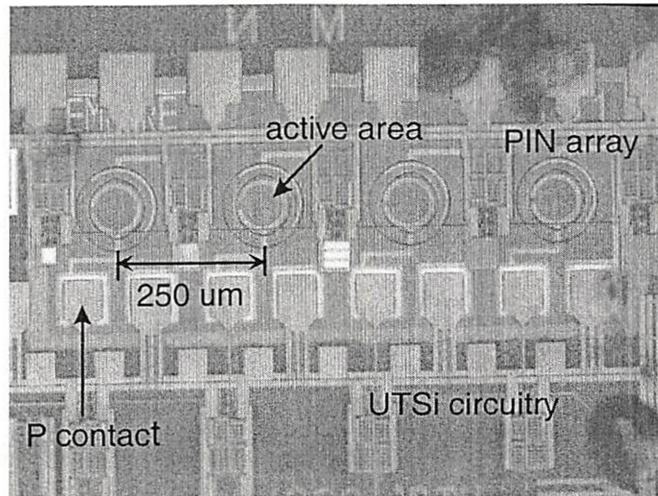
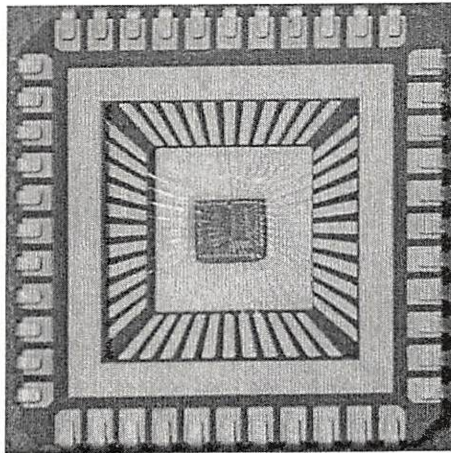
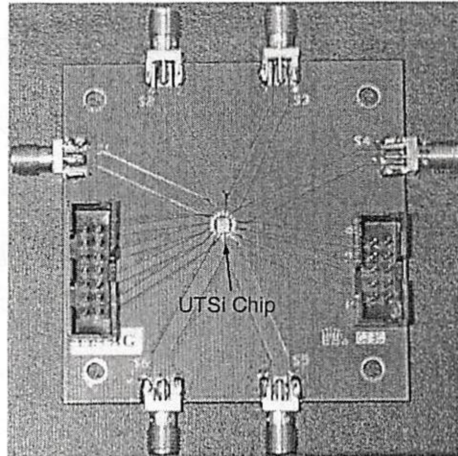


Figure 9-14. Flip-chip bonded PIN array on UTSi 2001 chip #1.



(a) Kyocera JLCC Package.



(b) PCB with SMA connectors

Figure 9-15. UTSi 2001 #1 chip in different packages.

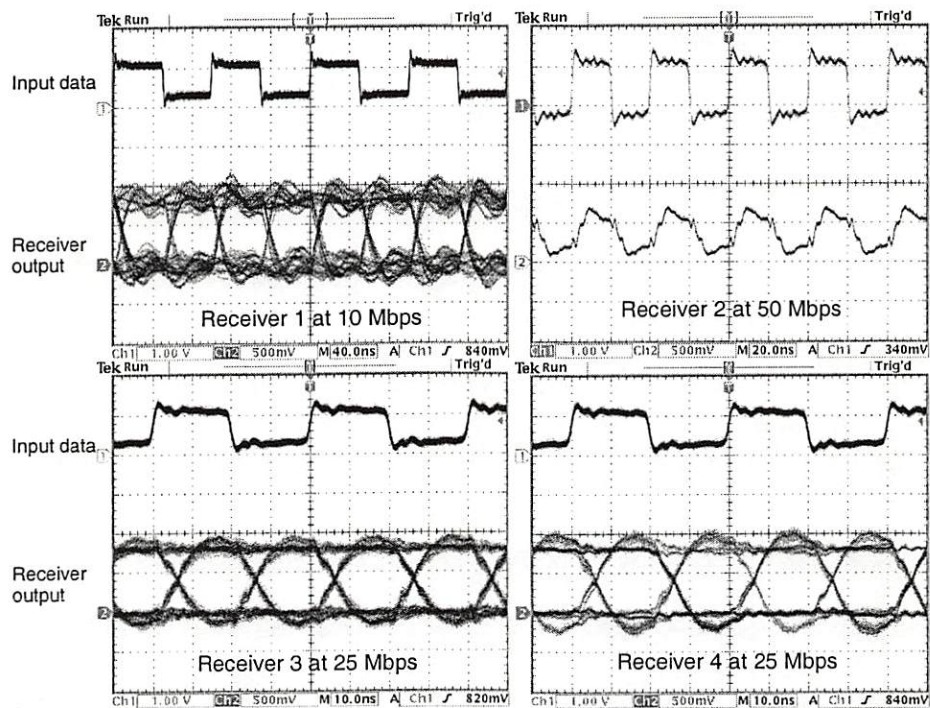


Figure 9-16. The four different receiver outputs of UTSi 2001 chip #1.

9.5 UTSi 2001 Chip #2

UTSi 2001 #2 chip contains four different flip-chip VCSEL drivers, another different LC-VCO design, a compact phase-locked loop (PLL)-based clock/data recovery (CDR) circuits and a multi-GHz frequency divider as shown in Fig 9-17 and 9-18. This VCO is a negative resistance-based balanced differential LC-tank VCO. The VCSEL drivers are based on high-speed low-voltage differential signals (LVDS) and are designed for flip-chip bonding to Emcore 1 × 4 VCSEL array that has a common cathode and individual anode. On the chip, 250 μm-pitch circular bonding pads are designed for the Emcore VCSEL array and Each VCSEL driver has individual inputs and bias voltage adjustments.

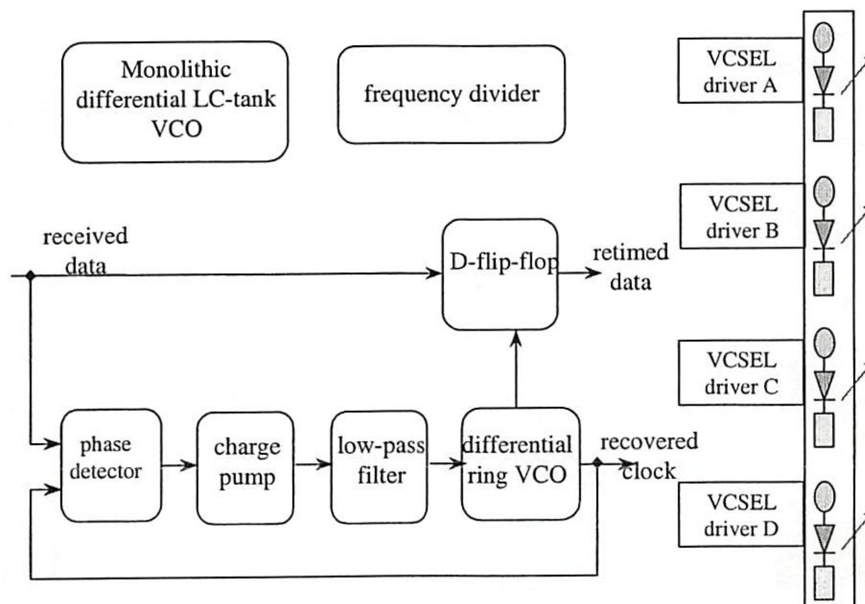


Figure 9-17. Block diagram of UTSi 2001 chip #2.

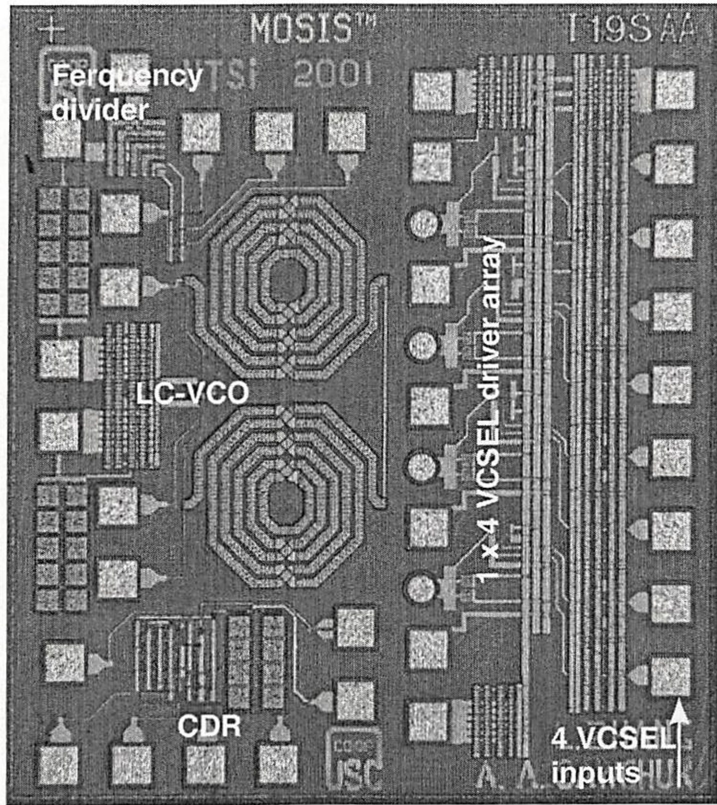


Figure 9-18. Picture of UTSi 2001 chip #2.

9.5.1 Testing of UTSi 2001 Chip #2

An Emcore 1 × 4 VCSEL array was flip-chip bonded onto the UTSi 2001 chip #2 to test its transmitter function. The specifications of the Emcore VCSEL array are summarized in Table 9-3. The flip-chip mounting of the VCSEL array on the UTSi chip was done by Peregrine Semiconductor Corp. Figure 9-19 shows the VCSEL array mounted on the UTSi chip. From the picture the VCSEL apertures are wide open through the substrate. The chip is packaged in a Kyocera 44-pin JLCC for low speed

tests, and a high-speed PCB with controlled-impedance copper wiring was designed for high-speed testing as in Fig 9-20. For the high-speed testing the bare die is mounted with epoxy and wirebonded directly to pads on the PCB. We have measured three different VCSEL driver outputs (drivers 1, 2, and 3) with the JLCC package. The test results are shown in Fig. 9-21 and indicate signal outputs of driver 1 at 10 Mbps, driver 2 at 1.5 Mbps, and driver 3 at 100 Kbps. We couldn't observed eye diagrams at those frequency because of noise.

Emission wavelength	850 nm
Data rate	3.125 GHz
Optical rise and fall time	60 ps
Slope efficiency	0.45 mW/mA
Threshold current	1.5 mA
Forward voltage	1.9 V
Divergence angle	28°

Table 9-3. Emcore 1×4 VCSEL array properties.

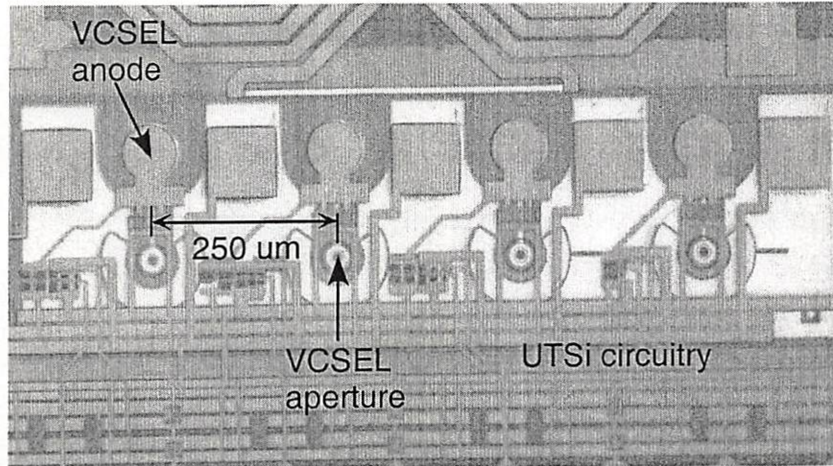
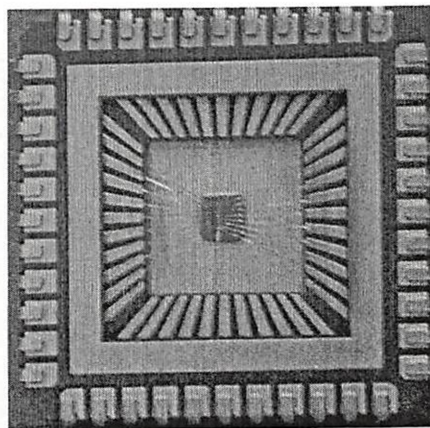
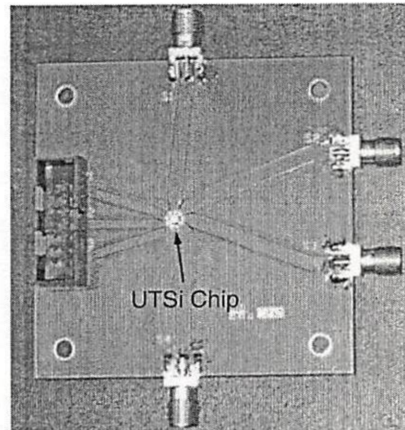


Figure 9-19. Flip-chip bonded VCSEL array on UTSi 2001 chip #2.





(a) Kyocera JLCC Package.

(b) PCB

Figure 9-20. UTSi 2001 chip #2 packages.

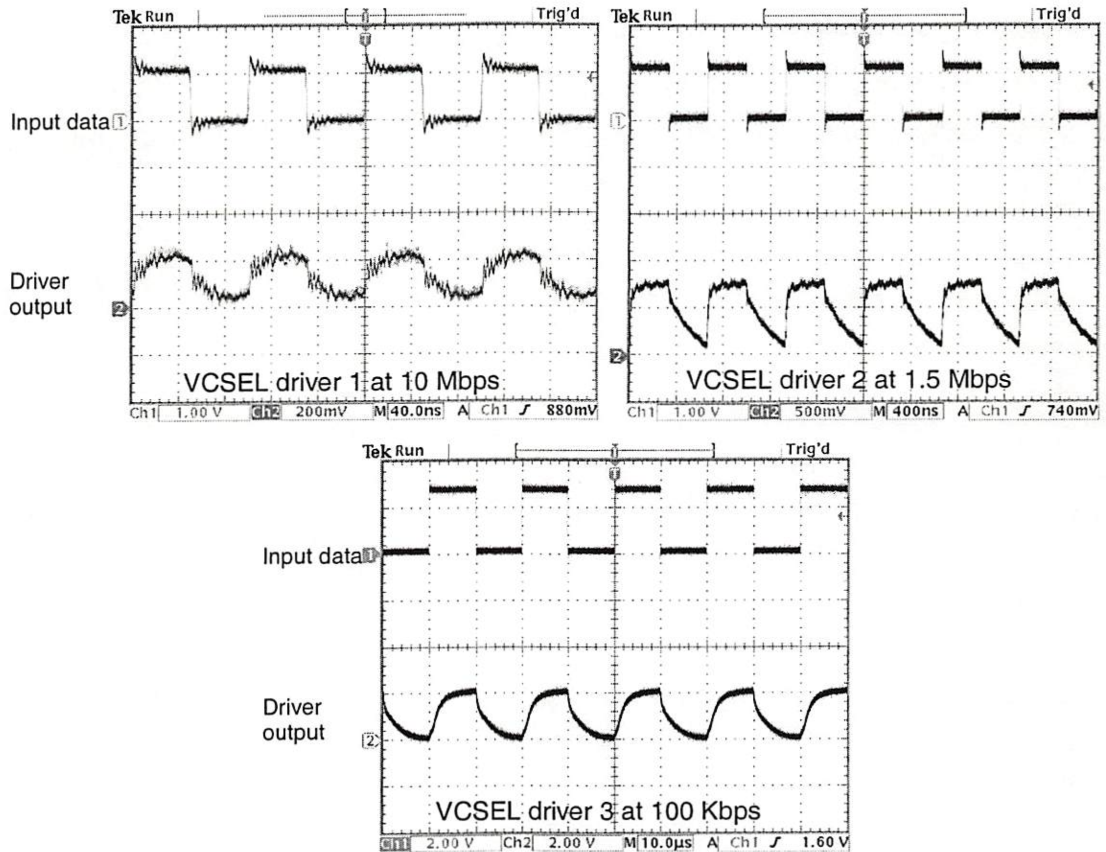


Figure 9-21. Three different VCSEL driver outputs of UTSi 2001 chip #2.

Chapter 10

Conclusions and Future Work

This research has explored optically interconnected optoelectronic-VLSI systems, addressing issues ranging from the physical design, optics, and the system demonstrations of Transpar and UTSi. Optoelectronic-VLSI is a promising technology to implement high performance data communication networks for future multimedia applications and should help alleviate bottlenecks due to bandwidth and delay of electronically interconnected systems.

10.1 Summary

We have designed and demonstrated optoelectronic-VLSI systems and summarize the key contributions as follows.

Modular Integration for Optoelectronic-VLSI: We have developed and tested a modular integration system called Transpar. Transpar is an optical interconnection system that is configured as a high throughput photonic ring network and transfers digital data using 3D optical parallel data packets propagating in free-space or fibers among nodes. The use of FPGA was introduced in Transpar system for reconfigurable networks and processors. Transpar can dynamically implement novel network protocols or reconfigurable processors. The advantage of Transpar modularity is that each

component can be individually tested and characterized before system integration. The disadvantages are the parasitic inductance and capacitance of the PCB and high latency and low power efficiency compared to a monolithic integration. We tested an optical interconnect system based on Transpar at up to 100 Mbps with low noise, and demonstrated two Transpar systems passing packets on a ring network.

Monolithic Integration for Optoelectronic-VLSI: Silicon-on-insulator CMOS is a promising technology for high-speed, low power, and low noise optoelectronic circuitry. We have explored 0.5 μm UTSi CMOS as a SOI technology for monolithic optoelectronic integration. UTSI CMOS enables the integration of different mixed signal components and is well suited for low-cost optical data communication systems. Moreover the transparent sapphire allows transmitting laser light through substrate and enables flip-chip bonding for top-emitting VCSEL or PIN arrays. We have fabricated four different UTSi chips through MOSIS and several PCBs to test high-speed performance of the chips. The UTSi chips contain transceiver arrays, TDM switch, PRBS generator, VCOs, and frequency dividers to perform different functions and network protocol. We demonstrated low noise signal outputs of each UTSi chip with different packages.

Optical Interconnections: Optical interconnections between laser source arrays and detector arrays are an essential part of optoelectronic-VLSI systems. We have investigated free-space optical interconnections using several techniques: bulk refractive lenses, DOEs, and FIGs. These different interconnect methods can be carefully chosen to optimize the performance and functionality of the system. Free-space

interconnections using bulk lenses produces the highest optical power efficiency, a DOE-based system has the smallest volume and offer efficient integration with VCSEL array, and FIGs offer easy optical alignment and advantages in packaging. A detailed computer simulation of waveguide propagation in FIGs was also investigated using RSOft's BeamPROP. The simulations were performed on different *x*-*y*-*z* directional alignments to analyze optical power output in FIGs. The maximum power output is obtained when the center of the laser aperture is well aligned to the core fiber of FIGs. This simulation results are also well supported by the experimental results.

10.2 Future Work

We have shown that optoelectronic-VLSI systems have great potential to improve bandwidth capacity and latency in digital information processing. However, an optimum technology for integrating optics and electronics has not been found yet. Some possible future work is:

(1) Monolithic integration of optoelectronic-VLSI system.

In optoelectronic-VLSI systems, system design for high-yield, low-cost, low noise, and alignment-tolerant is essential. We have designed optoelectronic components such as VCSEL driver, receiver, and VCO, etc. on different chips. We need to integrate these components on a chip to improve functionality and improve the cost and power budget. With flip-chip bonded VCSEL/PIN arrays, we can build a chip with VCSEL driver, receiver, and other devices on a chip. However, the technology for optoelectronic-VLSI integration for future high-speed data rate is still at early stage. Future optoelectronic-

VLSI integration requires (1) low drive voltages for future generations of silicon CMOS (below 1.0 V); (2) reduced crosstalk and improved isolation between digital and optoelectronic transceiver circuitries; (3) a new high-speed circuit techniques with very low jitter to address implementation of 40 Gb/s systems. Only a few picoseconds of timing jitter can have a detrimental effect on the performance of 40 Gb/s system. With these requirements, future photonic system-on-chip (SOC) must be operated at low power, low cost, and high performance.

(2) Low cost, low loss, and reliable optical packaging for optical interconnects.

A number of packaging issues for optical interconnects need to be considered. The requirements of optical packaging are reduction of power dissipation in interconnects, alignment-tolerant, and low-cost. In optical interconnections, optical data packets are transmitted by free-space, waveguides or fiber arrays. In guided-wave interconnection using 1D fiber array shows a possible cost-effective packaging technology. The interface can be connected ribbon-fiber connector such as MTP connector. Free-space interconnection is more suitable for 2D array applications between boards or planes. In this case the light beam is steered by lenses, mirrors, or prisms, and it is very difficult to find a reliable and low-cost packaging solution. FIGs are a good candidate to realize 2D data transmission conveniently, but there is still no known solution to interconnect FIGs with the light source array efficiently. Further work is needed to develop an efficient and low-cost FIG connector.

(3) Modeling and simulation tools for optoelectronic system.

We have shown the modeling and simulations for waveguide propagations in FIGs. Waveguide simulation tools such as BeamPROP can be used to predict the output field in waveguide-based optical systems. In electronic VLSI design, simulation tools such as SPICE are widely used. However there are no complete optoelectronic system level modeling tools to provide system level simulation and analysis with simulation of beam propagation in waveguide paths. Future system level simulation tools must be able to model optical signal propagation with alignment tolerances as well as the dynamics of optoelectronic components such as drivers and receivers. This procedure can then be used to reduce the bit error rate and improve the system optimization.

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Appendix

Beam Propagation Method (BPM)

The beam propagation method (BPM) is a widely used simulation technique for modeling integrated photonic and fiber optic waveguide devices. BPM is a very efficient and powerful method for waveguiding structures with a gradual variation along the propagation direction and can be applied to a complicated geometrical structure. In this appendix we review the basic principle and numerical techniques in the BPM.

The basic idea of the BPM is solving the paraxial approximation of the Helmholtz equation with the scalar filed assumption. The scalar field can be written as

$$E(x, y, z, t) = \Phi(x, y, z)e^{-i\omega t} \tag{1}$$

that satisfies the Helmholtz equation for monochromatic waves,

$$\frac{\partial^2\Phi}{\partial x^2} + \frac{\partial\ \Phi}{\partial y^2} + \frac{\partial^2\Phi}{\partial z^2} + k^2(x, y, z)\Phi = 0 \tag{2}$$

where the wave number k is

$$k = \frac{2\pi n}{\lambda}. \tag{3}$$

For a slowing varying field in which the flow of energy is predominantly along z direction, Φ can be expressed by

$$\Phi(x, y, z) = u(x, y, z)e^{-ik'z}, \tag{4}$$

where

$$k' = \frac{2\pi}{\lambda} n', \tag{5}$$

Here k' is a constant number to be chosen to represent the average phase variation of the field Φ, and is referred as the reference wavenumber. Under these conditions the Helmholtz equation becomes the following equation in slowing varying field,

$$\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} + \frac{\partial^2 u}{\partial z^2} - 2ik' \frac{\partial u}{\partial z} + (k^2 - k'^2)u = 0 \tag{6}$$

This equation is equivalent to Eq. (2). Now we assume that the variation of u with z is sufficiently slow so that the $\frac{\partial^2 u}{\partial z^2}$ term of Eq. (6) can be neglected. This approximation is also called the paraxial approximation. With this approximation Eq. (6) becomes

$$\frac{\partial u}{\partial z} = \frac{1}{2ik'} \left(\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} + (k^2 - k'^2)u \right). \tag{7}$$

This is the basic BPM equation in three-dimensional space.

This approach has certain computational advantages. First this approach allows that the computational grid in a certain direction (i.e. z direction) can be much coarser than other direction (x and y directions). Second, the second order boundary value problem requiring iteration or eigenvalue analysis can be converted to a first order initial value problem that can be solved by simple iteration of Eq. (7). This also can save the computational efficiency and time by a factor of at least of the order N_z (the number of longitudinal grid points) compared to full numerical solution of the Helmholtz equation.

However the slowly varying assumption gives some restrictions to using the approximation. The fields should propagate primarily along one particular direction with small divergence angle. The rate of the index changes along the propagation direction is limited and fields that have a complicated superposition of phase variation may not be accurately modeled. The elimination of the second derivative also eliminates the possibility for backward traveling wave solutions. Thus if the refection is significant this approximation will not be accurate. This problem can be improved by bi-directional BPM [56].