TIA Receiver Arrays (TIAR) with Adjustable Input Threshold and Programmable Inversion

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Overview

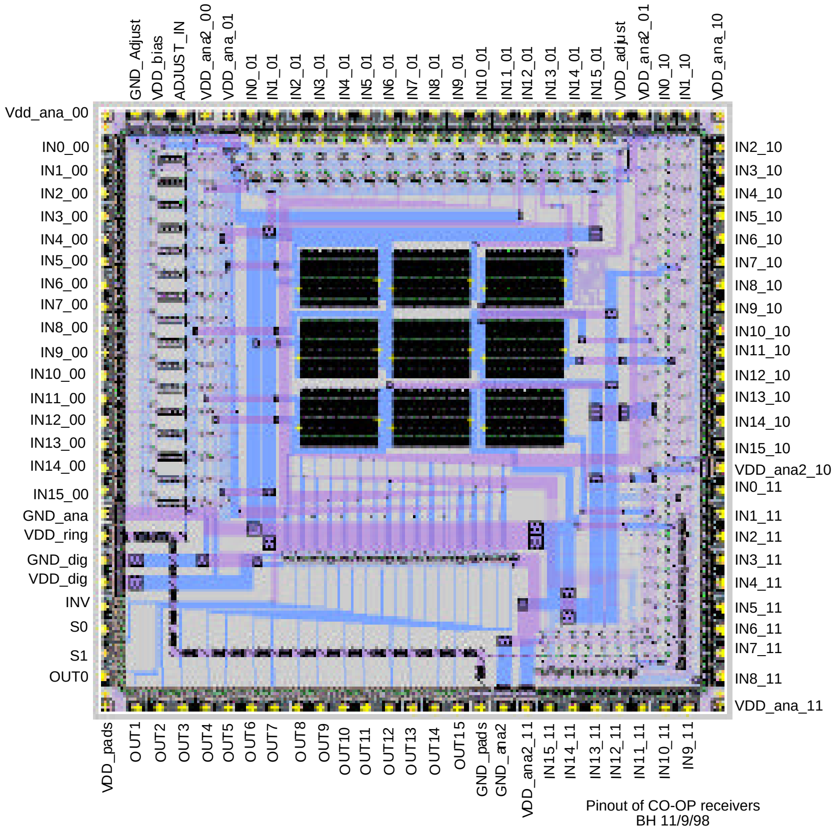
The TransImpedance Amplifier Receiver (TIAR) chip is intended for use with MSM detectors to convert photodetected current signals into 5 V CMOS compatible signals. The TIAR chip contains four distinct designs, 00, 01, 10, and 11, each design including an array of 16 receivers for the detection of 16 parallel channels. TIAR was fabricated using the AMI 1.2 μm process. It is packaged in a 108 pin 12x12 PGA package. We have tested and characterized each of the four different designs up to 2 Mb/s.

The TIAR should be placed on a printed circuit board (PCB) as close as possible to the MSM chip and electrical connections should be made between the output pins of the MSMs and the TIAR input pins. Each of the four TIA designs has a separate set of input pins, but they all share the same set of outputs, to save pins. For this reason, only one of the designs can be used at any given time, as selected by an on-chip multiplexer. Each design has its own power supplies and its own adjustment for the input current threshold (all channels of a design are supplied with the same threshold value). Because the positive direction for the input current depends on the conditions of the input (whether the MSM common pin is tied high or low), the user has the choice of inverting the output, by setting one of the input control bits. This allows the user to choose whether a “one” is a current entering or exiting the TIAR input pins. We recommend that the designs not used are not powered (by grounding the power supplies for the unused designs).

The layout of the chip is shown in Figure 1 below, which indicates the pin names on the padframe. The signification of each pin is indicated in the table below. We have used a large number of separate power supply pins to ensure good separation between the analog and the digital domains on chip. To reduce the number of power supplies required, some of the pins can be connected together on the PCB, or even better at the power supply (in this case, separate routing traces and separate decoupling capacitors should be used on the PCB to allow good decoupling). For example, it would be acceptable to connect all the analog power supplies together (all the VDD_ana*_**) and all the digital supplies together (VDD_)dig and VDD_pads) to separate 5V supplies. For best results, after deciding which design will be used, it is advisable to ground the power supplies for the designs that are not used. In all cases, it is fine to connect the ground pins (GND_ana, GND_ana2, GND_dig, and GND_pads) together at the power supply (not on the PCB). If using designs 00 or 01 VDD_bias can be used as a coarse threshold: adjusting VDD_bias controls the gain of the differential stages in these designs, as shown in Fig. 2. If desired, it could be connected to a separate power supply, or connected together with the VDD_adjust and the analog power supplies. If using one of the other two designs, 10 or 11, VDD_bias need not be connected (it should be grounded).

Pin Description Table

Pin Name	Description
IN0_00, .. IN15_00	current inputs to design 00
IN0_01, .. IN15_01	current inputs to design 01
IN0_10, .. IN15_10	current inputs to design 10
IN0_11, .. IN15_11	current inputs to design 11
OUT0, …, OUT15	digital outputs
INV	digital signal inverts the output when high; used to invert the received data or to achieve the correct data polarity independently of the "positive" direction of the input current (i.e. whether the MSM bias is connected to GND or to Vdd)
S1, S0	selection bits; designs 00, 01, 10, 11 are chosen by setting the selection bits (for example, set S1=1, S0=0 to choose design 10). The bits control a multiplexer that passes only the outputs of the chosen design to the output pins.
VDD_ADJUST	power for the threshold adjusting circuitry, 5V
VDD_PADS	power for the output pins, 5V
VDD_RING	power for the guard ring, 5V
VDD_ana2_00	power for the second stage amplifier, design 00, 5V
VDD_ana2_01	power for the second stage amplifier, design 01, 5V
VDD_ana2_10	power for the second stage amplifier, design 10, 5V
VDD_ana2_11	power for the second stage amplifier, design 11, 5V
VDD_ana_00	power for the first stage amplifier, design 00, 5V
VDD_ana_01	power for the first stage amplifier, design 00, 5V
VDD_ana_10	power for the first stage amplifier, design 00, 5V
VDD_ana_11	power for the first stage amplifier, design 00, 5V
VDD_bias	power for the internal biasing circuitry, 5V
VDD_dig	power for the digital (multiplexing) circuitry, 5V
GND_ADJUST	ground for the threshold adjusting circuitry
GND_ana	ground for the first stage amplifier, common to all designs
GND_ana2	ground for the second stage amplifier, common to all designs
GND_dig	ground for digital (multiplexing) circuitry
GND_pads	ground for the output pins
ADJUST_IN	threshold adjustment input; the choice of input voltage depends on the design used; for example, to achieve a threshold of 10 μA, the voltage should be approximately: · 2.00..2.11V for design 00 · 2.36..2.44V for design 01 · 3.90..4.00V for design 10 · 3.90..4.00V for design 11 These values are provided only as a guide, but the actual adjustment must be made to achieve optimum performance (widest eye opening or lowest bit error rate). Fine adjustments may also be needed as the circuitry heats up while operating.



Pinout of CO-OP receivers
BH 11/9/98

Figure 1 Layout of the TIAR chip indicating the pin names

We included on the chip four different designs, because, depending on the application, one of them may prove better then the others. All designs strive to achieve

- stable, wide bandwidth operation (100 Mb/s), with no oscillations;
- high transimpedance gain (50 kΩ); and
- ability to operate in a PCB environment, with a large input capacitance, 5-10 pF,

which are conflicting requirements, because a large transimpedance gain makes the amplifier more prone to oscillations, and a large input capacitance tends to reduce the available bandwidth. Similarly, a high transimpedance gain makes the circuit more susceptible to crosstalk. Uncertain about the optimum solution, we designed four different topologies, each of which may be better suited to satisfy one or more of the conflicting requirements. Designs 00 and 01 use differential stages, which are relatively immune to noise from the power supplies, while the two other designs use only inverter amplifiers, which have higher gain. Designs 01 and 11 use multistage feedback, which offers higher gain but less stable operation, while the designs 00 and 10 have single stage feedback, unconditionally stable. Additionally, to avoid input-to-output couplings that may make the amplifiers oscillate, we separated the power supplies for the analog input stage, the analog output stage and the digital stage and we used liberally guard rings.

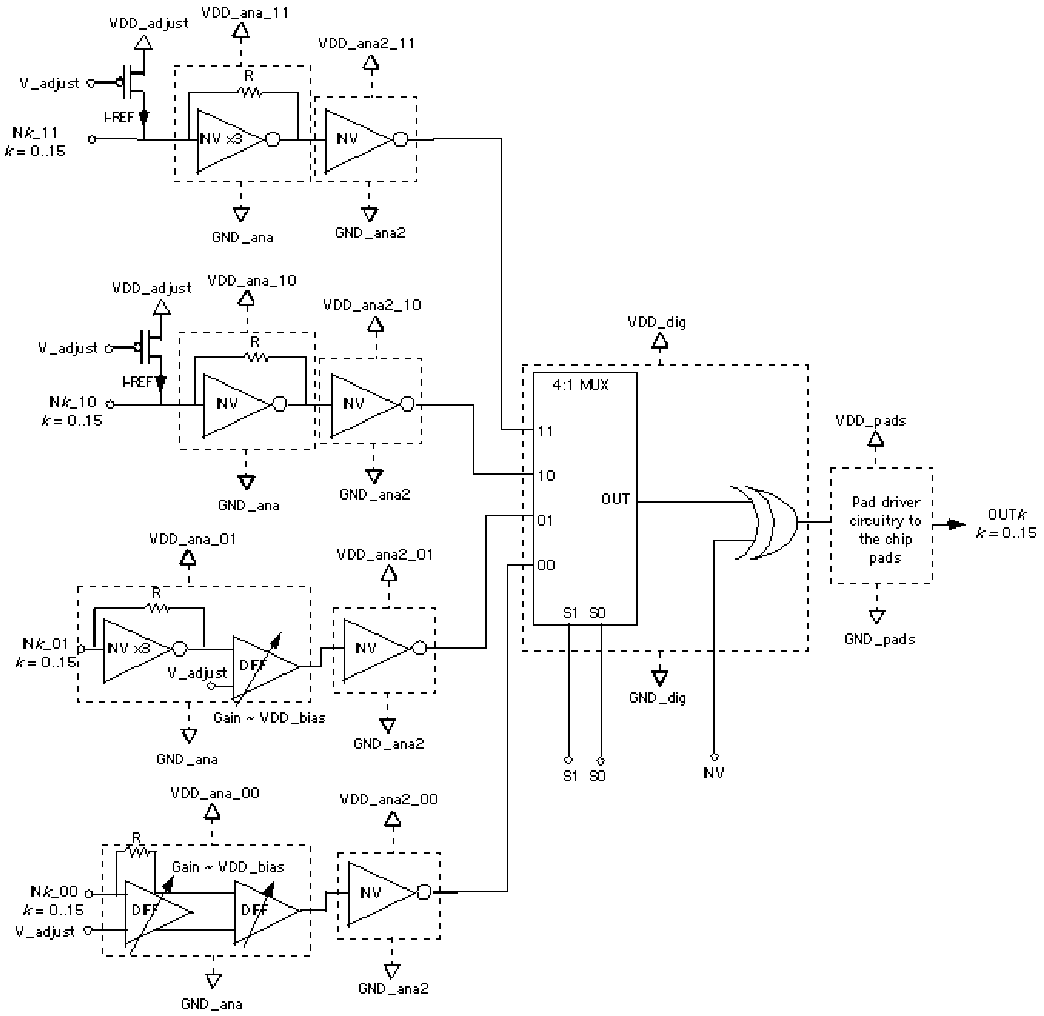


Figure 2 Block diagram of a single channel on the TIAR chip, showing the four different receiver topologies and the final multiplexing. Also indicated are the names of the pins for the power supplies (at the top and bottom of the dashed boxes surrounding each stage).

The block diagram in Fig. 2 above is provided to show the details of the multiplexing, as well as the power supply pin names connected to the different receiver blocks on the chip. Sixteen parallel and independent such channels are used on the chip. All sixteen channels in each design share the same thresholding circuitry and the same set of power supplies. The designs 01 and 11 are potentially less stable, and although they have been compensated with on-chip capacitors, they may need an additional capacitance on the input if they oscillate.

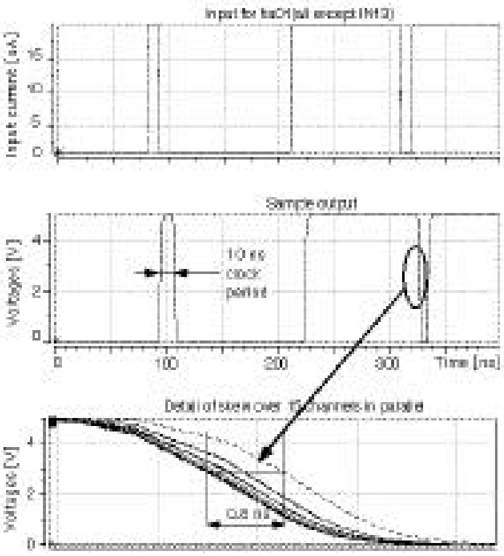


Figure 3 H-Spice simulations on tia01.

We simulated all except for design 00 at chip level at 100 Mb/s, with full capacitive loading of 5 pF on both the input and the output pins. The simulation included the chip parasitics, both capacitive and inductive. Design 00 operated correctly as a single channel, but did not operate as an array and with chip parasitics included (it did operate correctly once it was fabricated). We show the results of the H-Spice simulations for designs 01 through 10 in Figures 3 through 5.

We simulated the operation of the receivers in what we believe is the worst case scenario. If there is any coupling between the channels, this coupling would be worse when all but one channel are switching synchronously and the 16th channel is idle. We would expect that the idle channel would have some parasitic switching if the coupling is significant. In our case, left channel 13 idle and we drove all other channels with the same input current waveform. In each of the three figures, the top curve shows the input current (from the MSM) driving the receiver. The middle curve shows the superimposed output curves for the 15 channels driven with the input waveform and the last curve is a detail showing the skew between the channels. Channel 13 (the idle channel testing for the crosstalk) was perfectly flat to mV scales and is not shown in the figures.

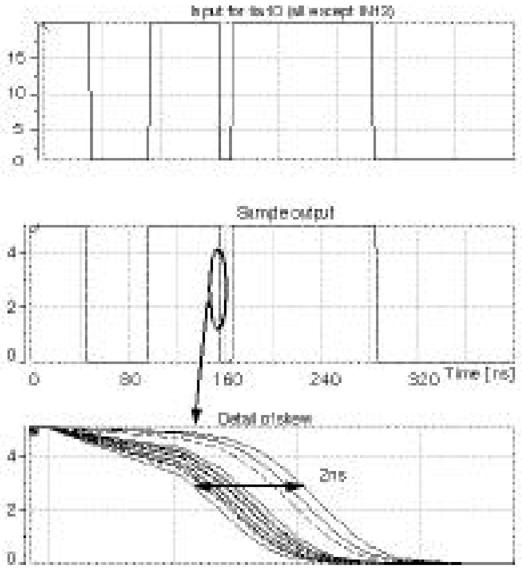


Figure 4 H-Spice simulations on tia10.

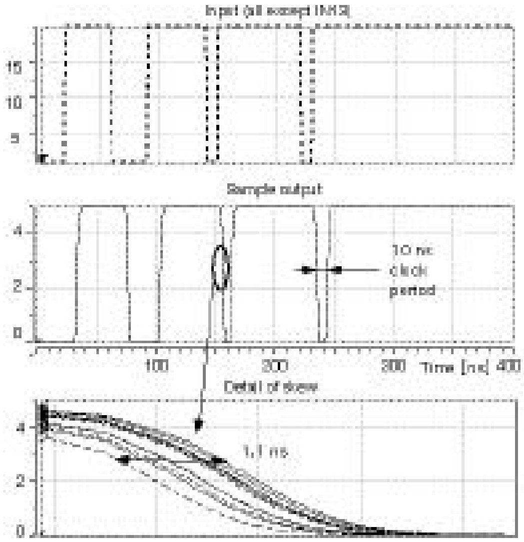


Figure 5 H-Spice simulations on tia11.