USC-SIPI REPORT #153

Integration of Technology-Based Design Systems for VLSI Circuits

by

Chung-Ping Wan

February 1990

Signal and Image Processing Institute
UNIVERSITY OF SOUTHERN CALIFORNIA
Department of Electrical Engineering-Systems
Powell Hall of Engineering
University Park/MC-0272
Los Angeles, CA 90089 U.S.A.

Copyright 1990 Chung-Ping Wan

Acknowledgment

I would like to express my appreciation to my research advisor, Professor Bing J. Sheu, for his guidance. I would also like to thank Professor Murray Gershenzon and Professor Ming-Deh Huang for serving on my dissertation committee. Their valuable comments and suggestions are very helpful in preparing the final version of this dissertation.

I would like to thank Hewlett-Packard Company for donation of the TECAP-3 program; The MOSIS Service at USC/Information Sciences Institute, Marina del Rey, CA, for its generous support; Stanford University, Stanford, CA, for the release of the PISCES and SUPREM programs; and University of California, Berkeley, for the release of the SPICE-3 program.

Valuable suggestions and assistance from my fellow graduate students in MOS VLSI Devices and Circuits group in PCE-210 are highly appreciated. Thanks are also given to Je-Hurn Shieh for help with the MESGEN program; to Antony H. Fung for helpful discussions on sensitive SPICE model parameters; to Ming Hsu for stimulating discussions on model parameter extraction; to Chih-Ching Shih for help with the capacitance measurement setup; and to Shih-Lien Lu for installing the PISCES and SUPREM programs.

This research was supported by National Science Foundation under Grant MIP-8710825, and by industrial grants from AT&T Company, Meta-Software Inc., and TRW Inc.

Last, but not the least, I would like to thank my parents and my wife for their support and encouragement. It is impossible for me to finish this dissertation without their constant encouragement.

Table of Contents

Chapter 1 - INTRODUCTION 1
Chapter 2 - COMPUTER-INTEGRATED MANUFACTURING SYSTEMS FOR VLSI CIRCUITS 6

2.1. Process-Level CAD Tools 7

2.1.1. Process Modeling 8

2.1.2. Simulation Tools 10

2.2. Device-Level CAD Tools 12

2.2.1. Semiconductor Equations 12

2.2.2. Simulation Tools 14

2.3. Circuit-Level CAD Tools 14

2.3.1. Equation Formulation 17

2.3.2. Simulation Tools 18

2.4. Equipment Modeling 18

Chapter 3 - INTEGRATION OF TECHNOLOGY CAD TOOLS 19

3.1. The Need 20

3.2. Integration Techniques for Device-to-Circuit Simulation 22

3.2.1. Table Look-Up Method 22

3.2.2. Conventional Parameter Extraction Method 23

3.2.3. Mixed-Mode Simulation Method 23

3.2.4. Smart Link Method 24

Chapter 4 - PARGEN: AN INTERFACE PROGRAM FOR PISCES-II AND SPICE-3 25

4.1. PARGEN 25

4.1.1. MOSGEN 27

4.1.2. MESGEN 32

4.2. Parameter Calculation 36

4.2.1. MOSFET Parameter Calculation 36

4.2.2. MESFET Parameter Calculation 41

4.3. PARGEN Results 41

4.3.1. MOSGEN Results 41

4.3.2. MESGEN Results 45

4.4. Applications 47

4.4.1. Integrated Simulation Environment 50

4.4.2. Determination of Geometric Dependences of Submicron MOS Transistor Parameters 61

Chapter 5 - SENSITIVE SPICE PARAMETERS FOR VLSI DESIGN 69

5.1. SPICE Modeling for VLSI Circuit Analysis 70

5.1.1. Circuit-Level Modeling Requirements 70

5.1.2. SPICE Built-In MOS Transistor Models 72

5.2. Parameter Extraction for Different Fabrication Technologies 73

5.3. Sensitive SPICE Parameter Subset 79

5.3.1. Sensitivity Analysis 79

5.3.2. Sensitivity Analysis Results 83

Chapter 6 - EFFICIENT SPICE TEMPERATURE DEPENDENCE MODELING 89

6.1. Temperature Dependence Modeling 90

6.1.1. Sensitive BSIM Parameter Subset 90

6.1.2. The New Approach 91

6.2. Experimental Results and Discussion 93

6.3. Theoretical Basis for BSIM Temperature Dependence 105

Chapter 7 - CONCLUSION 108

7.1. Summary 108

7.2. Suggested Future Work 109

7.2.1. Parameter Calculation for Micron/Submicron MOSFET Models 109

7.2.2. Parameter Calculation for Bipolar Transistor Models 110

Appendix A - PARGEN USER GUIDE 111

Appendix B - A NEW METHOD TO DETERMINE EFFECTIVE CHANNEL WIDTHS OF MOS TRANSISTORS 118

Appendix C - PARGEN PROGRAM LISTING 135

References 156

List of Figures

Figure 1–1: The hierarchical relationship in VLSI design. 2
Figure 1–2: Simulation-assisted technology development. 4
Figure 2–1: A selective region for process modeling and simulation. ... 9
Figure 2–2: Flowchart of the Newton's method. 15
Figure 2–3: Flowchart of the Gummel's method. 16
Figure 3–1: Flowchart of the conventional IC design approach. 21
Figure 4–1: Integrated simulation environment which allows a designer to examine how a microscopic fabrication variable affects final circuit performance and product yield. PARGEN is the interface program between PISCES and SPICE. 26
Figure 4–2: Organization of the PARGEN program. 28
Figure 4–3: Flowchart of the MOSGEN module which generates SPICE parameters for the Level-2 model. 31
Figure 4–4: Cross section of a GaAs MESFET. 35
Figure 4–5: Cross section of an MOS transistor highlighting the two-dimensional area for the calculation of inversion charge. ... 37
Figure 4–6: Cross section of an N-channel MOS transistor used in PISCES device simulation. 42
Figure 4–7: Comparison of I-V characteristics between SPICE simulation results with MOSGEN-extracted parameters and the direct PISCES data for an $L_{eff} = 1.1\ \mu m$ transistor. The Level-2 model is used. 43
Figure 4–8: Comparison of I-V characteristics between SPICE simulation results with TECAP-extracted parameters and the same set of PISCES data as in Figure 4-7. The Level-2 model is used. 44
Figure 4–9: Comparison of transistor I-V characteristics between MESGEN-SPICE simulation results and PISCES data for an $L = 0.8\ \mu m$ transistor. 48
Figure 4–10: Potential applications of the integrated simulation environment. 49

Figure 4–11: Simulated boron doping profiles on a silicon wafer for two ion implantation cases. The substrate doping is 1×10^{16} cm^{-3}. 51
Figure 4–12: Two-dimensional carrier distributions from PISCES simulation. (a) An implantation dose of 6×10^{11} cm^{-2} and an energy of 20 KeV. (b) An implantation dose of 5×10^{11} cm^{-2} and an energy of 30 KeV. 52
Figure 4–13: Circuit schematic of the core circuitry for a single-stage CMOS amplifier. 53
Figure 4–14: Plots of the open-loop voltage gain versus the boron implantation energy. The integrated simulation environment is used to produce the results. 55
Figure 4–15: A GaAs inverter circuit with four MESFET's and two level-shifting diodes. 56
Figure 4–16: The inverter transient responses with different transistor active-layer thicknesses. Δ: 0.19 μm, O: 0.17 μm, x: 0.15 μm. The solid line represents the input waveform. 57
Figure 4–17: The inverter transfer characteristics with different transistor active-layer thicknesses. Δ: 0.19 μm, O: 0.17 μm, x: 0.15 μm. 58
Figure 4–18: Circuit schematic of a single-stage GaAs Op-Amp. 59
Figure 4–19: The effect of the implantation dose on the open-loop voltage gain. 60
Figure 4–20: Electron concentration contours for an N-type LDD MOS transistor. (a) All terminals are grounded. (b) V_{GS} = 1.5 V, V_{DS} = 0 V, and V_{BS} = 0 V. 63
Figure 4–21: The plot of ΔV_{T0} versus $1/L_{eff}$. A straight line is fitted through the data points with the least-square-error technique. (a) PISCES-extracted results. The correlation coefficient is 0.998. (b) Measured data. The correlation coefficient is 0.991. 64
Figure 4–22: The plot of body-effect coefficient versus $1/L_{eff}$. The insert shows the logarithm of body-effect coefficient versus $1/L_{eff}$. (a) PISCES-extracted results. The correlation coefficient in the insert is -0.996. (b) Measured data. The correlation coefficient in the insert is -0.991. 66

Figure 4–23: The plot of the parameter C versus the peak doping concentration in the channel. 67

Figure 5–1: Three key considerations for SPICE transistor modeling. .. 71

Figure 5–2: Two-dimensional wafer mapping information. The test wafer was fabricated by a 1.2–μm technology. (a) Threshold voltage. (b) Body-effect coefficient. 77

Figure 5–3: Across-wafer variations of the threshold voltage and body-effect coefficient for (a) die locations A to G, and (b) die locations X, Y, D, and Z. 78

Figure 5–4: Two-dimensional wafer mapping information. The test wafer was fabricated by a 1.2–μm technology. (a) Gate-oxide thickness. (b) Channel-length reduction. 80

Figure 5–5: Across-wafer variations of the gate-oxide thickness and channel -length reduction for (a) die locations A to G, and (b) die locations X, Y, D, and Z. 81

Figure 5–6: Comparison of measured data and the simulated results using the Level-4 model. (a) A W/L = 1.4 μm/1.2 μm transistor. (b) A W/L = 4.5 μm/0.7 μm transistor. 82

Figure 6–1: Circuit performance verification procedure using the sensitive SPICE parameter subset approach. 92

Figure 6–2: Updating of the Level-4 model parameter values is done prior to circuit analysis at each given temperature. 94

Figure 6–3: Measured temperature dependences of sensitive Level-4 model parameters with W/L = 4.8 μm/1.2 μm (× × ×) and W/L = 14.4 μm/3.6 μm (filled Δ). Room temperature (298°K) is indicated by an arrow. 95

Figure 6–4: A comparison of the measured and simulated results for the temperature dependence of the threshold voltage. The Level-2 model is used in the simulation for an N-channel MOS transistor. 98

Figure 6–5: Comparisons of the measured and simulated I-V characteristics for a W/L = 14.4 μm/1.2 μm transistor at 70°C. (a) In simulation, only the temperature control command is used to update Level-2 model parameter values through SPICE. (b) In simulation, parameter values for the sensitive Level-2 model subset have been updated from new extraction. 99

Figure 6–6: Comparisons of the measured and simulated I-V characteristics for a W/L = 16 μm/2 μm transistor at 77°K. (a) In simulation, only the temperature control command is used to update Level-4 model parameter values through SPICE. (b) In simulation, parameter values for the sensitive Level-4 model subset have been updated from new extraction. 101

Figure 6–7: A comparison of the measured and simulated I-V characteristics at 70°C. In simulation, parameter values for the sensitive Level-4 model subset have been updated through the preprocessor. 102

Figure 6–8: Measured and simulated voltage transfer characteristics of two CMOS inverters at 70°C. 103

Figure 6–9: Measured and simulated frequencies of a 31-stage ring oscillator at different operating temperatures. "Δ Δ Δ": Using temperature control command."+++": Using the sensitive Level-4 model parameter subset approach. "• • •": Using all updated parameter values at 70°C. 104

Figure A–1: PISCES input deck to generate the data needed by MOSGEN. 114

Figure A–2: A sample MOSGEN.IN file. 116

Figure B–1: The resistance R_M versus L_{mask} for test wafer #1. 123

Figure B–2: The channel-length reduction ΔL versus $V_{GS} - V_{TH}$ for test wafer #2. 124

Figure B–3: The source/drain series resistance R_{SD} versus $V_{GS} - V_{TH}$ for test wafer #2. 125

Figure B–4: The channel conductance g_{CH} versus W_{mask} for test wafer #1 using the new method. The channel-width reduction ΔW is determined to be –0.13 μm. 126

Figure B–5: The conductance g_M versus W_{mask} for test wafer #1 using Ma's method. The channel-width reduction ΔW is determined to be –0.12 μm. 127

Figure B–6: The channel conductance g_{CH} versus W_{mask} for test wafer #2 using the new method. The channel-width reduction ΔW is determined to be 0.25 μm. 129

Figure B–7: The conductance g_M versus W_{mask} for test wafer #2 using Ma's method. 130

Figure B–8: Intrinsic gate capacitance versus W_{mask} for test wafer #1. The channel-width reduction ΔW is determined to be $-0.12\ \mu m$. 131

Figure B–9: Intrinsic gate capacitance versus W_{mask} for test wafer #2. The channel-width reduction ΔW is determined to be $0.18\ \mu m$. 132

Figure B–10: Measured capacitance (uncalibrated) versus V_{GS} for the capacitance method. 134

List of Tables

Table 4–1: Biasing conditions for PISCES runs to be used by MOSGEN. (An N-channel MOSFET is assumed.) 29
Table 4–2: Biasing conditions for PISCES runs to be used by MESGEN. 33
Table 4–3: MOSGEN-extracted SPICE Level-2 MOSFET model parameters. 46
Table 5–1: Comparison of important features among various existing SPICE MOSFET models. 74
Table 5–2: Sensitivity analysis results for the Level-2 MOSFET model parameters in a 3–μm technology. 85
Table 5–3: Sensitivity analysis results for the Level-2 MOSFET model parameters in a 1.2–μm technology. 86
Table 5–4: Sensitivity analysis results for the Level-4 MOSFET model parameters in a 2–μm technology. 87
Table 5–5: Sensitivity analysis results for the Level-4 MOSFET model parameters in a 1.2–μm technology. 88
Table 6–1: Temperature dependences of sensitive BSIM parameters. 96
Table B–1: Comparison of ΔW determined by the capacitance method and the new resistive method. 133

Abstract

Integration of technology-based design systems is strongly needed for the manufacturing of very-large-scale integrated circuits. The computer-aided design program PARGEN which provides accurate and efficient interface between the device simulator PISCES-IIB and the circuit simulator SPICE-3C1 in the technology-based design system is described. Algorithms to calculate parameter values for the built-in MOSFET and MESFET models have been developed and incorporated into this interface program. Only six device simulation results are required to extract a complete set of the popular Level-2 MOSFET model parameters and four device simulation results are needed for the MESFET model in the circuit simulator. This interface program, together with the process simulator, device simulator, and circuit simulator, form an integrated simulation environment for computer-integrated manufacturing of microelectronic chips. Such an integrated simulation environment greatly facilitates the designers to examine just how a microscopic fabrication variable, such as the implantation dose, affects final device and circuit performance and product yield. A methodology for efficient circuit modeling and simulation in the integrated simulation environment is also described. A subset of circuit-level sensitive parameters which have large effects on simulated transistor output characteristics is used in this methodology. The sensitive model parameters are identified through a sensitivity analysis. This methodology has been applied to the temperature dependence modeling of the BSIM (Berkeley short-channel IGFET model) for MOS transistors in the circuit simulators. Updating of model parameter values for the sensitive parameter subset is performed prior to circuit simulation at each given temperature. For a 1.2-μm CMOS fabrication process, the sensitive parameter subset for temperature

effects consists of only eight out of the sixty-seven BSIM parameters. Circuit simulation results using this sensitive model parameter subset approach agree with experimental data on transistor output characteristics, inverter transfer characteristics, and oscillation frequency of a 31-stage ring oscillator.

Chapter 1

Introduction

Rapid advances in very-large-scale-integration (VLSI) technology have resulted in the reduction of minimum feature sizes from several microns to submicrons over the past fifteen years. By the year 2000, the feature size can be reduced to 0.15 μm in an advanced CMOS process and a density of 10^8 transistors per chip can be achieved for memory devices [1.1]. With such a high level of integration, a complete electronic system can be fabricated onto a single chip. To successfully design complex VLSI circuits, extensive use of computer-aided design (CAD) tools is a necessity. The CAD tools are invaluable in integrated circuit designs.

Figure 1-1 shows a hierarchical method for VLSI design. The behavioral description of the system is transformed into an integrated circuit following several synthesis stages: high level synthesis, structural synthesis, physical design, and process design. An analysis step is performed after each synthesis stage to verify that the new description is functionally equivalent to the more abstract input description. If these descriptions do not match, changes are made in previous descriptions by following the appropriate feedback path to any of the earlier synthesis stages. In the design sequence, computer simulators are used for the process, device, circuit, logic, and behavioral simulations. Layout, placement, and routing tools are used to aid the physical design of VLSI circuits. These CAD tools play a critical role in the successful designs of VLSI systems.

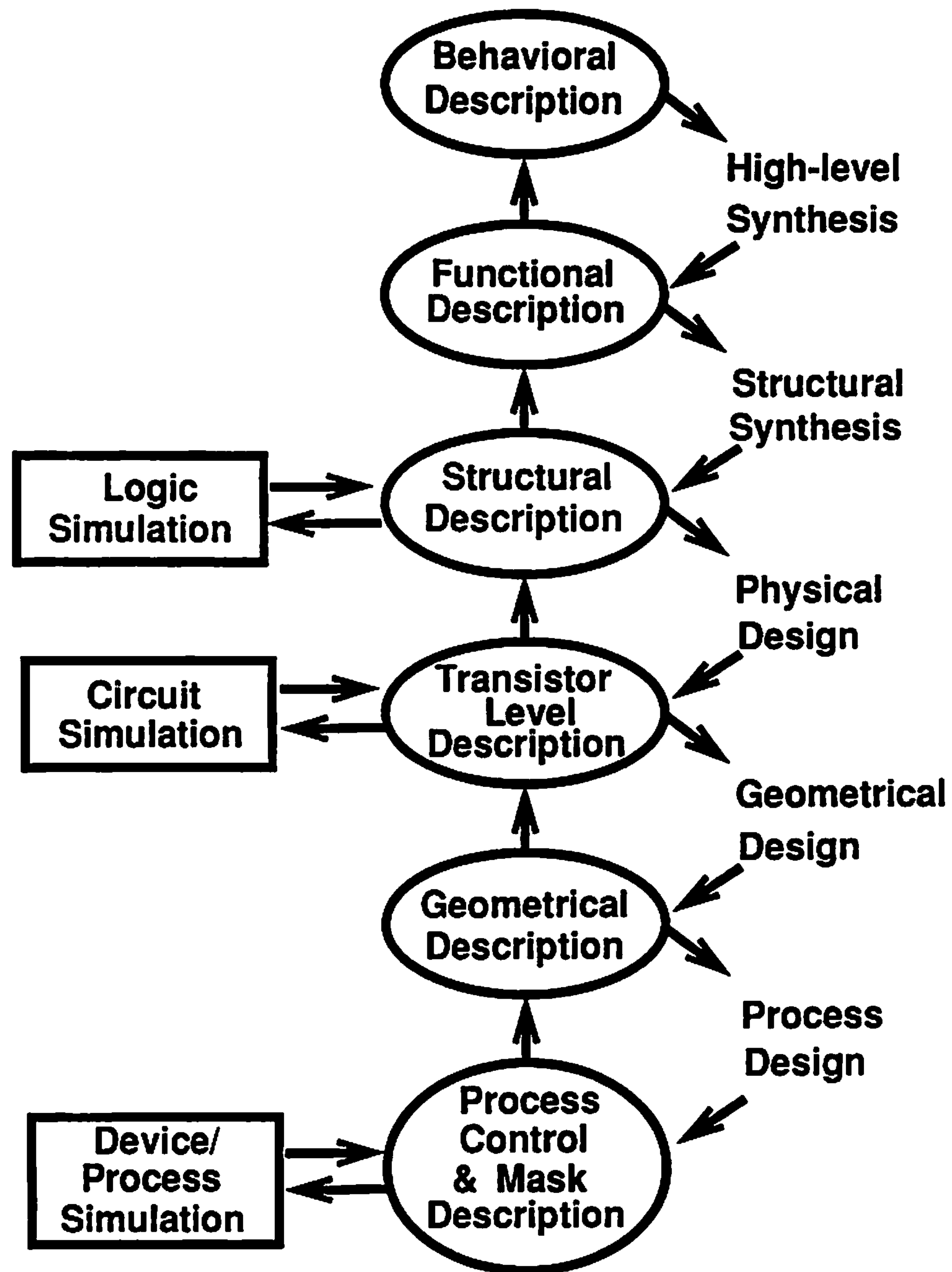


Figure 1-1 The hierarchical relationship in VLSI design.

The rapid rate of change in process technologies also mandates extensive uses of CAD tools for new technology development. The development of new technology traditionally has been guided by the experimental approach. Starting with an existing process, critical steps are modified and this modified process is realized by fabricating several lots. Finished test structures are then evaluated carefully to examine whether the design goals are achieved. This trial-and-error procedure requires many iterations to optimize a new process. However, with proper simulation programs, the development time and cost can be greatly reduced. As shown in Figure 1-2, the process design can be verified through computer simulations and adequate modifications to the process design can be made to obtain the desired design.

One key issue in the integrated-circuit fabrication is the yield and performance of VLSI circuits. Increasing emphasis on the yield and performance of VLSI design has driven the semiconductor industry toward automation of manufacturing facilities to fabricate complex integrated circuits with minimum feature sizes in the submicron range. An important concern in the complete automation of semiconductor manufacturing environment involves the integration of CAD tools to provide quick simulation so that the product yield can be optimized prior to fabrication. The integration of CAD tools requires the coupling between process, device, and circuit simulators.

The particular interest of this dissertation is the integration of technology-based design systems for VLSI circuits. One contribution of this work is the development of an efficient approach to coupling the device and circuit simulators. Different approaches have been developed to link the device and circuit simulators by other researchers [1.2-1.5]. However, their approaches require hundreds of device simulation runs and the computational cost is very high. In our approach, only several device simulation runs are required to accomplish the integration task using the newly developed computer-aided design program. The incorporation of this interface program into the simulation environment makes possible the efficient integration of process, device, and circuit

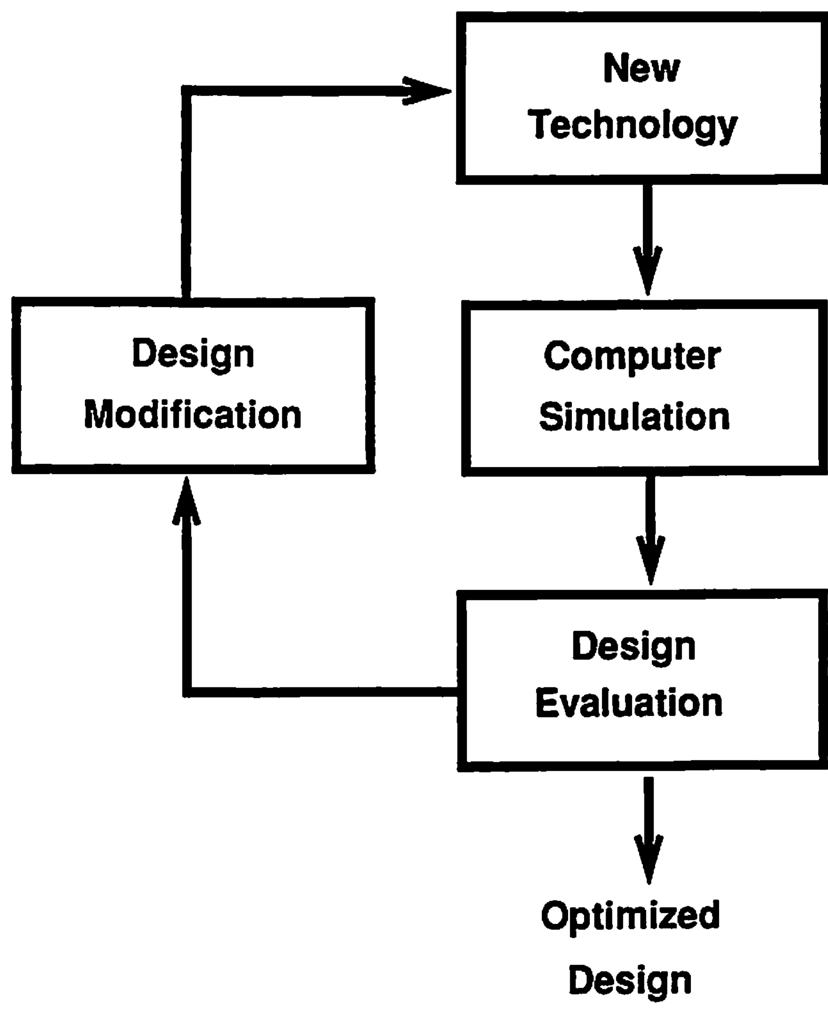


Figure 1-2 Simulation-assisted technology development.

simulators. The integrated simulation environment is of fundamental importance for the technology development and product yield optimization in computer-integrated manufacturing (CIM) systems for VLSI circuits.

The other contribution of this dissertation is the development of a new methodology for the technology-based design environment. As statistical process variations have more significant effects on VLSI device characteristics, a great number of device and circuit simulations have to be performed in the device and circuit designs. However, since the parameters of MOS transistor model do not have uniform influence on the device output characteristics, a set of sensitive circuit-level model parameters which have large effects on the transistor output characteristics can be identified for efficient circuit modeling and simulation. The use of sensitive model parameters facilitates VLSI circuit designs in the technology-based design environment.

In Chapter 2, the computer-integrated manufacturing systems and technology CAD tools are discussed. The need for the integration of technology CAD tools are discussed in Chapter 3. The interface program for the new approach is described and its applications are presented in Chapter 4. In Chapter 5, a new methodology using sensitive parameters is presented for efficient modeling in the technology-based design environment. The application of this new methodology to the temperature dependence modeling of SPICE Level-4 MOS transistor model parameters is described in Chapter 6. Chapter 7 concludes this work and suggests the future work along this research direction.

Chapter 2

Computer-Integrated Manufacturing Systems for VLSI Circuits

Fabrication of VLSI circuits is a very complicated manufacturing process. Hundreds of processing steps, such as oxidation, ion implantation, etch, lithography etc., are involved in the fabrication of VLSI circuits. The process schedule must be tested before it can be applied to real fabrication lines. Adequate control on the equipment for processing is needed to accomplish the desired processing steps. In-process measurements are to be made to monitor the process flow. Large amount of data is collected and analyzed so that feedback can be provided for the process and equipment control. The data storage, data analysis, and information exchange between different pieces of equipment are complicated tasks in the fabrication. The increasing sensitivity of circuit performance to inherent process variations due to decreasing device sizes also requires better process and equipment control to guarantee a high product yield and good performance of VLSI circuits.

Advanced computer-integrated manufacturing (CIM) systems are crucial in the reliable production of standard and application-specific VLSI circuits and systems. In CIM systems, information management, process and equipment control, testing and measurement, and design verification are all accomplished through the use of computers. Computers not only maintain control and improve productivity, but also make automation of manufacturing process possi-

ble. The complete automation of a semiconductor manufacturing facility involves the integration of design, wafer fabrication, assembly, and test with management information systems. Computer simulations play a vital role in the integration of design for CIM systems. A VLSI simulator for the manufacturing environment enables the prediction of device, circuit, and yield behavior of a complex VLSI process based on the specification of a process, the characteristics of the fabrication equipment and laboratory environment, and a description of the geometric pattern information. There is a strong need for the development of efficient and accurate computer simulation tools in manufacturing environment so that a designer may compare simulated results to measured data on a real-time basis.

Technology CAD tools have been widely used for VLSI technology development and integrated circuit design over the past two decades. These tools offer a predictive capability and they can be used to evaluate processing options and performance prior to fabrication. For a particular technology, process and device simulation tools can be used to optimize product yields and track variations in production, and circuit simulation tools are used for circuit analysis. These tools prove to be useful for systematic determination of the worst-case and best-case model parameters and they provide a means of understanding the underlying causes for observed variations and problems in the fabrication process and which parameters should be monitored and adjusted.

2.1. Process-Level CAD Tools

A VLSI fabrication process consists of hundreds of steps. Process level CAD tools are used to deal with all aspects of VLSI fabrication. Given a description of the processing steps and layout geometry, the process simulator determines the details of the resulting device structure, including the boundaries of the different material layers of the structure and the distribution of doping impurities within these layers.

The analysis capability of process-level CAD tools can be used for several purposes, including the evaluation of process models, the determination of physical coefficients and the calculation of electrical parameters. The capability of calculating electrical parameters allows a process designer to relate a process sequence to the electrical performance of devices fabricated using this process. This capability can provide the basis for optimizing the performance of individual devices and ultimately the circuits incorporating these devices.

2.1.1. Process Modeling

Integrated-circuit processing steps can be classified into three categories: thermal processing and doping, pattern definition, and pattern transfer. The thermal processing and doping steps include ion implantation, oxidation, epitaxial growth, and annealing. Various etching processes, such as wet chemical etching, plasma etching, and reactive ion etching, and deposition processes, such as CVD and evaporation, are classified as pattern definition. Pattern transfer processing includes optical, x-ray, electron-beam, and ion-beam lithography methods.

Process simulation involves the solution of physical equations for the processing steps needed to fabricate complete device structures. Modeling of the diffusion process is given here as an example. The problem of calculating the impurity profiles in semiconductor devices is that of the transport and redistribution of charged particles in the semiconductor crystal lattice. The processing steps that introduce and redistribute the impurities in selected regions alter the boundaries of the material layers in the device. The problem of calculating the change in these boundaries is that of keeping track of various material layers and their deformations due to the processing steps to which they are subjected.

Let (x,y,t) be the set of two spatial variables and time. Figure 2-1 shows a sample simulation region where x is the coordinate along the depth direction and y is the coordinate along a lateral direction. Two different material layers

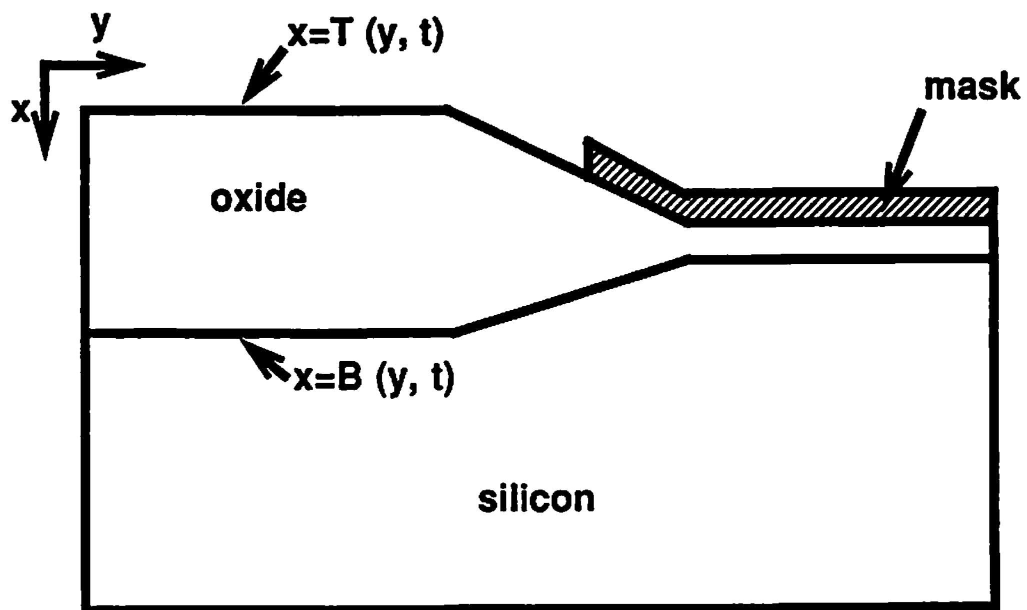


Figure 2-1 A selective region for process modeling and simulation.

(oxide and nitride) are depicted on top of the silicon substrate. The nitride layer forms a mask which blocks impurities and retards oxidation locally under the mask. The silicon-oxide interface is defined by x=B(y,t) and the top surface of the oxide is defined by x=T(y,t). Assume that there are m impurities present in the silicon. The continuity equation governs the transport of the ith impurity,

$$\frac{\partial C_i}{\partial t} = \operatorname{div} J_i$$
$$= \nabla(D_i \nabla C_i + Z_i \mu_i N_i E) \tag{2.1}$$

where C_i=C_i(x , y) and J_i are the concentration and the flux of the ith impurity, respectively, D_i is the concentration-dependent diffusion coefficient, Z_i and μ_i are the charge state and the mobility of the impurity, respectively, N_i is the electrically active concentration, and E is the electric field.

2.1.2. Simulation Tools

The use of computer programs to calculate the impurity profile in semiconductor devices has become a routine part of IC device design and process development since the availability of SUPREM [2.1-2.4] from Stanford University. Beginning with SUPREM-I and proceeding to SUPREM-II, each version has drawn from the models and physical understanding of fabrication processes then available.

The third generation SUPREM-III substantially upgrades the simulation capability. New and more accurate models for oxidation, diffusion, epitaxy, and ion implantation are included. Types of processing steps simulated by SUPREM-III include inert ambient drive in, oxidation of silicon and silicon-nitride, ion implantation, epitaxial growth of silicon, and low temperature deposition or etching of various materials. SUPREM-III simulates in one dimension the changes in a semiconductor structure as a result of the various processing

steps. The primary results of interest are the thickness of the structure and the distribution of impurities within those layers. The program also determines certain material properties such as polysilicon grain size and the sheet resistivity of diffused regions in silicon layers.

SUPREM-I, -II, and -III are essentially simulators which emphasize one-dimensional (1D) physical kinetic models. The new SUPREM-IV incorporates oxidation, ion implantation, and diffusion models in two-dimensional (2D) format. SUPREM-3.5 [2.5] was recently developed to simulate processes used to manufacture ion implanted GaAs devices. The process models in SUPREM-3.5 include ion implantation, diffusion, and activation.

SUPRA [2.6] is a two-dimensional process simulator which uses approximations in many cases to keep execution times low. It is therefore more difficult to obtain quantitative results with SUPRA than with SUPREM. It is used, however, for modeling structures that can not be treated with SUPREM and when only qualitative results are required.

BICEPS [2.7] is a comprehensive two-dimensional process simulation program developed at AT&T Bell Laboratories. BICEPS can accommodate the various processing steps of ion implantation, predeposition, oxidation, and epitaxy in one or two spatial dimensions as well as etching and deposition of oxide, nitride, photoresist, and polysilicon. One unique feature of BICEPS is that the boundary variations of the material layers of the device structure are calculated along with the impurity profiles in a consistent manner.

The simulation of optical lithography was pioneered by the SAMPLE program [2.8,2.9] at the University of California, Berkeley. Simulation has been particularly successfully in the development of proximity effect correction technique in electron-beam lithography. The simulation of etching and deposition is probably the least developed area in IC process simulation due to the complexity of the chemistry and physics of a variety of continually evolving techniques. The SAMPLE program models some of these steps based on empirical functions.

2.2. Device-Level CAD Tools

Numerical device simulators are extensively used to study device electrical phenomena which can not be easily formulated by analytical expressions. The simulation results provide a lot of insight into the underlying physics of the device operations. For MOS transistors, two-dimensional effects, such as short-channel and narrow-width effects, are significant as the device sizes scale down. Detailed and accurate analysis of these effects require 2D simulations to help understand the device physics of small-geometry transistors. CMOS latchup phenomena, hot carrier effects, and bipolar effects such as base-width modulation and base pushout, are often characterized using 2D simulators.

A device simulator is quite useful in the VLSI device development. Various device design options can be simulated and the design with the desired electrical characteristics is selected from these options. The process simulation and device simulation can be linked to allow process parameters and layout to be tailored to optimize device performance.

2.2.1. Semiconductor Equations

Device simulations involve the solution of a system of semiconductor equations over a spatial grid. Basically, there are three fundamental equations involved in the device simulation: Poisson's equation and continuity equations for electrons and holes. The Poisson's equation relates the electrostatic potential to the total charge density in the semiconductor,

$$\psi = -\frac{\rho}{\varepsilon_s} \ . \tag{2.2}$$

The electric field is the gradient of the electrostatic potential,

$$E = -\nabla\psi \, . \tag{2.3}$$

The total charge density is expressed as

$$\rho = q(p - n + N) \tag{2.4}$$

where $N = N_D^+ - N_A^-$ is the electrically active net impurity concentration, and p and n are the electron and hole carrier concentrations, respectively.

$$J_n = q\,\mu_n\, n\, E + q\, D_n \nabla n\,, \tag{2.5}$$

$$J_p = q\,\mu_p\, n\, E - q\, D_p \nabla p \tag{2.6}$$

where μ_n and μ_p are electron and hole mobilities, respectively, and D_n and D_p are electron and hole diffusivities, respectively. The carrier densities are related to the electrostatic potential by the Boltzmann approximation,

$$n = n_i \exp[\frac{q(\psi - \phi_F)}{kT}]\,, \tag{2.7}$$

$$p = p_i \exp[\frac{q(\phi_F - \psi)}{kT}] \tag{2.8}$$

where n_i is the intrinsic carrier concentration and ϕ_F is the Fermi potential in equilibrium. Under nonequilibrium condition, the carrier concentrations can be expressed using quasi-Fermi potential ϕ_n and ϕ_p as

$$n = n_i \exp[\frac{q(\psi - \phi_n)}{kT}]\,, \tag{2.9}$$

$$p = p_i \exp[\frac{q(\phi_p - \psi)}{kT}]\,. \tag{2.10}$$

The current continuity equations for electrons and holes are given by

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla J_n + G - R\,, \tag{2.11}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla J_p + G - R\,. \tag{2.12}$$

The term G incorporates generation phenomena, such as impact ionization or radiation-induced carrier generation and the term R includes Shockley-Read-

Hall and Auger recombination processes.

Two techniques are used to solve the coupled set of equations (2.2), (2.11) and (2.12): Newton's method and Gummel's method. The Newton's direct method applies to the three equations (2.2), (2.11), and (2.12) coupled over all space. The Gummel's iterative method applies sequentially to the individual equations. The flowcharts of these two methods are shown in Figures 2-2 and 2-3, respectively. The Gummel's method has major storage advantages and superior execution speeds for bias levels where the equations are not guaranteed. In contrast, the direct solution of the coupled equations using the Newton's method results in more costly solutions at lower biases but guarantees convergence at high bias levels.

2.2.2. Simulation Tools

PISCES-II [2.10] is a two-dimensional semiconductor device modeling program which simulates the electrical behavior of devices under steady-state or transient conditions. PISCES-II can analyze physical structures with completely arbitrary geometries (nonplanar as well as planar) with general doping profiles. A wide variety of materials and physical models are incorporated.

The device simulator MINIMOS [2.11] was developed at the University of Vienna, Austria. It can be operated in a hierarchy of levels. MINIMOS's major advantages are its speed and user friendliness. It is however limited to modeling conventional MOS structures.

2.3. Circuit-Level CAD Tools

Integrated circuit design is a complex task as the level of integration increases. Circuit simulation programs are important computer-aided design tools for the analysis of the electrical performance of integrated circuits. Circuit designers can verify their new designs simply by computer simulations and they can modify their designs until the specifications of the circuit performance is achieved. Circuit simulation programs can perform a variety of anal-

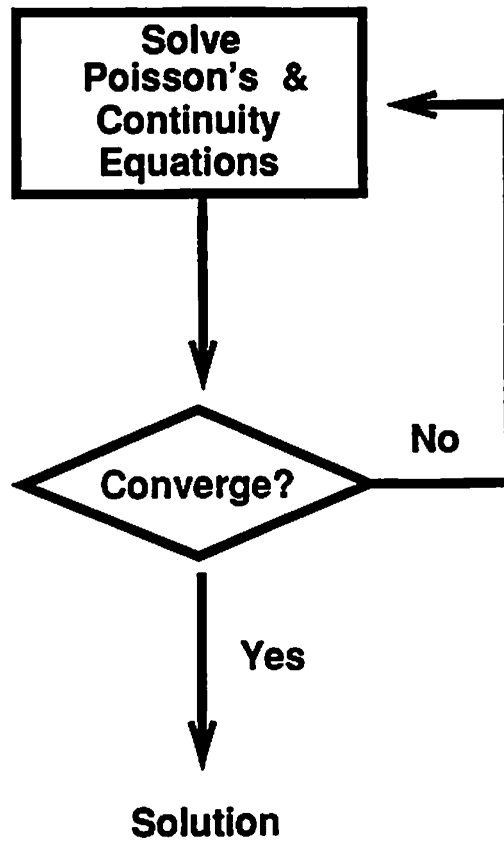


Figure 2-2 Flowchart of the Newton's method.

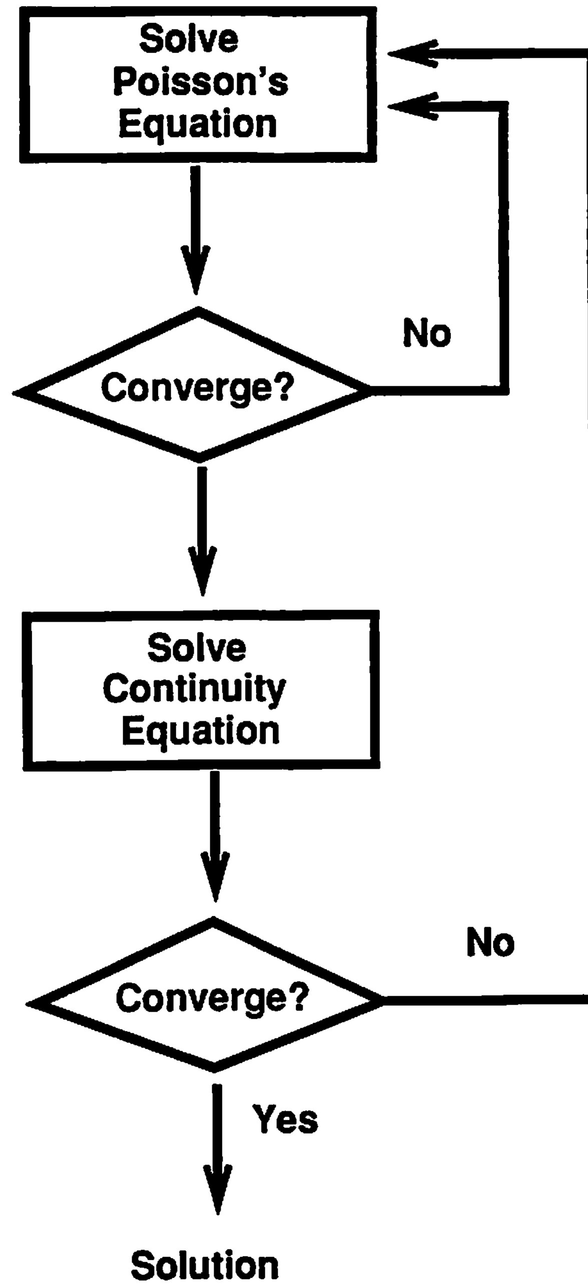


Figure 2-3 Flowchart of the Gummel's method.

yses, including dc, ac, and time-domain transient analyses of circuits containing a wide range of nonlinear active circuits.

2.3.1. Equation Formulation

Computer simulation of an electronic circuit involves the numerical analysis of mathematical models of the circuit. The circuit is modeled as an interconnection of branches. Each circuit element is associated with a branch and is modeled in mathematical expressions. Each branch is connected between two nodes and characterized by a branch-constituent relation. There are two types of branches: current-defined branch and voltage-defined branch. A branch is current-defined if the branch current is defined in terms of circuit parameters and circuit variables,

$$I_b = f(x) \tag{2.13}$$

where x is the vector of branch voltages and branch currents. In a voltage-defined branch, the branch voltage is defined in terms of circuit parameters and circuit variables,

$$V_b = f(x) \tag{2.14}$$

where x is the vector of branch voltages and branch currents. Examples of current-defined branches include independent and controlled current-sources, capacitors, and most branches embedded in semiconductor device models. Examples of voltage-defined branches include independent and controlled voltage sources, inductors, and transmission lines. The resistor is an element which can be modeled either as a voltage-defined branch or as a current-defined branch.

In general, branch-constituent relations are nonlinear, time-dependent, and may involve the time derivative operation. Therefore, the determination of node voltages and branch currents of a circuit generally involve solving a system of nonlinear, time-dependent differential equations of the form,

$$G(x) = 0 \tag{2.15}$$

where **x** is the vector of unknown circuit variables.

2.3.2. Simulation Tools

The SPICE program [2.12,2.13] is the most widely used circuit simulation program for IC design. A lot of circuit simulation programs used in the IC industry and universities are variations of the SPICE program. SPICE is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analyses. A circuit may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, transmission lines, switches, and five most common semiconductor devices: diodes, BJT's, MESFET's, JFET's, and MOSFET's. SPICE has built-in models for the semiconductor devices, and the users need to specify only the pertinent model parameter values.

2.4. Equipment Modeling

One new class of CAD tools for manufacturing requires fabrication equipment modeling. The equipment models are used to predict the performance of the factory, such as performance and throughput. Some work has been done on reactive ion etching, rapid thermal processing, and sputtering. Research in several universities is being conducted on the physical understanding of the equipment dynamics. More work on equipment and process modeling and characterization will lead to improved fundamental understanding, better capability for closed-loop process control, and improved equipment design.

Chapter 3

Integration of Technology CAD Tools

Integrated-circuit technology has progressed with a rapid pace over the past two decades. In the VLSI era, device feature sizes are scaled down to the submicron range and IC chips with component counts more than 10^7 have been in large-volume production. With increasing integration level and complexity of VLSI circuits, the development time and cost for a new VLSI technology tend to increase enormously. The huge manpower and cost spent on the process development for standard circuits are compensated by the large profits earned from high-volume production. Recently, application-specific integrated circuits (ASICs) have emerged as a very important type of IC products in the market [3.1]. It is essential for IC manufacturing companies to adopt new strategies for process development in order to remain highly competitive in this new market.

ASIC designs have several special features. First, very limited manpower and resources are to be allocated to each product. Second, tight delivery schedules usually demand a highly efficient design methodology to shorten the process and circuit development time. Third, circuit performance and product yield must meet the high standard demanded. These special features imply the heavy usage of computer-aided design (CAD) tools, careful tuning of the fabrication process, and the improvement of the device structure. The statistical nature of microelectronic fabrication is particularly important in VLSI de-

sign. Large statistical fluctuations in the performance of VLSI circuits will severely cause product yield loss. A good design practice is to employ circuit techniques to reduce the sensitivity of the final product to such variations, as well as to feedback pertinent information to process and device engineers for process optimization.

3.1. The Need

Model parameters are used in SPICE circuit simulation. Conventionally, model parameters are obtained from measurement of fabricated test devices. Figure 3-1 shows the flowchart of a conventional IC design approach. A process schedule specifies the wafer processing sequence and detailed operation information for each fabrication step, such as the oxidation temperature and time, implantation species and doses, and etching conditions. Once the fabrication steps are completed, electrical measurements can be performed on test devices to obtain transistor dc and capacitance characteristics. General parameter extraction software, such as TECAP [3.2,3.3], SUXES [3.4], and a dedicated extraction program, such as BSIM_Extract [3.5,3.6], can be used to extract the model parameters. These model parameters are employed in SPICE simulation to investigate circuit large-signal transient, or small-signal ac performance.

Simulation tools for the discrete design task have been available. At the process design level, process simulators SUPREM/SUPRA are capable of simulating fabrication steps such as oxidation, ion implantation, etch and diffusion. The lithography simulator SAMPLE provides information regarding photo-lithography results. At the device design level, the device simulator PISCES solves Poisson's equation and current continuity equations to provide detailed internal information of a device and the terminal current characteristics. The device simulator MINIMOS-3 [3.7] also takes into account energy balance inside the device.

At present, integration of technology-CAD tools is highly needed. Such in-

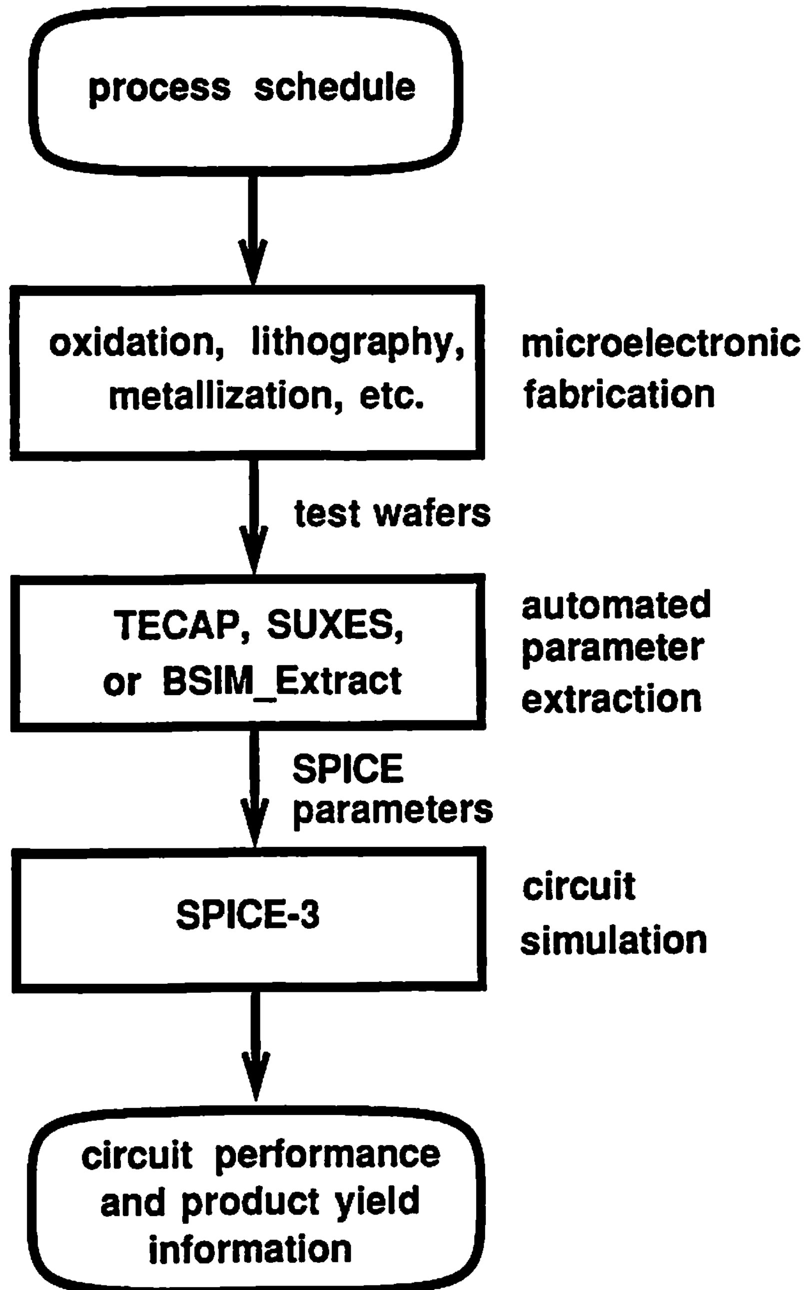


Figure 3-1 Flowchart of the conventional IC design approach.

tegration can relieve the designer from the cumbersome task of interpreting the outputs of one program and translating them into the proper input format for another program. The combined process and device simulation program FABRICS-II [3.8,3.9] represents one of such efforts. It is organized into two parts: FAB-1 and FAB-2. FAB-1 performs process simulation. A library of analytical models of manufacturing operations, as well as libraries of functions that simulate impurity profiles are used to speed up the simulation execution time. The results of FAB-1 are transferred to FAB-2, which performs device simulation. The current version of FABRICS-II provides key parameters for the SPICE Level-1 model.

Since SUPREM, PISCES, and SPICE have been widely used, it is essential to integrate these simulation tools. The output format of SUPREM is already compatible to the input format of PISCES. The link between PISCES and SPICE is yet to be established. Due to the mismatch between the device simulator output format and the circuit simulator input format, no circuit simulation can be directly performed based on the device simulation results in a simple and efficient way.

3.2. Integration Techniques for Device-to-Circuit Simulation

Several approaches may prove useful to couple a device simulator and a circuit simulator: table look-up method, conventional parameter extraction method, mixed-mode simulation method, and smart link method.

3.2.1. Table Look-Up Method

In this method, the I-V data are generated by a device simulator and are then used to set up three-dimensional tables. Interpolation techniques are used to obtain I-V characteristics at different bias conditions. In the table look-up method, the number of device sizes is known and small, and characteristic curves of some form are available for a wide sampling of the devices of interest. For a given set of bias points and device geometry, the table is

checked to determine if such a point has been previously measured or simulated. If not, interpolation is used between known points to generate the new value. The accuracy of this method can be quite good if enough data exist on which the interpolation is based. However, extrapolation can be a problem. In moving outside the known range, new physical effects may dominate that have not been adequately captured by the data base in use. After the initial accumulation of data, this method is reasonably fast, but has large data storage requirements.

3.2.2. Conventional Parameter Extraction Method

This method also requires a device simulator to generate I-V data. These data are used by model parameter extraction program, such as TECAP or SUXES, to obtain model parameter values. In a parameter extraction program, the parameter values are obtained by optimizing an objective function which can be expressed as

$$E_r = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left(\frac{I_{c,i} - I_{m,i}}{I_{m,i}}\right)^2} \tag{3.1}$$

where n is the number of data points, I_c is the calculated value, and I_m is the measured data. The expression can be modified to serve different purposes, such as for optimizing only current characteristics or for optimizing both current and output conductance characteristics. Various optimizing methods, such as steep-descent method, quasi-Newton method, and Levenberg-Marquardt method, can be used for parameter extraction purposes.

3.2.3. Mixed-Mode Simulation Method

In this method, the device simulation capability is embedded into a circuit simulator or vice versa. For critical devices which need detailed analyses in a circuit, numerical device simulations are performed to obtain device characteristics. Otherwise, analytical device models incorporated in a circuit simulator

are used to calculate the device characteristics.

The program CODECS [1.5] is a mixed-level circuit and device simulator which provides a direct link between technology parameters and circuit performance. Detailed and accurate analyses of semiconductor circuits are possible by use of numerical models for critical devices. This program provides a general framework for mixed-level circuit and device simulation and supports a wide variety of analysis capabilities and numerical models. It has been used in the simulation of high-level injection effects in BiCMOS driver circuits, non-quasi-static MOS operation, switch-induced error in MOS switched-capacitor circuits, and inductive turn off of p-i-n rectifiers.

3.2.4. Smart Link Method

The detailed device simulation results are directly used to calculate model parameter values for circuit simulation in the smart link method [3.10].

The table look-up method and the conventional parameter extraction method suffer from computational inefficiency since hundreds of device simulation runs are needed. The mixed-mode simulation method needs much more computational time than the table look-up method and the conventional parameter extraction method when the number of circuit components is large. The smart link method can efficiently and effectively accomplish the vertical integration for computer-integrated manufacturing systems.

Chapter 4

PARGEN: An Interface Program for PISCES-II and SPICE-3

A new computer-aided design program PARGEN (PARameter GENeration) was developed to accomplish the integration task in the smart link method. This program links a widely used device simulator, PISCES-IIB, and a circuit simulator, SPICE-3C1. Circuit-level model parameter values are generated by PARGEN from the internal device information provided by PISCES. These parameters are compatible with the transistor models implemented in SPICE. This interface program, together with SUPREM, PISCES, and SPICE, form an integrated simulation environment for VLSI technology development [4.1].

4.1. PARGEN

Figure 4-1 shows an integrated simulation environment with PARGEN serving as an efficient interface between PISCES and SPICE. The salient features of PARGEN are:

- strong device-physics basis,
- high computational efficiency,
- generation of the Level-2 MOSFET model parameters [4.2], and
- preliminary GaAs MESFET parameter generation.

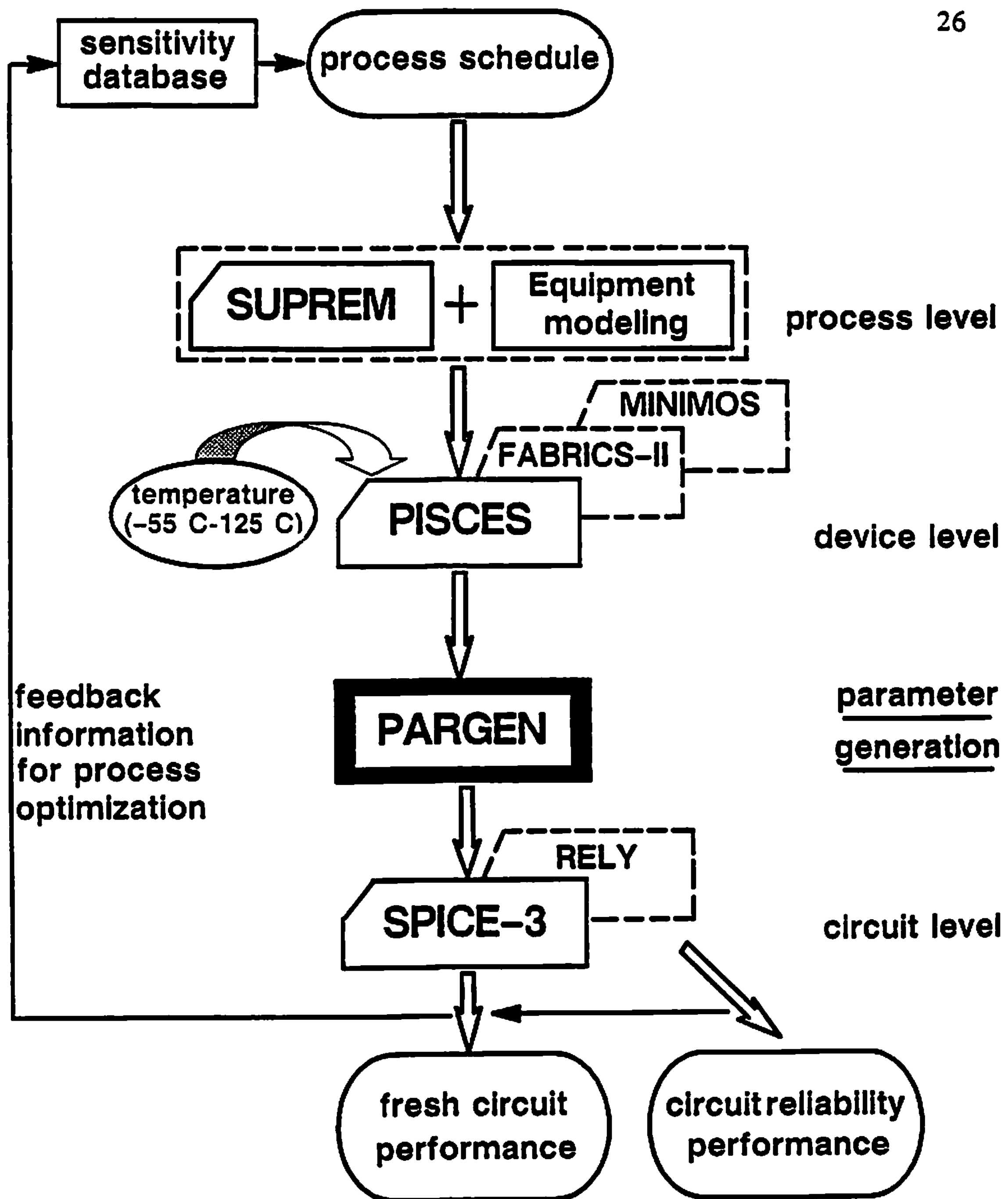


Figure 4-1 Integrated simulation environment which allows a designer to examine how a microscopic fabrication variable affects final circuit performance and product yield. PARGEN is the interface between PISCES and SPICE.

The PARGEN program consists of two major modules: MOSGEN (MOSFET parameter GENerator) and MESGEN (MESFET parameter GENerator). The MOSGEN module produces parameters for the SPICE built-in Level-2 MOSFET model. The MESGEN module generates parameter values for the SPICE built-in MESFET model [4.3]. The model parameters generated by PARGEN are completely compatible with the transistor models implemented in SPICE.

Figure 4-2 shows the organization of the PARGEN program. It is partitioned into three major parts:

- preprocessing,
- parameter calculation, and
- postprocessing.

The preprocessing part of PARGEN handles data read-in from PISCES output files. Two key tasks are accomplished in the parameter calculation part: the generation of linear-region parameters, the generation of saturation-region parameters. The postprocessing part of PARGEN prepares the model parameters a format for SPICE simulation. The PARGEN program is written in FORTRAN and contains about 1100 lines. It can be ported to various computer systems.

4.1.1. MOSGEN

PISCES runs at several bias conditions are required to provide adequate information. For the generation of SPICE Level-2 model parameter values, six bias conditions are sufficient, as listed in Table 4-1. If a p-channel transistor is used, polarities of the biasing voltages have to be changed accordingly. The algorithm can be described as

for i=1 to 6 **do**

  run PISCES at bias condition i;

while there are parameter values to be generated **do**

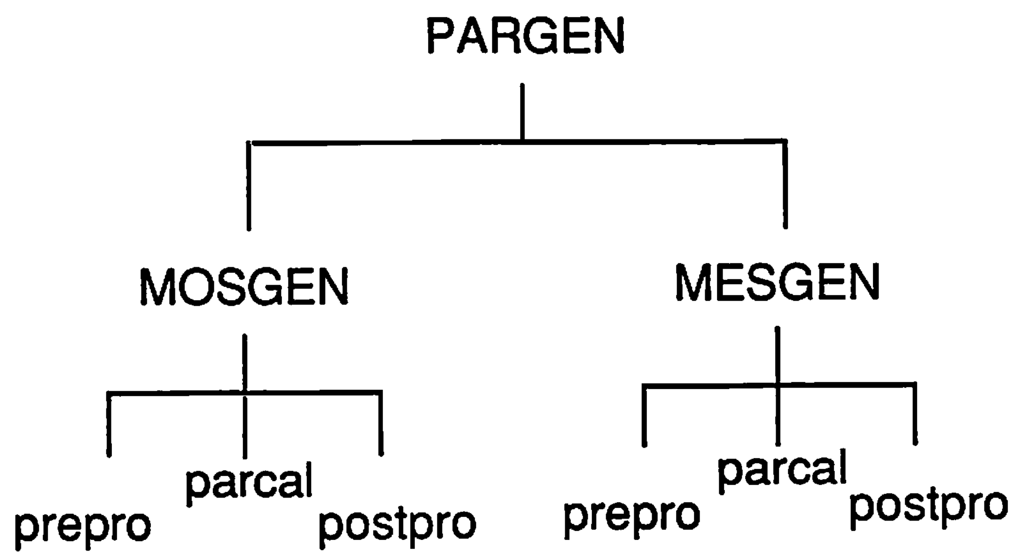


Figure 4-2 Organization of the PARGEN program.

Table 4-1 Biasing conditions for PISCES runs to be used by MOSGEN.
(An N-channel MOSFET is assumed.)

Condition \ Bias	V_{GS} (V)	V_{DS} (V)	V_{BS} (V)
1	0	0	0
2	0.6	0	0
3	1.5	0	0
4	3.0	0	0
5	1.5	0	-4.0
6	1.5	5.0	0

```
   begin
      call prepro;
      call parcal;.
      call postpro;
   end
end
```

The procedure *prepro* of MOSGEN handles data read-in from PISCES output files. Two key tasks are accomplished in the procedure *parcal*: the generation of linear-region parameters and the generation of saturation-region parameters. The procedure *postpro* prepares the model parameters into a SPICE-compatible format. Figure 4-3 illustrates the flowchart of MOSGEN for the generation of Level-2 model parameter values.

The useful information from PISCES includes carrier distribution, impurity distribution, internal electric field, electrostatic potential, mobility, and internal current distribution. PISCES results from condition 1, in which the gate, drain, source, and substrate are at zero potential, are used to determine basic model parameters. These basic model parameters include the bias-independent parameters, such as lateral diffusion (L_D) and metallurgical junction depth (X_J), and parameters under equilibrium condition, such as the bulk junction potential (P_B). The results from condition 2 are used to determine the subthreshold parameter (N_{FS}). The carrier concentration obtained from condition 3 is used to generate the zero-bias threshold voltage (V_{TO}). The algorithm to generate V_{TO} is described in detail in Section 4.2.1. From the carrier distribution and impurity distribution in condition 3, the total-channel-charge coefficient (N_{EFF}) can be obtained. Here, the transistor V_{TO} is assumed to be greater than 0.6 V and less than 1.5 V. If the transistor V_{TO} is outside the above range, then the gate biasing voltages in condition 2 and 3 have to be modified accordingly.

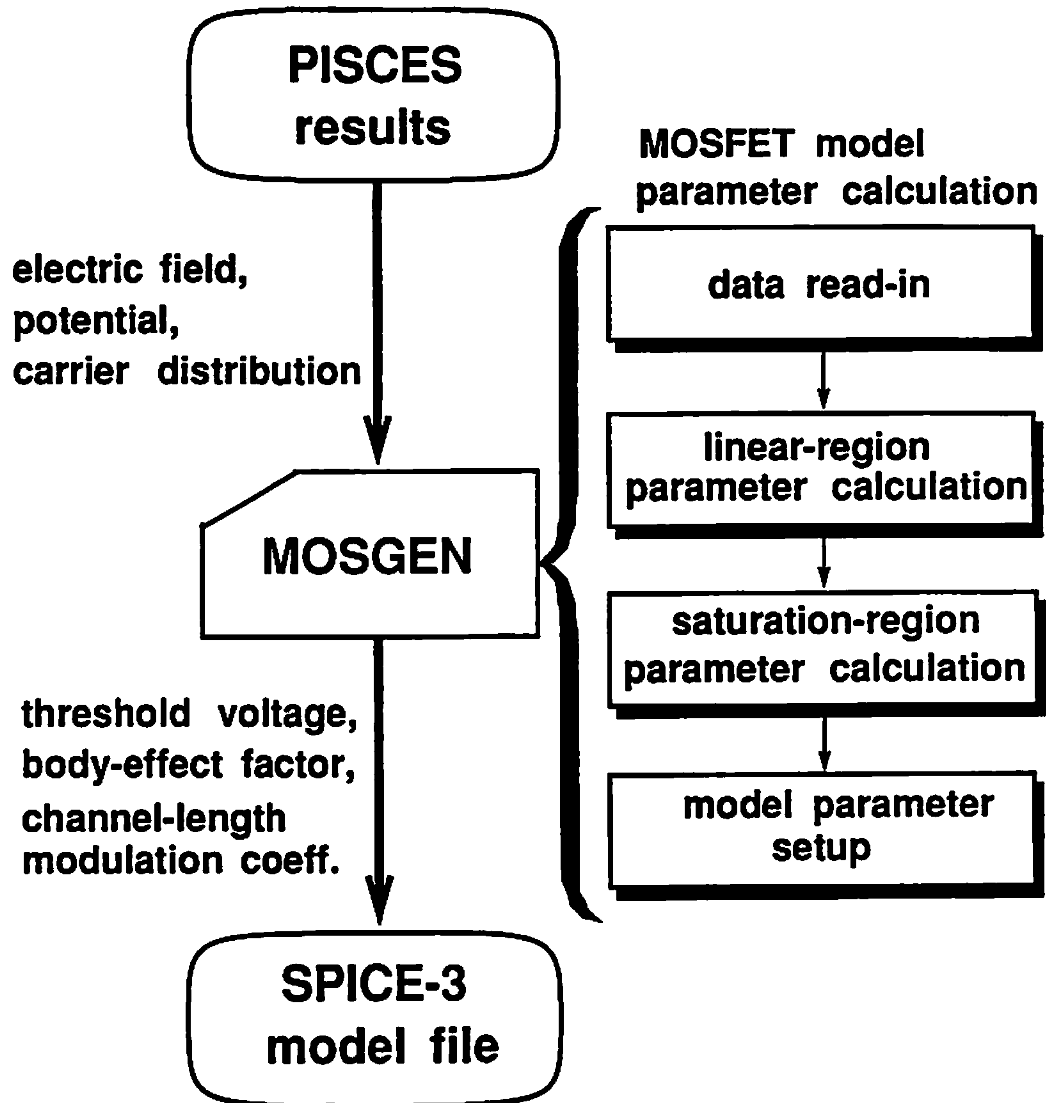


Figure 4-3 Flowchart of the MOSGEN module which generates SPICE parameters for the Level-2 model.

In condition 4, a large gate bias is applied to obtain the information on mobility under high vertical field, and the results combined with those from condition 2, in which the vertical field is low, are used to generate mobility-related parameters, such as the mobility-degradation coefficient (U_{CRIT}) and the critical field exponent (U_{EXP}) for the Level-2 model. The body-effect coefficient (G_{AMMA}) is extracted from the carrier distributions under two substrate biases (condition 3 and condition 5).

The channel-length modulation coefficient (L_{AMBDA}) is related to the amount of channel length reduction when the transistor is biased in the saturation region. In condition 6, a high drain voltage is applied to facilitate the determination of parameter L_{AMBDA}. In addition, the static feedback coefficient (E_{TA}) is obtained by comparing the threshold voltages determined from condition 3 and condition 6.

4.1.2. MESGEN

The model equation for MESFET drain current in SPICE-3 is given by

$$I_{DS} = \frac{\beta(V_{GS} - V_{TO})^2}{1 + B(V_{GS} - V_{TO})} \left[1-[1-\alpha \frac{V_{DS}}{3}]^3\right] (1 + \lambda V_{DS}) \qquad \text{for } 0 < V_{DS} < \frac{3}{\alpha}, \qquad (4.1)$$

$$I_{DS} = \frac{\beta(V_{GS} - V_{TO})^2}{1 + B(V_{GS} - V_{TO})} (1 + \lambda V_{DS}) \qquad \text{for } V_{DS} > \frac{3}{\alpha}, \qquad (4.2)$$

where V_{TO} is the pinch-off voltage, β is the transconductance parameter, B is the doping tail extending parameter, α is the saturation voltage parameter, and λ is the channel-length modulation parameter.

PISCES simulations at four bias conditions are required to provide the modeling information. The required bias conditions are listed in Table 4-2. The algorithm can be described as

Table 4-2 Biasing conditions for PISCES runs to be used by MESGEN.

Condition \ Bias	V_{GS} (V)	V_{DS} (V)
1	0	0
2	-0.5	0.5
3	-1	1
4	-1	2

```
for i=1 to 4 do
  run PISCES at bias condition i;
while there are parameter values to be generated do
  begin
    call prepro;
    call parcal;
    call postpro;
  end
end
```

The procedure *prepro* of MESGEN handles data read-in from PISCES output files. The PISCES simulation results are used by procedure *parcal* to calculate the parameters. The procedure *postpro* prepares the model parameters into a SPICE-compatible format.

In the zero-bias condition, PISCES solves the Poisson's equation to obtain the initial information of the transistor. The results are used to calculate the gate junction built-in potential, channel pinch-off voltage, doping tail extending parameter and transconductance parameter. The doping edge under the gate is defined in which the mobile carrier density is less than 10% of doping concentration. The built-in voltage is obtained by taking the spatial average of surface potential at the depletion edge.

The PISCES results under the bias condition 2 and 3 are used to generate the parameter for channel-length modulation effect. For GaAs MESFET's, current saturation occurs when the electrons in the channel reach a saturated velocity. At this stage, the channel under the gate can be divided into two regions as shown in Figure 4-4. In region I, electrons are transported with constant mobility between the source end of the gate and the velocity saturation point. In region II, electrons travel at their saturated velocity. At high drain bias, the velocity saturation point moves toward the source side, and the electric field near the drain end of the gate increases to accommodate the drain-to-source potential. In order to satisfy Gauss' law and current continuity equa-

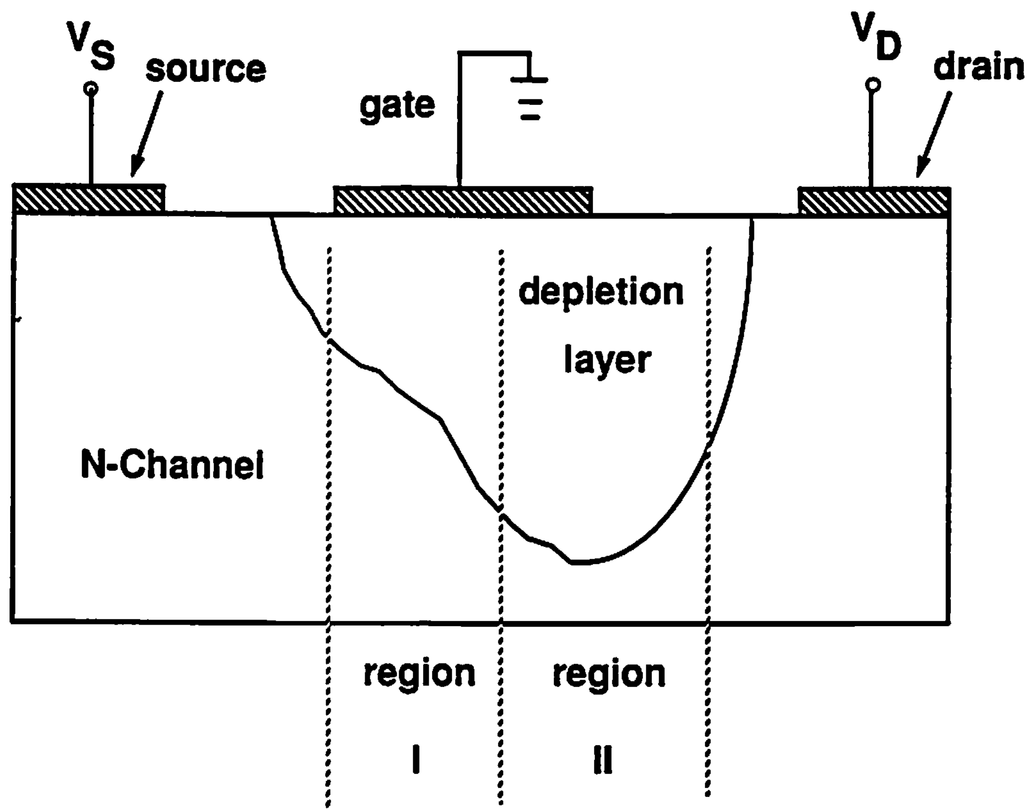


Figure 4-4 Cross section of a GaAs MESFET.

tions in the channel, the increase of longitudinal electric field must be accompanied by a reduction in the channel height and by carrier accumulation beyond the charge-neutral region. The channel length modulation parameter λ is obtained by comparing the current density from conditions 2 and 3.

In condition 4, a drain bias is applied to obtain the information on the distribution of current density. The results combined with those from condition 1, 2, and 3 are used to generate the saturation voltage parameter α.

4.2. Parameter Calculation

4.2.1. MOSFET Parameter Calculation

Accurate and efficient algorithms to generate the various model parameters have been developed.

(A) Zero-Bias Threshold Voltage

The inversion charge can be found by integrating the mobile carrier density over the channel region [4.4],

$$Q_N = - q\ W \int_{x_t}^{x_b}\int_{y_s}^{y_d} n(x,y)\ dx\ dy\ . \tag{4.3}$$

Here n(x,y) is the mobile carrier density. The integration limits x_t, x_b, y_s, and y_d define the boundaries of the two-dimensional area of the channel region. This area is bounded by the source diffusion edge and the drain diffusion edge in the horizontal direction and by the oxide-silicon interface and the boundary where the mid-band energy level (E_i) equals to the Fermi level (E_F) in the vertical direction, which is shown in Figure 4-5. The integration can be approximated by numerical summation with fine-enough grids in the device simulation,

$$Q_N = - q\ W \sum_j \sum_i\ n(x,y)\ \Delta x_i\ \Delta y_j \tag{4.4}$$

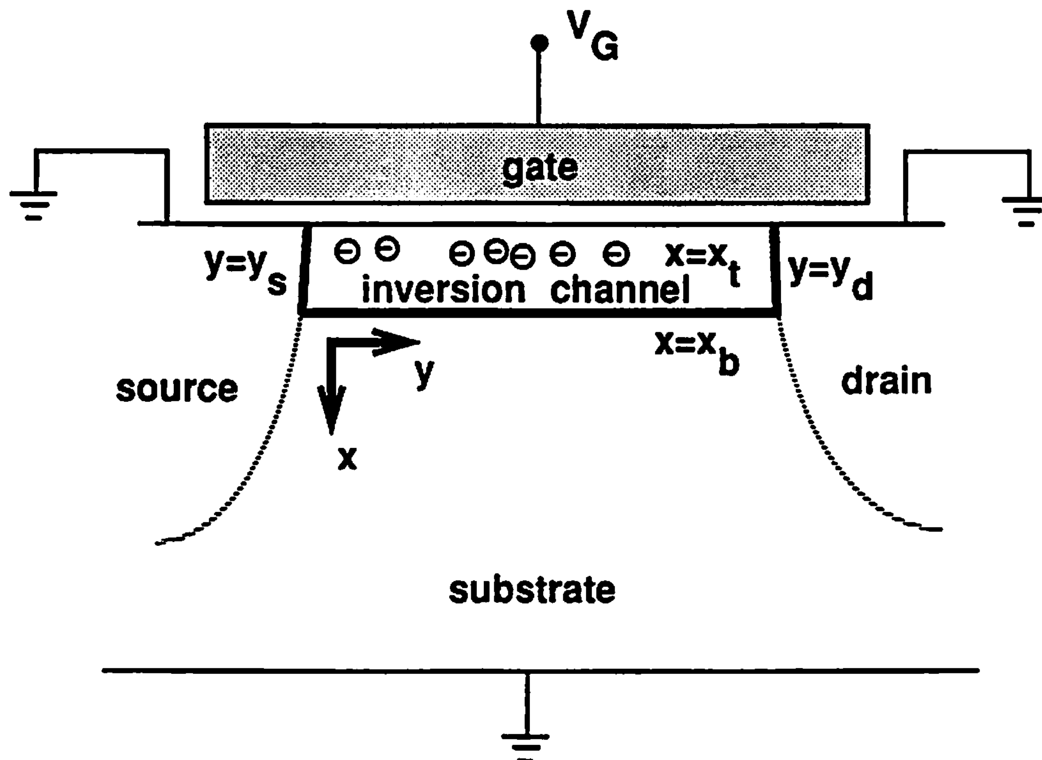


Figure 4-5 Cross section of an MOS transistor highlighting the two-dimensional area for the calculation of inversion charge.

where $n(x_i, y_j)$ is the effective carrier concentration in the differential area $\Delta x_i \Delta y_j$.

When an MOS transistor is biased in the strong-inversion region, the relationship among the channel inversion charge Q_{INV}, the gate voltage V_G, and the threshold voltage V_{TO} is [4.5]

$$Q_{INV} = -C_{OXT}(V_G - V_{TO}), \tag{4.5}$$

where gate capacitance C_{OXT} equals to C_{ox} W L. Here C_{ox} is the gate-oxide capacitance per unit area, and W and L are the transistor channel width and length, respectively. By applying a gate bias which results in strong inversion operation the inversion charge Q_{INV} is obtained. Once Q_{INV} is known, the threshold voltage can be determined from (4.5),

$$V_{TO} = \frac{Q_{INV}}{C_{OXT}} + V_G. \tag{4.6}$$

This method has been experimentally verified to be insensitive to the applied gate bias in (4.6) to determine the threshold voltage.

(B) Body-Effect Coefficient

The threshold voltage can be expressed as

$$V_T = V_{FB} + 2\phi_F - \frac{Q_{BD}}{C_{OXT}} \tag{4.7}$$

where V_{FB} is the flat-band voltage between the gate material and the substrate material, and Q_{BD} is the depletion charge in the substrate. Charge Q_{BD} consists of two components: the bias independent charge component, Q_{BD0}, and the substrate-bias induced charge component, Q'_{BD}. In the SPICE model, the following expression for the transistor threshold voltage is used,

$$V_T = V_{TO} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right) \tag{4.8}$$

where

$$V_{TO} = V_{FB} + 2\phi_F - \frac{Q_{BD0}}{C_{OXT}} \tag{4.9}$$

and

$$\frac{Q_{BD}}{C_{OXT}} = \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right) . \tag{4.10}$$

In general, the body-effect coefficient can be expressed as

$$\gamma = \frac{Q_{BD0} - Q_{BD}}{C_{OXT} \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)} . \tag{4.11}$$

In the extreme case of a long-channel device with constant substrate doping N_{SUB}, the expression of body-effect coefficient can be simplified to

$$\gamma = \frac{1}{C_{ox}} \sqrt{2 q \varepsilon_{Si} N_{SUB}} . \tag{4.12}$$

The charge neutrality principle requires the substrate depletion charge to be balanced by the gate charge Q_G, oxide-semiconductor interface charge Q_{SS}, and the channel inversion charge Q_{INV},

$$Q_{BD} = - \left(Q_G + Q_{SS} + Q_{INV} \right) . \tag{4.13}$$

The gate charge is a function of the voltage drop across the gate oxide,

$$Q_G = C_{OXT} \left(V_G - V_{FB} - \psi_S \right) . \tag{4.14}$$

Here, the flat-band voltage V_{FB} the surface potential ψ_S can be determined from the PISCES outputs. With the channel inversion charge determined from (4.4), the depletion charge Q'_{BD} can be calculated by

$$Q'_{BD} = (\psi_S - \psi_{S0}) C_{OXT} + (Q_{INV0} - Q_{INV}) \tag{4.15}$$

where ψ_{S0} and Q_{INV0} are the surface potential and channel inversion charge, respectively, at the zero substrate bias. Thus the body-effect coefficient can be determined from (4.11).

(C) Surface Potential

The surface potential parameter PHI can be expressed as

$$PHI = 2 | \phi_F | \tag{4.16}$$

where ϕ_F is the Fermi potential in the substrate and can be easily obtained from distribution of the electrostatic potential generated by PISCES.

(D) Bulk Junction Potential

The bulk junction potential is the difference between the quasi Fermi potentials in the source/drain and in the substrate, i. e.

$$PB = \phi_n - \phi_p \tag{4.17}$$

where ϕ_n and ϕ_p are the quasi Fermi potentials in the N-type and P-type semiconductors, respectively. The quasi Fermi potentials can be obtained from distribution of the electrostatic potential.

(E) Channel Length Modulation

The drain current I_{DS} in the saturation region can be expressed as

$$I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L - x_d} (V_{GS} - V_T)^2 \tag{4.18}$$

where x_d is the depletion region width at the drain junction. Equation (4.18) can also be expressed as an empirical formula

$$I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) . \tag{4.19}$$

By equating the above two equations λ can be expressed as

$$\lambda = \frac{x_d}{(L - x_d)\, V_{DS}} \quad . \tag{4.20}$$

The depletion region width x_d is determined by examining the charge distribution at the drain junction. The mobile charge is very small in the depletion region.

4.2.2. MESFET Parameter Calculation

(A) Threshold Voltage

The channel pinch-off voltage can be found by integrating the doping density in the channel,

$$V_{po} = \frac{1}{\varepsilon_s} \int_0^t N(x)x \; dx \tag{4.21}$$

where ε_s is the permittivity of the active layer and t is the thickness of the channel. The transistor threshold voltage is calculated by

$$V_{TH} = V_{po} - V_{bi} \tag{4.22}$$

where V_{bi} is the gate junction built-in potential.

4.3. PARGEN Results

Experimental results obtained from PARGEN are discussed in this section.

4.3.1. MOSGEN Results

The cross section of an N-channel MOS transistor is shown in Figure 4-6. Channel implant is used to adjust the transistor threshold voltage. In a typical 1.25-μm process, the source/drain junction depth is 0.2 μm, the gate-oxide thickness is 25 nm, and the transistor threshold voltage is 0.7 V.

Detailed investigation of the accuracy and computational efficiency of MOS-

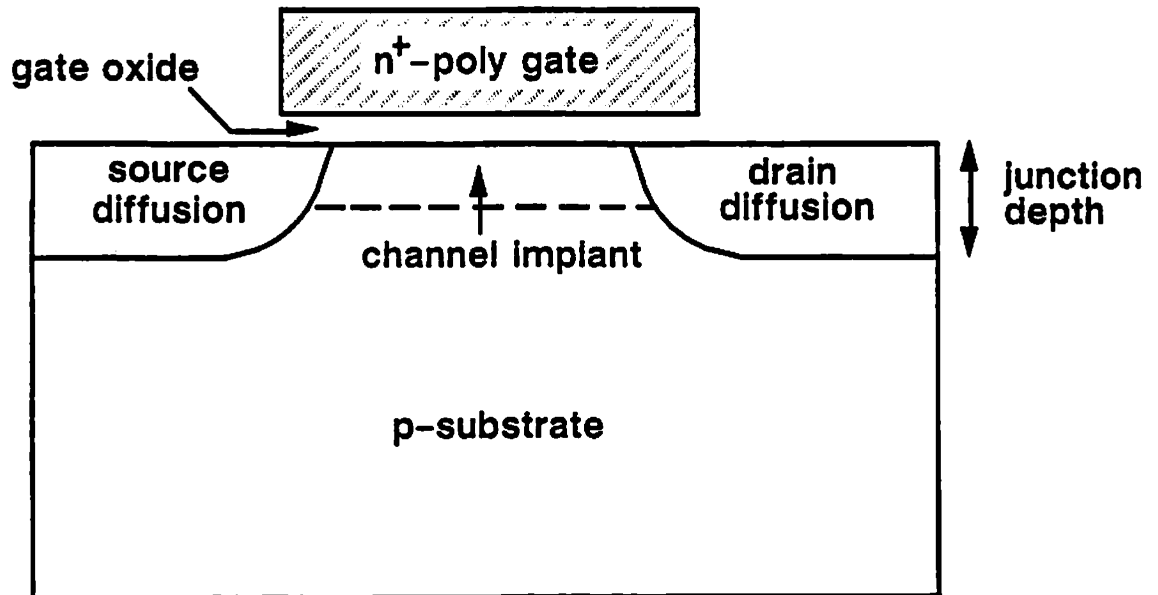


Figure 4-6 Cross section of an N-channel MOS transistor used in PISCES simulation.

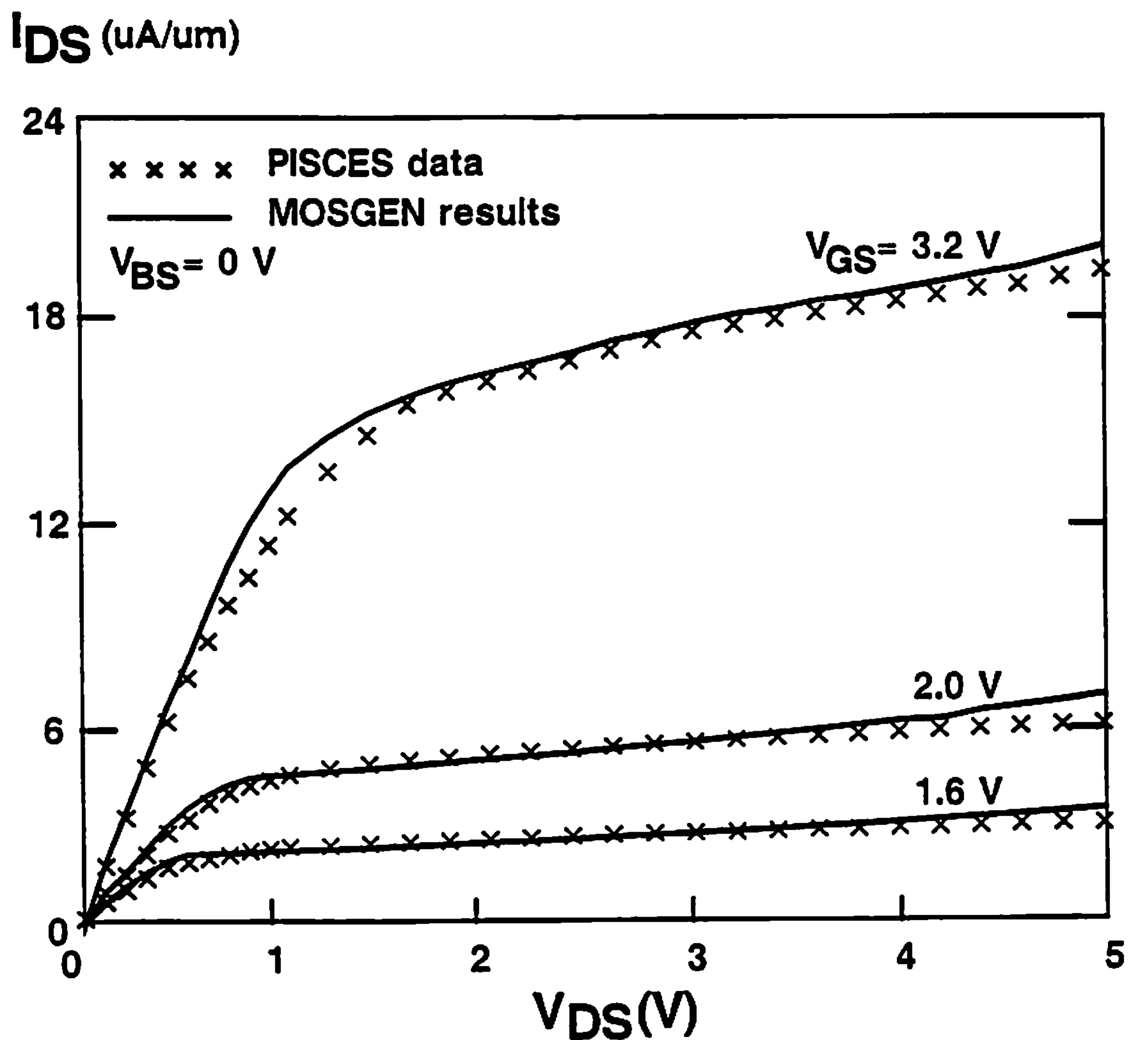


Figure 4-7 Comparison of I-V characteristics between SPICE simulation results with MOSGEN-extracted parameters and the direct PISCES data for an Leff = 1.1 um transistor. The Level-2 model is used.

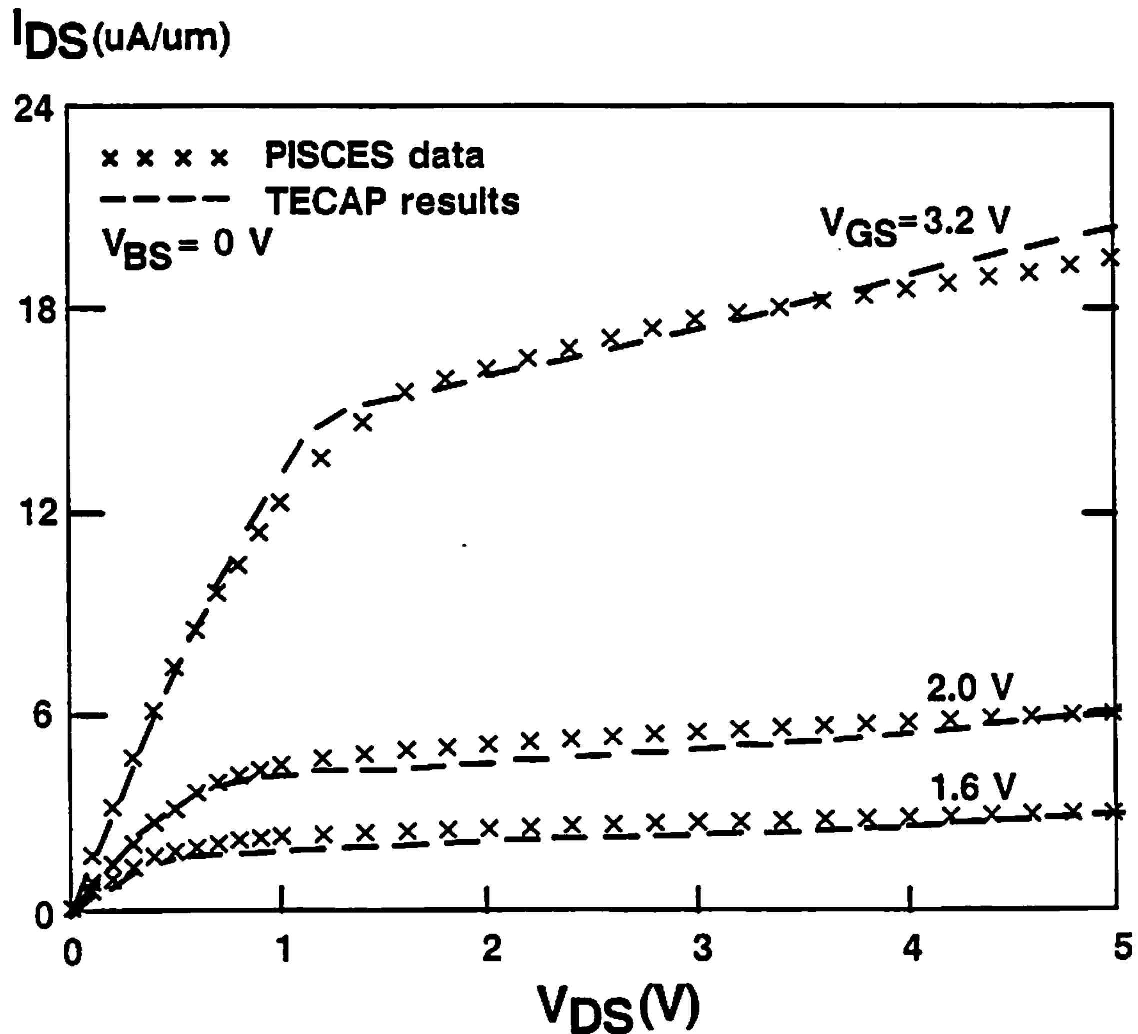


Figure 4-8 Comparison of I-V characteristics between SPICE simulation results with TECAP-extracted parameters and the same set of PISCES data as in Figure 4-7. The Level-2 model is used.

GEN has been carried out. The comparison reference consists of transistor drain-current data from 150 PISCES simulations. MOSGEN extracts SPICE parameters from six PISCES results. Figure 4-7 shows a comparison of I-V characteristics between SPICE simulation results using MOSGEN-extracted parameters and the direct PISCES data. Good agreement can be found. Figure 4-8 shows another comparison of I-V characteristics between the SPICE simulation results with the TECAP-generated parameters and the direct PISCES data. All the 150 PISCES data were needed by the TECAP program.

Notice that the accuracy of TECAP results is comparable to that of the MOSGEN results. However, the TECAP program requires hundreds of PISCES data points as the input, while only several PISCES runs are needed by MOSGEN. Significant saving in CPU-time as well as storage space for data has been achieved by using MOSGEN.

At present, PISCES does not offer device information along the width dimension. Therefore, the width-related SPICE parameters can not be accurately generated by the current version of the MOSGEN program. Default values of the width-related parameters are to be used in SPICE simulation. n This limitation can be eliminated once the 3-dimensional device information is available from a device simulator.

Table 4-3 lists the MOSGEN-extracted Level-2 parameter values for three fabrication processes. In process 1, gate-oxide thickness of 25 nm and channel implant dose of 6×10^{11} cm^{-2} were used. Notice that V_{TO} of 0.752 V, γ of 0.23 $V^{1/2}$, and λ of 0.013 V^{-1} were obtained. In process 2, a smaller channel implant dose is used. The SPICE parameter values change to V_{TO} being 0.683 V, γ being 0.22 $V^{1/2}$, and λ being 0.017 V^{-1}. In process 3, a larger gate-oxide thickness is used. The corresponding SPICE parameter values change to V_{TO} being 1.03 V, γ being 0.576 $V^{1/2}$, and λ being 0.091 V^{-1}.

Table 5-3 MOSGEN-extracted SPICE Level-2 MOSFET model parameters.

process	1	2	3
T_{OX} dose energy	25 nm $6\times10^{11}cm^{-2}$ 20 KeV	25 nm $5\times10^{11}cm^{-2}$ 30 KeV	40 nm $6\times10^{11}cm^{-2}$ 20 KeV
V_{TO}	0.752	0.683	1.03
K_P	8.28×10^{-5}	8.28×10^{-5}	5.17×10^{-5}
L_D	2.78×10^{-7}	2.78×10^{-7}	2.78×10^{-7}
γ	0.23	0.22	0.576
λ	0.013	0.017	0.091
N_{SUB}	1.0×10^{16}	1.0×10^{16}	1.0×10^{16}
X_J	0.3×10^{-6}	0.3×10^{-6}	0.3×10^{-6}
ϕ_B	0.726	0.726	0.726
$2\phi_F$	0.679	0.679	0.679
J_S	9.08×10^{-7}	9.04×10^{-7}	9.13×10^{-7}
μ	600	600	600
N_{SS}	1.0×10^{10}	1.0×10^{10}	1.0×10^{10}
v_{MAX}	1.0×10^{5}	1.0×10^{5}	1.0×10^{5}
N_{EFF}	2.28	2.40	1.44
U_{EXP}	0.531	0.574	0.449
U_{CRIT}	2288	4178	1250

4.3.2. MESGEN Results

The channel length of the MESFET used in the simulation is 0.8 μm. The drain and source electrodes are specified as ohmic contacts. The gate electrode is set to be a Schottky barrier contact with appropriate work function and modeled using the thermionic emission-diffusion theory. Since MESFET's are fabricated with highly doped N-type GaAs active layers, the transport properties of the device are dominated by electrons and the contribution of holes to the total current flow can be neglected.

The CPU time for PISCES simulations can be tremendously reduced by using MESGEN for parameter value generation. In the TECAP extraction case, 75 PISCES data are needed to generate the model parameter values, whereas only four PISCES runs are required by MESGEN. Figure 4-9 shows a comparison of I-V characteristics between the MESGEN-SPICE simulation results and the PISCES data. Good accuracy has been achieved

4.4. Applications

With PARGEN available as efficient and accurate interface between a device simulator and a circuit simulator, an integrated simulation environment containing pertinent process, device, and circuit simulation tools is established. Example applications of an integrated simulation environment are shown in Figure 4-10. The capability of offering quick simulation to evaluate the sensitivity of device model parameters to each process variable highly assists the development of new processes. The direct feedback of circuit response to the process engineer can facilitate better refinement of the fabrication process and device structure. Statistical process variation can also be efficiently addressed in this integrated simulation environment. In this section, the applications of PARGEN in the integrated simulation environment are presented.

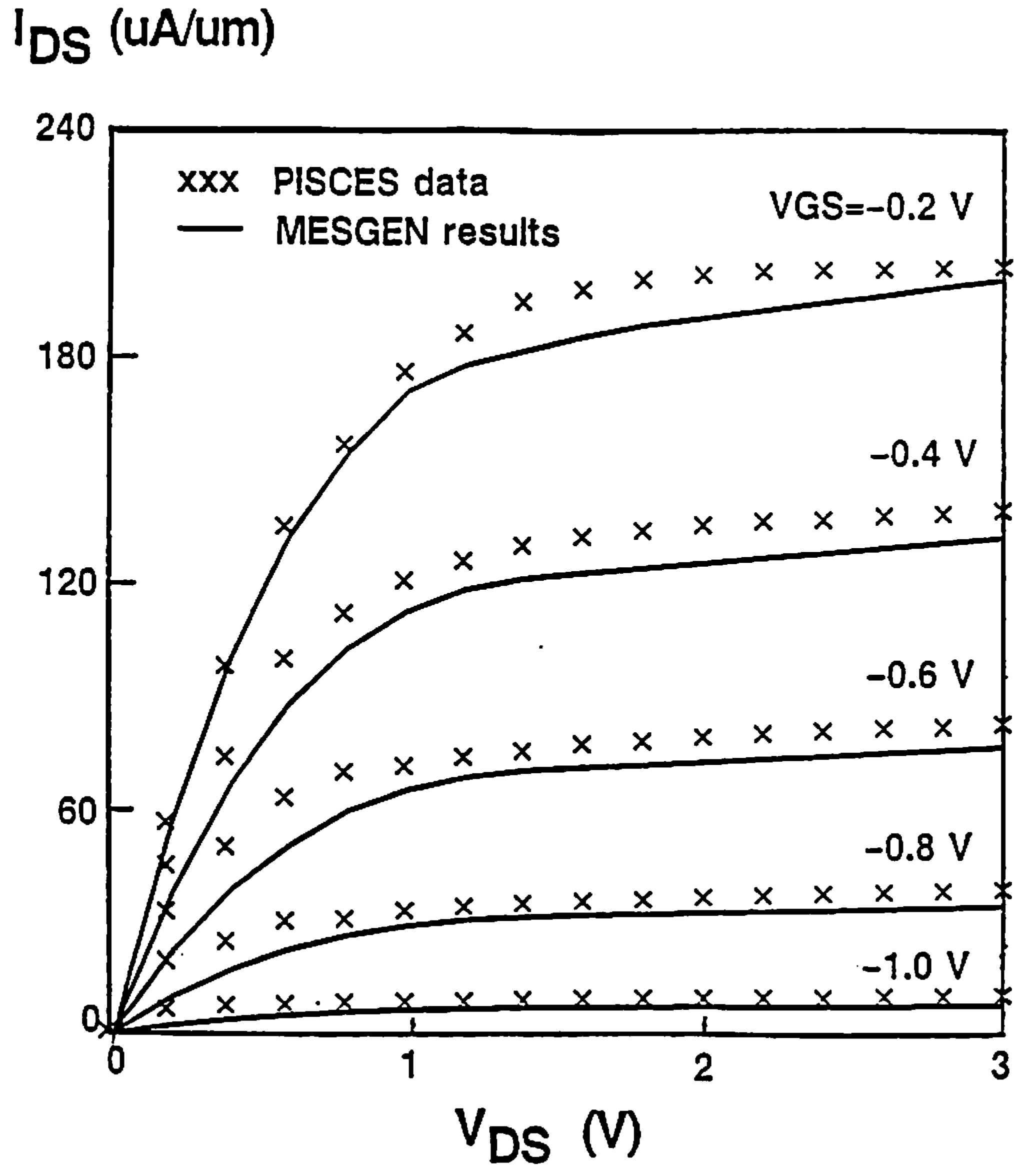


Figure 4-9 **Comparison of transistor I-V characteristics between MESGEN-SPICE simulation results and PISCES data for an L=0.8 um transistor.**

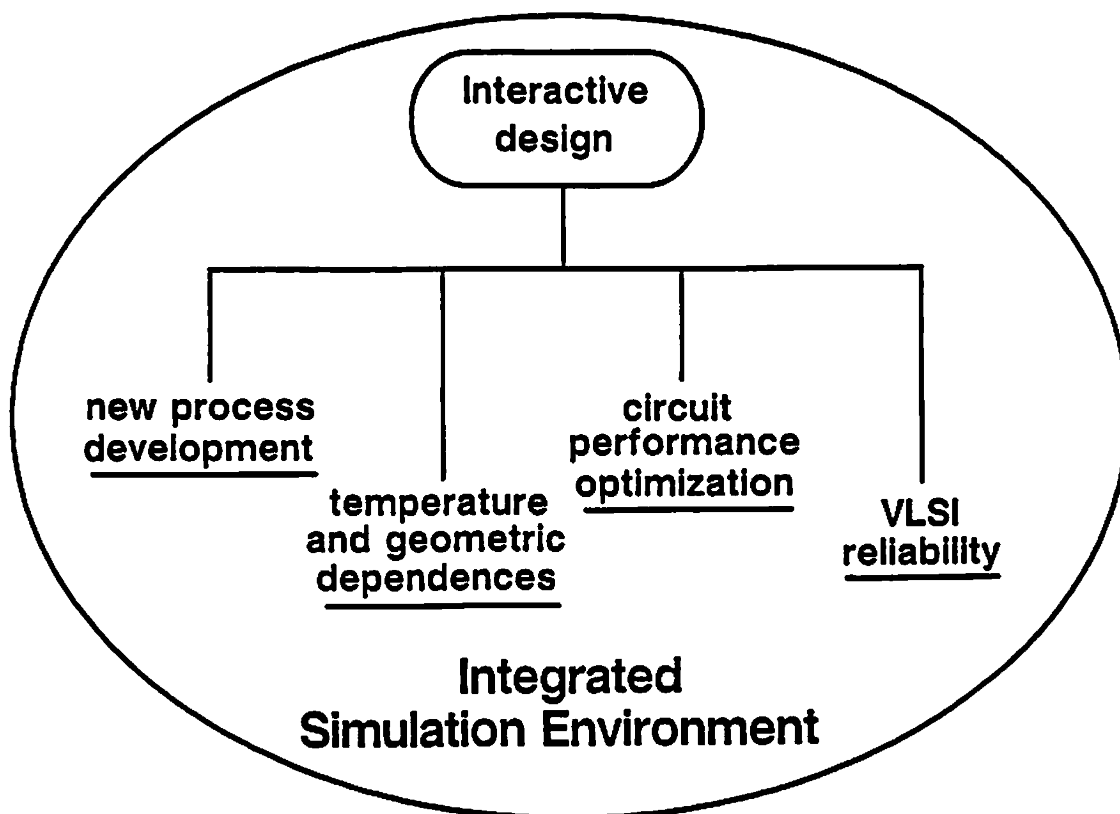


Figure 4–10 Potential applications of the integrated simulation environment.

4.4.1. Integrated Simulation Environment

Advanced computer-integrated manufacturing (CIM) systems are crucial in the competitive production of standard and application-specific VLSI circuits and systems [4.6,4.7]. Many design-oriented tools, such as SUPREM, FABRICS, and SPICE, have become widely used in the IC industry. To be further useful in the manufacturing environment, these tools need to be intelligently integrated so that the manufacturing organization could efficiently examine just how a microscopic variable, such as diffusion time, affects final device and circuit performance and product yield.

Several examples are presented to illustrate the applications of PARGEN in predicting the effect of process variables on device and circuit performance.

(A) Example 1

Impurity distribution after annealing in the channel due to ion implantation can be approximated by the Gaussian function,

$$N(x) = \frac{N_s}{\sqrt{2\pi}\,\Delta R_p} \exp\left[- \frac{(x - R_p)^2}{2\,\Delta R_p^2} \right] \tag{4.23}$$

where N_s is the implant dose, R_p is the projected range, and ΔR_p is the standard deviation of the impurity distribution. For the case of threshold adjust implant with boron at an implantation energy of 30 KeV, the tabulated R_p and ΔR_p values are 0.1 μm and 0.038 μm, respectively. Figure 4-11 shows the PISCES-simulated boron doping profiles in a silicon substrate using Gaussian approximation for two ion implantation cases. The corresponding two-dimensional carrier distributions are shown in Figure 4-12(a) and (b). The substrate concentration is 1×10^{16} cm^{-3} . The case shown in Figure 4-12(a) has a larger boron charge in the channel region than the case shown in Figure 4-12(b). Therefore, its threshold voltage is greater. The threshold voltages determined by MOSGEN are 0.752 V and 0.683 V for the two cases shown in Figure 4-12(a) and (b), respectively.

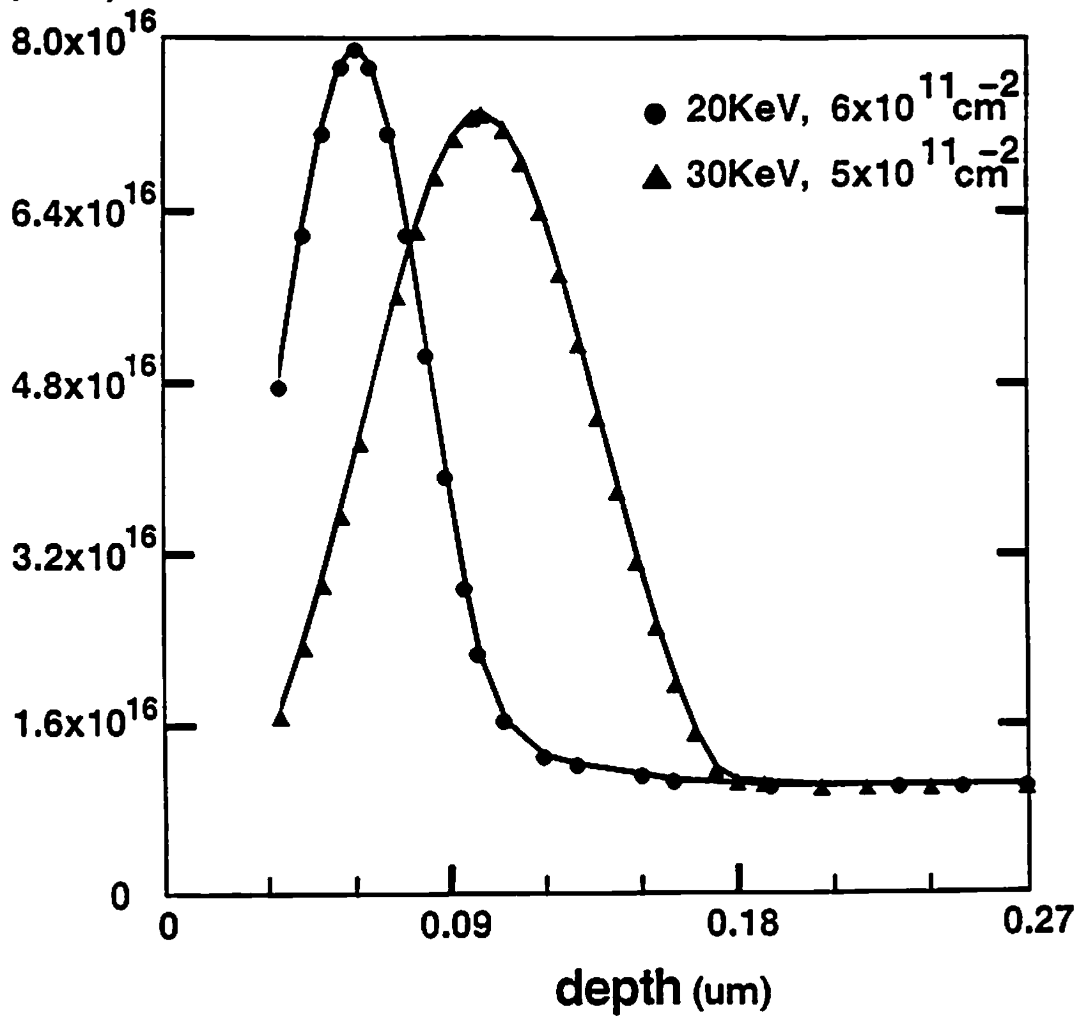


Figure 4-11 Simulated boron doping profiles on a silicon wafer for two ion implantation cases. The substrate doping is $1 \times 10^{16} cm^{-3}$.

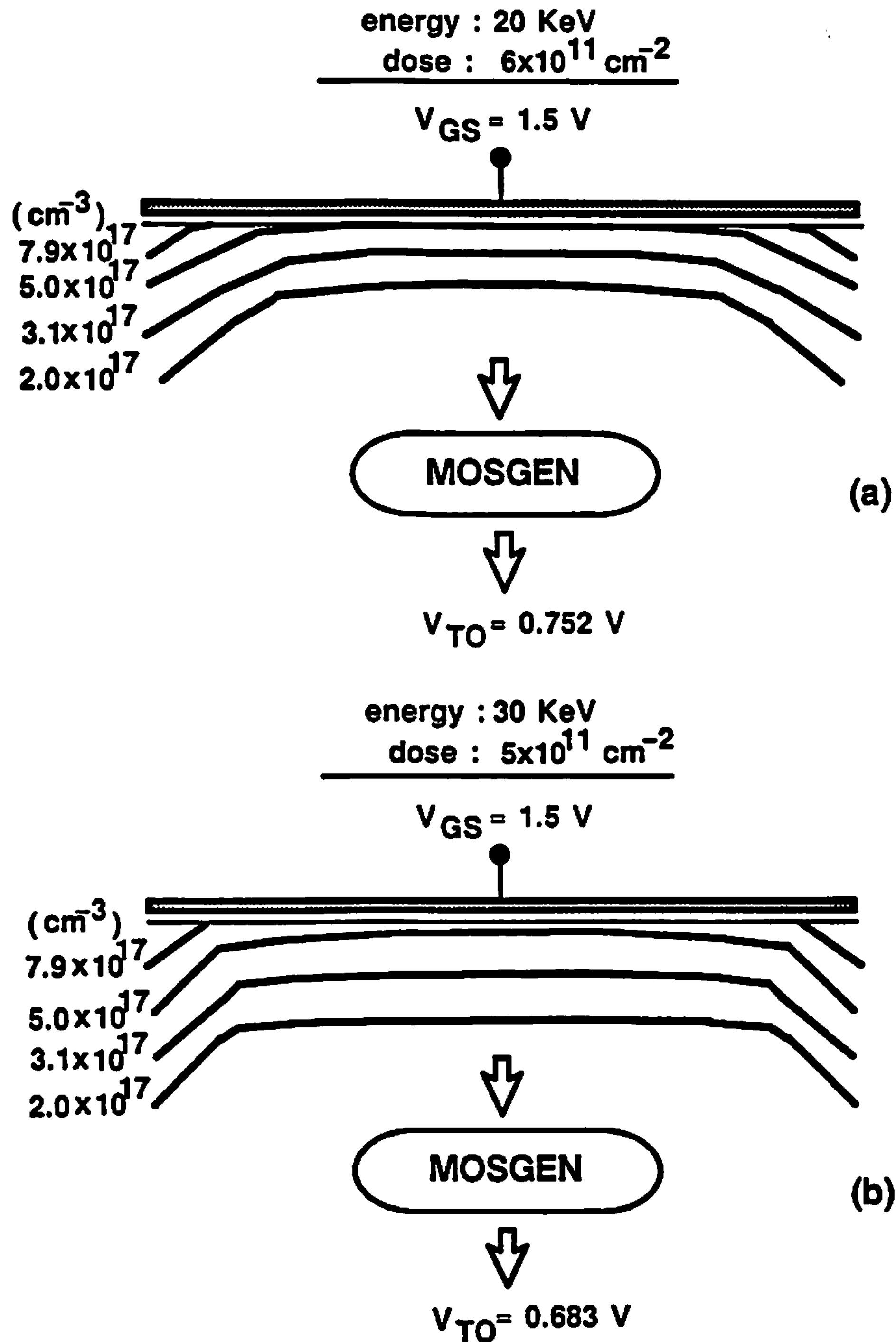


Figure 4-12 Two-dimensional carrier distributions from PISCES simulation. (a) An implantation dose of $6 \times 10^{11} cm^{-2}$ and an energy of 20 KeV. (b) An implantation dose of $5 \times 10^{11} cm^{-2}$ and an energy of 30 KeV.

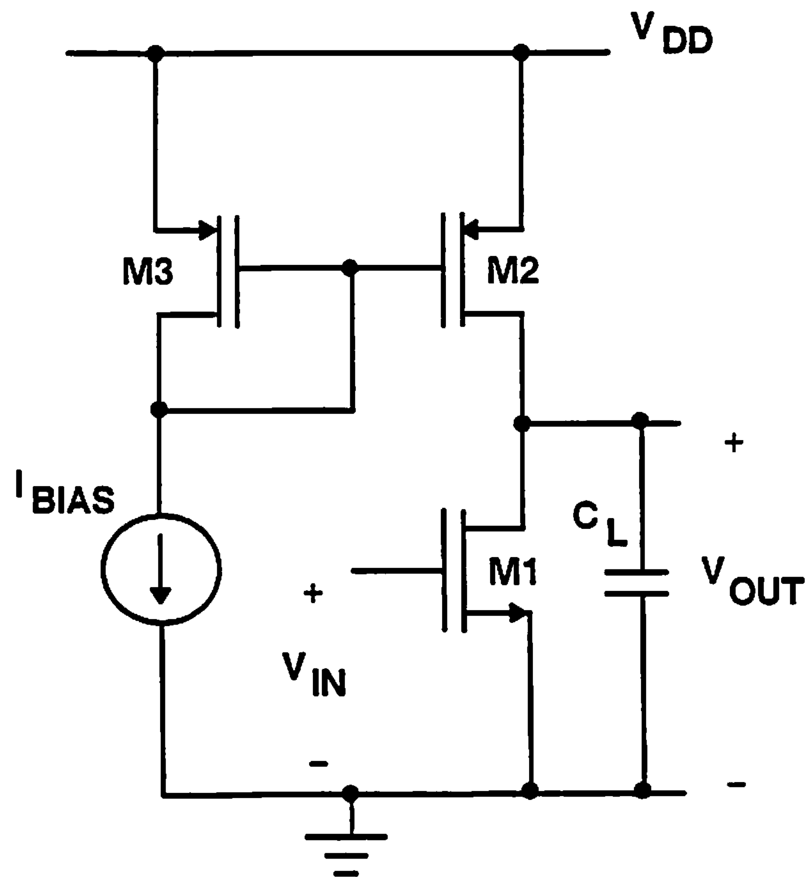


Figure 4-13 Circuit schematic of the core circuitry for a single-stage CMOS amplifier.

(B) Example 2

Figure 4-13 shows the circuit schematic of a single-stage CMOS amplifier. The open-loop voltage gain can be expressed as,

$$A_{v0} = -\frac{g_{m1}}{g_{o1} + g_{o2}} \tag{4.24}$$

where g_{o1} and g_{o2} are the output conductances of transistors M1 and M2, respectively, and g_{m1} is the transconductance of transistor M1.

The effect of channel implantation energy on the open-loop voltage gain is shown in Figure 4-14. In the range of interested implantation energy, the voltage gain is a monotonically increasing function of the implantation energy. This is because the implantation energy determines the detailed impurity distribution near the drain region, which in turn affects the magnitude of channel-length modulation. The PISCES results show that the doping concentrations along the current path are higher for a larger implantation energy. Hence, the voltage gain increases with the implantation energy.

(C) Example 3

Figure 4-15 shows a GaAs inverter with four MESFET's and two level-shifting diodes. The effects of active-layer thickness on the inverter characteristics are investigated. The active-layer thicknesses of 0.15 μm, 0.17 μm, and 0.19 μm are used. The transient responses are shown in Figure 4-16 and the transfer characteristics are shown in Figure 4-17. Notice that the distinct slopes in the transition region of the transfer characteristics for three different thicknesses.

(D) Example 4

Figure 4-18 shows a single-stage GaAs operational amplifier. The changes in device parameter values due to different implantation doses were obtained from the MESGEN program. The parameter values can then be used by the circuit simulator SPICE-3 to simulate the open-loop voltage gain. The effect of implantation dose on the open-loop voltage gain is shown in Figure

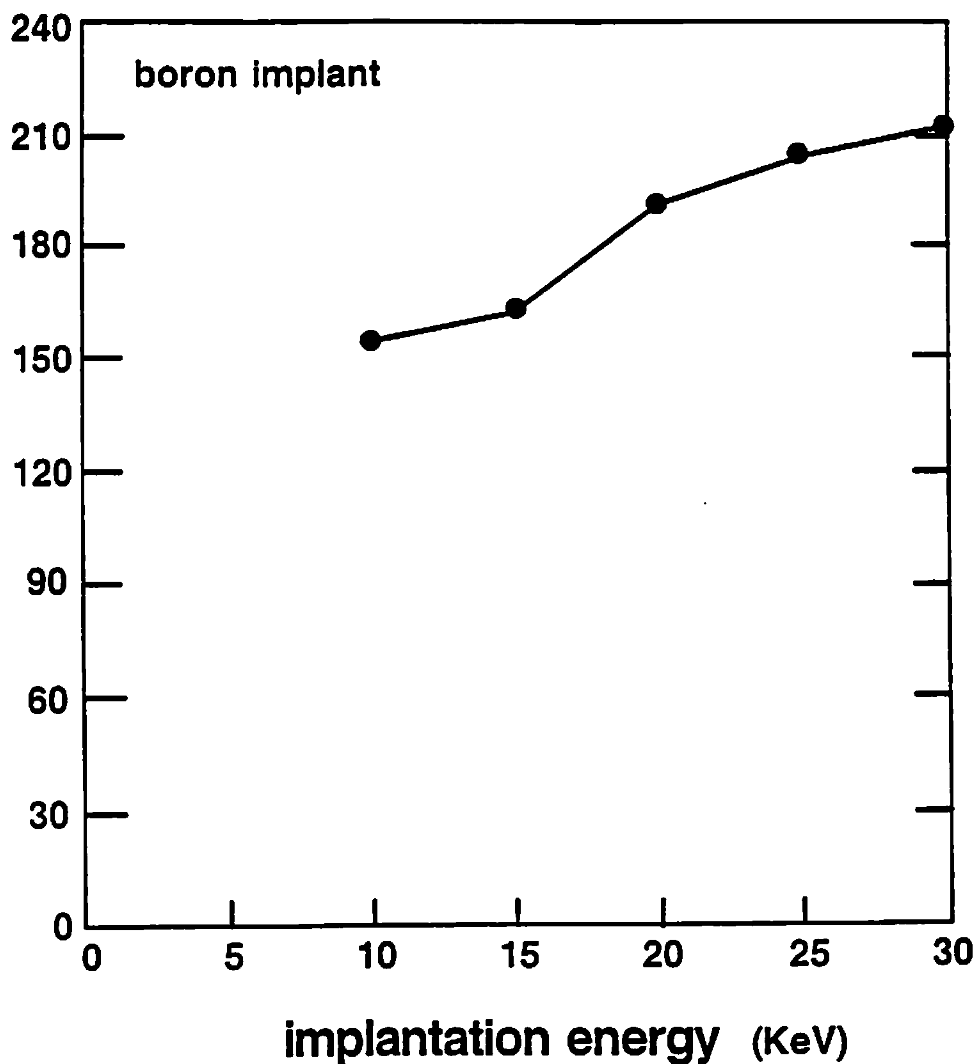


Figure 4-14 Plot of the open-loop voltage gain versus the boron ion implantation energy. The integrated simulation environment is used to produce the results.

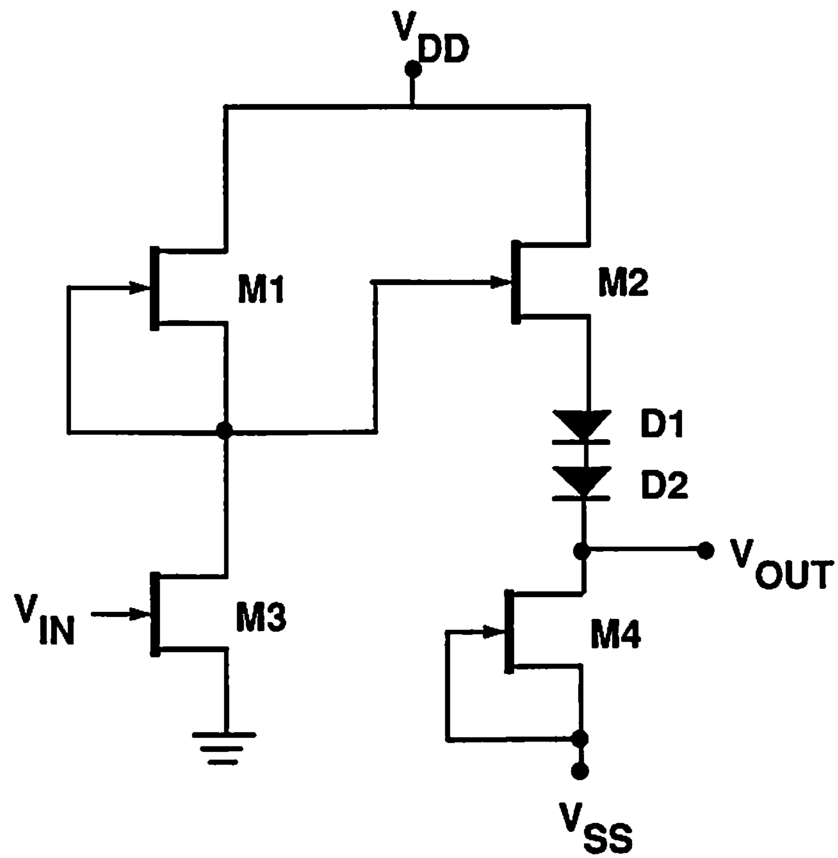


Figure 4-15 A GaAs inverter circuit with four MESFET's and two level-shifting diodes.

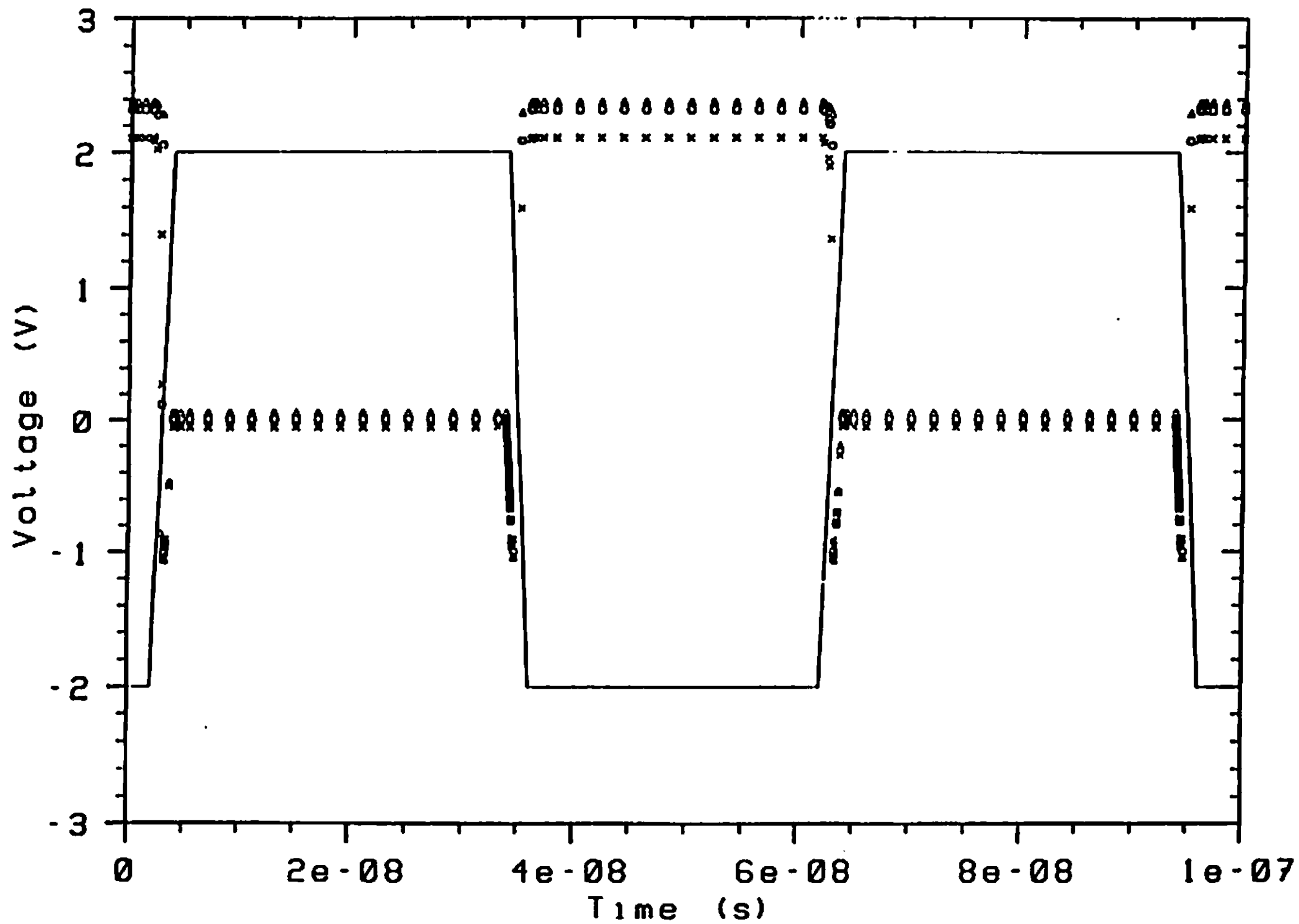


Figure 4-16 The inverter transient responses with different transistor active-layer thicknesses. Δ: 0.19 um, O: 0.17 um, x: 0.15 um The solid line represents the input waveform.

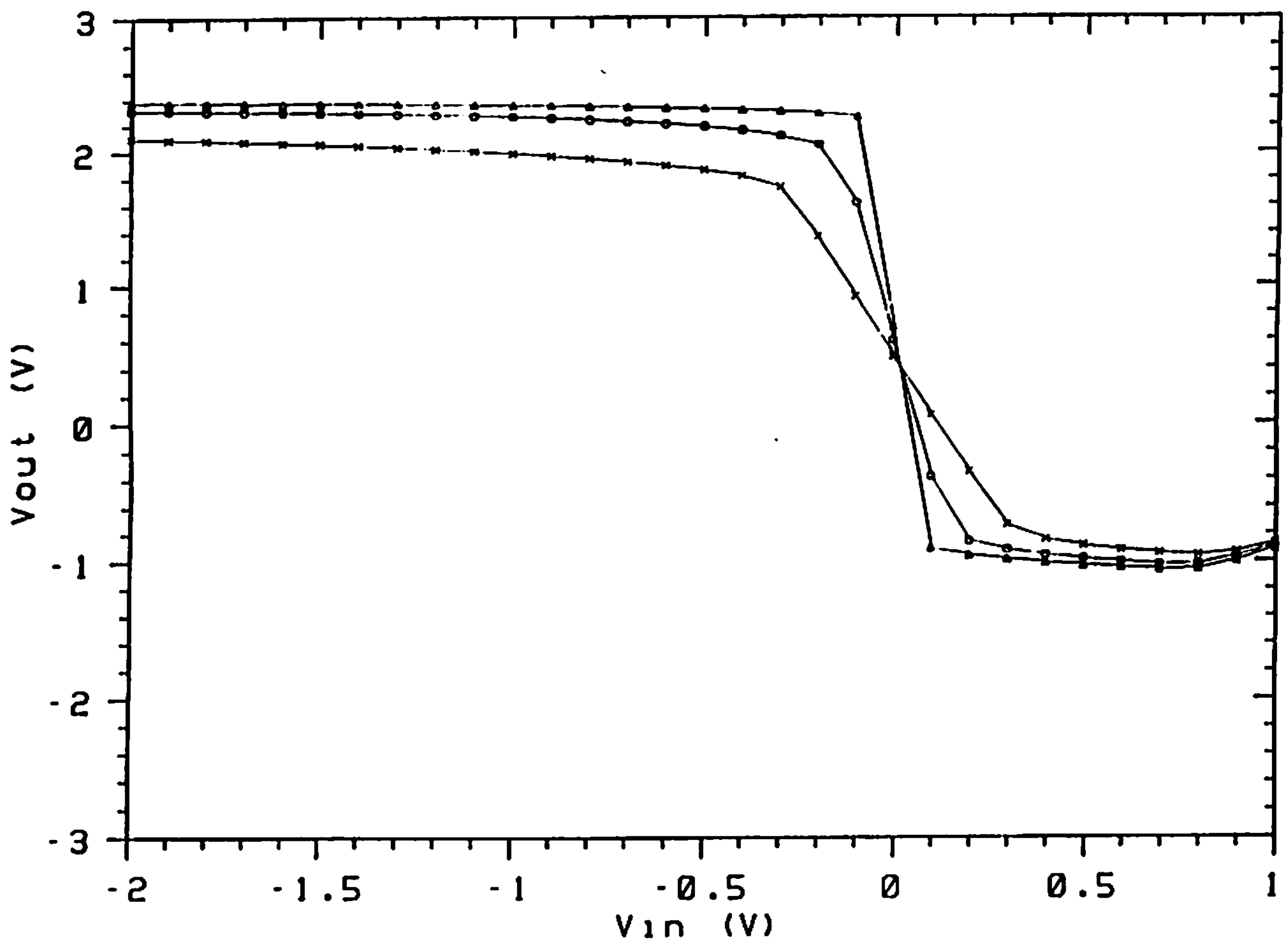


Figure 4-17 The inverter transfer characteristics with different transistor active-layer thicknesses. Δ: 0.19 um, O: 0.17 um, x: 0.15 um.

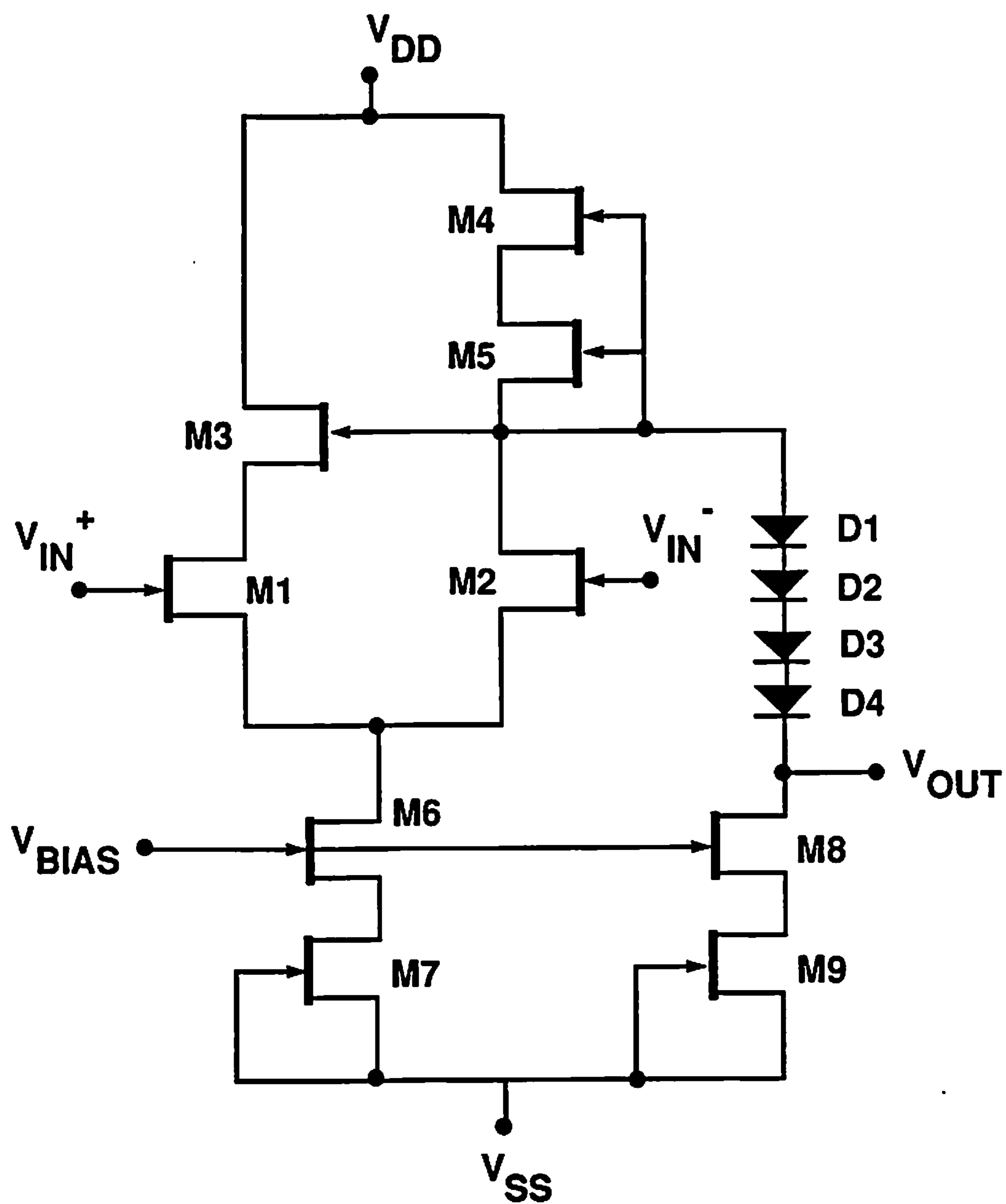


Figure 4-18 Circuit schematic of a single-stage GaAs Op-Amp.

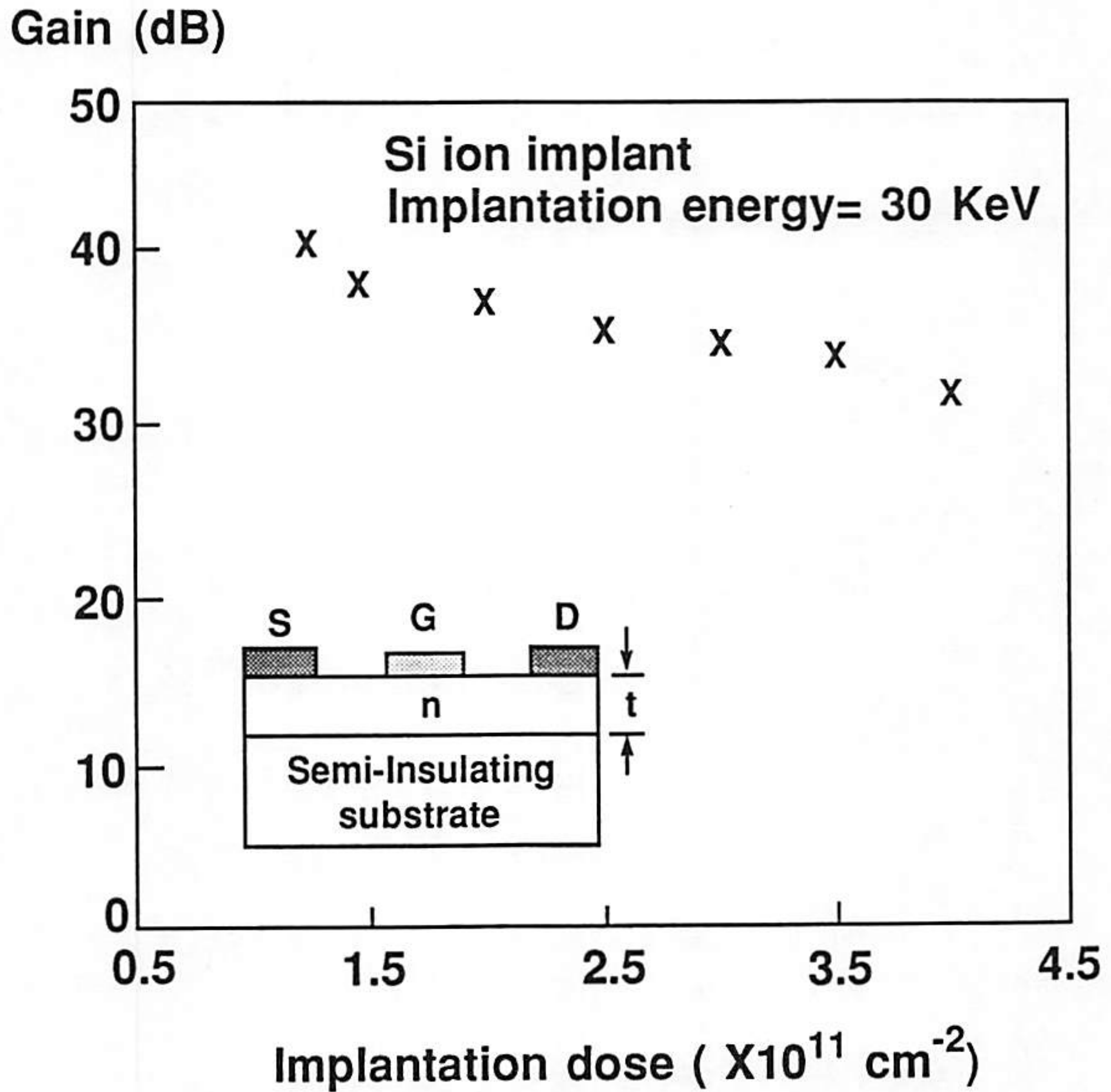


Figure 4-19 The effect of the implantation dose on the open-loop voltage gain.

4-19. The sensitivity of the voltage gain to the implantation dose is useful information for the process optimization to achieve the desired circuit performance.

4.4.2. Determination of Geometric Dependences of Submicron MOS Transistor Parameters

As MOS transistor dimensions are shrunk to the submicrometer range, device electrical parameters show significant dependences on the channel length and width [4.8]. The zero-bias threshold voltage and the body-effect coefficient decrease with reduced channel length due to the depletion charge sharing from the source and drain terminals.

A major requirement in constructing MOS transistor models for VLSI circuit simulation applications is to provide accurate geometric dependences of the electrical parameters. Inverse-geometry dependences of electrical parameters were found to be adequate for devices with conventional structures [4.9]. However, few results have been obtained on the geometric dependences for advanced VLSI device structures, such as structures with the inclusion of lightly-doped-drain (LDD) regions [4.10] and multiple channel implants. Due to the complex two-dimensional small-geometry effects in submicron transistors, derivation of closed-form expressions for electrical parameters based on pure device-physics is extremely difficult. Efficient device-circuit simulation can be very useful in the design and analysis of new VLSI device structures.

(A) The Method

The method used was described in Section 4.2.1. No *a priori* geometric shape of the bulk depletion region is assumed in the analysis. This makes it applicable to devices with various source/drain structures since the depletion charge sharing from source and drain terminals needs not to be calculated to obtain the electrical parameter values. This method is efficient because no ex-

tensive I-V data points are needed from the device simulator to extract electrical parameter values.

(B) Experimental Results and Discussion

To determine the extraction resolution for the threshold voltage, six different gate biases from 1.3 V to 1.8 V in an increment of 0.1 V were applied to a conventional transistor with an effective channel length of 1.8 μm. The sensitivity of the extracted threshold voltage to the applied gate bias is less than 3%.

MOS transistors with LDD structure were used in our simulation. The gate-oxide thickness is 10.0 nm, the substrate doping is 8×10^{15} cm^{-3} , and the channel region is implanted by boron with an energy of 10 KeV and a dose of 3×10^{11} cm^{-2} . The peak doping concentration of the n^- region is 7×10^{18} cm^{-3} and that of the n^+ source/drain regions is 1×10^{20} cm^{-3} . The junction depths of the n^- and the n^+ regions are 0.2 μm and 0.25 μm, respectively. Figure 4-20 shows the cross section of an LDD MOS transistor with L_{eff} = 0.5 μm and the electron concentration contours.

The threshold-voltage reduction (ΔV_{T0}) is defined as

$$\Delta V_{T0} \equiv V_{T0(Long)} - V_{T0(Short)} . \tag{4.25}$$

In the simulation, an L_{eff} = 9.8 μm transistor was used as the reference long-channel device. The simulated zero-bias threshold voltage of the reference transistor is 0.72 V. To investigate the channel-length dependence of ΔV_{T0} , threshold voltages of ten transistors were determined. Figure 4-21(a) shows the plot of ΔV_{T0} versus $1/L_{eff}$. The correlation coefficient for the plot is 0.998. The threshold-voltage reduction for a channel length in the submicron range can be well modeled by the inverse-linear function. The inverse-linear dependence was proposed to be clamped at some channel length because the thresh-

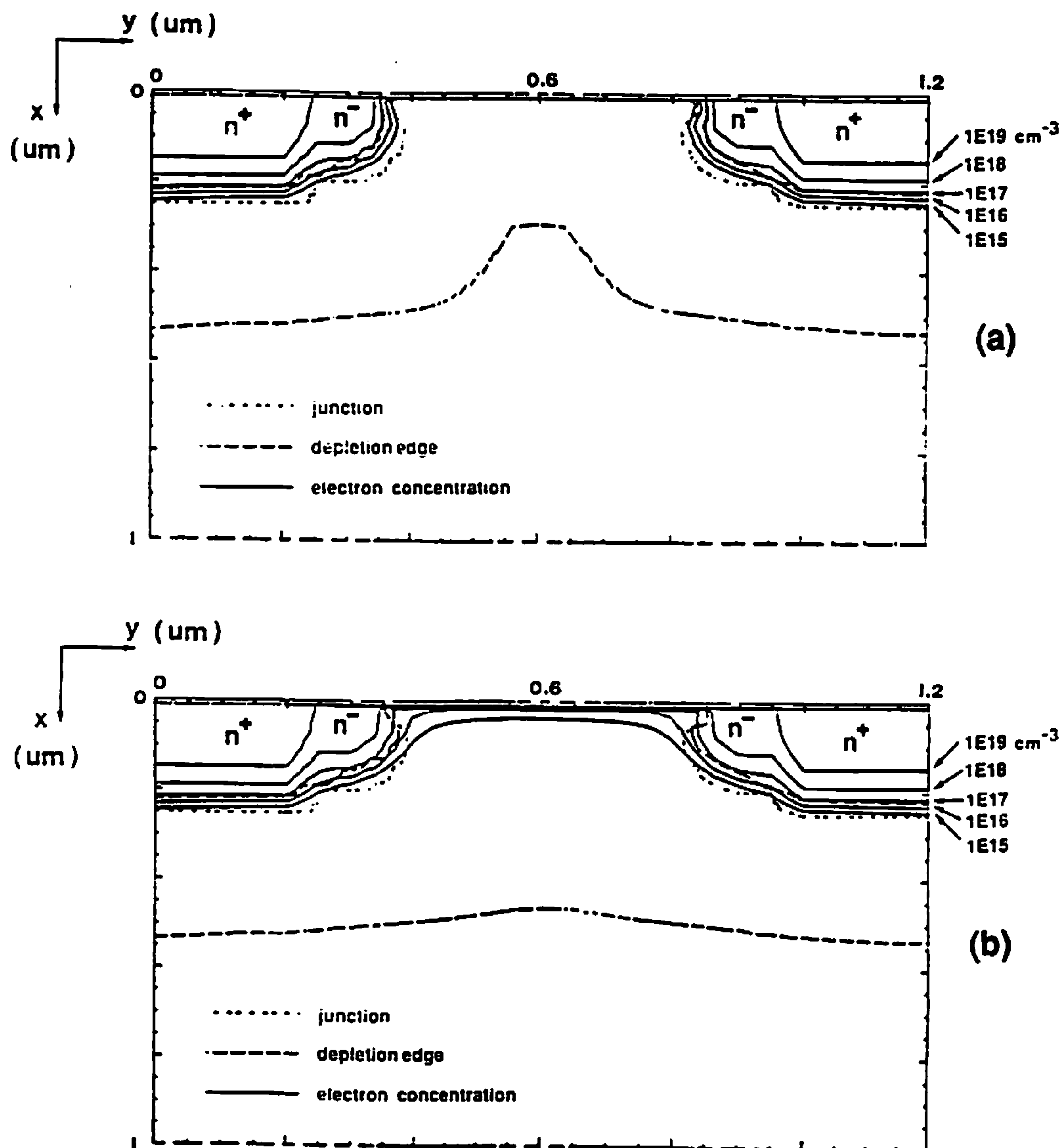
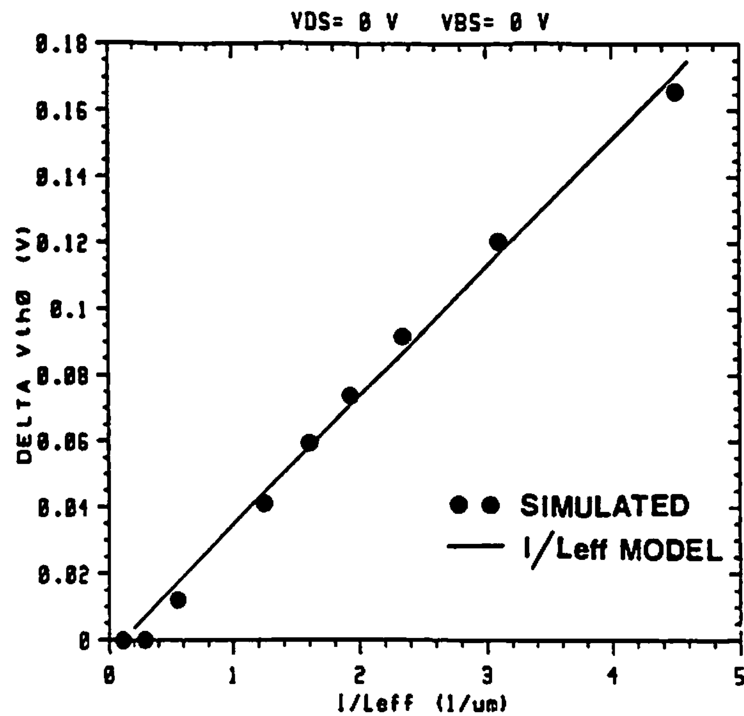


Figure 4-20 Electron concentration contours for an N-type LDD MOS transistor. (a) All terminals are grounded. (b) V_{GS} = 1.5 V, V_{DS}= 0 V, and V_{BS} = 0 V.



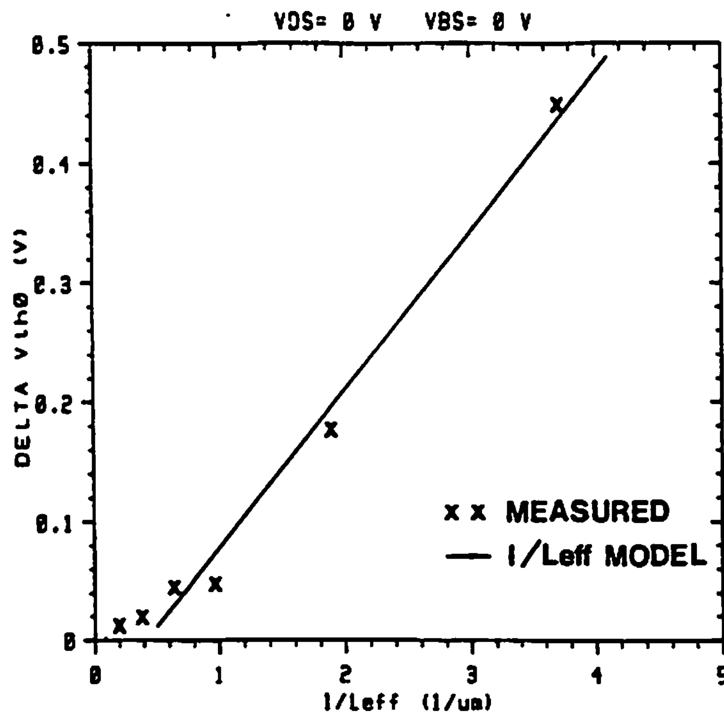


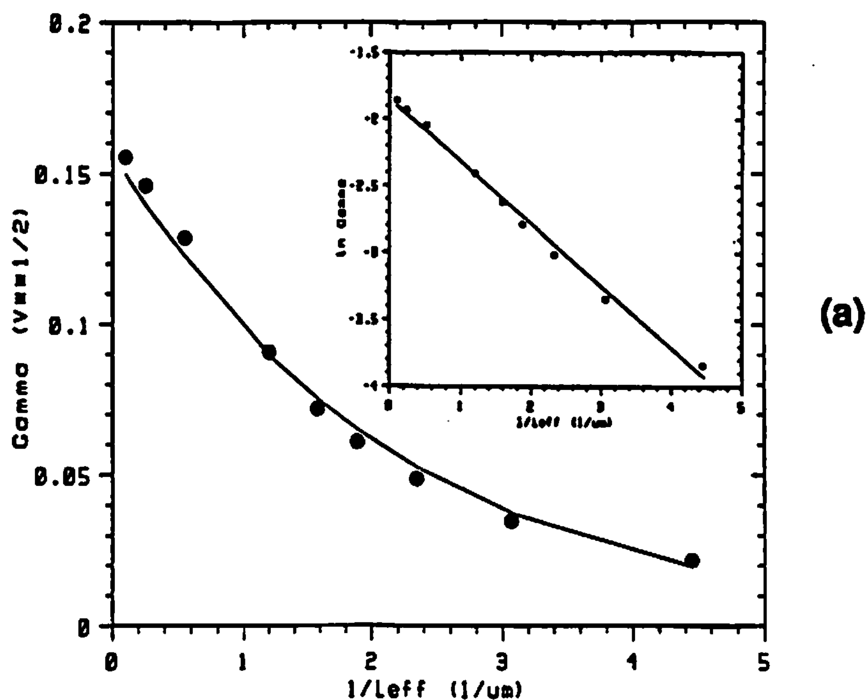
Figure 4-21 The plot of ΔV_{T0} versus $1/L_{eff}$. A straight line is fitted through the data points with the least-square-error technique. (a) PISCES-extracted results. The correlation coefficient is 0.998. (b) Measured data. The correlation coefficient is 0.991.

old voltage reduction is zero for long-channel transistors [4.9].

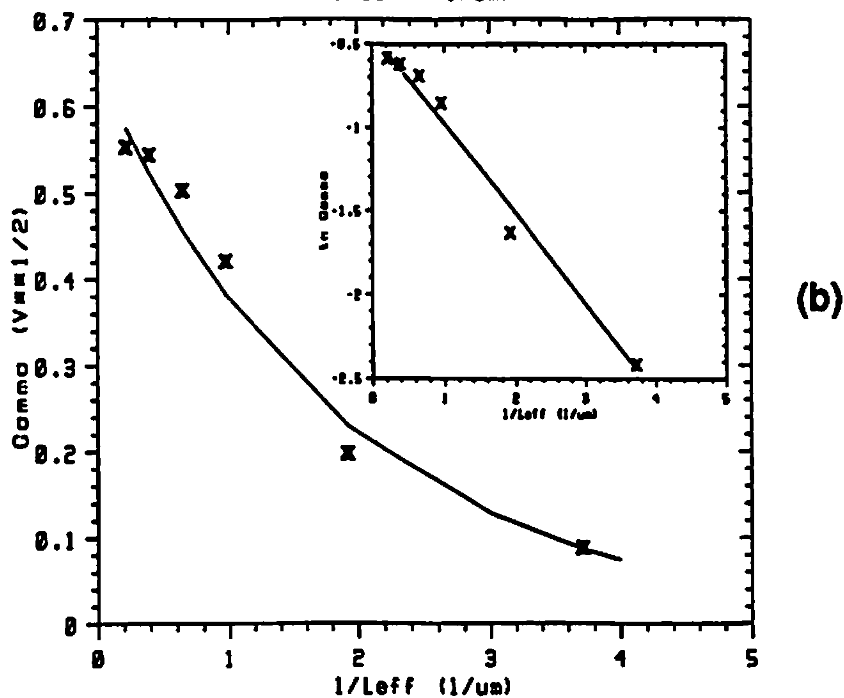
Measured results were obtained from experimental short-channel transistors fabricated by 0.6-μm CMOS technology from Hewlett-Packard Company. For N-type transistors, the substrate doping is 1.4×10^{16} cm^{-3} and the enhancement implant is 1×10^{12} cm^{-2}. The n^- region is formed by implanting 4×10^{12} cm^{-2} phosphorus at 80 KeV, followed by an n^+-implant masked by a 0.3 μm oxide spacer. The gate-oxide thickness is 20.0 nm. Threshold voltages were determined by the linear extrapolation of I_{DS}-V_{GS} characteristics. The zero-bias threshold voltage of the L_{eff} = 9.5 μm reference transistor is 0.68 V. The plot of measured ΔV_{T0} versus $1/L_{eff}$ is shown in Figure 4-21(b). The correlation coefficient for the measured data points is 0.991. These measurement results confirm that the inverse-linear dependence is a good representation of the threshold-voltage reduction.

The PISCES-extracted and measured body-effect coefficients are plotted against $1/L_{eff}$ in Figure 4-22(a) and (b), respectively. Extracted body-effect coefficients were obtained from (8) with V_{BS} = -1 V and measured results were determined from the plot of V_T against $\sqrt{2\phi_F - V_{BS}}$. The potential in the bulk of the silicon ϕ_F was determined from the substrate doping concentration. For nonuniformly doped transistors, V_T does not vary linearly with $\sqrt{2\phi_F - V_{BS}}$. However, a straight line was fitted through the data by the linear regression with a correlation coefficient better than 0.99.

The solid lines in Figure 4-22 represent a function of $\exp(-C / L_{eff})$, where C is a fitting parameter determined by effective substrate doping concentration. Notice that this exponential function can be used to model the channel-length dependence of the body-effect coefficient accurately. Figure 4-23 shows a plot of parameter C versus the peak doping concentration in the chan-



(a)



(b)

Figure 4-22 The plot of body-effect coefficient versus $1/L_{eff}$. The insert shows the logarithm of body-effect coefficient versus $1/L_{eff}$. (a) PISCES-extracted results. The correlation coefficient in the insert is -0.996. (b) Measured data The correlation coefficient in the insert is -0.991.

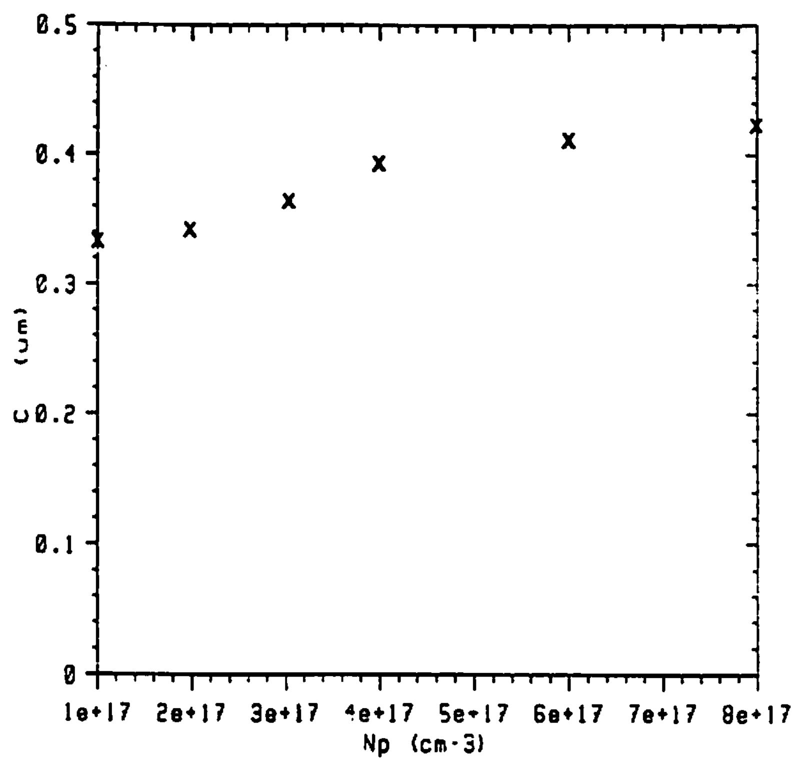


Figure 4-23 The plot of the parameter C versus the peak doping concentration in the channel.

nel. The data in this plot were obtained from device simulation results for different channel implant doses. The value of parameter C slightly increases with increasing channel doping concentration. This is due to a larger change in the body-effect coefficient for higher channel doping concentration.

Chapter 5

Sensitive SPICE Parameters for VLSI Design

With PARGEN available as an interface for device and circuit simulators, technology-based design systems can be integrated for VLSI design. However, as device sizes are scaled down to the micron or submicron range, process variations have significant effects on the circuit performance and a great number of simulations in the integrated design environment must be performed to verify the circuit performance. With hundreds of thousands of transistors in a VLSI circuit and thirty to forty model parameters for each transistor, it is impractical for circuit designers to trace the effect of each model parameter on the circuit performance. Since the parameters of an MOS transistor model do not have uniform influence on the simulated output characteristics, circuit designers are concerned with the sensitive parameters which have large effects on the transistor characteristics. With a set of sensitive parameters, the number of circuit simulations for statistical design analysis can be reduced and the integrated simulation environment is more efficient for circuit designers to use.

In this chapter, a methodology using sensitive parameters for efficient circuit modeling and simulation is discussed. A sensitivity analysis is performed to identify a set of sensitive SPICE parameters for VLSI circuit design. The set of sensitive parameters was found to be dependent on the fabrication technologies [5.1].

5.1. SPICE Modeling for VLSI Circuit Analysis

Device models developed for the purpose of understanding basic device physics contain complicated mathematical equations. It may require a computer program just to solve these equations. The device simulator PISCES incorporates Poisson's and current continuity equations in a very detailed format to provide accurate internal and output device characteristics. These complex equations are not directly suitable for the circuit analysis purpose due to the large amount of computational time needed.

The table look-up modeling approach greatly reduces the model evaluation time by storing measured data in a computer. It requires interpolation formulas to obtain the device output characteristics. One major drawback of the table look-up approach is the limited number of device sizes that can be accurately simulated. The vast amount of information to be stored for each transistor further limits its applications.

5.1.1. Circuit-Level Modeling Requirements

Three key issues have to be carefully addressed in developing a transistor model for circuit simulation:

- device physics,
- computational efficiency, and
- circuit analysis accuracy.

Figure 5-1 shows the transistor modeling considerations and their associated features. An MOS transistor model must be not only physically meaningful and accurate, but also computationally efficient and memory effective to serve the VLSI circuit analysis needs.

Thorough understanding of device operation provides pertinent information for the development of a physics-based model which employs simple analytical expressions and associated parameters to represent the huge amount of

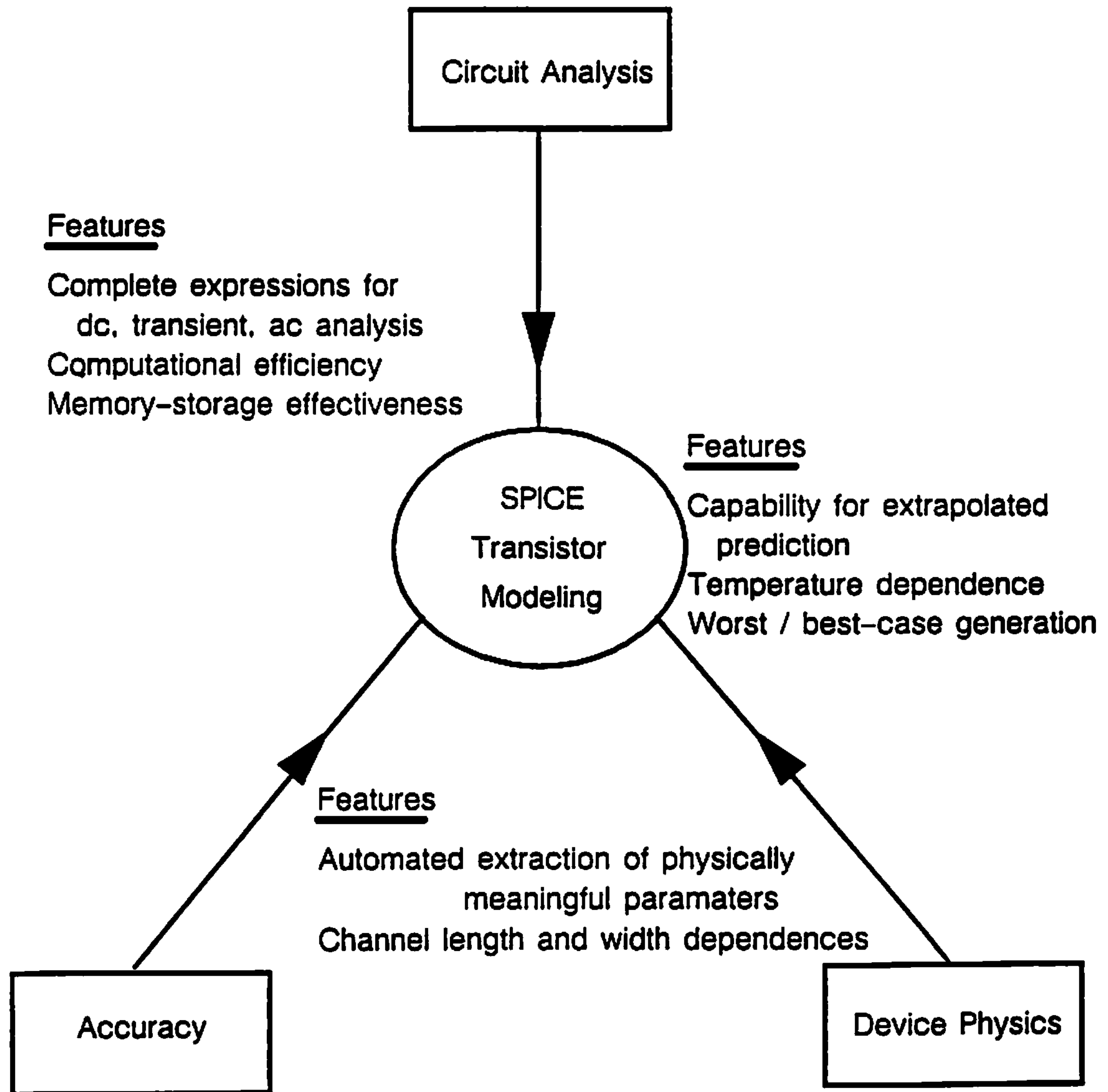


Figure 5-1 Three key considerations for SPICE transistor modeling.

device data. Temperature dependence and process-induced device characteristics variations can be incorporated by extending the device physics-based modeling expressions. Such a model is able to predict device and circuit behaviors beyond the measurement range.

The dc transfer analysis, large-signal transient analysis, and small-signal ac analysis are typical features available from a circuit simulator. An MOS transistor model for the circuit simulation purpose should include expressions for the drain current at both the strong-inversion region and the weak-inversion region, expressions for the terminal charges and inter-terminal capacitances, as well as expressions for small-signal conductances. Because the model expressions are to be evaluated thousands of times during each simulation task, complex mathematical expressions such as the logarithmic and hyperbolic functions should be avoided to the greatest extent. Continuous expressions for the drain current and terminal charges must be assured, while their first derivatives are preferred to be continuous.

5.1.2. SPICE Built-in MOS Transistor Models

At present, there are four MOS transistor models implemented in the SPICE-2G6B and SPICE-3C1 programs. Each model differs in complexity and is suitable for different fabrication technologies. The Level-1 model contains fairly simple expressions developed by Shichman et al. [5.2]. It is based on fundamental device physics and exclude detailed second-order effects. Therefore, it is most suitable for preliminary estimation of circuit performance. The Level-1 model is equipped with 8 parameters to model the channel-region characteristics. Additional 16 parameters are associated with the modeling of the source and drain components, and are shared by the Level-2 and Level-3 models.

The Level-2 model, which was developed by Vladimirescu et al., takes into account several second-order effects such as velocity saturation, transverse field induced mobility degradation, and noise. It was designed with 23 parame-

ters to model the channel-region characteristics. Some effects are modeled with different set of equations. When parameter V_{MAX} is assigned a finite value, the Baum's expression of modeling carrier velocity saturation [5.3] is used; otherwise, an expression corresponding to the pinch-off condition [5.4] is used. When parameter X_{QC} is assigned a value between 0 and 0.5, the Ward-Dutton's charge-based capacitance model [5.5] is used; while the default capacitance model uses the Meyer's capacitance model [5.6].

The Level-3 model represents an attempt at pursuing the semi-empirical modeling approach for short-channel devices. It only approximates device physics and relies on the proper choice of empirical parameters to accurately reproduce device characteristics. Twenty-one parameters are needed to model the channel-region characteristics.

The Level-4 model (BSIM) [5.7], which was developed by Sheu et al., can accurately model transistors fabricated by state-of-the-art 1-μm CMOS technologies. Both the channel length and width dependences of electrical parameters are incorporated into the model. It requires 67 parameters to model the channel-region characteristics.

Table 5-1 lists a comparison of important features available from existing SPICE MOS transistor models. The applicable fabrication technologies for the SPICE models are around 4 μm for the Level-1 model, 2 μm for the Level-2 and Level-3 models, and approximately 1-μm for the Level-4 model. Temperature dependence and noise expression need to be incorporated to make the Level-4 model more applicable for analog IC designs.

5.2. Parameter Extraction for Different Fabrication Technologies

Process-induced variation directly affect circuit performance and product yield. The application-specific ICs should be designed with the process-induced variations being carefully considered. In order to accomplish this task, accurate extraction of device parameter values and identification of a set of

Table 5-1 Comparison of important features among various existing SPICE MOSFET models.

Features \ MOS Models	LEVEL-1	LEVEL-2	LEVEL-3	LEVEL-4 (BSIM)
Developers	Shichman et al.(1968)	Vladimirescu et al.(1980)	Vladimirescu et al.(1980)	Sheu et al. (1985)
# Parameters for Channel Region	8	23	21	67
Small-Geometry Effects	NO	Emphasize Short-Channel Effect	Emphasize Short-Channel Effect	Short-Chan. & Narrow-Width Effects
Noise Modeling	NO	YES	YES	NO
Temperature Dependence	**Limited**	**YES**	**YES**	**NO**
Charge-based Capacitance Model	NO	YES	NO	YES
Subthreshold Conduction	NO	YES	YES	Continuity in Current & First Deriv.
Applicable Technology	4 um	2 um	2 um	1 um

sensitive parameters are indispensable.

In a typical extraction procedure, parameters are extracted sequentially, one at a time or in small groups. The value of each parameter is assumed fixed and accurate for use in extracting further parameters. A small portion of the model and data from a limited part of a device's operating range are used in extracting each parameter. A linear least-square-error fit is often used over each region. For example, the values of threshold- and mobility- related parameters are extracted in the linear region of operation, and these values are used in extracting velocity saturation and channel-length modulation parameters. These parameter values are usually extracted from the measured current data. While the simulated current results may compare well with the measured current data, the simulated output conductance, transconductance, and back-gate transconductance results can deviate significantly from the measured data.

Global optimization techniques using the Levenberg-Marquardt method, and the modified Gauss method have been widely used in general-purpose parameter extraction programs [5.8]. The quantity to be minimized is the mean-squared error between the calculated and measured results,

$$E_r = \frac{w_1}{m}\sum_A\left[\frac{I_{DS} - I^*_{DS}}{\max(I^*_{DS}, I_{DS0})}\right]^2 + \frac{w_2}{n}\sum_B\left[\frac{g_d - g^*_d}{\max(g^*_d, g_{d0})}\right]^2$$

$$+ \frac{w_3}{n}\sum_B\left[\frac{g_m - g^*_m}{\max(g^*_m, g_{m0})}\right]^2 + \frac{w_4}{n}\sum_B\left[\frac{g_{mb} - g^*_{mb}}{\max(g^*_{mb}, g_{mb0})}\right]^2$$

$$+ \frac{w_5}{n}\sum_B\left[\frac{C_{gs} - C^*_{gs}}{\max(C^*_{gs}, C_{gs0})}\right]^2 + \frac{w_6}{n}\sum_B\left[\frac{C_{gd} - C^*_{gd}}{\max(C^*_{gd}, C_{gd0})}\right]^2 \quad (5.1)$$

where

$$w_i \geq 0, \quad 1 \leq i \leq 6$$

and

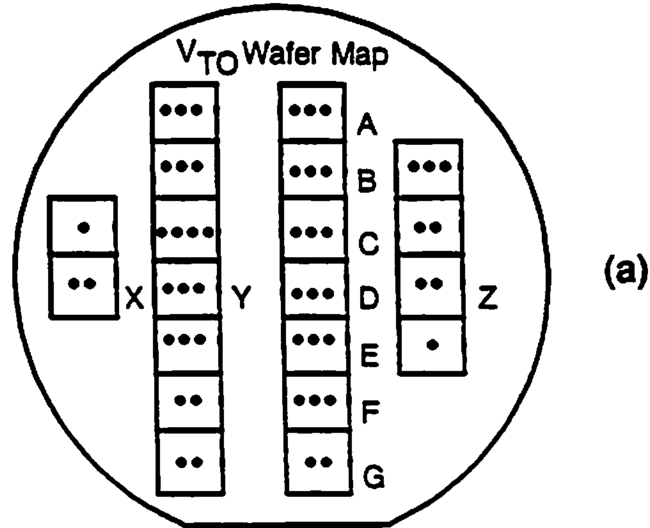
$$\sum_i w_i = 1 \, . \tag{5.2}$$

Here I_{DS}, g_d, g_m, g_{mb}, C_{gs}, and C_{gd} are the calculated drain current, output conductance, transconductance, back-gate transconductance, gate-to-source capacitance, and gate-to-drain capacitance, respectively; I_{DS}^*, g_d^*, g_m^*, g_{mb}^*, C_{gs}^*, and C_{gd}^* are the corresponding measured results. Coefficient w_i is the relative weighting factor and m and n are the numbers of data points in the summations. The summation spaces A and B contain the bias ranges of interest. The user inputs I_{DS0}, g_{d0}, g_{m0}, g_{mb0}, C_{gs0}, and C_{gd0} determine whether a relative or absolute error is used. By specifying the user input values, percentage errors of the low-level terms will not be over-emphasized.

Various terms in (5.1) can be emphasized or de-emphasized to meet the specific design requirements by the use of different w_i weightings. In digital IC design, the current-driving capability is of the primary interest. The weighting factor a is typically chosen to be 1. In analog IC design, the bias current, output conductance, and transconductance are all important. An equal weight can be assigned to the various terms in (5.1) with $w_1=w_2=w_3=w_4=w_5=w_6=1/6$.

The solution obtained by a pure global optimization method is merely a combination of parameter values that minimize the norm of the error vector, with very little regard to the physical meaning. A better approach is to combine local extraction with global optimization. Parameters with related physical meanings are extracted together when the transistor is biased in each operation region with the global optimization techniques being employed to improve the overall fit. This hybrid approach relieves the designer from supplying initial guesses to the parameter optimizer. A good example of the

• 0.74 V to 0.76 V ••• 0.78 V to 0.80 V
•• 0.76 V to 0.78 V •••• 0.80 V to 0.82 V



• 0.35 $V^{1/2}$ to 0.37 $V^{1/2}$ ••• 0.39 $V^{1/2}$ to 0.41 $V^{1/2}$
•• 0.37 $V^{1/2}$ to 0.39 $V^{1/2}$

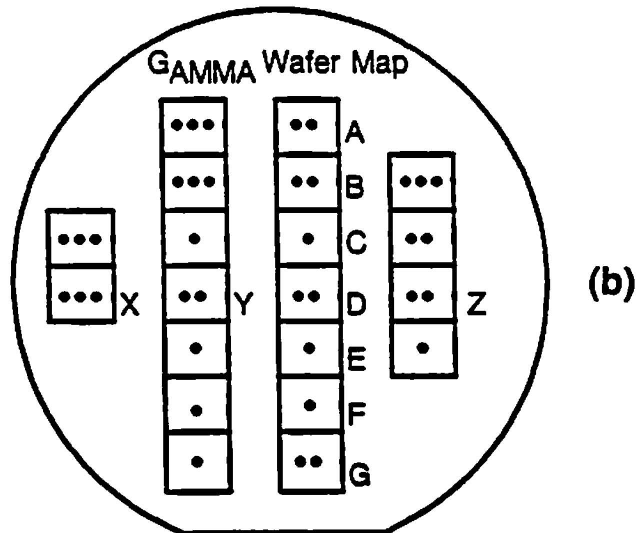
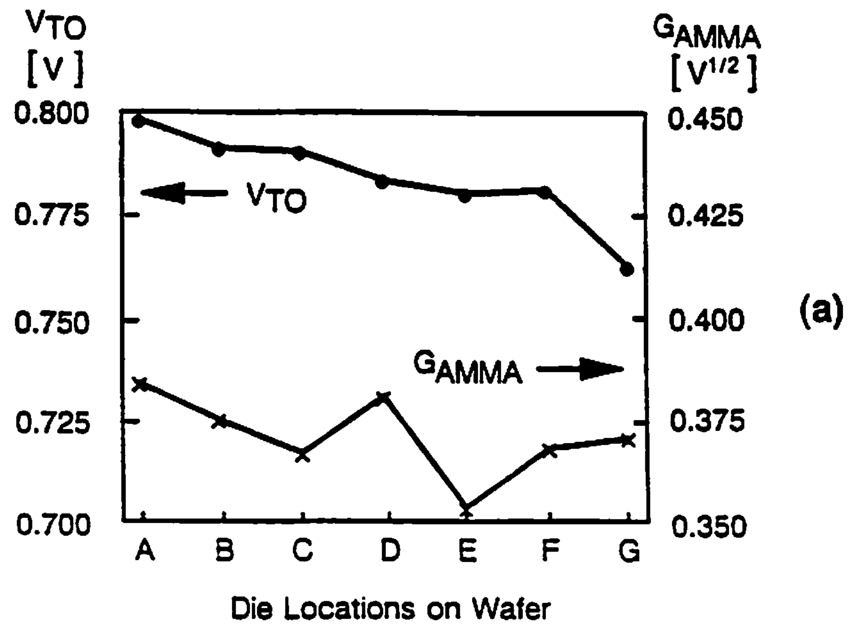


Figure 5-2 Two-dimensional wafer mapping information. The test wafer was fabricated by a 1.2-um technology. (a) Threshold voltage. (b) Body-effect coefficient.



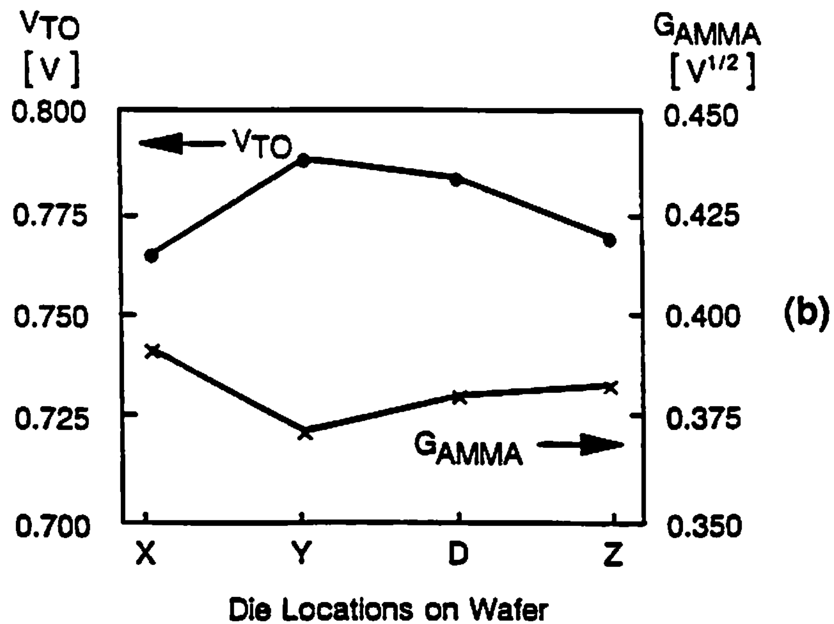


Figure 5-3 **Across-wafer variations of the threshold voltage and body-effect coefficient for (a) die locations A to G, and (b) die locations X, Y, D, and Z.**

hybrid approach is the dedicated extraction program for BSIM.

Test wafers used in the experiments were fabricated by various MOSIS technologies. Measurements were also conducted on test wafers from Hewlett-Packard Laboratories with submicron transistors. Figure 5-2 shows the plots of two-dimensional wafer mapping information for the threshold voltage and body-effect coefficient. The corresponding plots of one-dimensional across-wafer variations are shown in Figure 5-3. Test devices fabricated by the 1.2-μm technology were used. Very mild variations in the device parameters have been found. Similar plots for gate-oxide thickness, and channel-length reduction are shown in Figures 5-4 and 5-5, respectively.

Complete characterization of the test dies were conducted by using the TECAP and BSIM_Extract programs. A comparison of the measured data with simulated results using the BSIM for a W/L=1.4 μm/1.2 μm transistor from the MOSIS Service and a W/L=4.5 μm/0.7 μm transistor from Hewlett-Packward Laboratories is shown in Figure 5-6(a) and (b). The BSIM needs to be enhanced to more accurately determine the drain current saturation point for submicron devices.

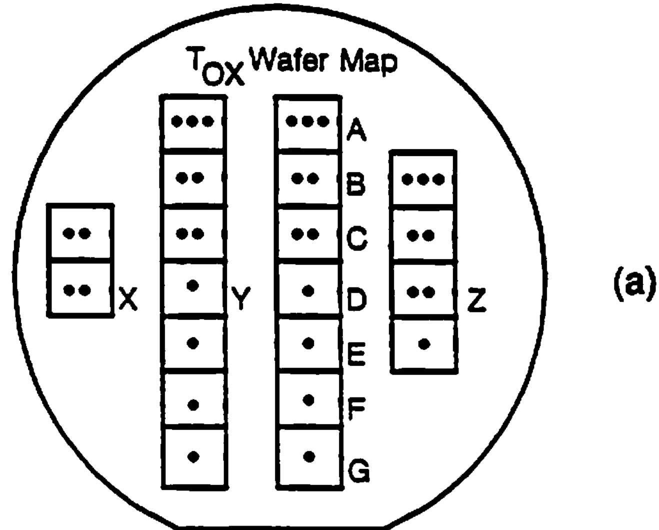
5.3. Sensitive SPICE Parameter Subset

An MOS transistor shows nonlinear output characteristics. Therefore, model parameters do not have a uniform influence on the simulated output characteristics of a transistor. The sensitivity parameters are those parameters which have large effects on the terminal characteristics of MOS transistors. A sensitivity analysis is performed to identify the sensitive parameters.

5.3.1. Sensitivity Analysis

A basic sensitivity function of a transistor output characteristic variable Q with respect to a model parameter P_i can be determined from [5.9]

- • 27.0 nm to 27.2 nm
- •• 27.2 nm to 27.4 nm
- ••• 27.4 nm to 27.6 nm



- • 0.15 um to 0.20 um
- •• 0.20 um to 0.25 um
- ••• 0.25 um to 0.30 um
- •••• 0.30 um to 0.35 um

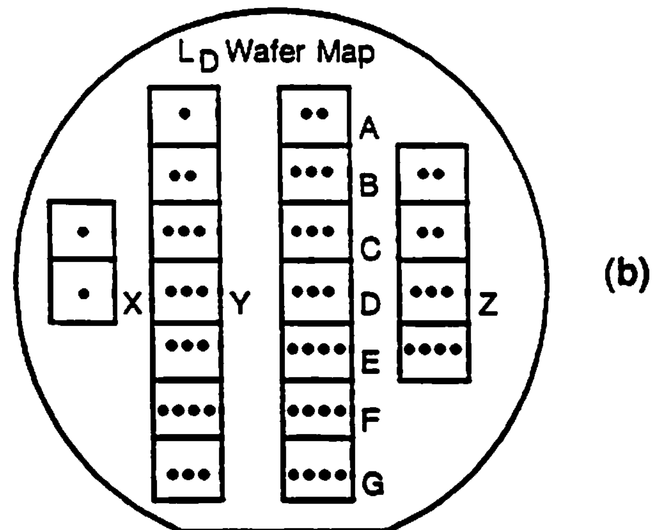
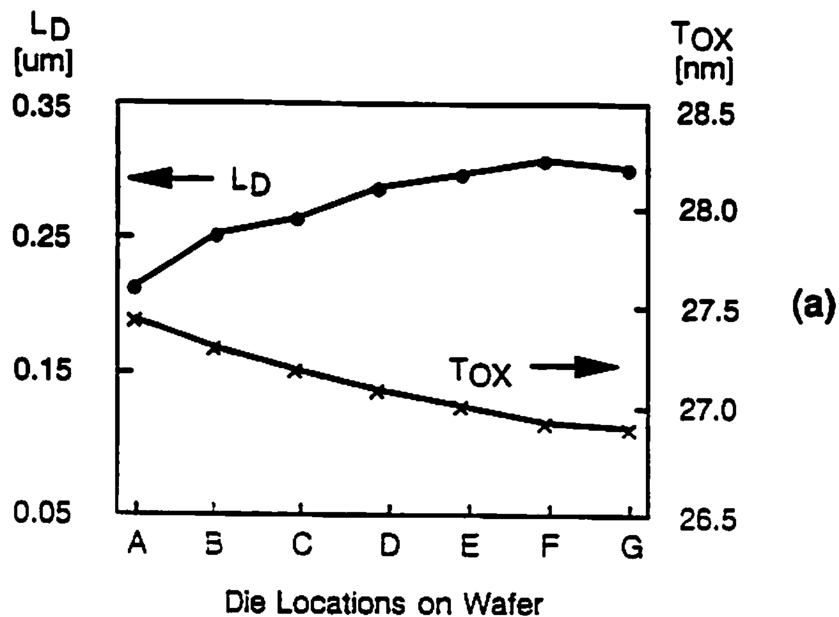


Figure 5-4 Two-dimensional wafer mapping information. The test wafer was fabricated by a 1.2-um technology. (a) Gate-oxide thickness. (b) Channel-length reduction.



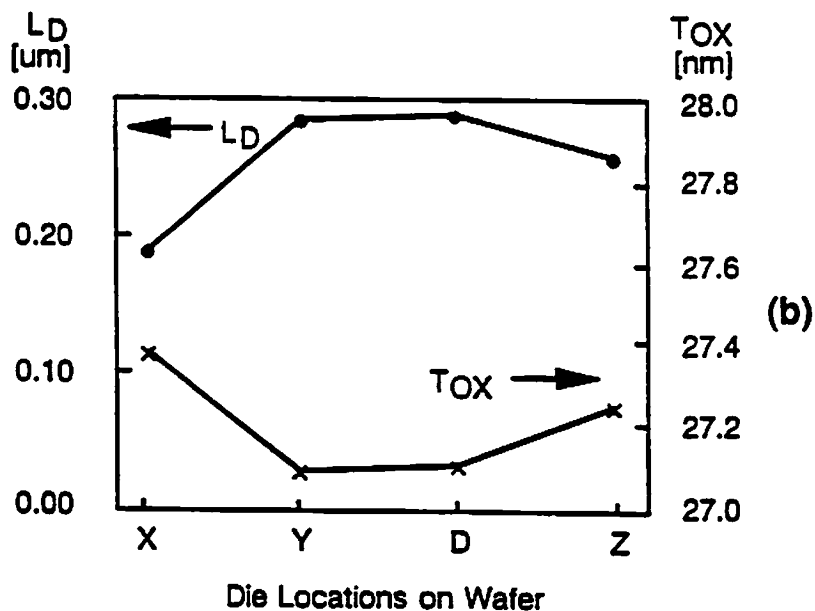
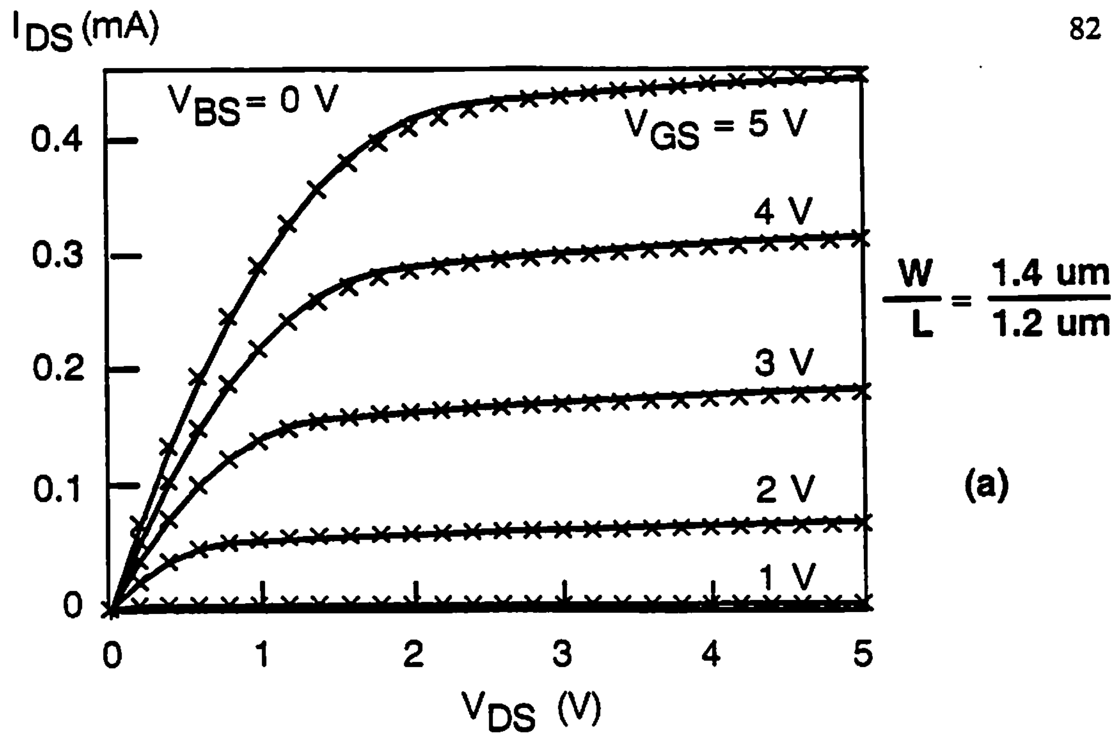


Figure 5-5 Across-wafer variations of the gate-oxide thickness and channel-length reduction for (a) die locations A to G, and (b) die locations X, Y, D, and Z.



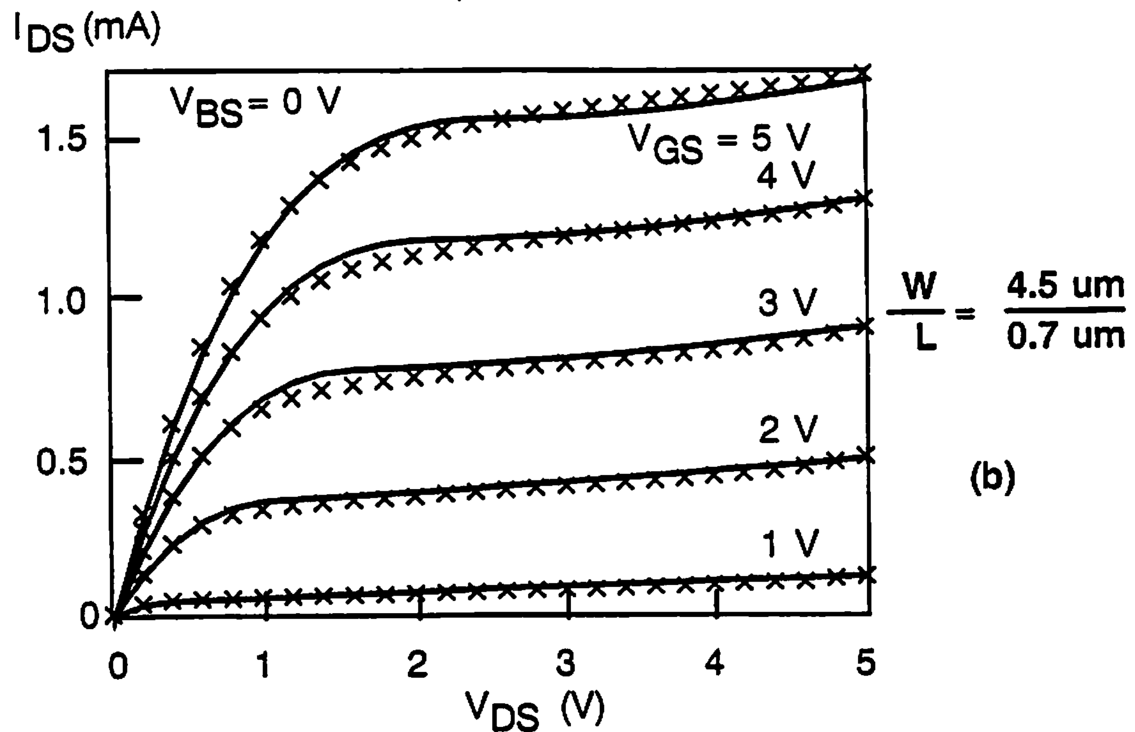


Figure 5-6 Comparison of measured data and the simulated results using the Level-4 model. (a) A W/L = 1.4um/1.2um transistor. (b) A W/L = 4.5um/0.7um transistor.

$$S_{Q|Pi} = \left(\frac{\partial Q}{\partial P_i}\right) / \left(\frac{Q}{P_i}\right). \tag{5.3}$$

For digital IC design, the key output characteristic variable is the drain current; while for analog IC design, it includes the drain current, transconductance, output conductance, back-gate transconductance, gate-to-source capacitance, and gate-to-drain capacitance. The modified sensitivity function for the drain current over a biasing space A can be expressed as

$$\hat{S}_{I_{DS}|P_i} = \frac{1}{(\partial P_i / P_i)} \sqrt{\frac{1}{m} \sum_{A} \left[\frac{I_{DS} - I_{DS,Pi}}{\max(I_{DS}, I_{DS0})}\right]^2} \tag{5.4}$$

where $I_{DS,Pi}$ is the simulated drain current with parameter P_i being perturbed. User input I_{DS0} determines whether a relative or absolute error is used. Both the linear region and saturation region are included in the biasing space A with m being the total number of data points. The modified sensitivity function for the output conductance over a biasing space B is

$$\hat{S}_{g_d|P_i} = \frac{1}{(\partial P_i / P_i)} \sqrt{\frac{1}{n} \sum_{B} \left[\frac{g_d - g_{d,Pi}}{\max(g_d, g_{d0})}\right]^2} \tag{5.5}$$

where $g_{d,Pi}$ is the simulated output conductance with parameter P_i being perturbed. Only the saturation region is included in the biasing space B because the transistors are typically biased in this region to achieve large output resistance. Here, n is the total number of data points. Similar sensitivity function expressions can be constructed for the transconductance, back-gate transconductance, and gate capacitances.

5.3.2. Sensitivity Analysis Results

The sensitivity analysis results are of fundamental importance to the VLSI

design because it provides the information to identify a set of sensitive parameters for each fabrication technology. The worst/best-case parameter files can then be established with special emphasis on these sensitive parameters to conduct statistical design analysis. Expressions for the temperature dependences of these parameters carry the necessary information for predicting circuit performance at various operating temperatures.

Tables 5-2 and 5-3 list the drain-current and output-conductance sensitivity results for the Level-2 model with 3-μm and 1.2-μm technologies. In regard to the drain current, the most sensitive parameters for the 3-μm technology are TOX, UO, GAMMA, and VTO. Parameter LD is an additional sensitive parameter for the 1.2-μm technology. In regard to the output conductance, the most sensitive parameters for the 3-μm technology are TOX, LAMBDA, UO, VTO, and GAMMA, and those for the 1.2-μm technology are LD, LAMBDA, TOX, VMAX, VTO, and UO.

Tables 5-4 and 5-5 list the drain-current and output-conductance sensitivity results for the Level-4 model with 2-μm and 1.2-μm technologies. In regard to the drain current, the most sensitive parameters are K_1, μ_S, TOX, ϕ_S, and V_{FB}. In regard to the output conductance, the most sensitive parameters for the 2-μm technology are K_1, μ_S, μ_Z, ϕ_S, μ_{sd}, U_{1d}, and TOX, and those for the 1.2-μm technology are μ_S, μ_Z, U_{1d} and μ_{sd}.

Table 5-2 Sensitivity analysis results for the Level-2 MOSFET model parameters in a 3-um technology.

Model Parameter	Drain Current Sensitivity $S_{I_{DS},P}$	Model Parameter	Output Conduc. Sensitivity $S_{g_d,P}$
TOX	0.744 (-)	TOX	0.873 (-)
UO	0.680	LAMBDA	0.770
GAMMA	0.665 (-)	UO	0.753
VTO	0.621 (-)	VTO	0.747 (-)
PHI	0.193	GAMMA	0.630 (-)
LD	0.189	LD	0.280
DELTA	0.088 (-)	PHI	0.248
NSUB	0.084 (-)	NSUB	0.182 (-)
VMAX	0.076	XJ	0.166
XJ	0.056	VMAX	0.120
LAMBDA	0.052	DELTA	0.111 (-)
NFS	< 0.001	NFS	0.004
NEFF	< 0.001	NEFF	< 0.001
UEXP	< 0.001	UEXP	< 0.001
UCRIT	< 0.001	UCRIT	< 0.001

Note: (-) signifies that positive perturbation of the parameter would have a negative effect on the output characteristics

Table 5-3 Sensitivity analysis results for the Level-2 MOSFET model parameters in a 1.2-um technology.

Model Parameter	Drain Current Sensitivity $S_{I_{DS},P}$	Model Parameter	Output Conduc. Sensitivity $S_{g_d,P}$
TOX	0.717 (-)	LD	0.999
VTO	0.644 (-)	LAMBDA	0.973
UO	0.605	TOX	0.877 (-)
LD	0.527	VMAX	0.613
VMAX	0.272	VTO	0.464 (-)
UEXP	0.172 (-)	UO	0.362
PHI	0.083	GAMMA	0.268
GAMMA	0.078 (-)	XJ	0.182
LAMBDA	0.068	NSUB	0.150 (-)
NSUB	0.056 (-)	UEXP	0.113 (-)
UCRIT	0.052	PHI	0.088
XJ	0.049	UCRIT	0.025
NFS	0.001	DELTA	0.001 (-)
DELTA	0.001 (-)	NFS	0.001
NEFF	< 0.001	NEFF	< 0.001

Note: (-) signifies that positive perturbation of the parameter would have a negative effect on the output characteristics

Table 5-4 Sensitivity analysis results for the Level-4 MOSFET model parameters in a 2-um technology.

Model Parameters	Drain Current Sensitivity $S_{I_{DS},P}$	Model Parameters	Output Conduc. Sensitivity $S_{g_d,P}$
k1	1.307 (-)	μ_s	2.182
TOX	0.753 (-)	μ_z	1.808 (-)
μ_s	0.752	U_{1d}	0.927 (-)
ϕ_s	0.600 (-)	μ_{sd}	0.623
VFB	0.502	TOX	0.502 (-)
k2	0.459	k1	0.458 (-)
μ_z	0.327	U_{1z}	0.289
U_{1z}	0.312 (-)	μ_{sb}	0.218 (-)
U_{oz}	0.143 (-)	η_b	0.191
U_{1d}	0.082	ϕ_s	0.185 (-)
μ_{sb}	0.079 (-)	VFB	0.146
μ_{sd}	0.054 (-)	k2	0.143
η_b	0.053	U_{oz}	0.117 (-)
U_{1b}	0.029	μ_{zb}	0.093
η_o	0.023	η_o	0.085
μ_{zb}	0.018 (-)	η_d	0.033 (-)
U_{ob}	0.008	U_{1b}	0.026 (-)
η_d	0.005	U_{ob}	0.007

Table 5–5 Sensitivity analysis results for the Level–4 MOSFET model parameters in a 1.2–um technology.

Model Parameters	Drain Current Sensitivity $S_{I_{DS},P}$	Model Parameters	Output Conduc. Sensitivity $S_{g_d,P}$
k1	1.307 (–)	μ_s	2.182
TOX	0.753 (–)	μ_z	1.808 (–)
μ_s	0.752	U_{1d}	0.927 (–)
ϕ_s	0.600 (–)	μ_{sd}	0.623
VFB	0.502	TOX	0.502 (–)
k2	0.459	k1	0.458 (–)
μ_z	0.327	U_{1z}	0.289
U_{1z}	0.312 (–)	μ_{sb}	0.218 (–)
U_{oz}	0.143 (–)	η_b	0.191
U_{1d}	0.082	ϕ_s	0.185 (–)
μ_{sb}	0.079 (–)	VFB	0.146
μ_{sd}	0.054 (–)	k2	0.143
η_b	0.053	U_{oz}	0.117 (–)
U_{1b}	0.029	μ_{zb}	0.093
η_o	0.023	η_o	0.085
μ_{zb}	0.018 (–)	η_d	0.033 (–)
U_{ob}	0.008	U_{1b}	0.026 (–)
η_d	0.005	U_{ob}	0.007

Chapter 6

Efficient SPICE Temperature Dependence Modeling

Computer-aided design tools have become indispensable in design automation for digital and analog VLSI circuits. Circuit simulation plays an important role during the initial design and final verification phases of VLSI realization. Quick and accurate SPICE simulation results can not only assist in achieving high circuit performance, but also reduce the design time. Since the accuracy of circuit simulation results depends on the transistor models implemented in a circuit simulator, efficient yet accurate transistor modeling is essential to VLSI circuit analysis. Temperature dependence, noise behavior, and process-induced transistor characteristic variations must all be included in the transistor models for complete circuit analysis [6.1].

Performance of VLSI circuits has to be verified over a wide temperature range of 0 to 70 °C for commercial applications and of -55 to 125 °C for military applications. With the complexity of hundreds of thousands of active devices in a chip, proper circuit function at various operating temperatures heavily relies on computer simulation. In order to simulate circuit performance at different temperatures, the temperature dependences of model parameters must be included in the circuit simulator. The temperature dependence was incorporated in the SPICE Level-2 and -3 models. So far, temperature effects have not yet been included in the Level-4 model. Since a large number of mod-

el parameters are used in the Level-4 model, the incorporation of temperature dependences of model parameters needs to be carefully addressed.

In this chapter, an accurate and efficient semi-empirical temperature dependence modeling method for BSIM using sensitive SPICE parameters is described. A sensitive model parameter subset which has large effects on the transistor output characteristics is first determined from the sensitivity analysis. Instead of tracking temperature dependences of all the model parameters, only temperature dependences of the sensitive parameters are sufficient to predict the circuit performance at various operating temperatures.

6.1. Temperature Dependence Modeling

In general, fully physics-based models derived from detailed device physics are mathematically complicated. When all the governing physical effects are incorporated, expensive computational time is required to obtain device I-V characteristics from device simulators, such as PISCES, MINIMOS, and BAMBI [6.2]. An MOS transistor model has to be evaluated thousands of times during each circuit simulation. This renders direct applications of fully physics-based models computationally inefficient for the circuit analysis purpose.

To achieve good simulation accuracy and computational efficiency, MOS transistor models widely used in circuit simulators [6.3-6.6] are essentially semi-empirical in nature. Terms with strong physical meaning are employed to model the fundamental physical effects while model parameters are judiciously introduced to embrace subtle device characteristics. This approach serves best for the circuit-analysis purpose especially as two- and three-dimensional small-geometry effects become more prominent.

6.1.1. Sensitive BSIM Parameter Subset

The Level-4 model (BSIM) marks a significant progress in the semi-empirical approach. It uses 67 model parameters because the following formula is

used to describe the geometric dependence of each electrical parameter P_i :

$$P_i = P_{0i} + \frac{P_{Li}}{L} + \frac{P_{Wi}}{W} . \tag{6.1}$$

Here, P_i is an electrical parameter and P_{0i}, P_{Li}, and P_{Wi} are the corresponding offset, channel-length sensitivity, and channel-width sensitivity values. The effective channel length L and channel width W are used in the calculation. The sensitivity analysis results for an L=1.2 μm transistor using the BSIM are listed in Table 5-5. The sensitive parameter subset is determined to be $\{K_1, \mu_S, \phi_S, V_{FB}, K_2, \mu_Z, U_{1Z}, U_{0Z}\}$.

6.1.2. The New Approach

In order to precisely model the temperature dependences of VLSI circuits, a completely updated model parameter set $\{P_1^{(T)}, P_2^{(T)}, \ldots, P_T^{(T)}\}$ is required when there is a perturbation to circuit performance due to temperature. Here, $P_i^{(T)}$ is the updated value for the i-th parameter. However, as a large number of semi-empirical parameters are used in modeling small-geometry devices, it is very difficult to include the temperature dependence for every model parameter. An efficient modeling approach for temperature dependence is to make use of the partially updated parameter set $\{P_1^{(T)}, P_2^{(T)}, \ldots, P_S^{(T)}, P_{S+1}^{(0)}, \ldots, P_T^{(0)}\}$ instead of the completely updated parameter set. Here, $\{P_1, P_2, \ldots, P_S\}$ is the sensitive parameter subset.

The circuit verification procedure using the sensitive SPICE parameter subset approach is shown in Figure 6-1. For a given CMOS fabrication process, transistor output characteristics of the test wafers are measured and model parameter values are extracted using TECAP or SUXES general-purpose parameter extraction programs, or the BSIM_Extract dedicated software. The

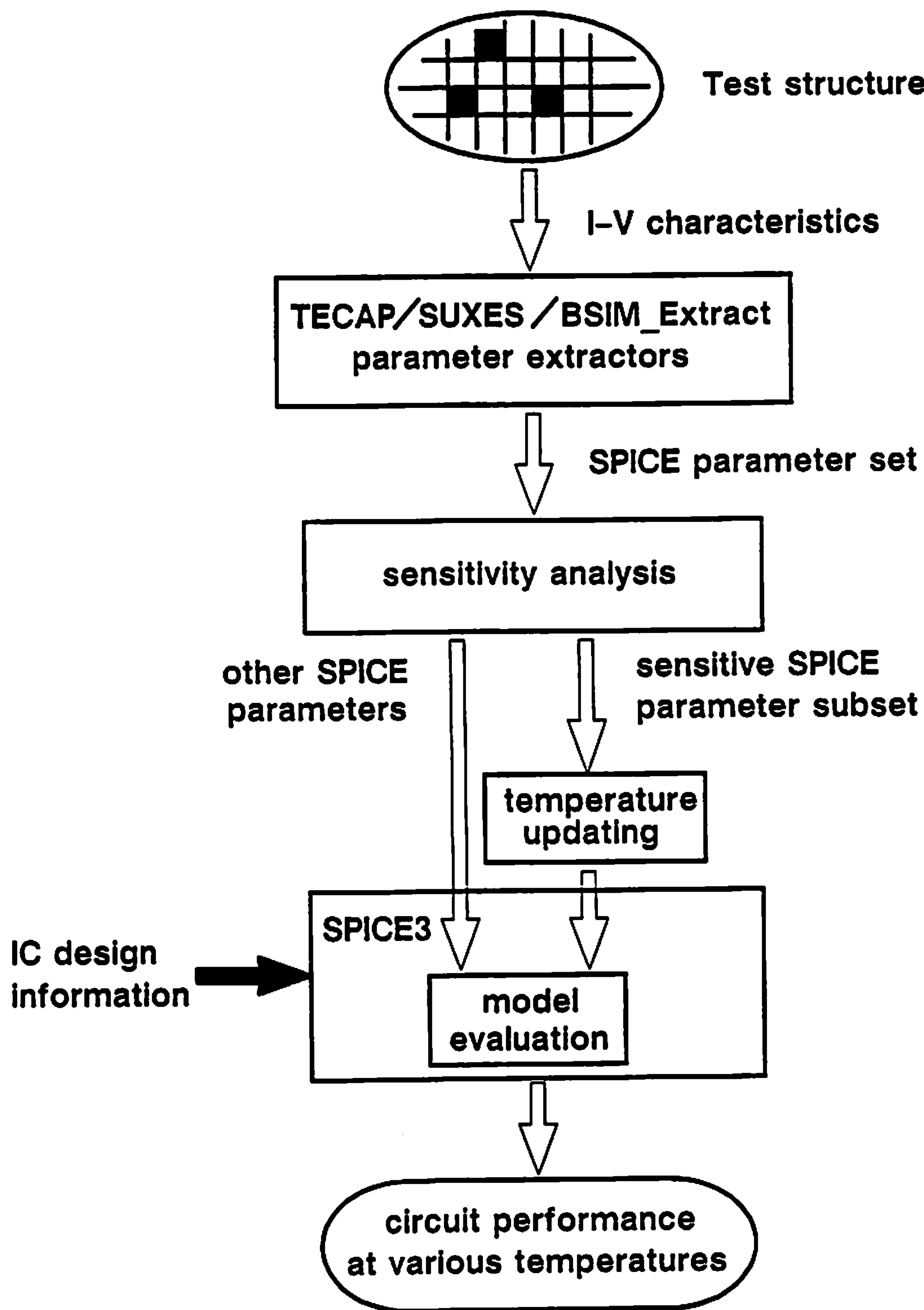


Figure 6-1 Circuit performance verification procedure using the sensitive SPICE parameter subset. approach.

sensitive SPICE parameter subset is identified from the complete SPICE parameter set through the sensitivity analysis discussed in Section 5.3. To simulate the temperature dependences of VLSI circuits, the temperature behaviors of the sensitive SPICE parameters are incorporated. Figure 6-2 shows the configuration of a BSIM parameter file. The parameter values shown in shaded regions are updated through a processing module when the circuit performance at a different temperature is simulated. In circuit simulation, the updating of model parameter values is done prior to the analysis for each given temperature. Since the number of parameters in the sensitive subset is small, this semi-empirical temperature dependence modeling approach is highly compatible with the computer-integrated manufacturing systems for VLSI and ULSI circuits.

6.2. Experimental Results and Discussion

The temperature dependences of sensitive BSIM parameters are presented in Figure 6-3. The effective channel widths and lengths of the transistors used in our experiment are W/L = 4.8 μm/1.2 μm and 14.4 μm/3.6 μm. Values of model parameters were extracted automatically from measured I-V data using the BSIM_Extract program. Values of parameters K_1, K_2, U_{0Z}, V_{FB}, and ϕ_S were fitted by a linear function of temperature using the least-square-error method. Values of μ_Z and μ_S were fitted by functions of $T^{-1.5}$ and values of U_{1Z} were fitted by $T^{-2.5}$. The temperature coefficients and correlation coefficients for the curve fitting are listed in Table 6-1. Small temperature coefficients for K_1, K_2, and U_{0Z} indicate that these parameters are not very sensitive to temperature variations. Parameters μ_Z and μ_S can be modeled well by the $T^{-1.5}$ dependence and parameter U_{1Z} varies with $T^{-2.5}$. The temperature coefficients have no significant dependence on transistor geometries.

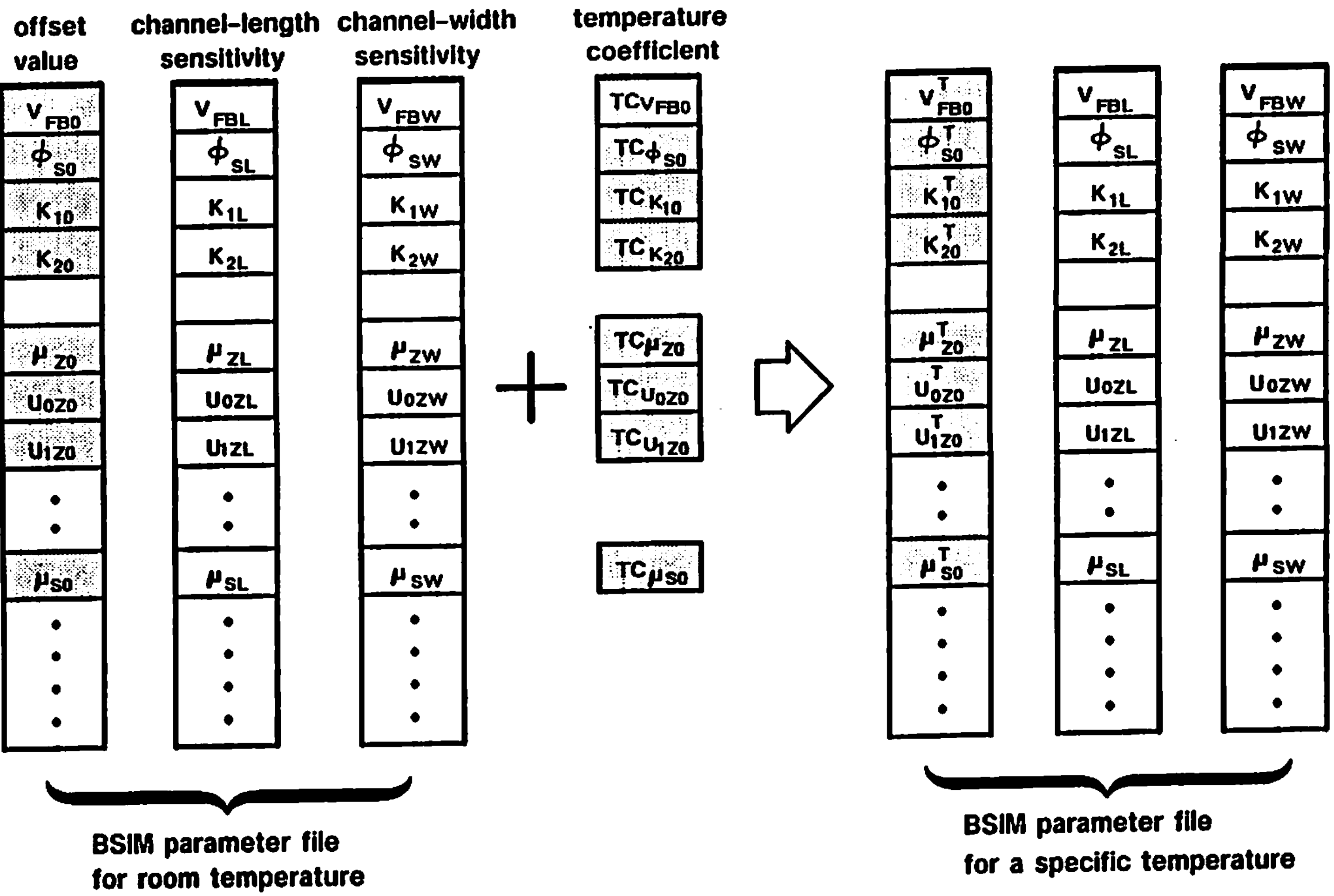


Figure 6-2 Updating of the Level-4 model parameter values is done prior to circuit analysis at each given temperature.

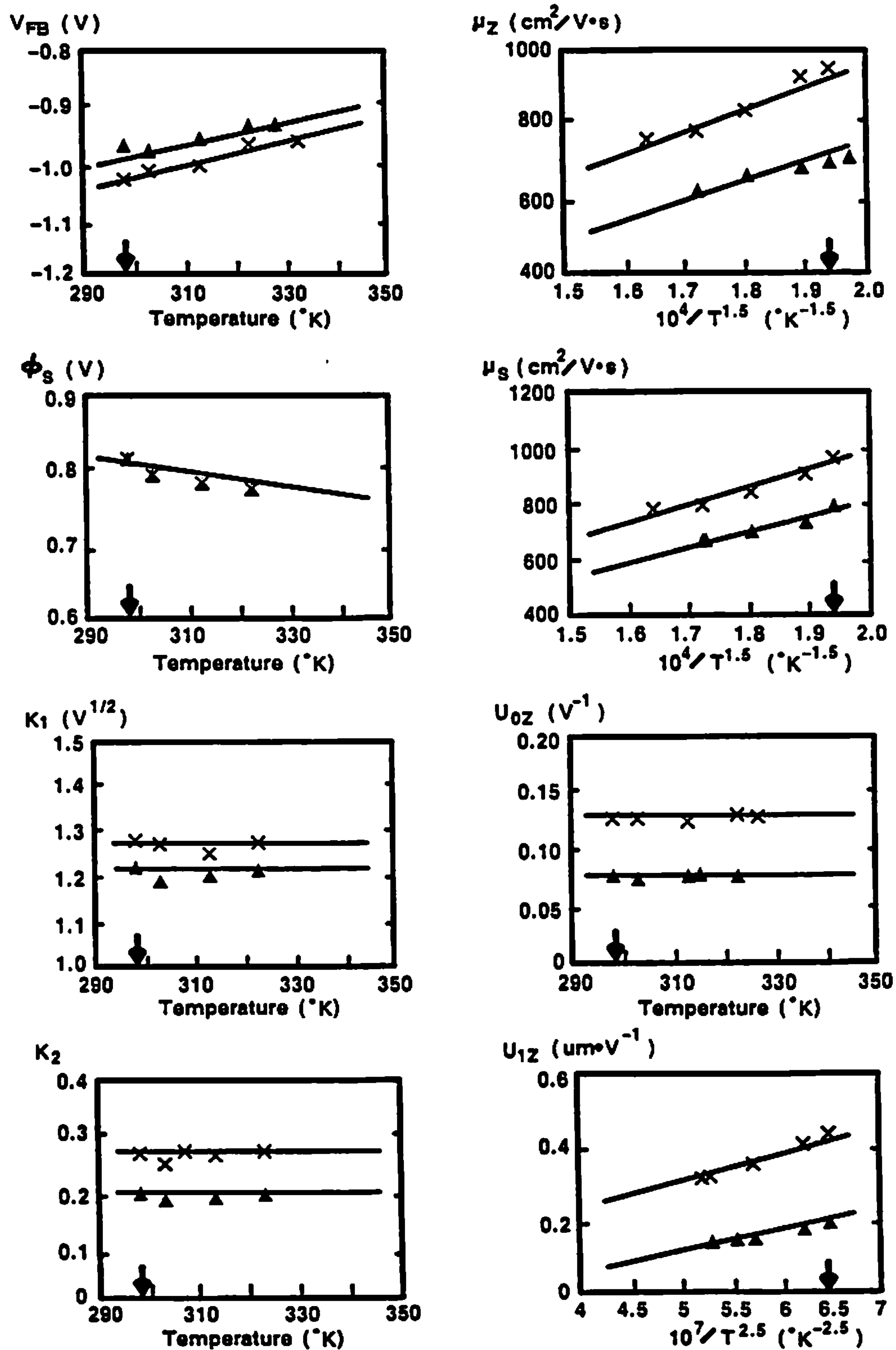


Figure 6-3 Measured temperature dependences of sensitive Level-4 model parameters with W/L = 4.8 um/1.2 um (x x x) and W/L = 14.4 um/3.6 um (filled Δ). Room temperature (298 °K) is indicated by an arrow.

Table 6-1 Temperature dependences of sensitive BSIM parameters.

sensitive BSIM parameter	temperature coefficient	correlation coefficient
K_1	0.00053	0.769
μ_S	1050.4	0.956
ϕ_S	-0.00085	-0.977
V_{FB}	0.00186	-0.930
K_2	0.00041	0.907
μ_Z	989.9	0.985
U_{1Z}	0.4678	0.939
U_{0Z}	0.00004	0.221

When circuit simulation is to be performed at a given temperature, a preprocessor reads in the sensitive parameter values at room temperature, the temperature coefficients, the temperature-dependence exponents for μ_S and μ_Z, and the new temperature value. It then calculates the sensitive parameter values at the new temperature and outputs the updated parameter file.

Figure 6-4 shows the temperature dependence of the zero-bias threshold voltage for an N-channel transistor with W/L = 4.5 μm/2.4 μm. The measured threshold voltage is determined by extrapolating the linear plot of I_{DS} vs. V_{GS} using the least-square-error method. The temperature coefficient of the threshold voltage was found to be -1.9 mV/ °C. The threshold voltage predicted by the Level-2 model is also shown in Figure 6-4. The predicted temperature coefficient is -2.2 mV/ °C. The theoretical temperature coefficient value obtained from (6.4), (6.6) and (6.7) in Section 6.3 is -2.1 mV/ °C over the interested temperature range.

To illustrate the usage of the sensitive SPICE parameter subset approach, experiments were made on several test transistors. Figure 6-5(a) shows a comparison between measured transistor I-V data and SPICE simulated results at 70 °C. An N-channel MOS transistor with W/L = 14.4 μm/1.2 μm was used. The SUXES-extracted Level-2 model parameter values were obtained at the room temperature. SPICE simulation results were obtained by using the temperature control command. The simple SPICE prediction has moderate discrepancy. In Figure 6-5(b), the simulated transistor I-V characteristics were obtained using sensitive parameter values which were extracted at 70 °C while other parameter values are kept the same as those at the room temperature. The simulated results are in better agreement with the measured data. The error between the simulated and measured I-V characteristics in Figure 6-5(a) and (b) are 13.2% and 4.1%, respectively. A comparison of measured I-V data and SPICE simulated results using the BSIM at 77

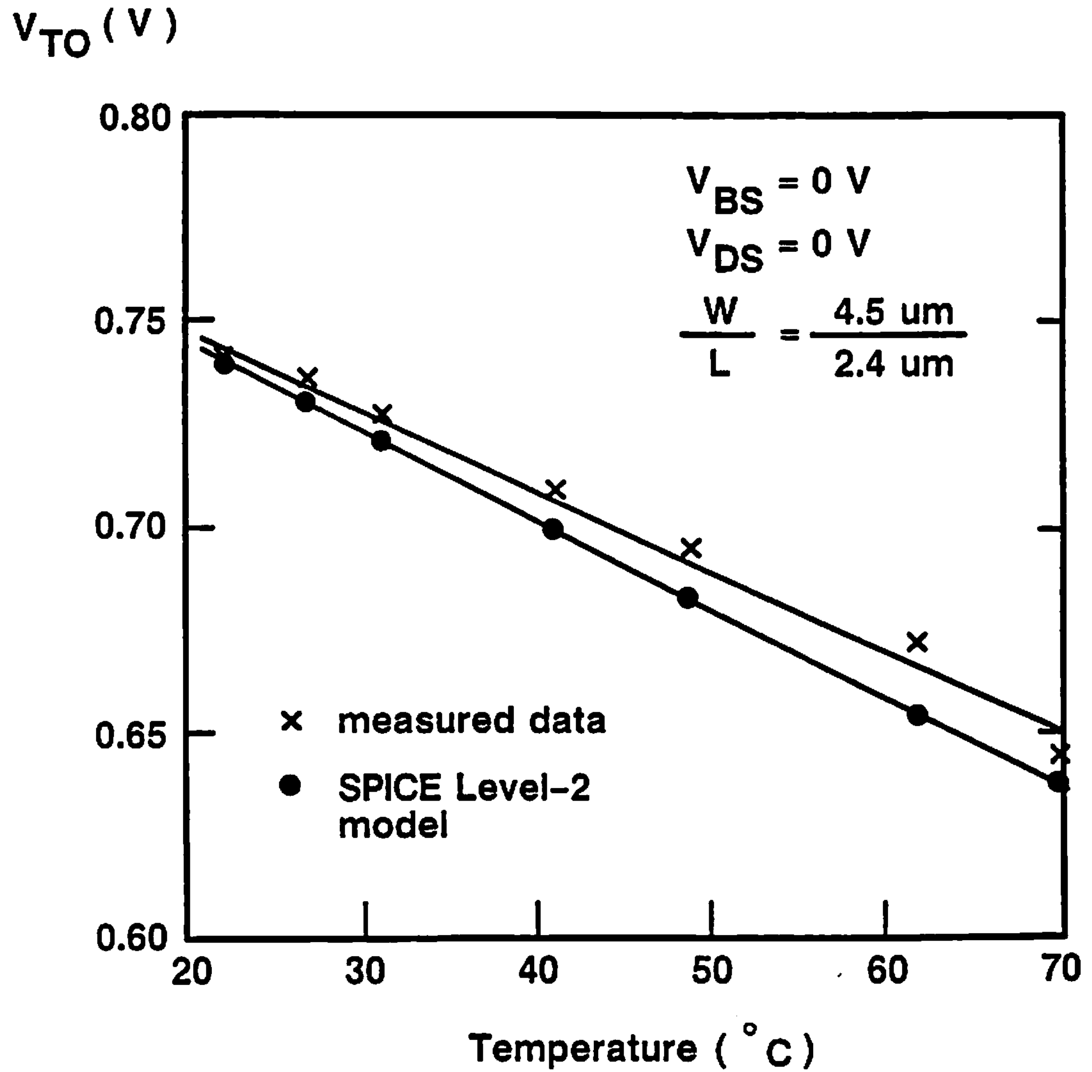


Figure 6-4 A comparison of the measured and simulated results for the temperature dependence of the threshold voltage. The Level-2 model is used in the simulation for an N-channel MOS transistor.

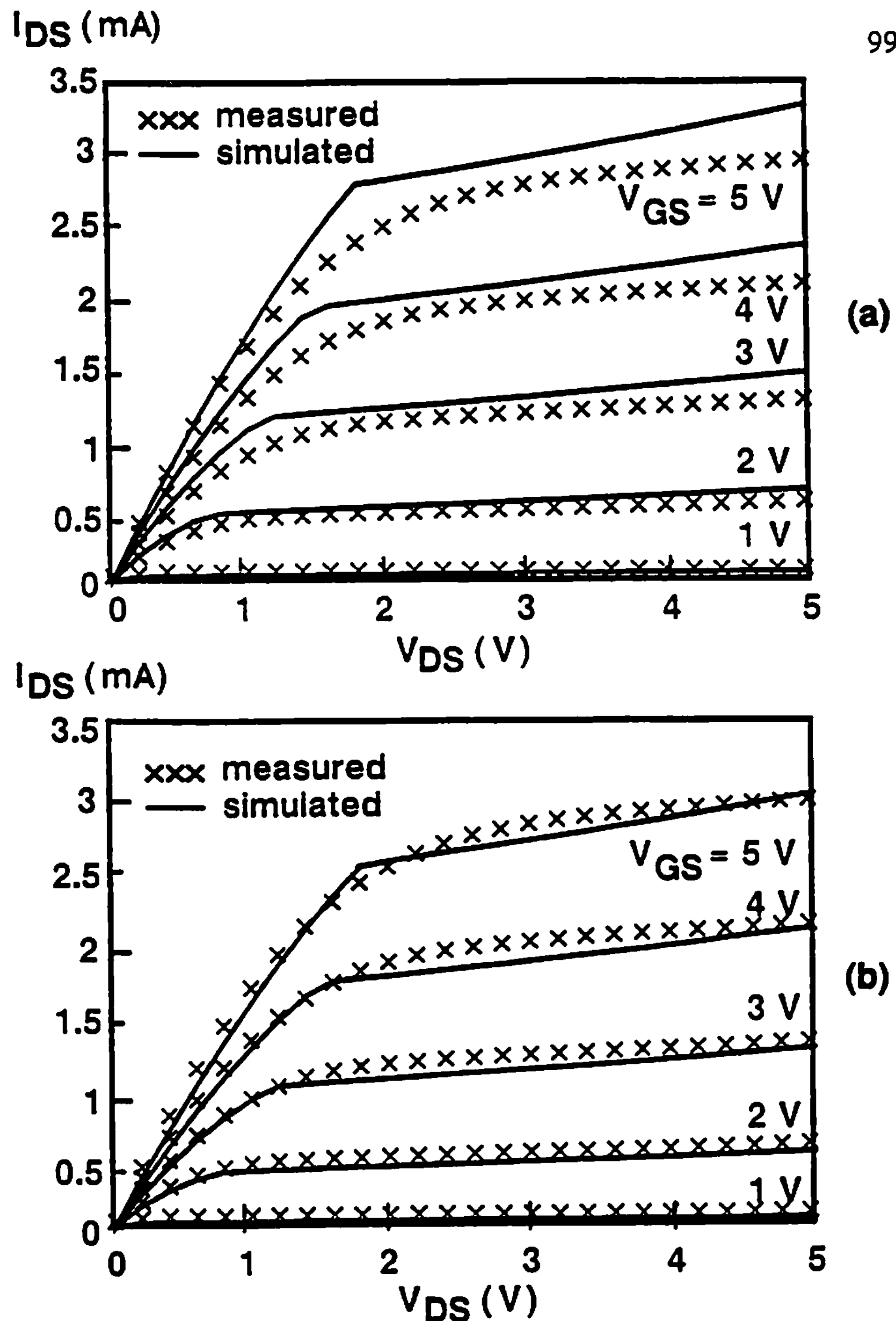


Figure 6–5 Comparison of the measured and simulated I–V characteristics for a W/L=14.4 um/ 1.2 um transistor at 70 °C. (a) In simulation, only the temperature control command is used to update Level-2 model parameter values through SPICE. (b) In simulation, parameter values for the sensitive Level–2 model subset have been updated from new extraction.

°K is shown in Figure 6-6(a). The simple prediction using the temperature control command has big discrepancy. In Figure 6-6(b), the simulated results were obtained using sensitive parameter values at 77 °K while other parameter values were kept the same as those at room temperature. The simulated results in Figure 6-6(b) are in good agreement with the measured data.

To further demonstrate the temperature-effect prediction capability of the sensitive subset approach, a comparison between measured I-V data and simulated results using the BSIM is shown in Figure 6-7. The measured data were obtained at 70 °C. The sensitive BSIM parameter subset was updated by the preprocessor using the temperature coefficients from Figure 6-3. Good agreement has been achieved.

Two circuit examples of using the sensitive parameter subset approach to model the temperature dependence of circuit performance have been studied. Figure 6-8 shows the comparison results of two CMOS inverters with different geometry aspect ratios. The effective channel length of the transistors is 1.2-μm. Voltage transfer characteristics of the inverters were measured at 70 °C. Simulated results were obtained using the sensitive BSIM parameter values updated by the preprocessor. The measured transfer characteristics agree well with the simulated results.

Figure 6-9 shows a comparison of the measured and simulated frequencies of a 31-stage ring oscillator at various operating temperatures. The ring oscillator was fabricated by a 1.2-μm CMOS technology. The measured frequency of the ring oscillator was found to decrease with temperature. This is due to smaller carrier mobility value at a higher temperature which reduces the drain current and hence increases the switching time. Notice that the original SPICE built-in BSIM has not included the temperature prediction capability. The sensitive parameter subset approach provides the adequate BSIM temperature dependence modeling for VLSI circuits [6.7].

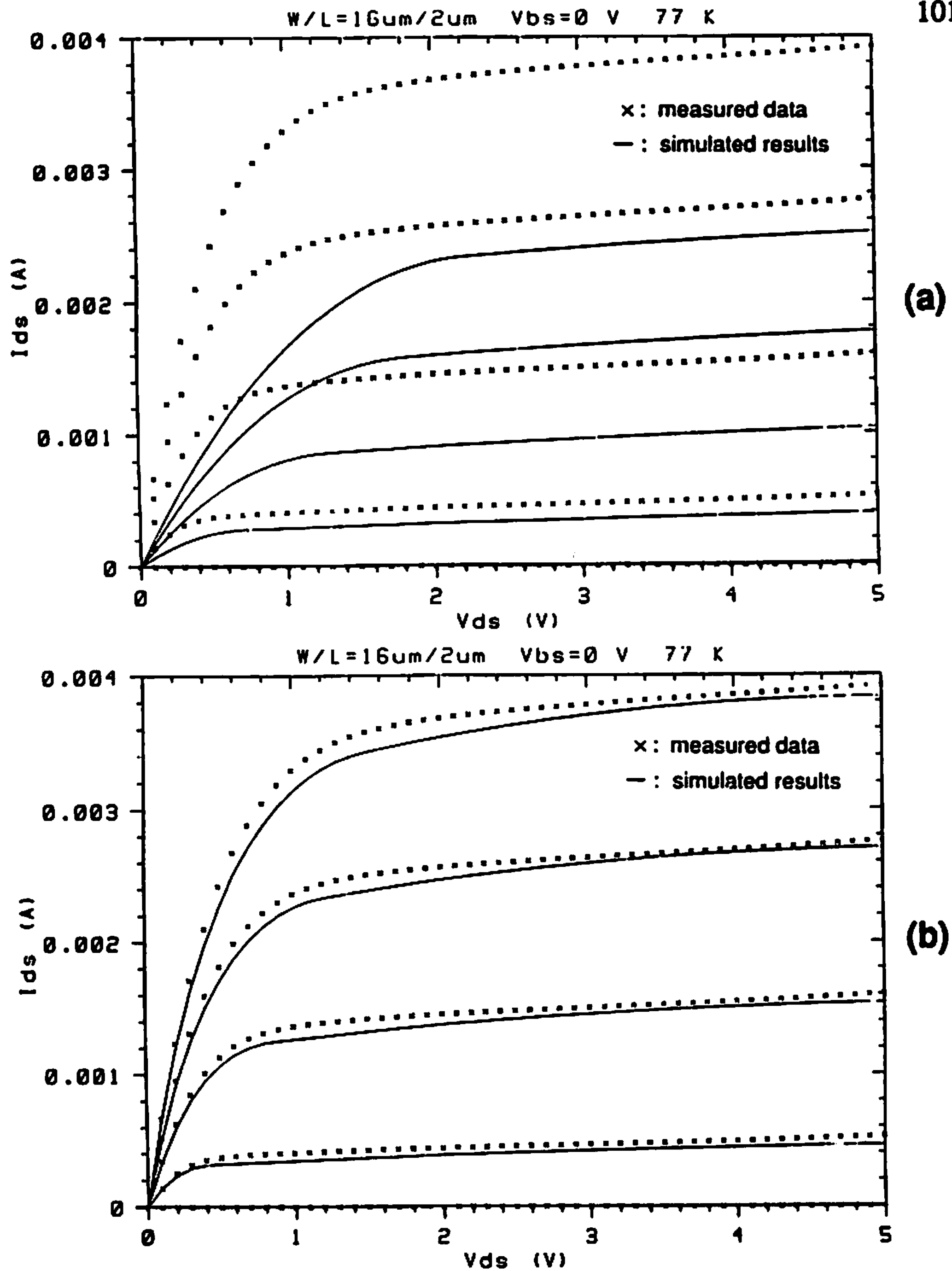


Figure 6-6 Comparisons of the measured and simulated I-V characteristics for a W/L = 16 um/2 um transistor at 77 °K. (a) In simulation, only the temperature control command is used to update Level-4 model parameter values through SPICE. (b) In simulation, parameter values for the sensitive Level-4 model subset have been updated from new extraction.

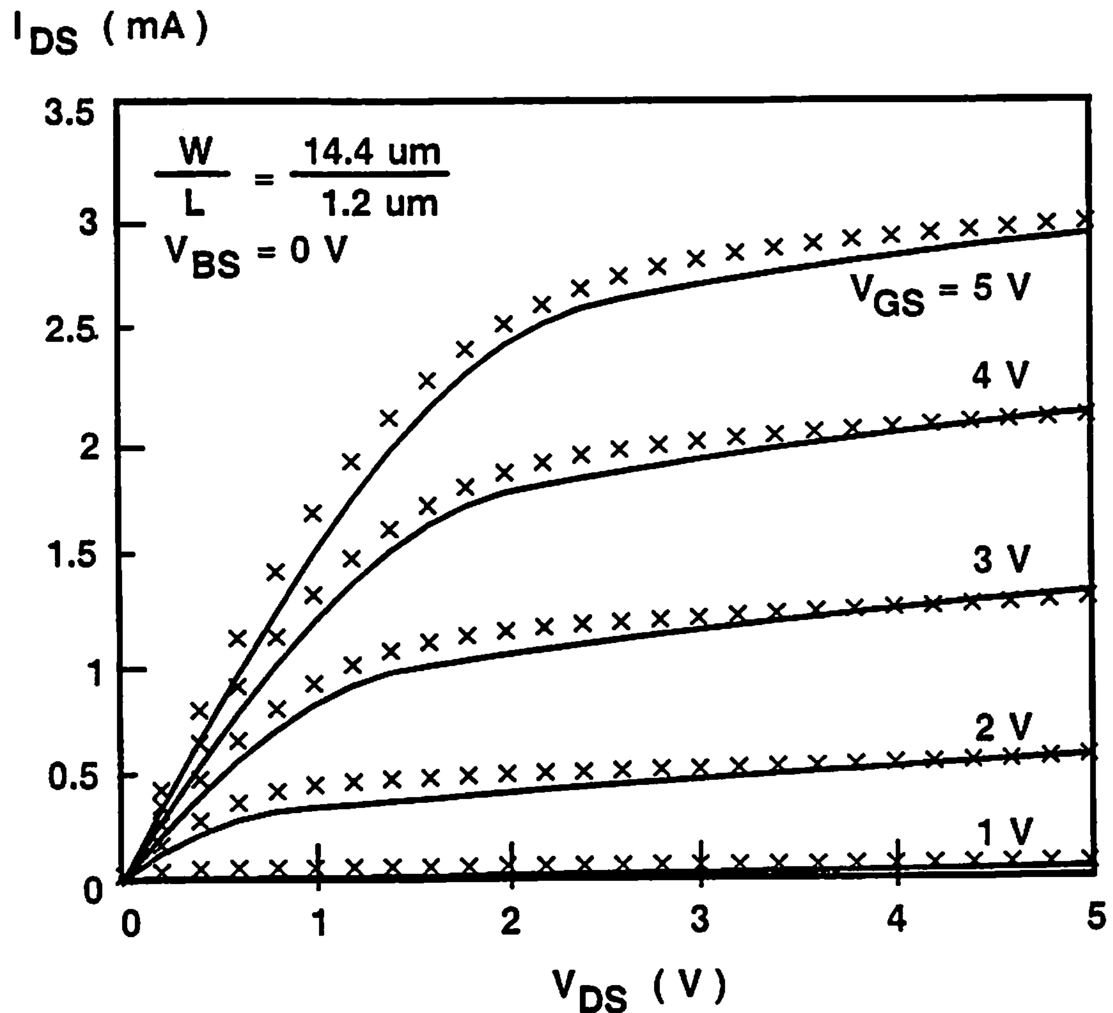


Figure 6-7 A comparison of the measured and simulated I-V characteristics at 70 °C. In simulation, parameter values for the sensitive Level-4 model subset have been updated through the preprocessor.

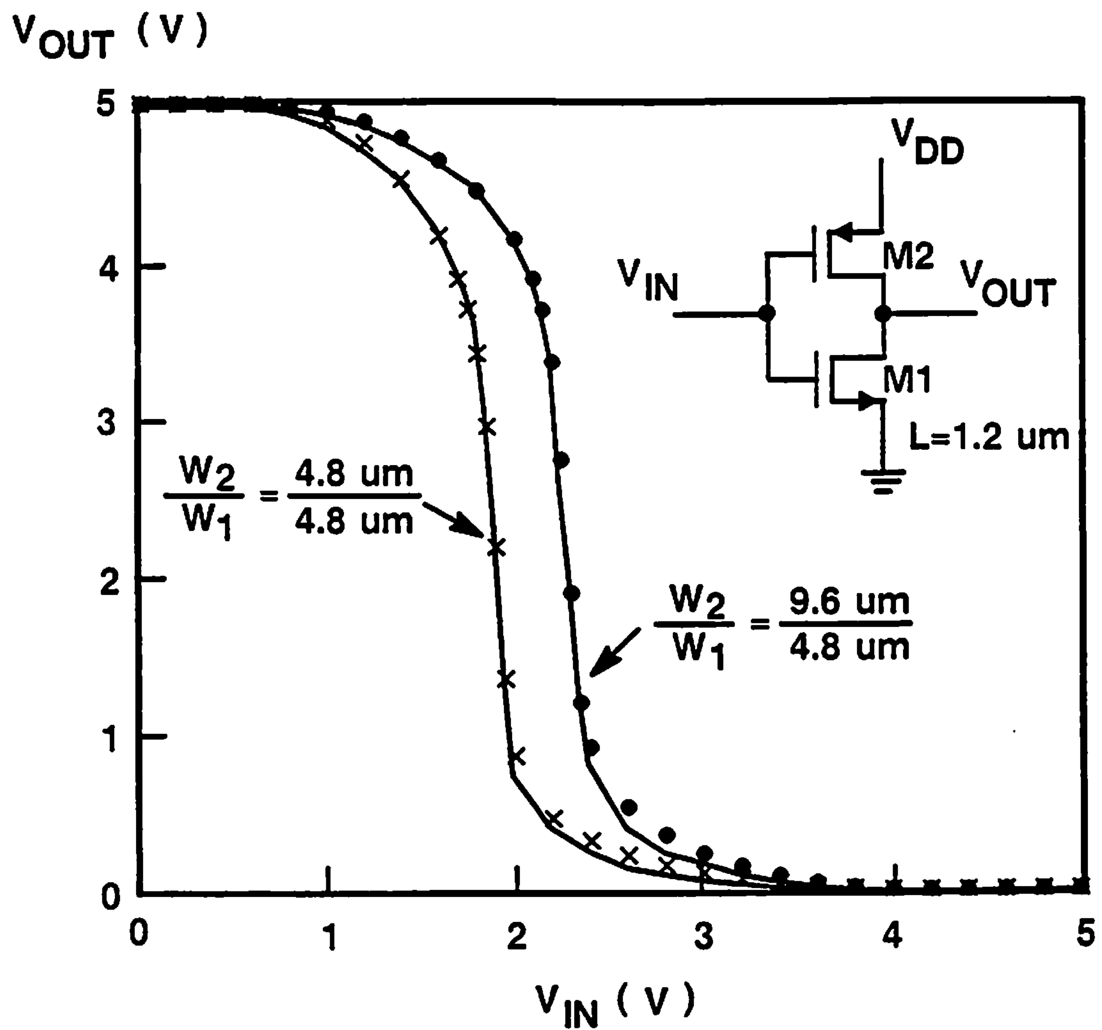


Figure 6-8 Measured and simulated voltage transfer characteristics of two CMOS inverters at 70 °C.

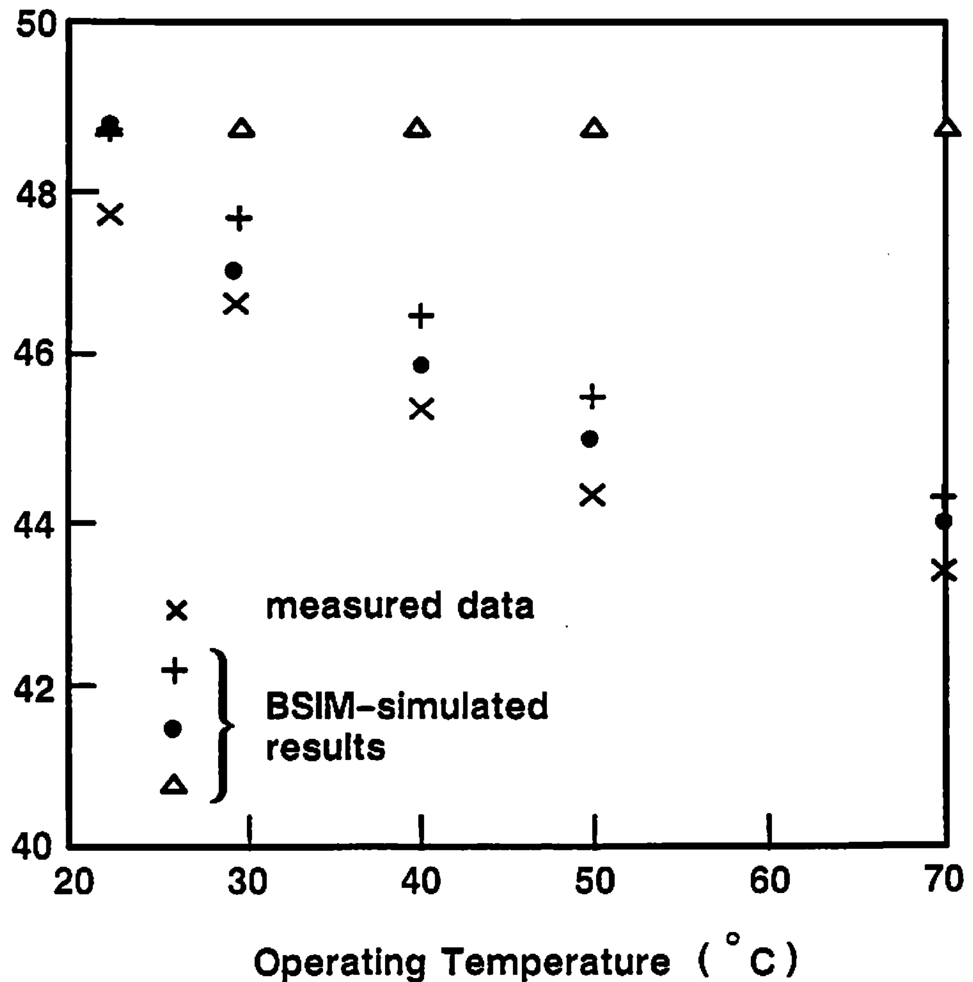


Figure 6-9 Measured and simulated frequencies of a 31-stage ring oscillator at different operating temperatures. "△△△": Using temperature control command. "+++": Using the sensitive Level-4 model parameter subset approach. "●●●": Using all updated parameter values at 70 °C.

6.3. Theoretical Basis for BSIM Temperature Dependence

Theoretical basis for the temperature dependences of the sensitive BSIM parameters is described here. Parameters V_{FB}, ϕ_S, K_1, and K_2, in the sensitive BSIM parameter subset are related to the transistor threshold voltage. The threshold voltage in the BSIM is expressed as [5.7]

$$V_{th} = V_{FB} + \phi_S + K_1\sqrt{\phi_S - V_{BS}} - K_2 (\phi_S - V_{BS}) - \eta V_{DS} \tag{6.2}$$

where V_{FB} is the flat-band voltage, ϕ_S is the surface potential at strong inversion, K_1 is the body-effect coefficient, K_2 is the source/drain charge sharing coefficient, and η is the drain-induced barrier lowering coefficient. The temperature sensitivity of the threshold voltage can be determined from the following partial derivative:

$$\frac{\partial V_{th}}{\partial T} = \frac{\partial V_{FB}}{\partial T} + \frac{\partial \phi_S}{\partial T} + \frac{\partial K_1}{\partial T}\sqrt{\phi_S - V_{BS}} + \frac{K_1}{2\sqrt{\phi_S - V_{BS}}}\frac{\partial \phi_S}{\partial T} - \frac{\partial K_2}{\partial T}(\phi_S - V_{BS}) - K_2\frac{\partial \phi_S}{\partial T} - \frac{\partial \eta}{\partial T} V_{DS} \, . \tag{6.3}$$

Coefficient K_1 does not strongly depend on temperature because $K_1 = \sqrt{2\, \varepsilon_{Si}\, q\, N_A} / C_{ox}$. Coefficient K_2 was found to be quite independent of the operating temperature [6.8]. Coefficient η is usually on the order of 10^{-2} and does not change appreciably with temperature. The threshold voltage change with temperature is contributed by changes of the flat-band voltage and the surface potential with temperature. Therefore, (6.3) can be simplified to

$$\frac{\partial V_{th}}{\partial T} \approx \frac{\partial V_{FB}}{\partial T} + \left(1 + \frac{K_1}{2\sqrt{\phi_S - V_{BS}}} - K_2 \right) \frac{\partial \phi_S}{\partial T} \, . \tag{6.4}$$

For N-channel transistors with N^+-poly gates, the flat-band voltage is equal to

$$V_{FB} = -\frac{E_g}{2} - \frac{\phi_S}{2} - \frac{Q_{SS}}{C_{ox}} \tag{6.5}$$

where E_g is the energy bandgap and Q_{SS} is the effective surface charge. The effective surface charge is quite stable in the normal operating temperature range. The expressions for the differentials $\partial E_g/\partial T$ and $\partial \phi_S/\partial T$ can be obtained from [6.9],

$$\frac{\partial \phi_S}{\partial T} = -\frac{1}{T}\left(\frac{E_g|_{T=0^\circ K}}{q} - \phi_S\right) \tag{6.6}$$

and

$$\frac{\partial V_{FB}}{\partial T} = 1.3 \times 10^{-4} + \frac{1}{T}\left(\frac{E_g|_{T=0^\circ K}}{2q} - \frac{\phi_S}{2}\right) . \tag{6.7}$$

Parameter μ_Z, which is the zero-bias carrier mobility, and parameter μ_S, which is the carrier mobility at zero substrate bias and $V_{DS} = V_{DD}$, decrease with temperature. A commonly used temperature dependence is [6.10]

$$\mu|_T = \mu|_{T_r}\left(\frac{T}{T_r}\right)^{-1.5} \tag{6.8}$$

where T is absolute temperature and T_r is the room temperature in °K. The velocity saturation coefficient U_{1Z} is proportional to the ratio of mobility to saturation velocity. The saturation velocity can be approximated by a linear function of $(T/T_r)^{-1}$ in the temperature range of interest from the data report-

ed in [6.11]. Therefore, U_{1Z} has a temperature dependence of $(T/\ T_r\ )^{-2.5}$. The vertical field mobility degradation coefficient, U_{0Z}, is related to surface-roughness scattering and is not very sensitive to temperature variations.

Chapter 7

Conclusion

7.1. Summary

Integration of technology-based design systems is strongly needed for the manufacturing of high-performance VLSI circuits and systems. An interface program PARGEN has been developed to intelligently link the PISCES device simulator and the SPICE circuit simulator. This interface program together with SUPREM, PISCES, and SPICE form an integrated simulation environment for the computer-integrated manufacturing system. Width-related SPICE parameters can not be produced by the current version of PARGEN because the PISCES program does not provide device information along the width dimension. Default values of the width-related SPICE parameters are to be used before a three-dimensional device simulator becomes available.

Example applications of PARGEN have been demonstrated. In computer integrated manufacturing, the direct feedback of circuit response to the process engineer can facilitate better refinement of the fabrication process and device structures. The capability of offering quick simulation to evaluate the sensitivity of circuit performance to each process variable highly assists the optimization of the manufacturing schedule. The PARGEN program has been used to determine the geometric dependences of submicron MOS transistor electrical parameters from device simulation results. No a priori geometric shape of the bulk depletion region is assumed, which makes this method very useful in the

design of new device structures and development of new fabrication processes. By applying this method to determine the basic electrical parameters of submicron LDD transistors, the threshold-voltage reduction and body-effect coefficient show the linear dependence and exponential dependence on $1/L_{eff}$, respectively, which agree with measured data.

A new methodology for the integrated simulation environment incorporating PARGEN to investigate statistical modeling and temperature dependence modeling has been presented. A new sensitivity function is developed for identifying the sensitive SPICE parameters to assist the design of digital and analog application-specific ICs. This new sensitivity function, with the capability of selecting either a relative or an absolute error term, gives a better representation over the bias range of interest. Detailed sensitivity analysis with respect to the drain current and output conductance has been conducted. It can be directly extended to include the transconductance, back-gate transconductance, and gate capacitance.

The application of the new methodology to the temperature dependence modeling of the SPICE Level-4 model for MOS VLSI circuit simulation has been presented. Updating of the sensitive parameter values at a given temperature is performed by a preprocessor prior to the circuit analysis. Circuit simulation using the sensitive subset approach to predict temperature effects has shown good agreement with experimental data on transistor output characteristics, inverter transfer characteristics, and oscillation frequency of a 31-stage ring oscillator.

7.2. Suggested Future Work

7.2.1. Parameter Calculation for Micron/Submicron MOSFET Models

The current version of the PARGEN program calculates the SPICE Level-2 MOSFET model parameter values. The Level-2 MOSFET model is only application to 2-μm technology. This work can be enhanced to calculate the Lev-

el-4 model parameter values, which can be used for 1-μm technology. To extend this work for submicron MOS transistors, detailed device information from three-dimensional numerical device simulators, instead of from two-dimensional device simulators, are needed. New algorithms which use three-dimensional device information can be implemented into the PARGEN program to extract parameter values for submicron MOSFET models.

7.2.2. Parameter Calculation for Bipolar Transistor Models

Parameter calculation for bipolar transistor models is another area the PARGEN program can explore. PARGEN can be extended to the generation of Gummel-Poon model parameter values. The Gummel-Poon model is the most widely- used model for silicon bipolar transistors and is suitable for different technologies with only minor modifications. With the capability of generating both bipolar and MOS transistor model parameter values, the integrated simulation environment can be used for advanced BiCMOS technologies.

Appendix A

PARGEN User Guide

A.1. Introduction

The PARGEN interface program is to link the device simulator PISCES-II and the circuit simulator SPICE. MOS transistor model and MESFET model parameter values are produced by the MOSGEN module and the MESGEN module, respectively, from the internal device information provided by PISCES. These model parameters are compatible with the transistor models implemented in SPICE. This interface program, together with SUPREM, PISCES, and SPICE, form an integrated simulation environment. Such an integrated simulation environment greatly facilitate the designers to examine just how a microscopic fabrication variable, such as implantation dose, affects final device and circuit performance and product yield.

In this appendix, Section A.2. is the 'PARGEN program reference' which briefly describes the function of each subroutine. Section A.3. is the 'PARGEN user guide'.

A.2. Program Reference

A.2.1. MOSGEN

The MOSGEN module contains the following subroutines:

(A) subroutine *INPISC*:

This subroutine reads in data from PISCES output files and stores them in arrays for subsequent computation.

(B) subroutine *CALPAR*:

All the parameters for Level-2 MOS transistor model of SPICE-3 are calculated in this subroutine.

(C) subroutine *UPCASE*:

This subroutine handles the pre-processing of the data files from PISCES. It converts all lower-case letters in the data files to upper-case letters and removes all spaces between the characters. This facilitates the *'INPISC'* subroutine to recognize the data portion of the output files from PISCES and to store them into proper arrays.

(D) subroutine *CALQINV*:

The amount of charge in an inversion layer is needed for the calculation of the threshold voltage and the body-effect coefficient. This subroutine determines the amount of inversion charge.

(E) subroutine *AVAG*:

Since the doping concentrations may vary in different positions within a device, some electrical quantities, such as built-in junction potential and mobility, are functions of the position. The space average is calculated by this subroutine as the representative value for the electrical quantity.

(F) subroutine *CALDOP*:

This subroutine is used for the calculation of the total channel charge coefficient, N_{EFF}, which accounts for the fact that in the channel there is both mobile and fixed charge.

(G) subroutine *OUTPAR*:

This subroutine outputs the model parameters in a format compatible with SPICE input deck.

A.2.2. MESGEN

The MESGEN module contains corresponding subroutines which perform

similar tasks as the ones in MOSGEN except that there is no subroutine *CAL-QINV* in MESGEN.

A.3. User Guide

The following describes how users should prepare the files for running PARGEN.

A.3.1. MOSGEN

(A) PISCES Files

MOSGEN requires PISCES results from six biasing conditions, as are listed in Table 4-1 for an N-channel MOS transistors. If a P-channel transistor is used, polarities of the biasing voltages have to be changed accordingly.

In running PISCES, the following input cards must be included so that the MOSGEN can get all information needed from PISCES output files. These input cards include:

print solution;
print points;
print material;
print que; and
print current.

Figure A-1 shows a typical PISCES input file. This file is used to simulate the electrical behavior of an MOS transistor.

(B) File for Running MOSGEN Automatically

In order to run MOSGEN automatically the following information is written in a file called MOSGEN.IN:

1. output file name
2. output logical unit
3. model name
4. device type
5. number of grid lines in the horizontal direction (x direction)

```
title n-channel mosfet
mesh rect nx=37 ny=26 outf=nmosmesh
x.m n=1 l=0 r=1
x.m n=4 l=2 r=1
x.m n=12 l=2.15 r=0.8
x.m n=17 l=2.3 r=1.25
x.m n=19 l=2.5 r=1
x.m n=21 l=2.7 r=1
x.m n=26 l=2.85 r=0.8
x.m n=34 l=3 r=1.25
x.m n=37 l=5 r=1
y.m n=1 l=0 r=1
y.m n=2 l=0.01 r=1
y.m n=14 l=0.02 r=1.25
y.m n=20 l=0.2 r=0.8
y.m n=24 l=0.4 r=1.25
y.m n=26 l=1 r=1
region num=1 ix.l=1 ix.h=37 iy.l=1 iy.h=2 oxide
region num=2 ix.l=1 ix.h=37 iy.l=2 iy.h=26 silicon
elect num=1 ix.l=4 ix.h=34 iy.l=1 iy.h=1
elect num=2 ix.l=2 ix.h=3 iy.l=2 iy.h=2
elect num=3 ix.l=35 ix.h=36 iy.l=2 iy.h=2
elect num=4 ix.l=1 ix.h=37 iy.l=26 iy.h=26
doping region=2 p.type conc=8e15 uniform
doping region=2 p.type gaussian conc=4e17 x.l=2.0
+       x.r=3.0 peak=0.015 char=0.02
doping region=2 n.type gaussian conc=1e20 junction=0.25
+       x.l=0 x.r=2.0 peak=0.05
doping region=2 n.type gaussian conc=1e20 junction=0.25
+       x.l=3.0 x.r=5.0 peak=0.05
interface x.min=0 x.max=5 y.min=0.01 y.max=0.01 qf=1e10
symb gummel carriers=0
method iccg damped
material region=2 g.suf=0.6
contact num=1 n.poly
models conmob fld consrh
solve init outf=ninit
print solu
print points
print ix.l=1 ix.h=37 iy.l=2 iy.h=26 material
print cue
print current
end
```

Figure A-1 PISCES input deck to generate the data needed by MOSGEN.

6. number of grid lines in the vertical direction (y direction)
7. output file name from condition 1
8. SPICE level number
9. oxide thickness
10. substrate concentration
11. surface state density
12. the grid line which passes the source-channel boundary
13. the grid line which passes the drain-channel boundary
14. the grid line which passes along the oxide-silicon interface
15. output file name from condition 2
16. output file name from condition 3
17. the applied gate voltage in condition 3
18. output file name from condition 4
19. output file name from condition 5
20. the applied substrate voltage in condition 5
21. output file name from condition 6
22. the applied drain voltage in condition 6.

A sample of MOSGEN.IN is show in Figure A-2.

A.3.2. MESGEN

(A) PISCES Files

Four PISCES output files are needed by MESGEN. The bias conditions for these output files are listed in Table 4-2. The five print cards mentioned in Section A.3.1. must be also included in the PISCES input files.

(B) File for Running MESGEN Automatically

The following information is stored in a file MESGEN.IN to be used for running MESGEN in an automatic mode:

1. output file name
2. output logical unit
3. number of grid lines in the horizontal direction (x direction)

```
modpara
5
nmos
nmos
37
26
pisc1
2
100
8e15
1e10
4
34
2
pisc2
pisc3
1.5
pisc4
pisc5
-4.0
pisc6
5.0
```

Figure A-2 A sample MOSGEN.IN file.

4. number of grid lines in the vertical direction (y direction)
5. output file name from condition 1
6. gate length in μm
7. active layer thickness in μm
8. the grid line which passes the gate near the source side
9. the grid line which passes the gate near the drain side
10. output file name from condition 2
11. the applied drain voltage in condition 2
12. output file name from condition 3
13. the applied drain voltage in condition 3
14. output file name from condition 4
15. the applied gate voltage in condition 4
16. the applied drain voltage in condition 4.

Appendix B

A New Method to Determine Effective Channel Widths of MOS Transistors

Electrical characteristics of MOS transistors are strongly dependent on the channel dimensions. Accurate characterization of effective channel dimensions is therefore of fundamental importance in the VLSI device design and process control. As small-geometry transistors with channel sizes in the micron or submicron range are widely used on VLSI circuits, it is more critical to accurately determine the effective channel length and width of MOS transistors.

Various methods have been proposed to determine effective channel lengths of MOS transistors [B.1-B.6]. However, little effort has been devoted to the extraction method for the effective channel width based on electrical measurement. The method proposed by Ma et al. [B.7] determines the effective channel width by plotting g_{DS} versus W_{mask} for different gate-source voltages at a fixed low V_{DS} bias. The source/drain series resistance was neglected in their method. It is not accurate when the source/drain series resistance is comparable to the intrinsic channel resistance. Sheu et al. [B.8] used a method to determine channel widths based on capacitance measurement. It requires a high accuracy measurement system to obtain small intrinsic gate capacitance values on the order of femto Farads.

In this work, a new resistive method is presented to determine the effective channel widths of MOS transistors. In this method, the series resistance is

first determined using the channel-length characterization method. A practical approximation is then used to calculate the series resistance for transistors with different channel widths. The test structure for this method consists of two sets of transistors. One set consists of transistors with different channel lengths and same channel width. The other set contains transistors with different channel widths and same channel length. This method is suitable for test structures with transistor channel-length in the submicrometer range.

B.1. The Channel-Length Determination Method

The measured resistance from the source to the drain terminals ($R_M \equiv V_{DS}/ I_{DS}$) for an MOS transistor operated in the linear region can be expressed as

$$R_M = R_{SD}+R_{CH} \quad \text{(B.1)}$$

where

$$R_{CH} = [W_{eff}\, \mu\, C_{ox}\, (V_{GS} - V_{TH} - \frac{1}{2} V_{DS})]^{-1} L_{eff}\ . \quad \text{(B.2)}$$

Here $W_{eff} = W_{mask}-\Delta W$ and $L_{eff} = L_{mask}-\Delta L$ are the effective channel width and length, respectively, R_{SD} is the source/drain series resistance, and R_{CH} is the channel resistance. (B.1) can be rewritten as

$$R_M = A\, L_{mask}+ B \quad \text{(B.3)}$$

where

$$A = [W_{eff}\, \mu\, C_{ox}\, (V_{GS} - V_{TH} - \frac{1}{2} V_{DS})]^{-1} \quad \text{(B.4)}$$

and

$$B = -A\,\Delta L + R_{SD}\,. \tag{B.5}$$

The resistance R_M is measured under a selected set of gate biases for transistors with different channel lengths and same channel width. Two successive linear regressions are then performed to determine the effective channel length, as described in [B.1]. However, for transistors with lightly-doped-drain (LDD) structures, the method in [B.1] can not be used since R_{SD} is a function of the gate bias and the method in [B.6] can be used.

B.2. The New Channel-Width Determination Method

The channel conductance ($g_{CH} \equiv 1/R_{CH}$) is given by

$$\begin{aligned} g_{CH} &= \frac{1}{R_M - R_{SD}} \\ &= \frac{W_{eff}}{L_{eff}}\mu\, C_{ox}\,(\,V_{GS} - V_{TH} - \frac{1}{2}V_{DS}\,)\,. \end{aligned} \tag{B.6}$$

(B.6) can be rewritten as

$$g_{CH} = C\,(\,W_{mask} - \Delta W\,) \tag{B.7}$$

where

$$C = \frac{1}{L_{eff}}\mu\, C_{ox}\,(\,V_{GS} - V_{TH} - \frac{1}{2}V_{DS}\,)\,. \tag{B.8}$$

In plotting g_{CH} versus W_{mask} for a constant C, a straight line is fitted through the data. The channel-width reduction ΔW is given by the intercept of the straight line on the abscissa.

In [B.7], the series resistance R_{SD} is neglected so that g_{CH} is approximated by g_M ($\equiv 1/R_M$). The typical ratio of the source/drain series resistance

to the channel resistance is 20 Ω / 150 Ω for a conventional MOS transistor with t_{ox} = 15 nm, L_{eff} = 0.8 μm, W_{eff} = 10 μm, and a gate bias of 5 V. The series resistance is comparable to the intrinsic channel resistance for short-channel and thin-oxide devices and the method in [B.7] is not accurate for the determination of ΔW. In our method, the series resistance is taken into account to calculate g_{CH}. The procedures for the new method are:

(i) Measure R_M for a set of transistors with same L_{mask} and different W_{mask}'s under a selected set of gate biases.

(ii) Obtain the series resistance R_{SD1} of a transistor with wide channel width W_{mask1} from the effective channel length characterization. The method mentioned in the previous section is used for the effective channel length characterization. Wide channel transistors are used such that $W_{mask1} \approx W_{eff1}$.

(iii) Use an approximate expression to determine the series resistances associated with different W_{mask}'s,

$$R_{SD2} = R_{SD1} \frac{W_{mask1}}{W_{mask2}} \quad . \tag{B.9}$$

(iv) Plot calculated g_{CH} versus W_{mask} for different gate biases. A straight line is fitted through data for a given gate bias. The channel-width reduction (ΔW) is determined from the intercept of all straight lines on the abscissa.

B.3. Experimental Results and Discussion

Two wafers with test transistors fabricated by different technologies were used. Test transistors on wafer #1 were fabricated by 2-μm technology with the conventional source/drain structure and the gate-oxide thickness is 40 nm. Transistors on wafer #2 were fabricated by 2-μm technology with the LDD structure and the gate-oxide thickness is 25 nm. In the characterization

of the effective channel length and the series resistance, the set of transistors on wafer #1 consists of four devices with W_{mask} = 20 μm, and L_{mask} = 1.5, 2, 3, and 20 μm, respectively, and the set of transistors on wafer #2 has four devices with W_{mask} = 10 μm and L_{mask}= 1.5, 2, 3, and 5 μm, respectively. The drain bias V_{DS} is 0.1 V and the gate drive V_{GS}-V_{TH} varies from 2 V to 6 V. The threshold voltage was measured for each transistor in the experiment.

For wafer #1, the channel-length reduction (ΔL) is 0.47 μm and the series resistance for a W_{mask} = 20 μm transistor is $58.5 Ω. Figure B-1 shows the plot of R_M versus L_{mask} . The correlation coefficients for all straight lines are better than 0.999. The channel-length reduction and the series resistance for wafer #2 vary with the gate bias since the transistors on the wafer have LDD structures. The method in [B.6] was used to determine ΔL and R_{SD} . The channel-length reduction varies from 0.13 μm at V_{GS}-V_{TH} = 2 V to 0.05 μm at V_{GS} - V_{TH}= 6 V, as is shown in Fig. B-2. Figure B-3 shows the series resistance for a W_{mask} = 10 μm transistor on wafer #2 under different gate biases. The series resistance changes from 51.5 Ω at V_{GS}-V_{TH}= 2 V to 45.7 Ω at V_{GS}-V_{TH}= 6 V.

The set of transistors used for the determination of ΔW for wafer #1 consists of four devices with L_{mask} = 20 μm and W_{mask}= 2, 3, 4, and 20 μm , respectively. The set of transistors on wafer #2 has three devices with L_{mask} = 1.5 μm and W_{mask} = 3, 5, and 10 μm, respectively. The channel-width reduction for wafer #1 determined by our method is -0.13 μm and that determined by Ma's method is -0.12 μm, which are shown in Figures B-4 and B-5, respectively. The difference between the results obtained by our method and

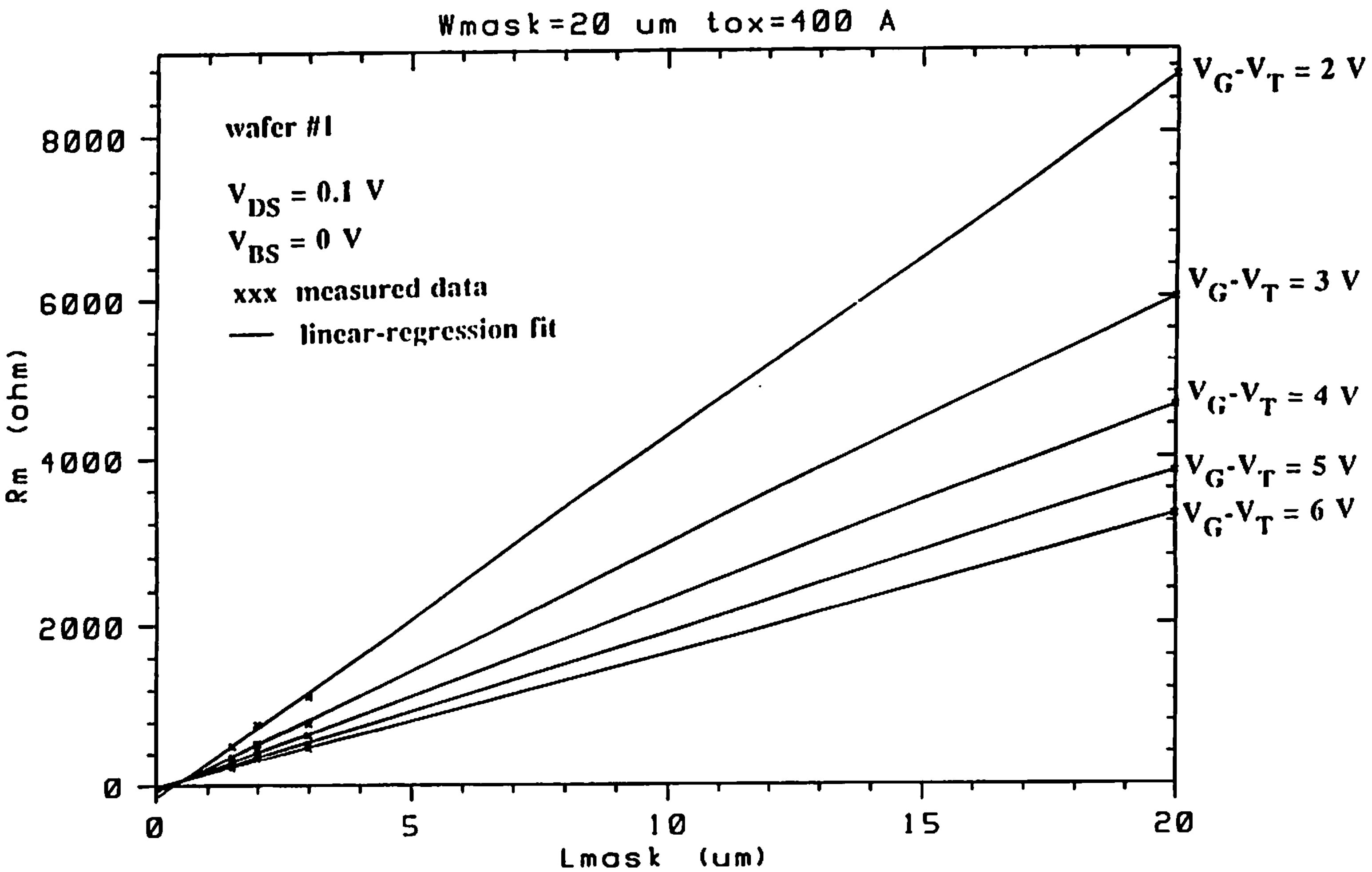


Figure B-1 The resistance R_M versus L_{mask} for test wafer #1.

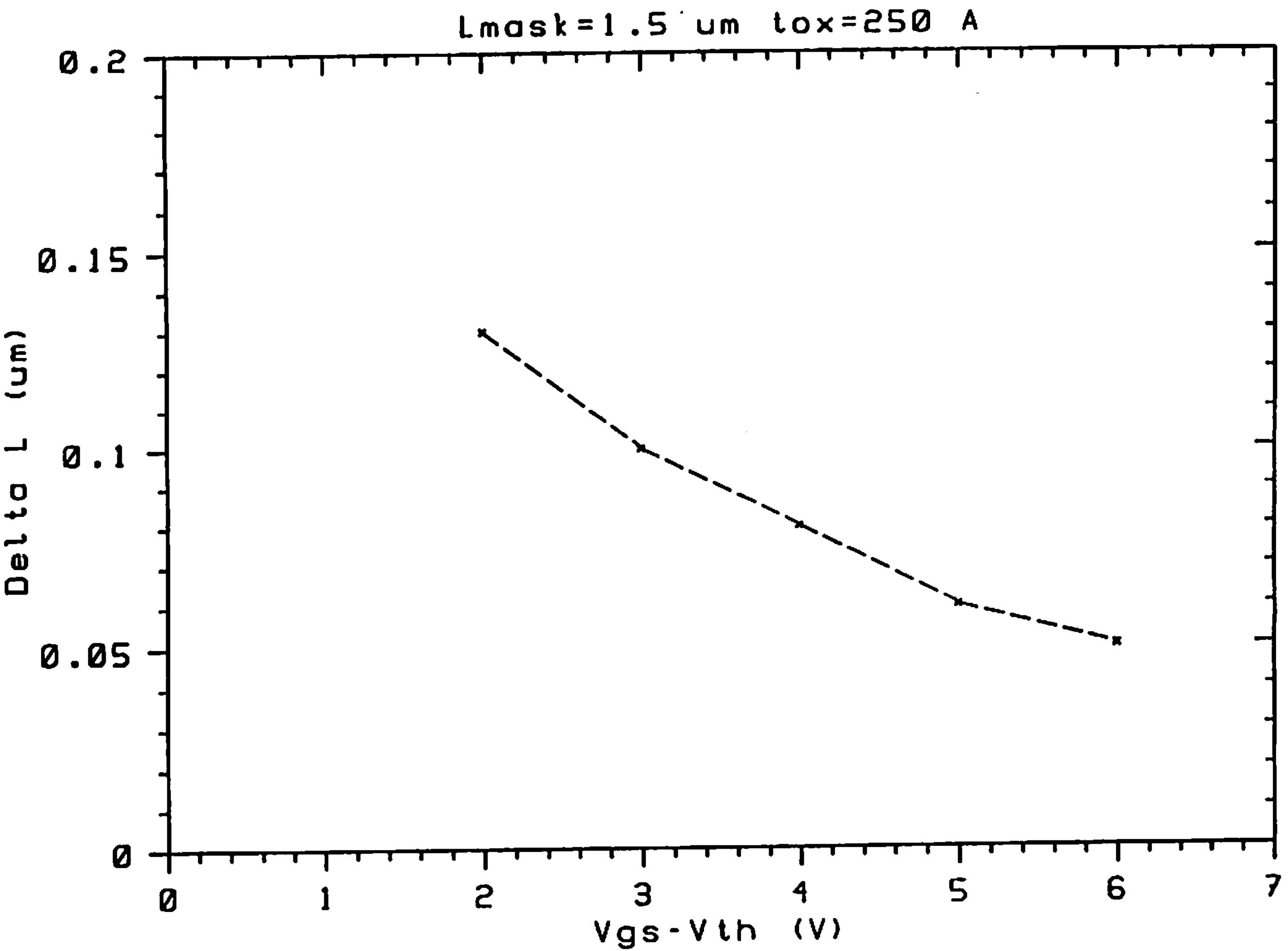


Figure B-2 **The channel-length reduction ΔL versus $V_{GS} - V_{TH}$ for test wafer #2.**

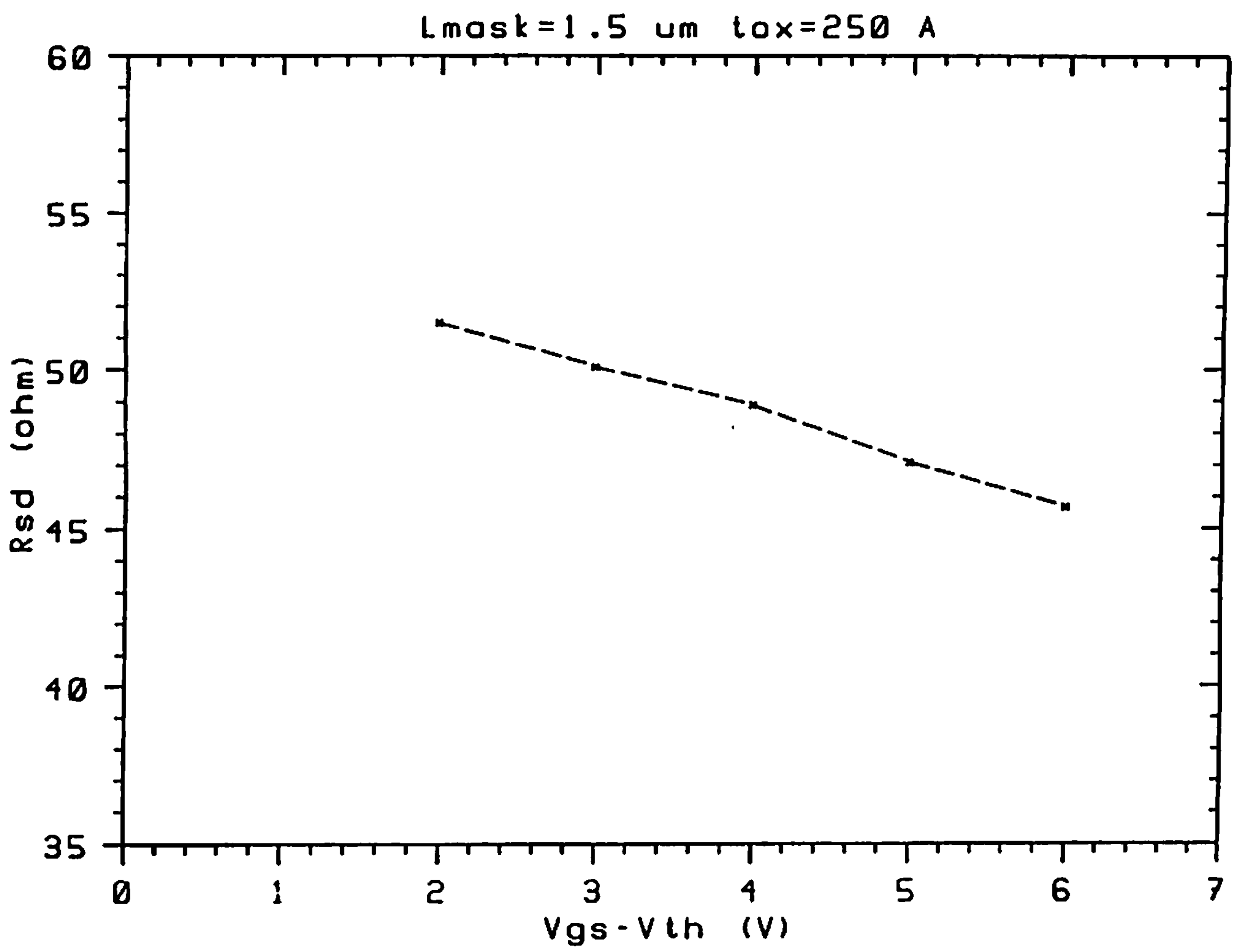


Figure B-3 **The source/drain series resistance R_{SD} versus $V_{GS} - V_{TH}$ for test wafer #2.**

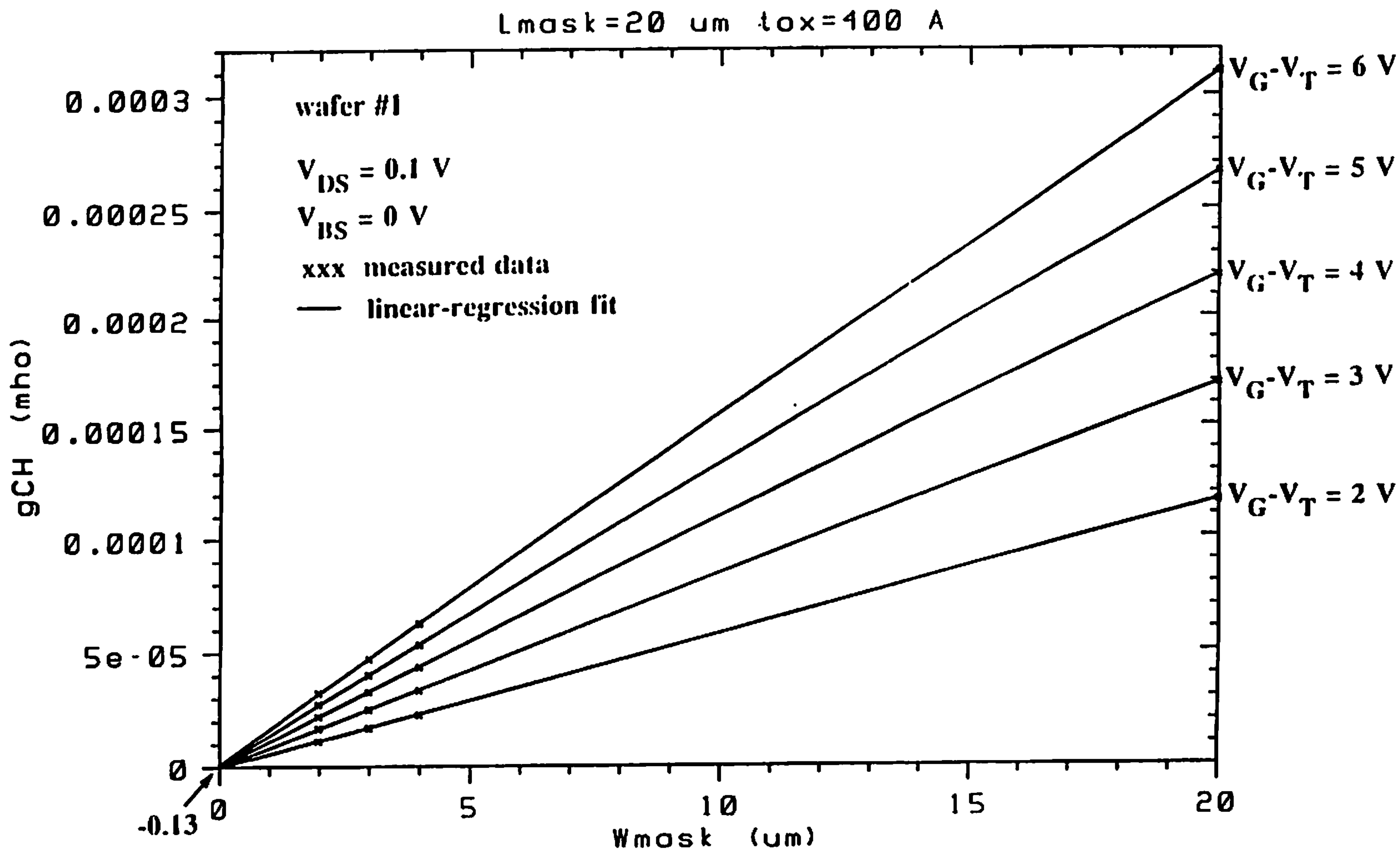


Figure B-4 The channel conductance g_{CH} versus W_{mask} for test wafer #1 using the new method. The channel-width reduction ΔW is determined to be -0.13 um.

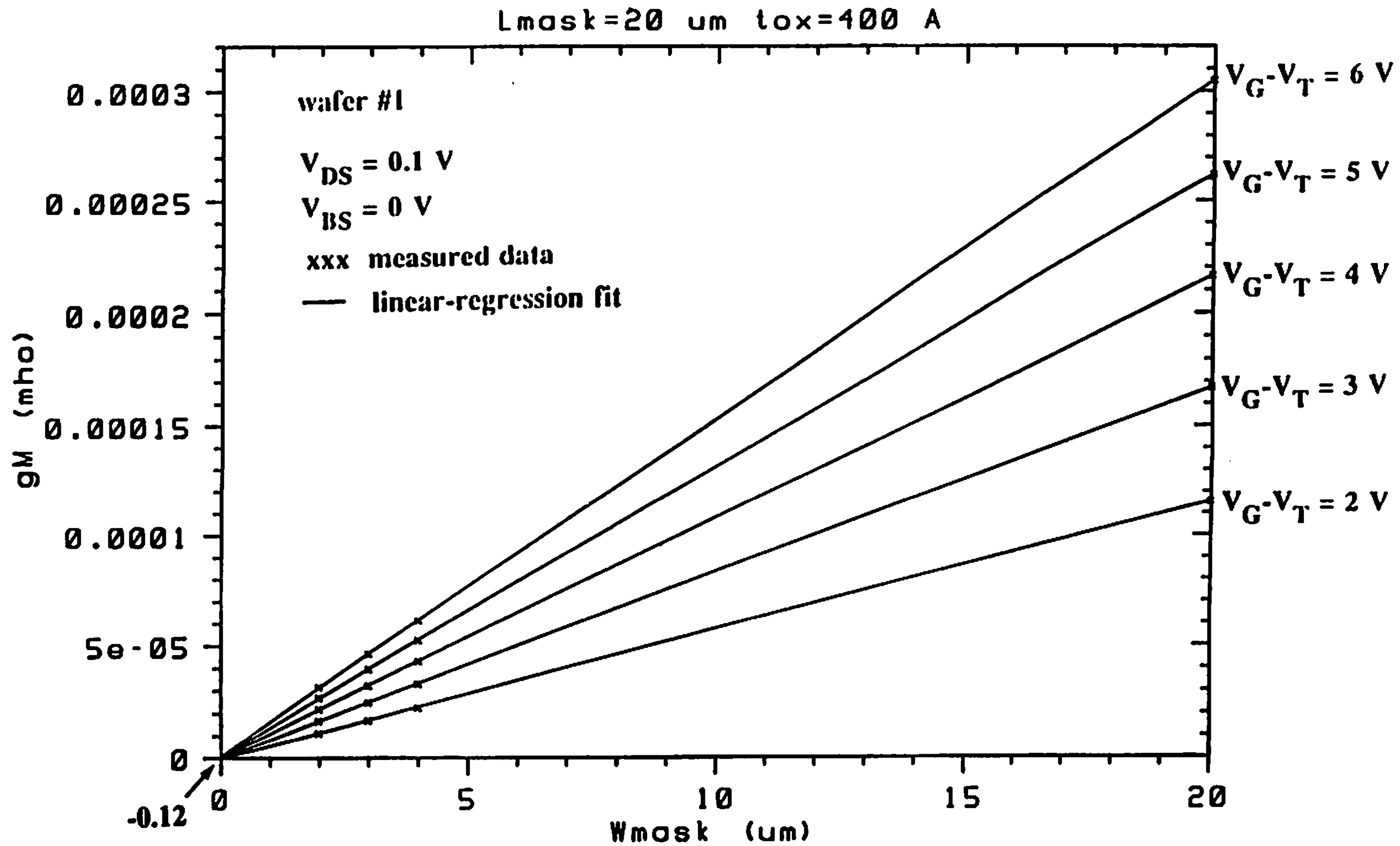


Figure B-5 The conductance g_M versus W_{mask} for test wafer #1 using Ma's method. The channel-width reduction ΔW is determined to be -0.12 um.

Ma's method is very small since the channel resistance is dominant over the series resistance for wafer #1. The channel-width reduction for wafer #2 using our method is determined to be 0.25 μm, which is shown in Figure B-6. No significant change in ΔW for different gate biases was observed. The result obtained by Ma's method is shown in Figure B-7. The channel-width reduction is different for different gate biases but it shows no trend with the gate bias. The results in Figures B-6 and B-7 are much different since the series resistance is not negligible compared to the channel resistance for wafer #2.

Figures B-8 and B-9 show the results using capacitance method to determine ΔW. The comparison of ΔW determined by the capacitance method and our new method is listed in Table B-1. The difference between the results obtained by the two methods can be ascribed to the inherent inaccuracy of the capacitance method. As shown in Figure B-10, the capacitance value in the strong inversion region changes with the gate bias.

In conclusion, a new method is presented to determine the effective widths of MOS transistors. It is based on the resistance measurement made on a series of transistors with the dimensional dependence of series resistance taken into account. The experimental results show that this method can be used with good accuracy when the series resistance is comparable to the channel resistance. It is suitable for test structures with transistor channel-length in the submicrometer range.

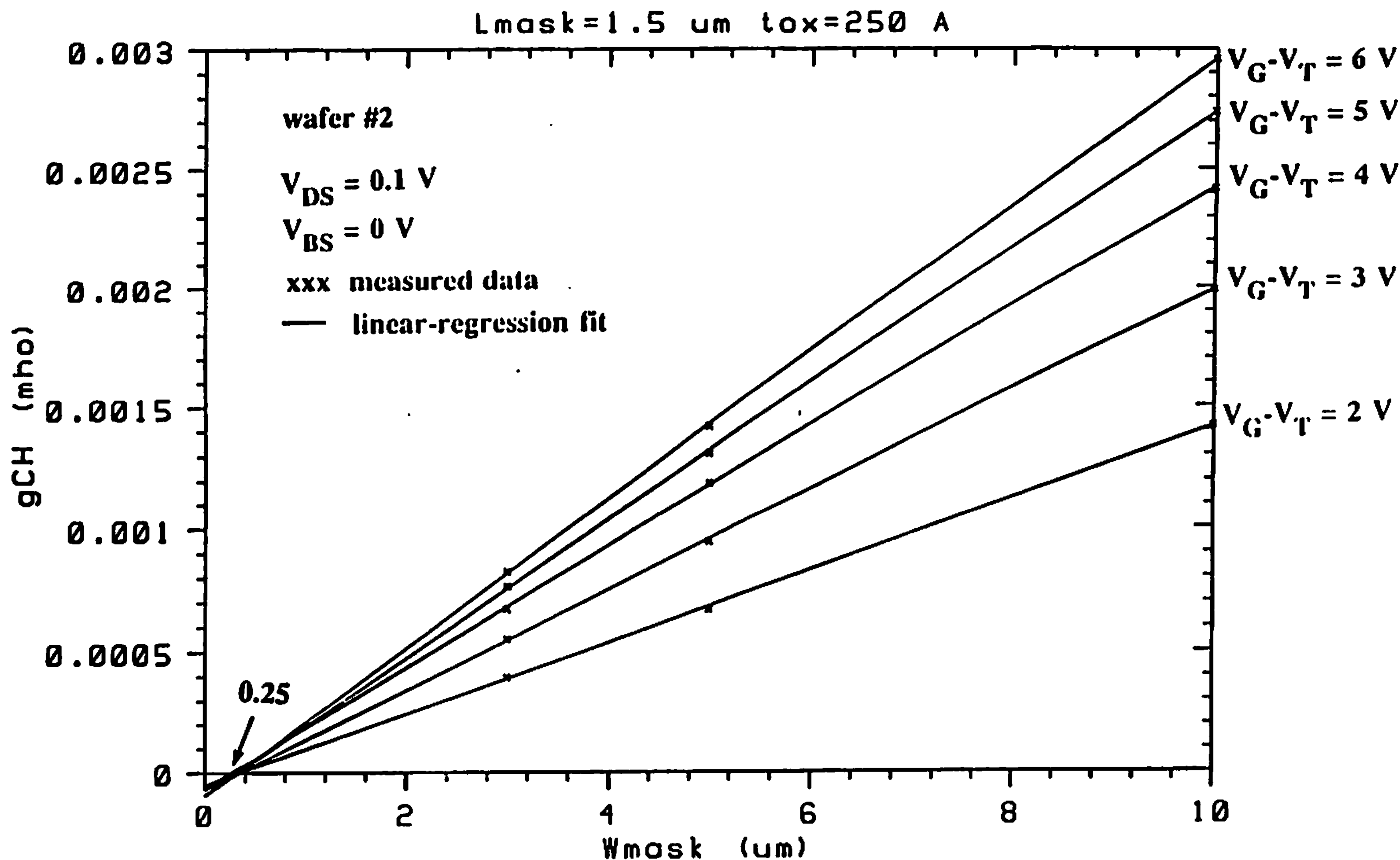


Figure B-6 The channel conductance g_{CH} versus W_{mask} for test wafer #2 using the new method. The channel-width reduction ΔW is determined to be 0.25 um.

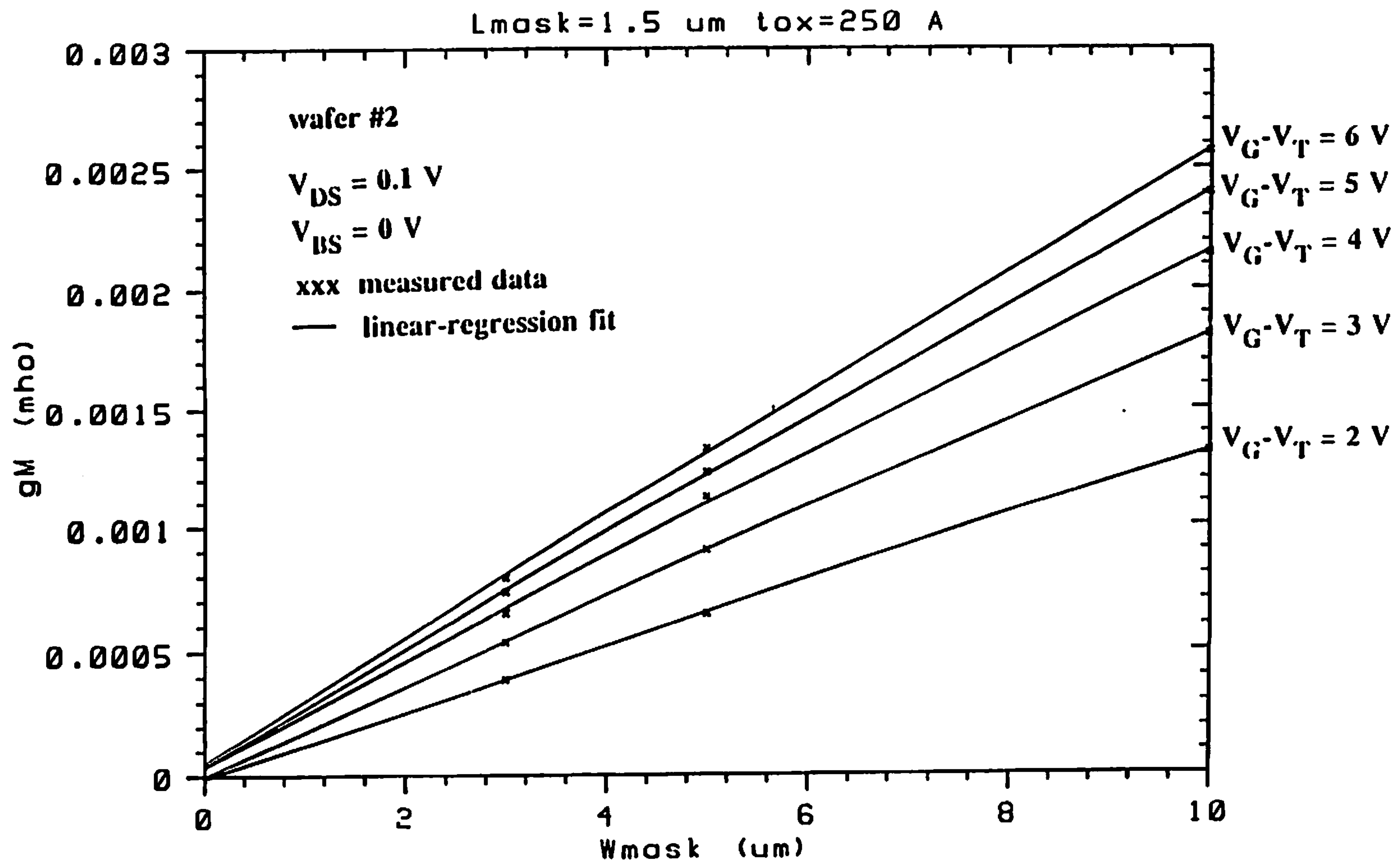


Figure B-7 The conductance g_M versus W_{mask} for test wafer #2 using Ma's method.

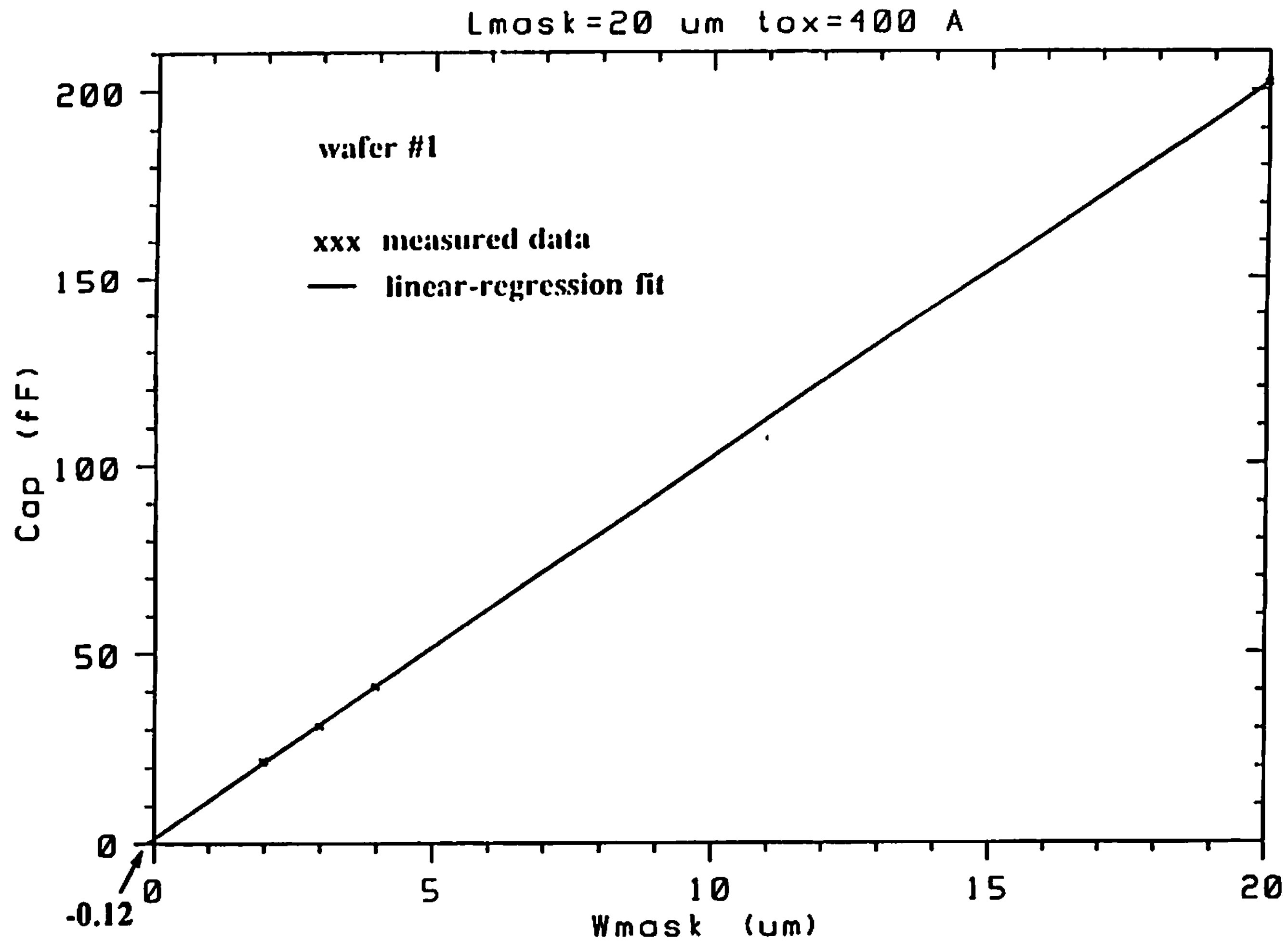


Figure B-8 Intrinsic gate capacitance versus W_{mask} for test wafer #1. The channel-width reduction ΔW is determined to be -0.12 um.

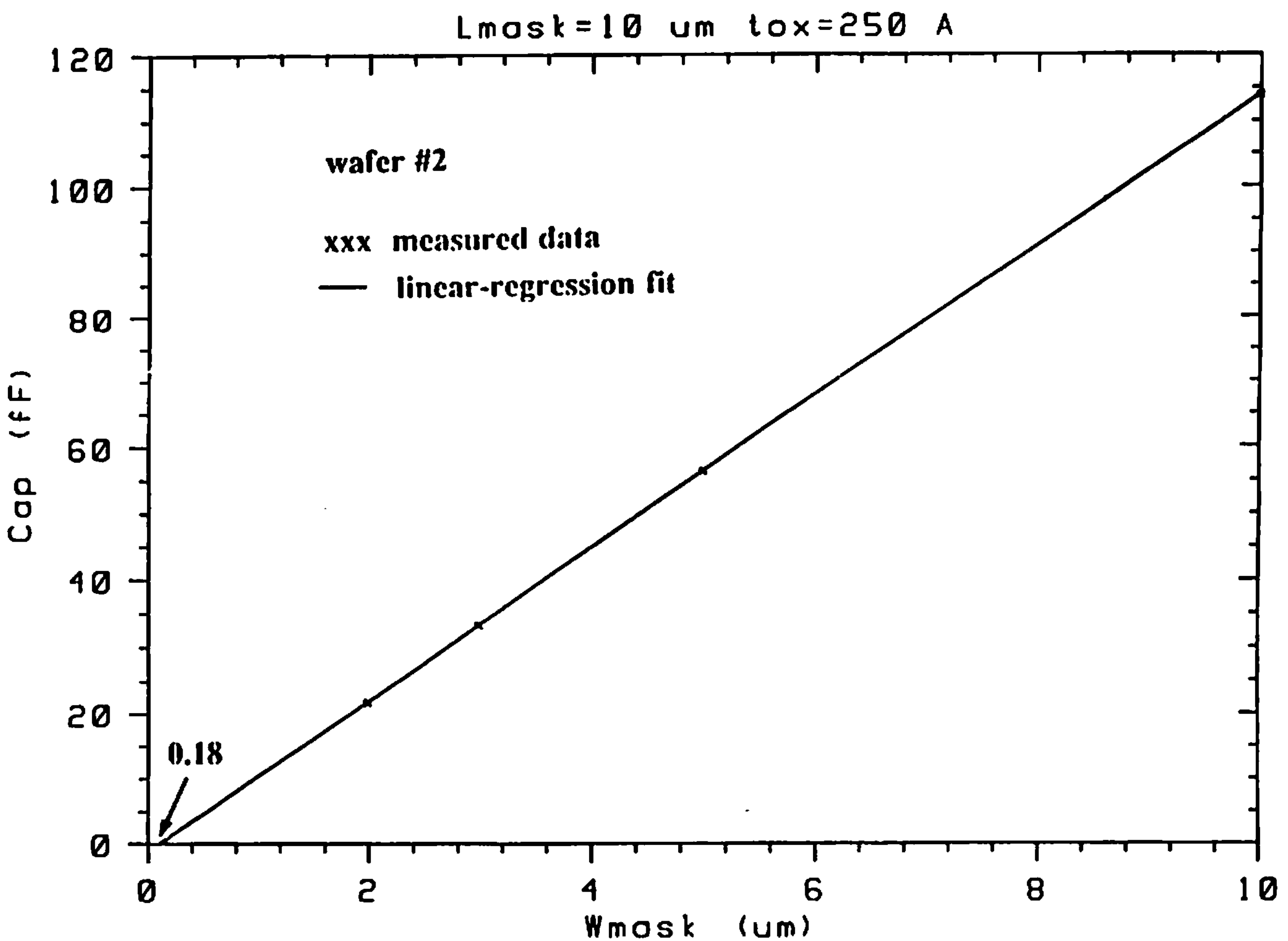


Figure B-9 Intrinsic gate capacitance versus W_{mask} for test wafer #2. The channel-width reduction ΔW is determined to be 0.18 um.

Table B-1 Comparison of ΔW determined by the capacitance method and the new resistive method.

ΔW wafer / method	# 1	# 2
capacitance method	- 0.12 um	0.18 um
new resistive method	- 0.13 um	0.25 um

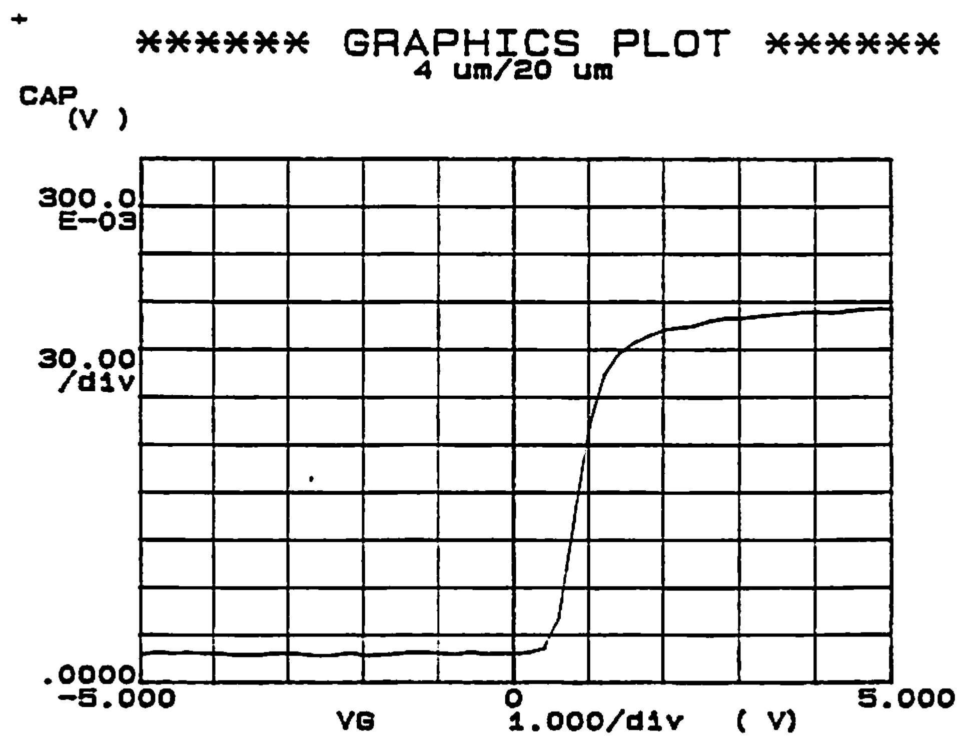


Figure B-10 Measured capacitance (uncalibrated) versus V_{GS} for the capacitance method.

Appendix C

PARGEN Program Listing

```
      PROGRAM MOSGEN
      IMPLICIT INTEGER (I-N)
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
      DOUBLE PRECISION KP,LAMBDA,IS,MJ,MJSW,JS,
     +  NSUB,NSS,NFS,LD,NEFF,KF,COORX,COORY,VOL,NC,
     +  PC,QFN,QFP,K1,K2
     +  DOP,MOBN,MOBP,JSAT,MOB0
      CHARACTER FILIN*20,FILOUT*20,
     +  BLANK*81,MODNAM*6,DEVTYP*4
      INTEGER*2 DEVIN,DEVOUT,DEVIN2
      DIMENSION VOL(100,100),NC(100,100),PC(100,100),
     + QFN(100,100),
     + QFP(100,100),COORX(100,100),COORY(100,100),
     + DOP(100,100),MOBN(100,100),MOBP(100,100),E(100,100),
     + JSAT(100,100)

      COMMON /BLOCK1/LEVEL,VTO,KP,GAMMA,PHI,LAMBDA,RD,RS,CBD,CBS,
     +  IS,PB,CGSO,CGDO,CGBO,RSH,CJ,MJ,CJSW,MJSW,JS,TOX,NSUB,NSS,NFS,
     +  TPG,XJ,LD,UO,UCRIT,UEXP,UTRA,VMAX,NEFF,XQC,KF,AF,FC,DELTA,
     +  THETA,ETA,KAPPA,ILEVEL,IVTO,IKP,IGAMMA,IPHI,ILAMBDA,IRD,IRS,
     +  ICBD,ICBS,IIS,IPB,ICGSO,ICGDO,ICGBO,IRSH,ICJ,IMJ,ICJSW,IMJSW,
     +  IJS,ITOX,INSUB,INSS,INFS,ITPG,IXJ,ILD,IUO,IUCRIT,IUEXP,IUTRA,
     +  IVMAX,INEFF,IXQC,IKF,IAF,IFC,IDELTA,ITHETA,IETA,IKAPPA
      COMMON /BLOCK3/ DEVIN,DEVOUT,DEVIN2
     +      /BLOCK4/ FILIN,FILOUT,MODNAM,DEVTYP
     +      /BLOCK6/ IMAX,JMAX
      COMMON /BLOCK5/VOL,NC,PC,QFN,QFP
      COMMON /BLOCK7/DOP,E,QINV
      COMMON /BLOCK8/MOBN,MOBP,JSAT
      COMMON /BLOCK9/COORX,COORY
      COMMON /BLOCK11/VSAT,MOB0,UDEG
      COMMON   /BLOCK15/UOZ,U1Z,US,UZ,K1,K2

      BLANK=' '
      DATA ILEVEL,IVTO,IKP,IGAMMA,IPHI,ILAMBDA,IRD,IRS,ICBD,ICBS,
     +   IIS,IPB,ICGSO,ICGDO,ICGBO,IRSH,ICJ,IMJ,ICJSW,IMJSW,IJS,
     +   ITOX,INSUB,INSS,INFS,ITPG,IXJ,ILD,IUO,IUCRIT,IUEXP,IUTRA,
     +   IVMAX,INEFF,IXQC,IKF,IAF,IFC,IDELTA,ITHETA,IETA,IKAPPA
     +   /42*0/

C     INITIALIZE ALL THE DEFAULT PARAMETERS

      LEVEL=1
      VTO=0.0
      KP=2.0E-5
      GAMMA=0.0
      PHI=0.6
      LAMBDA=0.0
      RD=0.0
      RS=0.0
```

```
      CBD=0.0
      CBS=0.0
      IS=1.0E-14
      PB=0.8
      CGSO=0.0
      CGDO=0.0
      CGBO=0.0
      RSH=0.0
      CJ=0.0
      MJ=0.5
      CJSW=0.0
      MJSW=0.33
      JS=0.0
      TOX=1.0E-7
      NSUB=0.0
      NSS=0.0
      NFS=0.0
      TPG=1.0
      XJ=0.0
      LD=0.0
      UO=600
      UCRIT=1.0E4
      UEXP=0.0
      UTRA=0.0
      VMAX=0.0
      NEFF=1.0
      XQC=1.0
      KF=0.0
      AF=1.0
      FC=0.5
      DELTA=0.0
      THETA=0.0
      ETA=0.0
      KAPPA=0.2

      DEVIN2=3
      OPEN(UNIT=DEVIN2,STATUS='UNKNOWN',file='mosgen1.in')
10     FORMAT(A20)
      READ(DEVIN2,10)FILOUT
      READ(DEVIN2,20)DEVOUT
20     FORMAT(I2)
      READ(DEVIN2,30)MODNAM
30     FORMAT(A6)
      READ(DEVIN2,40)DEVTYP
40     FORMAT(A4)
      READ(DEVIN2,50)IMAX
50     FORMAT(I5)
      READ(DEVIN2,60)JMAX
60     FORMAT(I5)
      OPEN(UNIT=DEVOUT,STATUS='OLD',FILE=FILOUT)
```

```
      CALL INPISC()
      CALL CALPAR()
      CALL OUTPAR()
      CLOSE(DEVIN)
      CLOSE(DEVOUT)
      STOP
      END


      SUBROUTINE INPISC
      IMPLICIT INTEGER (I-N)
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
      CHARACTER LINE*81,KOOL*81
      INTEGER*2 N,I,J,DEVIN,DEVOUT,DEVIN2
      CHARACTER FILIN*20,FILOUT*20,MODNAM*6,DEVTYP*4
      DOUBLE PRECISION VOL,NC,PC,QFN,QFP,COORX,COORY,
     +  DOP,MOBN,MOBP,JSAT,MOB0
      DIMENSION VOL(100,100),NC(100,100),PC(100,100)
     + ,QFN(100,100),QFP(100,100),COORX(100,100),COORY(100,100),
     +  DOP(100,100),MOBN(100,100),MOBP(100,100),E(100,100),
     +  JSAT(100,100)

      COMMON /BLOCK3/ DEVIN,DEVOUT,DEVIN2
      COMMON /BLOCK4/ FILIN,FILOUT,MODNAM,DEVTYP
      COMMON /BLOCK6/ IMAX,JMAX
      COMMON /BLOCK5/ VOL,NC,PC,QFN,QFP
      COMMON /BLOCK7/DOP,E,QINV
      COMMON /BLOCK8/MOBN,MOBP,JSAT
      COMMON /BLOCK9/COORX,COORY
      COMMON /BLOCK11/VSAT,MOB0,UDEG

      READ(DEVIN2,1)FILIN
1      FORMAT(A20)
      M=1
      K=1
      DEVIN=4
      OPEN(UNIT=DEVIN,STATUS='OLD',FILE=FILIN)
5      READ(DEVIN,10,END=30)LINE
10      FORMAT(A80)
      KOOL=' '
      I=1
      DO 20 N=1,LEN(LINE)
      IF((LINE(N:N).NE.' ').AND.(LINE(N:N).NE.'	'))THEN
      KOOL(I:I)=LINE(N:N)
      I=I+1
      ENDIF
20      CONTINUE
      CALL UPCASE(KOOL)
C      OPEN(UNIT=DEVOUT,STATUS='OLD',FILE=FILOUT)
C      WRITE(DEVOUT,40)KOOL
```

```
      IF(KOOL(1:13).EQ.'NODEVNPQFNQFP')THEN
      GO TO 60
      ELSE IF(KOOL(1:10).EQ.'NODEXCOORD') THEN
      GO TO 90
      ELSE IF(KOOL(1:12).EQ.'NODEMOBILITY') THEN
      GO TO 150
      ELSE IF(KOOL(1:13) .EQ. 'MOBILITYMODEL')THEN
      READ(DEVIN,15)UDEG
 15    FORMAT(13X,D13.6)
      K=K+1
      IF(K .NE. 2) M=M-1
      GO TO 25
      ELSE IF(KOOL(1:10) .EQ. 'LOG10(NI)=')THEN
      READ(DEVIN,35)MOB0
      GO TO 25
      ELSE IF(KOOL(1:11) .EQ. 'P-MOBILITY=')THEN
      READ(DEVIN,35)VSAT
 35    FORMAT(16X,D16.2)
      WRITE(DEVOUT,35)MOB0,VSAT
      GO TO 25
      ELSE
      GO TO 5
      ENDIF
 60    DO 65 I=1,IMAX
      DO 65 J=1,JMAX
 50    READ(DEVIN,70,END=30)VOL(I,J),NC(I,J),PC(I,J),QFN(I,J),
    +   QFP(I,J)
 70    FORMAT(8X,F10.5,4D12.4)
      VOL(I,J)=VOL(I,J)*1.D0
C      WRITE(DEVOUT,80)I,J,VOL(I,J),NC(I,J),QFN(I,J)
 80    FORMAT(1H ,3X,'FOR POINT(',I5,',',I5,')','VALUES ARE',F10.5,2E12.4)
65    CONTINUE
      GO TO 25
 40    FORMAT(1H ,A80)
 90    READ(DEVIN,85)
 85    FORMAT(/)
100    DO 110 K=1,IMAX
      DO 110 L=1,JMAX
120    READ(DEVIN,130) COORX(K,L),COORY(K,L),DOP(K,L)
130    FORMAT(5X,2D11.3,D12.3)
C      WRITE(DEVOUT,140)K,L,COORX(K,L),COORY(K,L),DOP(K,L)
140    FORMAT(1X,'COORD(',I5,',',I5,')=',1P2E11.3,E12.3)
110    CONTINUE
      GO TO 25
150    READ(DEVIN,155)
155    FORMAT(1X)
      DO 160 I=1,IMAX
      DO 160 J=2,JMAX
      READ(DEVIN,170)MOBN(I,J),MOBP(I,J)
170    FORMAT(5X,F15.2,F16.2)
```

```
C      WRITE(DEVOUT,170)MOBN(I,J),MOBP(I,J)
160    CONTINUE
       GO TO 25
 25    M=M+1
       IF(M .NE. 7)GO TO 5
 30    CONTINUE
       RETURN
       END


       SUBROUTINE CALPAR()
       IMPLICIT INTEGER(I-N)
       IMPLICIT DOUBLE PRECISION (A-H,O-Z)
       INTEGER*2 DEVIN,DEVOUT,DEVIN2
       DOUBLE PRECISION VOL,NC,PC,QFN,QFP,COORX,COORY,
     + KP,LAMBDA,IS,MJ,MJSW,JS,NSUB,NSS,NFS,K1,K2,
     + LD,NEFF,KF,DOP,MOBN,MOBP,AVA,JSAT,NCINV,NC0,MOB0
       DIMENSION VOL(100,100),NC(100,100),PC(100,100),QFN(100,100)
     +  ,QFP(100,100),COORX(100,100),COORY(100,100),
     +   DOP(100,100),MOBN(100,100),MOBP(100,100),
     +   E(100,100),JNEDGE(100),JPEDGE(100),ISTART(100),IEND(100),
     + JSAT(100,100),NCINV(100,100),NC0(100,100),JPOINT(100)
        COMMON /BLOCK1/ LEVEL,VTO,KP,GAMMA,PHI,LAMBDA,RD,RS,CBD,CBS,
     + IS,PB,CGSO,CGDO,CGBO,RSH,CJ,MJ,CJSW,MJSW,JS,TOX,NSUB,NSS,NFS,
     + TPG,XJ,LD,UO,UCRIT,UEXP,UTRA,VMAX,NEFF,XQC,KF,AF,FC,DELTA,
     + THETA,ETA,KAPPA,ILEVEL,IVTO,IKP,IGAMMA,IPHI,ILAMBDA,IRD,IRS,
     + ICBD,ICBS,IIS,IPB,ICGSO,ICGDO,ICGBO,IRSH,ICJ,IMJ,ICJSW,IMJSW,
     + IJS,ITOX,INSUB,INSS,INFS,ITPG,IXJ,ILD,IUO,IUCRIT,IUEXP,IUTRA,
     + IVMAX,INEFF,IXQC,IKF,IAF,IFC,IDELTA,ITHETA,IETA,IKAPPA
       COMMON /BLOCK5/VOL,NC,PC,QFN,
     +   QFP
       COMMON /BLOCK6/IMAX,JMAX
       COMMON /BLOCK7/DOP,E,QINV
       COMMON /BLOCK8/MOBN,MOBP,JSAT
       COMMON /BLOCK9/COORX,COORY
       COMMON /BLOCK3/DEVIN,DEVOUT,DEVIN2
       COMMON /BLOCK10/AVA
       COMMON /BLOCK11/VSAT,MOB0,UDEG
       COMMON /BLOCK15/UOZ,U1Z,US,UZ,K1,K2
       COMMON /BLOCK12/QDOP
       READ(DEVIN2,3)LEVEL
       ILEVEL=1
       READ(DEVIN2,2)TOX1
 2     FORMAT(D11.4)
       TOX=TOX1*1.D-8
       ITOX=1
       READ(DEVIN2,2)NSUB
       INSUB=1
       READ(DEVIN2,2)NSS
       INSS=1
```

```
      READ(DEVIN2,3)ISMASK
3     FORMAT(I3)
      READ(DEVIN2,3)IDMASK
      READ(DEVIN2,3)JSTART
      JEND=JSTART
      DO 5 L=1,JMAX-JSTART+1
4     DO 5 K=1,IMAX
      IF(DOP(K,L+JSTART-1) .GT. 0. .AND. DOP(K+1,L+JSTART-1)
    + .LT. 0.)THEN
      ISTART(L)=K+1
      ELSE IF(DOP(K,L+JSTART-1) .LT. 0. .AND.
    + DOP(K+1,L+JSTART-1) .GT. 0.)THEN
      IEND(L)=K
      GO TO 5
      ENDIF
5     CONTINUE
C 200   WRITE(DEVOUT,210)(ISTART(J),IEND(J),J=1,JMAX-JSTART+1)
 210   FORMAT(1X,2I5)
      CHALEN=(COORX(IEND(1),JEND)-COORX(ISTART(1),JSTART))*1.D-4
C  CALCULATE LD
      LD=(COORX(ISTART(1),JSTART)-COORX(ISMASK,JSTART))*1.D-6
      ILD=1
C       WRITE(DEVOUT,80)COORX(ISTART,JSTART),COORX(IEND,JEND)
C CALCULATE XJ
      DO 10 J=JSTART,JMAX
      IF(DOP(ISMASK-1,J) .GT. 0. .AND. DOP(ISMASK-1,J+1) .LT.
    + 0. ) THEN
      XJ=COORY(ISMASK-1,J)*1.D-6
      IXJ=1
      GO TO 15
      ENDIF
 10   CONTINUE
C CALCULATE PHI, PB
 15   DO 130 I=1,ISMASK
 110   DO 130 J=JSTART,JMAX
      IF(DOP(I,J) .LT. 0.)GO TO 120
      IF((DOP(I,J)-NC(I,J))/DOP(I,J) .GT. 0.1
    + .AND.  (DOP(I,J)-NC(I,J))/DOP(I,J) .LT. 1)THEN
      JNEDGE(I)=J
      ENDIF
      GO TO 130
 120   IF((ABS(DOP(I,J))-PC(I,J))/ABS(DOP(I,J)) .GT. 0.1
    + .AND.  (ABS(DOP(I,J))-PC(I,J))/ABS(DOP(I,J)) .LT. 1)THEN
      JPEDGE(I)=J
      ENDIF
 130   CONTINUE
C CALCUALTE PHIN
      ISO=1
      CALL AVAG(ISO,ISMASK,JNEDGE,VOL,COORX)
      PHIN=AVA
```

```
C CALCULATE PHIP
      CALL AVAG(ISO,ISMASK,JPEDGE,VOL,COORX)
      PHIP=AVA
      PB=PHIN-PHIP
      IPB=1
      PHI=2*ABS(PHIP)
      IPHI=1
      DO 60 I=1,IMAX
      JPOINT(I)=JSTART
 60   CONTINUE
C CALCULATE KP
      DO 66 I=1,IMAX
      DO 66 J=JSTART,JMAX
        MOBN(I,J)=MOBN(I,J)*UDEG/DSQRT(1+(MOBN(I,J)*UDEG
     +     *E(I,J)/VSAT)**2)
 66   CONTINUE
      CALL AVAG(ISTART,IEND,JPOINT,MOBN,COORX)
      UO=AVA
      IUO=1
      KP=UO*3.9*8.85D-14/TOX
      IKP=1
C CALCULATE VTO
      CALL INPISC
      DO 65 I=1,IMAX
      DO 65 J=1,JMAX
      NC0(I,J)=NC(I,J).
 65   CONTINUE
      CALL INPISC
      DO 70 I=1,IMAX
      DO 70 J=1,JMAX
      NCINV(I,J)=NC(I,J)
 70   CONTINUE
      CALL CALQINV(ISTART,JSTART,IEND,JEND,COORX,COORY,NC0)
      QINVO=QINV
      READ(DEVIN2,75)VGS
 75   FORMAT(F11.4)
      VTO=VGS-QINV*TOX/3.9/8.85D-14
      WRITE(DEVOUT,2)VTO,QINVO
      IVTO=1
      CALL AVAG(ISTART,IEND,JPOINT,VOL,COORX)
      PSIO=AVA
      WRITE(DEVOUT,59)VSAT
 59   FORMAT(1X,D16.3)
C     IF(LEVEL .EQ. 4) GO TO 1000
C CALCULATE GAMMA
      CALL INPISC
      CALL CALQINV(ISTART,JSTART,IEND,JEND,COORX,COORY,NC0)
      READ(DEVIN2,75)VBS
      READ(DEVIN2,75)VGS
      COX=3.9*8.85E-14/TOX
```

```
      SRT=(DSQRT((PHI-VBS))-DSQRT(PHI))
      CALL AVAG(ISTART,IEND,JPOINT,VOL,COORX)
      PSI=AVA
C QINVO AND QINV ARE POSITIVE IN HERE.
      QBD=(QINVO-QINV)/1.6D-19
      GAMMA=((PSIO-PSI)*COX+(QINVO-QINV))/COX/SRT
      IGAMMA=1
      VT1=VGS-QINV*TOX/3.9/8.85D-14
C PRINTOUT PSIO, PSI, QBD
      WRITE(DEVOUT,69) VGS,PSIO
 69   FORMAT(1X,'SURFACE POTENTIAL AT VGS= ',F6.3,'V  IS',
   +        F8.4,'V')
      WRITE(DEVOUT,79) VGS, VBS, PSI
 79   FORMAT(1X,'SURFACE PATENTIAL AT VGS= ',F6.3,'V  AND VBS= ',
   +        F6.3,'V  IS',F8.4,'V')
      WRITE(DEVOUT,89) QBD
 89   FORMAT(1X,'SUBSTRATE-INDUCED DEPLETION CHARGE IS ',
   +        D16.3,' CM-2')
      IF(LEVEL .EQ. 4)GO TO 1000
C CALCULATE JS
C     CALL AVAG(ISO+1,ISMASK,JPEDGE,JSAT,COORX)
C     JS=AVA
C     IJS=1
C CALCULATE LAMBDA
C  VMAX
      IF(LEVEL .NE. 1)THEN
      VMAX=VSAT/100.
      IVMAX=1
      ENDIF
 80   FORMAT(1X,3D17.5)
1000  IF(LEVEL .EQ. 4) THEN
      CALL INPISC
      DO 300 I=1,IMAX
      DO 300 J=JSATRT,JMAX
      MOBN(I,J)=MOBN(I,J)*UDEG/DSQRT(1+(MOBN(I,J)*
   + UDEG*E(I,J)/VSAT)**2)
 300  CONTINUE
      CALL AVAG(ISTART,IEND,JPOINT,MOBN,COORX)
      USO=AVA
C CALCULATE UOZ
      READ(DEVIN2,75)VGS
      UOZ=(UO/USO-1)/(VGS-VTO)
      CALL INPISC
      DO 320 I=1,IMAX
      DO 320 J=JSTART,JMAX
      MOBN(I,J)=MOBN(I,J)*UDEG/DSQRT(1+(MOBN(I,J)*
   +    UDEG*E(I,J)/VSAT)**2)
 320  CONTINUE
      CALL AVAG(ISTART,IEND,JPOINT,MOBN,COORX)
      USO=AVA
```

```
      READ(DEVIN2,75)VDS
      U1Z=(UO/USO-1)*CHALEN/VDS
      US=USO*(1+U1Z*VDS/CHALEN)
      CALL INPISC
      DO 330 I=1,IMAX
      DO 330 J=JSTART,JMAX
      MOBN(I,J)=MOBN(I,J)*UDEG/DSQRT(1+(MOBN(I,J)*
     +   UDEG*E(I,J)/VSAT)**2)
330   CONTINUE
      CALL AVAG(ISTART,IEND,JPOINT,MOBN,COORX)
      UZ=AVA
C      CALL INPISC
C      READ(DEVIN2,75)VBS1
C      READ(DEVIN2,75)VGS
C      CALL CALQINV(ISTART,JSTART,IEND,JEND,COORX,COORY,NC0)
C       VT1=VGS-QINV*TOX/3.9/8.85D-14
C      CALL INPISC
C      READ(DEVIN2,75)VBS2
C      READ(DEVIN2,75)VGS
C      CALL CALQINV(ISTART,JSTART,IEND,JEND,COORX,COORY,NC0)
C      VT2=VGS-QINV*TOX/3.9/8.85D-14
C CALCULATE K1,K2
      K1=GAMMA
      K2=-(VTO-VT1-K1*(DSQRT(PHI)-DSQRT(PHI-VBS)))/VBS
C      DENOM=DSQRT(PHI-VBS2)*(PHI-VBS1)-DSQRT(PHI-VBS1)*
C    +        (PHI-VBS2)
C      XT1=VT1+0.8-PHI
C      XT2=VT2+0.8-PHI
C      K1=(XT2*(PHI-VBS1)-XT1*(PHI-VBS2))/DENOM
C      K2=(XT2*DSQRT(PHI-VBS1)-XT1*DSQRT(PHI-VBS2))/DENOM
      ENDIF
      WRITE(DEVOUT,75)VT1,VT2,K1,K2
      RETURN
      END


      SUBROUTINE OUTPAR()
      IMPLICIT INTEGER(I-N)
      IMPLICIT DOUBLE PRECISION(A-H,O-Z)
      DOUBLE PRECISION KP,LAMBDA,IS,MJ,MJSW,JS,NSUB,
     +          NSS,NFS,LD,NEFF,KF,K1,K2
      CHARACTER FILIN*20,FILOUT*20,
     +      MODNAM*6,DEVTYP*4,PCHAR*9
      INTEGER*2 DEVIN,DEVOUT,DEVIN2
      COMMON /BLOCK1/LEVEL,VTO,KP,GAMMA,PHI,LAMBDA,RD,RS,CBD,CBS,
     +  IS,PB,CGSO,CGDO,CGBO,RSH,CJ,MJ,CJSW,MJSW,JS,TOX,NSUB,
     +  NSS,NFS,TPG,XJ,LD,UO,UCRIT,UEXP,UTRA,VMAX,NEFF,XQC,KF,AF,
     +  FC,DELTA,THETA,ETA,KAPPA,ILEVEL,IVTO,IKP,IGAMMA,IPHI,
     +  ILAMBDA,IRD,IRS,ICBD,ICBS,IIS,IPB,ICGSO,ICGDO,ICGBO,IRSH,
     +  ICJ,IMJ,ICJSW,IMJSW,IJS,ITOX,INSUB,INSS,INFS,ITPG,IXJ,ILD,
```

```
     +   IUO,IUCRIT,IUEXP,IUTRA,IVMAX,INEFF,IXQC,IKF,IAF,IFC,IDELTA,
     +   ITHETA,IETA,IKAPPA
      COMMON /BLOCK3/ DEVIN,DEVOUT,DEVIN2
     +  /BLOCK4/ FILIN,FILOUT,MODNAM,DEVTYP
     +  /BLOCK6/ IMAX,JMAX
      COMMON  /BLOCK15/UOZ,U1Z,US,UZ,K1,K2

      WRITE(DEVOUT,10)MODNAM,DEVTYP
10     FORMAT(' ','.MODEL',2X,A6,2X,A4)
20     FORMAT(' ','+',2X,A9,2X,1PE15.8)
30     FORMAT(' ','+',2X,A9,2X,I2)
      IF(ILEVEL.EQ.1)THEN
      PCHAR='LEVEL = '
      WRITE(DEVOUT,30)PCHAR,LEVEL
      ENDIF
      IF(LEVEL .EQ. 4)GO TO 100
      IF(IVTO.EQ.1)THEN
      PCHAR='VTO = '
      WRITE(DEVOUT,20)PCHAR,VTO
      ENDIF
      IF(IKP.EQ.1)THEN
      PCHAR='KP = '
      WRITE(DEVOUT,20)PCHAR,KP
      ENDIF
      IF(ILD .EQ. 1)THEN
      PCHAR='LD = '
      WRITE(DEVOUT,20)PCHAR,LD
      ENDIF
      IF(IXJ .EQ. 1)THEN
      PCHAR='XJ = '
      WRITE(DEVOUT,20)PCHAR,XJ
      ENDIF
      IF(IPB .EQ. 1)THEN
      PCHAR='PB = '
      WRITE(DEVOUT,20)PCHAR,PB
      ENDIF
      IF(IPHI .EQ. 1)THEN
      PCHAR='PHI = '
      WRITE(DEVOUT,20)PCHAR,PHI
      ENDIF
      IF(IGAMMA .EQ. 1)THEN
      PCHAR='GAMMA = '
      WRITE(DEVOUT,20)PCHAR,GAMMA
      ENDIF
      IF(IJS .EQ. 1)THEN
      PCHAR='JS = '
      WRITE(DEVOUT,20)PCHAR,JS
      ENDIF
      IF(ILAMBDA .EQ. 1)THEN
      PCHAR='LAMBDA = '
```

```
      WRITE(DEVOUT,20)PCHAR,LAMBDA
      ENDIF
      IF(IUO .EQ. 1)THEN
      PCHAR='UO = '
      WRITE(DEVOUT,20)PCHAR,UO
      ENDIF
      IF(ITOX .EQ. 1)THEN
      PCHAR='TOX = '
      TOX=TOX/100.
      WRITE(DEVOUT,20)PCHAR,TOX
      ENDIF
      IF(INSS .EQ. 1)THEN
      PCHAR='NSS = '
      WRITE(DEVOUT,20)PCHAR,NSS
      ENDIF
      IF(INSUB .EQ. 1)THEN
      PCHAR='NSUB = '
      WRITE(DEVOUT,20)PCHAR,NSUB
      ENDIF
      IF(IVMAX .EQ. 1)THEN
      PCHAR='VMAX = '
      WRITE(DEVOUT,20)PCHAR,VMAX
      ENDIF
      IF(INEFF .EQ. 1)THEN
      PCHAR='NEFF ='
      WRITE(DEVOUT,20)PCHAR,NEFF
      ENDIF
      IF(IUEXP .EQ. 1)THEN
      PCHAR='UEXP = '
      WRITE(DEVOUT,20)PCHAR,UEXP
      ENDIF
      IF(IUCRIT .EQ. 1)THEN
      PCHAR='UCRIT = '
      WRITE(DEVOUT,20)PCHAR,UCRIT
      ENDIF
      IF(IETA .EQ. 1)THEN
      PCHAR='ETA = '
      WRITE(DEVOUT,20)PCHAR,ETA
      ENDIF
      IF(ITHETA .EQ. 1)THEN
      PCHAR='THETA= '
      WRITE(DEVOUT,20)PCHAR,THETA
      ENDIF
100   PCHAR='PHIS= '
      WRITE(DEVOUT,20)PCHAR,PHI
      PCHAR='US= '
      WRITE(DEVOUT,20)PCHAR,US
      PCHAR='UZ= '
      WRITE(DEVOUT,20)PCHAR,UZ
      PCHAR='UOZ= '
```

```
      WRITE(DEVOUT,20)PCHAR,UOZ
      PCHAR='U1Z= '
      WRITE(DEVOUT,20)PCHAR,U1Z
      PCHAR='K1= '
      WRITE(DEVOUT,20)PCHAR,K1
      PCHAR='K2= '
      WRITE(DEVOUT,20)PCHAR,K2
      RETURN
      END


      SUBROUTINE UPCASE(LINE)
      INTEGER*2 I
      CHARACTER LINE*80,A*1
      DO 10 I=1,LEN(LINE)
      A=LINE(I:I)
      IF (ICHAR(A).GE.ICHAR('a').AND.ICHAR(A).LE.ICHAR('z'))THEN
      LINE(I:I)=CHAR(ICHAR(LINE(I:I))-ICHAR('a')+ICHAR('A'))
      ENDIF
10     CONTINUE
      RETURN
      END


      SUBROUTINE CALQINV(ISTART,JSTART,IEND,JEND,COORX,COORY,NC0)
      IMPLICIT INTEGER (I-N)
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
      INTEGER*2 DEVIN,DEVOUT,DEVIN2
      DOUBLE PRECISION VOL,NC,PC,QFN,QFP,COORX,COORY,COORYMAX,
     +   KP,LAMBDA,IS,MJ,MJSW,JS,NSUB,NSS,NFS,

     +   LD,NEFF,KF,DOP,MOBN,MOBP,JSAT,NC0
      DIMENSION VOL(100,100),NC(100,100),PC(100,100),QFN(100,100)
     +   ,QFP(100,100),COORX(100,100),COORY(100,100),Q(100,100),
     +    DOP(100,100),MOBN(100,100),MOBP(100,100)
     +   ,COORYMAX(100,100),E(100,100),JSAT(100,100),NC0(100,100)
     +   ,ISTART(100),IEND(100)
      COMMON /BLOCK1/ LEVEL,VTO,KP,GAMMA,PHI,LAMBDA,RD,RS,CBD,CBS,
     +   IS,PB,CGSO,CGDO,CGBO,RSH,CJ,MJ,CJSW,MJSW,JS,TOX,NSUB,NSS,NFS,
     +   TPG,XJ,LD,UO,UCRIT,UEXP,UTRA,VMAX,NEFF,XQC,KF,AF,FC,DELTA,
     +   THETA,ETA,KAPPA,ILEVEL,IVTO,IKP,IGAMMA,IPHI,ILAMBDA,IRD,IRS,
     +   ICBD,ICBS,IIS,IPB,ICGSO,ICGDO,ICGBO,IRSH,ICJ,IMJ,ICJSW,IMJSW,
     +   IJS,ITOX,INSUB,INSS,INFS,ITPG,IXJ,ILD,IUO,IUCRIT,IUEXP,IUTRA,
     +   IVMAX,INEFF,IXQC,IKF,IAF,IFC,IDELTA,ITHETA,IETA,IKAPPA
      COMMON /BLOCK5/VOL,NC,PC,QFN,
     +   QFP
      COMMON /BLOCK6/IMAX,JMAX
      COMMON /BLOCK7/DOP,E,QINV
      COMMON /BLOCK8/MOBN,MOBP,JSAT
      COMMON /BLOCK3/DEVIN,DEVOUT,DEVIN2
```

```
      QSUM=0.
      N=1
      J=JSTART
      DO 10 M=ISTART(1),IEND(1)
      COORY(M,J-1)=COORY(M,J)
10    CONTINUE
20    K=ISTART(N)
      L=IEND(N)
      COORX(K-1,J)=COORX(K,J)
      COORX(L+1,J)=COORX(L,J)
      IF(VOL(ISTART(N+1)+1,J+1) .LT. 0) GO TO 50
      DO 30 I=K,L
      Q(I,J)=(NC(I,J)-NC0(I,J))*(COORX(I+1,J)-COORX(I-1,J))
     + *(COORY(I,J+1)-COORY(I,J-1))*1.D-8/4.
      QSUM=Q(I,J)+QSUM
c     WRITE(DEVOUT,25)QSUM
25    FORMAT(1X,E12.5)
30    CONTINUE
      N=N+1
      J=J+1
      IF(J .GT. JMAX)THEN
      WRITE(DEVOUT,31)J
31    FORMAT(1X,I3)
      STOP
      ENDIF
      GO TO 20
50    M=ISTART(N+1)+1
      YEDGE=(VOL(M,J)*COORY(M,J+1)-VOL(M,J+1)*COORY(M,J))
     + /(VOL(M,J)-VOL(M,J+1))
      DO 60 M=K,L
      COORYMAX(M,J)=YEDGE
60    CONTINUE
      DO 70 I=K,L
      Q(I,J)=(NC(I,J)-NC0(I,J))*(COORX(I+1,J)-COORX(I-1,J))
     + *(COORYMAX(I,J)-(COORY(I,J)+COORY(I,J-1))/2.)*1.D-8/2.
      QSUM=Q(I,J)+QSUM
70    CONTINUE
      CHALEN=(COORX(IEND(1),JEND)-COORX(ISTART(1),JSTART))*1.D-4
      QINV=QSUM/CHALEN*1.6D-19
      RETURN
      END


      SUBROUTINE AVAG(IS,IE,JPOINT,VAR,CORDX)
      IMPLICIT INTEGER (I-N)
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
      DIMENSION JPOINT(100),VAR(100,100),CORDX(100,100)
      COMMON /BLOCK10/AVA
      SUM=0.
      DO 10 I=IS+1,IE-1
```

```
      SUM=SUM+VAR(I,JPOINT(I))*(CORDX(I+1,JPOINT(I+1))-
     +  CORDX(I-1,JPOINT(I-1)))/2.
      SUM=SUM+VAR(I,JPOINT(I))*(CORDX(I+1,JPOINT(I+1))-
     +  CORDX(I-1,JPOINT(I-1)))/2.
 10   CONTINUE
      SUM=SUM+VAR(IS,JPOINT(IS))*(CORDX(IS+1,JPOINT(IS+1))-
     +    CORDX(IS,JPOINT(IS)
     +  ))/2.+VAR(IE,JPOINT(IE))*(CORDX(IE,JPOINT(IE))-
     +    CORDX(IE-1,
     +  JPOINT(IE-1)))/2.
      AVA=SUM/(CORDX(IE,JPOINT(IE))-CORDX(IS,JPOINT(IS)))
      RETURN
      END



      PROGRAM MESGEN
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
      CHARACTER FILIN*20,FILOUT*20,
     +  BLANK*81
      INTEGER*2 DEVIN,DEVOUT
      COMMON /PAR/ VTH,VBI,BETA,B,ALPHA,XLAMBDA
      COMMON /BLOCK3/ DEVIN,DEVOUT
     +      /BLOCK4/ FILIN,FILOUT
      M=0
      BLANK=' '

C     INITIALIZE ALL THE DEFAULT PARAMETERS

      VPO=1.5
      VBI=0.6
      BETA=1.0E-04
      B=0.3
      ALPHA=1.5
      XLAMBDA=0.04

      PRINT *,'*************** MESGEN PROGRAM *******************'
      FILIN='MESGEN.IN'
      FILOUT='MESGEN.OUT'
      PRINT *,'OUTPUT FILE(DEFAULT:MESGEN.OUT):'
      READ(*,10)FILOUT
 10   FORMAT(A20)
      DEVIN1=3
      OPEN (UNIT=DEVIN, STATUS='OLD',FILE=FILIN)
      READ(DEVIN1,20)DEVOUT
 20   FORMAT(I2)
      OPEN(UNIT=DEVOUT,STATUS='NEW',FILE=FILOUT)
      READ (DEVIN1,25) IMAX
      READ (DEVIN1,25) JMAX
 25   FORMAT (I5)
```

```
      CALL INPISC()
      CALL CALPAR()
      WRITE(DEVOUT,21)
21     FORMAT(/,3X,'*MESGEN PROGRAM FOR SPICE3 MODEL PARAMETERS*',//)
      WRITE(DEVOUT,251)VTH,VBI,BETA,B,XLAMBDA,ALPHA
251    FORMAT(3X,'VTH=',f8.5,/,3X,'VBI=',f8.5,/,
     + 3X,'BETA=',E12.5,/,3X,'B=',f6.4,/,3X,
     + 'LAMBDA=',E12.5,/,3X,'ALPHA=',f8.5,/)
      CLOSE(DEVIN)
      CLOSE(DEVOUT)
      STOP
      END


      SUBROUTINE INPISC
      IMPLICIT INTEGER (I-N)
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
      CHARACTER LINE*81,KOOL*81
      INTEGER*2 N,I,J,DEVIN,DEVOUT
      CHARACTER FILIN*20,FILOUT*20
      DIMENSION COORX(100,100),COORY(100,100),
     +  DOP(100,100),Q(100,100),CJN(100,100)
      COMMON /BLOCK3/ DEVIN,DEVOUT
      COMMON /BLOCK4/ FILIN,FILOUT
      COMMON /BLOCK6/ IMAX,JMAX
      COMMON/BLOCK5/ VOL(100,100),RNC(100,100)
      COMMON /BLOCK7/Q,CJN
      COMMON /BLOCK9/COORX,COORY,DOP
      COMMON /BLOCK11/VSAT,RMOBO
      COMMON /INDIC/ M,RJC
      M=0
      DEVIN=4
       READ(DEVIN,1)FILIN
1      FORMAT(A20)
      OPEN(UNIT=DEVIN,STATUS='OLD',FILE=FILIN)
5      READ(DEVIN,10,END=30)LINE
10     FORMAT(A80)
      KOOL=' '
      I=1
      DO 20 N=1,LEN(LINE)
      IF((LINE(N:N).NE.' ').AND.(LINE(N:N).NE.'      '))THEN
      KOOL(I:I)=LINE(N:N)
      I=I+1
      ENDIF
20     CONTINUE
      CALL UPCASE(KOOL)
      IF(KOOL(1:13).EQ.'NODEVNPQFNQFP')THEN
      GO TO 60
      ELSE IF(KOOL(1:10).EQ.'NODEXCOORD') THEN
      GO TO 90
```

```
      ELSE IF(KOOL(1:7) .EQ. 'NODEQQA')THEN
      GO TO 180
      ELSE IF(KOOL(1:8) .EQ. 'NODE|JN|')THEN
      GO TO 210
      ELSE IF(KOOL(1:10) .EQ. 'LOG10(NI)=')THEN
      READ(DEVIN,35)RMOBO
      GO TO 25
      ELSE IF(KOOL(1:11) .EQ. 'P-MOBILITY=')THEN
      READ(DEVIN,35)VSAT
35    FORMAT(16X,D16.2)
      GO TO 25
      ELSE IF(KOOL(1:16).EQ.'ELECTRODEVOLTAGE') THEN
      READ(DEVIN,11)RJC
11    FORMAT(/,54X,D15.6)
      GO TO 25
      ELSE
      GO TO 5
      ENDIF
60    DO 65 I=1,IMAX
      DO 66 J=1,JMAX
50    READ(DEVIN,70,END=30)VOL(I,J),RNC(I,J)
70    FORMAT(8X,F10.5,E12.4)
66    CONTINUE
65    CONTINUE
      GO TO 25
40    FORMAT(1H ,A80)
90    READ(DEVIN,85)
85    FORMAT(/)
100   DO 110 K=1,IMAX
      DO 110 L=1,JMAX
120   READ(DEVIN,130) COORX(K,L),COORY(K,L),DOP(K,L)
130   FORMAT(5X,2E11.3,E12.3)
110   CONTINUE
      GO TO 25
180   DO 200 K=1,IMAX
      DO 200 L=1,JMAX
      READ(DEVIN,190)Q(K,L)
190   FORMAT(8X,E12.4)
200   CONTINUE
      GO TO 25
210   DO 211 K=1,IMAX
      DO 211 L=1,JMAX
      READ(DEVIN,212)CJN(K,L)
212   FORMAT(9X,E10.4)
211   CONTINUE
25    M=M+1
      IF(M .NE. 7)GO TO 5
30    CONTINUE
      RETURN
      END
```

```
      SUBROUTINE CALPAR()
      IMPLICIT INTEGER(I-N)
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
      DIMENSION  DOP(100,100),Q(100,100),COORX(100,100),COORY(100,100),
     +  JNEDGE(40),V(40),CJN(100,100)
      COMMON /PAR/ VTH,VBI,BETA,B,ALPHA,XLAMBDA
      COMMON/BLOCK5/ VOL(100,100),RNC(100,100)
      COMMON /BLOCK6/IMAX,JMAX
      COMMON /BLOCK7/Q,CJN
      COMMON /BLOCK9/COORX,COORY,DOP
      COMMON /BLOCK10/AVA
      COMMON /BLOCK11/VSAT,RMOBO
      COMMON /INDIC/ M,RJC
      READ(DEVIN1,*)XL
      READ(DEVIN1,*)XD
      READ(DEVIN1,3)ISMASK
3      FORMAT(I3)
       READ(DEVIN1,3)IDMASK
      K=0
      DO 12 I=ISMASK,IDMASK
       K=K+1
      DO 13 J=1,JMAX
      IF(RNC(I,J)/DOP(I,J).GT.0.1)THEN
      JNEDGE(K)=J-1
      GO TO 12
      ELSE
      ENDIF
13     CONTINUE
12     CONTINUE
      CALL AVAG(ISMASK,IDMASK,JNEDGE)
      VBI=AVA
      WRITE(6,200)VBI
200    FORMAT(/,3X,'**** VBI= *****',F8.4)
      BETA=RMOBO*13.1*8.854E-14/(2*XL*XD*1.0E-04)
      CALL CALDOP(ISMASK,1,IDMASK,JMAX,DOP,DOPN)
      VPO=1.6E-19*DOPN*XD**2*1.0E-08/(2*13.1*8.854E-14)
      WRITE(6,*)VPO
      K=0
      VTH=0
      DO 20 I=ISMASK,IDMASK
      K=K+1
      L=JNEDGE(K)+1
      JNEDGE(K)=L
      V(I)=0
      DO 21 J=L,JMAX
21     V(I)=V(I)+(DOP(I,J)+DOP(I,J-1))*(COORY(I,J)+
     +    COORY(I,J-1))*(COORY(I,J)-COORY(I,J-1))/4
      V(I)=1.6E-19*V(I)/(13.1*8.854E-06)
      VTH=V(I)+VTH
20     CONTINUE
```

```
      VTH=VTH/(IDMASK-ISMASK+1)
      WRITE(6,23)VTH,BETA
23     FORMAT(/,3X,'VTH=',F8.4,5x,'BETA=',E12.4)
      CALL CALDOP(ISMASK,1,IDMASK,JMAX,RNC,DOPN)
      TEMP=DOPN
      CALL CALDOP(ISMASK,1,IDMASK,JMAX,DOP,DOPN)
      B=TEMP/DOPN
      WRITE(6,*)B
      CALL INPISC
      READ(DEVIN1,*)VDS
      ISTART=ISMASK
      IDSTART=IDMASK
      CALL CALDOP(ISTART,1,IDTART,JMAX,CJN,DOPN)
      TEMP=DOPN
      CALL INPISC
      READ(DEVIN1,*)VDS
      CALL CALDOP(ISTART,1,IDTART,JMAX,CJN,DOPN)
      RLAMB=(DOPN-TEMP)/TEMP
      XLAMBDA=RLAMB
      WRITE(6,202)RLAMB
202    FORMAT(/,3X,'*** LAMBDA= ***',D12.5)
      CALL INPISC
      READ(DEVIN1,*)VGS
      READ(DEVIN1,*)VDS
      ALPHA=CURRENT*(1+B*(VGS+VTH))
      ALPHA=ALPHA/(VDS*(VGS+VTH)**2*BETA*(1+RLAMB*VDS))
      RETURN
      END


      SUBROUTINE UPCASE(LINE)
      INTEGER*2 I
      CHARACTER LINE*80,A*1
      DO 10 I=1,LEN(LINE)
      A=LINE(I:I)
      IF (ICHAR(A).GE.ICHAR('a').AND.ICHAR(A).LE.ICHAR('z'))THEN
      LINE(I:I)=CHAR(ICHAR(LINE(I:I))-ICHAR('a')+ICHAR('A'))
      ENDIF
 10    CONTINUE
      RETURN
      END


      SUBROUTINE AVAG(IS,IE,JPOINT)
      IMPLICIT INTEGER (I-N)
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
      DIMENSION JPOINT(100),COORX(100,100),COORY(100,100),DOP(100,100)
      COMMON /BLOCK10/AVA
      COMMON /BLOCK9/COORX,COORY,DOP
      COMMON/BLOCK5/ VOL(100,100),RNC(100,100)
```

```
      SUM=0.
      K=0
      DO 10 I=IS,IE-1
      K=K+1
      SUM=SUM+(VOL(I,JPOINT(K))+VOL(I+1,JPOINT(K+1)))/2*
     + (COORX(I+1,JPOINT(K+1))-COORX(I,JPOINT(K)))
 10   CONTINUE
      AVA=SUM/(COORX(IE,1)-COORX(IS,1))
      RETURN
      END


      SUBROUTINE CALDOP(ISTART,JSTART,IEND,JEND,RDOP,DOPN)
      IMPLICIT INTEGER (I-N)
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
      DIMENSION COORX(100,100),COORY(100,100),
     + RDOP(100,100),DOP(100,100)
       COMMON /BLOCK9/COORX,COORY,DOP
      QSUM=0.
      DO 10 I=ISTART+1,IEND-1
      DO 11 J=JSTART+1,JEND-1
      QSUM=QSUM+ABS(RDOP(I,J))*((COORX(I+1,J)+COORX(I,J))/2-
     + (COORX(I,J)+COORX(I-1,J))/2)*((COORY(I,J+1)+COORY(I,J))/2-
     + (COORY(I,J)+COORY(I,J-1))/2)*1D-8
 11   CONTINUE
 10   CONTINUE
      DO 12 I=ISTART+1,IEND-1
      QSUM=QSUM+ABS(RDOP(I,1))*((COORX(I+1,1)+COORX(I,1))/2-
     + (COORX(I,1)+COORX(I-1,1))/2)*((COORY(I,2)-COORY(I,1))/2)
     + *1D-8
      QSUM=QSUM+ABS(RDOP(I,JEND))*((COORX(I+1,JEND)+COORX(I,JEND))/2-
     + (COORX(I,JEND)+COORX(I-1,JEND))/2)*((COORY(I,JEND)-
     + COORY(I,JEND-1))/2)*1D-8
 12   CONTINUE
      DO 13 J=2,JEND-1
      QSUM=QSUM+ABS(RDOP(ISTART,J))*((COORY(ISTART,J)+
     + COORY(ISTART,J+1))/2-
     + (COORY(ISTART,J)+COORY(ISTART,J-1))/2)*
     + ((COORX(ISTART+1,J)-COORX(ISTART,J))/2)*1D-8
      QSUM=QSUM+ABS(RDOP(IEND,J))*((COORY(IEND,J)+
     + COORY(IEND,J+1))/2-
     + (COORY(IEND,J)+COORY(IEND,J-1))/2)*
     + ((COORX(IEND,J)-COORX(IEND-1,J))/2)*1D-8
 13   CONTINUE
      QSUM=QSUM+1D-08*(ABS(RDOP(ISTART,1))*(COORX(ISTART+1,1)-
     + COORX(ISTART,1))/2*(COORY(ISTART,2)-COORY(ISTART,1))/2+
     + ABS(RDOP(IEND,1))*(COORX(IEND,1)-
     + COORX(IEND-1,1))/2*(COORY(IEND,2)-COORY(IEND,1))/2+
     + ABS(RDOP(ISTART,JEND))*(COORX(ISTART+1,JEND)-
     + COORX(ISTART,JEND))/2*(COORY(ISTART,JEND)-COORY
```

```
+ (ISTART,JEND-1))/2+
+ ABS(RDOP(IEND,JEND))*(COORX(IEND,JEND)-
+ COORX(IEND-1,JEND))/2*(COORY(IEND,JEND)-COORY(IEND,JEND-1))/2)
  DOPN=QSUM*1d8/(COORX(IEND,1)-COORX(ISTART,1))/
+ (COORY(ISTART,JEND)-COORY(ISTART,1))
  RETURN
  END
```

References

[1.1] R. K. Cavin III, L. W. Sumney, and R. M. Burger, "The Semiconductor Research Corporation: cooperative research," *Proc. IEEE,* vol. 77, pp. 1327-1344, Sep. 1989.

[1.2] R. J. Sokel and D. B. Macmillen, "Practical integration of process, device, and circuit simulation," *IEEE Trans. Electron Devices,* vol. ED-32, pp. 2110-2116, Oct. 1985.

[1.3] T. Shima, "Device and circuit simulator integration techniques," in *Process and Device Modeling,* W. L. Engl (Editor), Elsevier Science Publisher B. V., North-Holland, 1986, pp. 433-459.

[1.4] J. G. Rollins and J. Choma, Jr, "Mixed mode PISCES-SPICE coupled circuit and device solver," *IEEE Trans. Computer-Aided Design,* vol. CAD-7, pp. 862-867, Aug. 1988.

[1.5] K. Mayraram and D. O. Pederson, "CODECS: a mixed-level device and circuit simulator," *Proc. IEEE Custom Integrated Circuits Conf.,* pp. 112-115, 1988.

[2.1] D. A. Antoniadis, S. E. Hansen, R. W. Dutton, and A. G. Gonzalez, "SUPREM I - a program for IC process modeling and simulation," Stanford Electronics Lab. Stanford University, Stanford, CA, Tech. Rep. 5019-1, May 1977.

[2.2] D. A. Antoniadis and R. W. Dutton, "Models for computer simulation of complete IC fabrication process," *IEEE Trans. Electron Devices,* vol. ED-26, pp. 490-500, Apr. 1979.

[2.3] C. P. Ho, J. D. Plummer, S. E. Hansen, and R. W. Dutton, " VLSI process modeling - SUPREM III," *IEEE Trans. Electron Devices,* vol. ED-30, pp. 1438-1453, Nov. 1983.

[2.4] M. W. Law, C. S. Rafferty, and R. W. Dutton, "SUPREM IV user's manual," Integrated Circuits Lab., Stanford University, Stanford, CA, Tech. Rep., Dec. 1988.

[2.5] M. D. Deal, S. E. Hansen, and T. W. Sigmon, "SUPREM 3.5 - process modeling of GaAs integrated circuit technology," *IEEE Trans. Computer-Aided Design,* vol. CAD-8, pp. 939-951, Sep. 1989.

[2.6] D. Chin, M. Kump, H. Lee, and R. W. Dutton, "Process design using two-dimensional process and device simulators," *IEEE Trans. Electron Devices,* vol. ED-29, pp. 336-340, Feb. 1982.

[2.7] B. R. Penumalli, "A comprehensive two-dimensional VLSI process simulation program, BICEPS," *IEEE Trans. Electron Devices,* vol. ED-30, pp. 986-992, Sep. 1983.

[2.8] W. G. Oldham, S. N. Nangaonka, A. R. Neureuther, and M. O'Toole, "A general simulator for VLSI lithography and etching processes: part I - application to projection lithography," *IEEE Trans. Electron Devices,* vol. ED-26, pp. 717-722, Apr. 1979.

[2.9] W. G. Oldham, A. R. Neureuther, C. Sung, J. L. Reynolds, and S. N. Nandgaonkar, "A general simulator for lithography and etching processes: part II - application to deposition and etching," *IEEE Trans. Electron Devices,* vol. ED-27, pp. 1455-1459, Aug. 1980.

[2.10] M. R. Pinto, C. Rafferty, and R. W. Dutton, "PISCES-II: Poisson continuity equation solver," *Stanford Electronics Lab., Stanford Univ., Tech. Rep.,* 1984.

[2.11] S. Selberher, A. Schutz, and H. W. Potzl, "MINIMOS - a two-dimensional MOS transistor analyzer," *IEEE Trans. Electron Devices,* vol. ED-27, pp. 1540-1550, Aug. 1980.

[2.12] L. W. Nagel, "SPICE2: A computer program to simulate semiconductor circuits," *Electron. Res. Lab. Memo ERL-M520,* University of California, Berkeley, May 1975.

[2.13] T. Quarles, A. R. Newton, D. O. Pederson, and A. Sangiovanni-Vincentelli, *SPICE-3C1 User's Guide,* Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, April 1989.

[3.1] R. A. Hughes and J. D. Schott, "The future of automation for high-volume wafer fabrication and ASIC manufacturing," *Proc. IEEE*, vol. 74, pp. 1775-1793, Dec. 1986.

[3.2] E. Khalily, P. H. Decker, and D. A. Teegarden, "TECAP2: An interactive device characterization and model development system," *IEEE Inter. Conf. on Computer-Aided Design*, pp. 149-151, Nov. 1984.

[3.3] The TECAP-3B Manual, Hewlett-Packard Company, 1987.

[3.4] K. Doganis and D. L. Scharfetter, "General optimization and extraction of IC devices model parameters," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1219-1228, Sep. 1983.

[3.5] B. J. Sheu, "MOS transistor modeling and characterization for circuit simulation," *Electron. Res. Lab. Memo ERL-M85/22*, University of California, Berkeley, Oct. 1985.

[3.6] M.-C. Jeng, B. J. Sheu, and P. K. Ko, "BSIM parameter extraction--algorithms and user's guide," *Electron. Res. Lab. Memo ERL-M85/79*, University of California, Berkeley, Oct. 1985.

[3.7] S. Selberherr, A. S. Schutz, and H. W. Potzl, "MINIMOS 3: A MOSFET simulator that includes energy balance," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 1074-1078, May 1987.

[3.8] S. R. Nassif, A. J. Strojwas, and S. W. Director, "FABRICS II: A statistically based IC fabrication process simulator," *IEEE Trans. Computer-Aided Des.*, vol. CAD-3, pp. 40-46, Jan. 1984.

[3.9] S. R. Nassif, A. J. Strojwas, and S. W. Director, "FABRICS II, A statistical simulator of the IC fabrication process: user's manual," *SRC-CMU Center for Computer-Aided Design*, 1983.

[3.10] C.-P. Wan and B. J. Sheu, "Algorithms and modeling techniques for circuit simulation in computer integrated manufacturing," *Proc. IEEE Inter. Symposium on Circuits and Systems*, pp. 893-896, Portland, OR, May 1989.

[4.1] C.-P. Wan, B. J. Sheu, and S.-L. Lu, "Device and circuit simulation interface for an integrated VLSI design environment," *IEEE Trans. Computer-Aided Design*, vol. CAD-7, pp. 998-1004, Sep. 1988.

[4.2] A. Vladimirescu and S. Liu, "The simulation of MOS integrated circuits using SPICE2," *Electron. Res. Lab. Memo ERL-M80/7*, University of California, Berkeley, Oct. 1980.

[4.3] H. Statz et. al, " GaAs FET device and circuit simulation in SPICE," *IEEE Trans. Electron. Devices*, vol. ED-34, pp. 160-169, Feb. 1987.

[4.4] A. S. Grove, B. E. Deal, E. H. Snow, and C. T. Sah, "Investigation of thermally oxidized silicon surfaces using metal-oxide-semiconductor structures," *Solid State Electronics*, vol. 8, pp. 145-163, Feb. 1965.

[4.5] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, Wiley, New York, 1977, p. 325.

[4.6] D. A. Hodges and L. A. Rowe, "Information management for CIM," in *Advanced Research in VLSI*, Proc. 1987 Stanford Conf. (Paul Losleben Ed.) The MIT press.

[4.7] C.-P. Wan and B. J. Sheu, "A new method to determine geometrical dependences of submicron MOS transistor parameters," *IEE Proceedings-G*, 1990.

[4.8] D. A. Hodges, "Opportunities in computer integrated manufacturing," *Proc. 25th ACM/IEEE Design Automation Conf.*, pp. 82-83, Anaheim, CA, June 1988.

[4.9] M. C. Hsu, and B. J. Sheu, "Inverse-geometry dependence of MOS transistor electrical parameters," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. CAD-6, pp. 582-585, July 1987.

[4.10] P. J. Tsang, S. Ogura, and W. W. Walker, J. F. Shepard, and D. L. Critchlow, "Fabrication of high-performance LDDFET's with sidewall space technology," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 590-596, Apr. 1982.

[5.1] B. J. Sheu, C.-P. Wan, C.-C. Shih, W.-J. Hsu, and M. C. Hsu, "Determination of process-dependent critical SPICE parameters for application-specific ICs," *Proc. IEEE Inter. Conf. on Microelectronic Test Structures*, pp. 73-78, Long Beach, CA, Feb. 1988.

[5.2] H. Schichman and D. A. Hodges, "Modeling and simulation of insulated-gate field effect transistor switching circuits," in *IEEE Jour. Solid-State Circuits*, vol. SC-3, pp. 285-289, Sep. 1968.

[5.3] G. Baum and H. Beneking, "Drift velocity saturation in MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-17, pp. 481-482, June 1970.

[5.4] D. Frohman-Bentchkowsky, "On the effect of mobility variation on MOS device characteristics," *Proc. IEEE*, vol. 56, pp. 217-218 , Feb. 1968.

[5.5] D. E. Ward, "Charge-based modeling of capacitance in MOS transistor," Ph. D. Dissertation, Integrated Circuit Laboratory, Stanford University, June 1981.

[5.6] J. E. Meyer, "MOS models and circuit simulation," *RCA Review*, vol. 32, pp. 42-63, Mar. 1971.

[5.7] B. J. Sheu, D. L. Scharfetter, P. K. Ko, and M.-C. Jeng, "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE Jour. of Solid-State Circuits*, vol. SC-22, pp. 558-566, 1987.

[5.8] S.-J. Wang, J.-Y. Lee, and C.-Y. Chang, "An efficient and reliable approach for semiconductor device parameter extraction," *IEEE Trans. Computer-Aided Design*, vol. CAD-5, pp. 170-179, Jan. 1986.

[5.9] P. Tomovic, *Sensitivity Analysis of Dynamic Systems*, New York: McGraw-Hill, 1963.

[6.1] C.-P. Wan and B. J. Sheu, "Temperature Dependence Modeling for MOS VLSI circuit simulation," *IEEE Trans. Computer-Aided Design*, vol. CAD-8, pp. 1065-1073, Oct. 1989.

[6.2] A. F. Franz and G. A. Franz, "BAMBI--A design model for power MOSFET's," *IEEE Trans. Computer-Aided Design*, vol. CAD-4, pp. 177-189, July 1985.

[6.3] HSPICE User Guide, Meta-Software Inc., 1989.

[6.4] J. White and A. L. Sangiovanni-Vincentelli, "RELAX2: A new waveform relaxation approach for the analysis of LSI MOS circuits," Proc. IEEE Inter. Symposium on Circuits and Systems, Newport Beach, CA, May 1983.

[6.5] R. A. Saleh, J. E. Kleckner, and A. R. Newton, "Iterated timing analysis and SPLICE1," Proc. IEEE Inter. Conf. on Computer-Aided Design, Santa Clara, CA, Sep. 1983.

[6.6] P. Yang and P. K. Chatterjee, "SPICE modeling for small geometry MOSFET circuits," *IEEE Trans. Computer-Aided Design*, vol. CAD-1, pp. 169-182, Oct. 1982.

[6.7] C.-P. Wan, J.-C. Lee, and B. J. Sheu, "SPICE Temperature modeling for VLSI design using the Level-4 model," *Proc. Inter. Symposium on VLSI Technology, Systems, and Applications*, pp. 111-115, Taipei, Taiwan, May 1989.

[6.8] S. K. Tewksbury, "N-channel enhancement-mode MOSFET characteristics from 10 to 300 K," *IEEE Trans. Electron Devices*, vol. ED-28, pp. 1519-1529, Dec. 1981.

[6.9] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley-Interscience, 1981, p. 15 and p. 452.

[6.10] F. M. Klaassen, "Compact MOSFET modeling," in *Process and Device Modeling*, ed. W. L. Engl, Amsterdam: Elsevier Science Publisher, 1986, pp. 393-412.

[6.11] C. Jacoboni, C. Canali, G. Ottaviani, and A. A. Quaranta, "A review of some charge transport properties of silicon," *Solid State Electron.*, vol. 20, pp. 77-89, Feb. 1977.

[B-1] K. Tereda and H. Muta, "A new method to determine effective MOS-FET channel length," *Japan. J. Appl. Phys.*, vol. 18, pp. 953-959, May 1979.

[B-2] J. Chern, P. Chang, R. Motta, and N. Godinho, "A new method to determine MOSFET channel length," *IEEE Electron Device Lett.*, vol. EDL-1, pp. 170-173, Sept. 1980.

[B-3] K. Peng and M. Afromowitz, "An improved method to determine MOSFET channel length," *IEEE Electron Device Lett.*, vol. EDL-3, pp. 360-362, Dec. 1982.

[B-4] B. J. Sheu and P. K. Ko, "A capacitance method to determine channel lengths for conventional and LDD MOSFET's," *IEEE Electron Device Lett.*, vol. EDL-5, pp. 491-493, Nov. 1984.

[B-5] J. Whitfield, "A modification on 'An improved method to determine MOSFET channel length'," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 109-110, Mar. 1985

[B-6] G. J. Hu, C. Chang, and Y.-T. Chia, "Gate-voltage-dependent effective channel length and series resistance of LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 2469-2475, Dec. 1987.

[B-7] Y.-R. Ma and K. L. Wang, "A new method to electrically determine effective MOSFET channel width," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 1825-1827, Dec. 1982.

[B-8] B. J. Sheu and P. K. Ko, "A simple method to determine channel widths for conventional and LDD MOSFET's," *IEEE Electron Device Lett.*, vol. EDL-5, pp. 485-486, Nov. 1984.

[B-9] C.-P. Wan, H. Yang, and B. J. Sheu, "A new method to determine effective channel widths of MOS transistors for VLSI device design," *Proc. IEEE Inter. Conf. on Microelectronic Test Structures*, San Diego, Mar. 1990.