USC–SIPI REPORT #225

BSIM_plus: An Advanced MOS Transistor Model for VLSI Circuits

by

Sudhir M. A. M. Gowda

November 1992

Signal and Image Processing Institute
UNIVERSITY OF SOUTHERN CALIFORNIA
Department of Electrical Engineering-Systems
3740 McClintock Avenue, Room 400
Los Angeles, CA 90089-2564 U.S.A.

Dedication

I dedicate this dissertation to my parents, Appaji Muniswamy Gowda and Shantha Devi Muniswamy Gowda.

Acknowledgments

I am deeply grateful to my research advisor, Professor Bing Sheu, for his generous guidance, encouragement, and support throughout these years of graduate study. I am also grateful to Professor Clarence Crowell and Professor Wlodek Proskurowski for providing valuable discussions and serving on my dissertation committee. I would like to thank Professor C. S. Raghavendra and Professor Sarma Sastry for also serving on my Ph.D. guidance committee.

I am very grateful to Professor Hans Kuehl, Chairman of EE-Electrophysics Department, Professor Melvin Breuer, Chairman of EE-Systems Department, and Professor Leonard Silverman, Dean of the School of Engineering for providing the excellent research environment at USC. I also thank Ms. Ramona Gordon, Senior Administrative Assistant in EE-Electrophysics Department for her patient and efficient assistance. The support of several research organizations including the DARPA-sponsored National Center for Integrated Photonic Technology (NCIPT), the Signal and Image Processing Institute (SIPI), the Center for Photonic Technology (CPT), the Center for Neural Engineering (CNE), and the Information Sciences Institute (ISI) is appreciated.

Valuable industrial support and funding for this research was provided by Dr. Chang-Gyu Hwang, Executive Director of Memory Division, Dr. Dae-Je Chin, and Mr. Yoon-Woo Lee, the Vice President of Kihung R&D Center of Samsung Electronics Co. Supplementary support was also

provided by Dr. James Cable, Advanced Technology Manager, and Mr. Mark Miscione, VHSIC Program Manager of TRW Electronic Systems Group. Assistance from Dr. George Lewicki and Mr. Cesar Pina, former and current Directors of the MOSIS Service of USC/Information Sciences Institute at Marina del Rey, CA, and other members of the institute are also highly appreciated.

I am very grateful to the previous graduates from the VLSI Signal Processing Laboratory for their help, encouragement, and friendship. I would like to thank Dr. Bang Lee, Dr. Ji-Chien Lee, and Dr. Chung-Ping Wan for valuable discussions. I am very grateful to Dr. Wen-Jay Hsu for his help on circuit reliability studies. My colleagues made my job of managing the VLSI Signal Processing laboratory very pleasant and enjoyable during 1991-1992. Professor Bing Sheu serves as the Laboratory Director. Important discussions with Mr. Joongho Choi, Ms. Chia-Fen Chang, and Mr. Sa-Hyun Bang are greatly appreciated. I would also like to thank Mr. Oscal Chen for coordinating the computing facility. Mr. Chen-Hao Chang's efforts in device characterization and circuit simulation were very helpful.

I am eternally grateful to my parents, Shantha Devi M. Gowda and A. Muniswamy Gowda, and my sisters, Veena Ganesh and Malathi Lingaraju, for their love and support. I cannot adequately express my appreciation and gratitude for the love, inspiration, and encouragement of my wife, Poornima Raghu S. Gowda, who is currently pursuing her Ph.D. degree in the Center for Applied Mathematical Sciences, Department of Mathematics, at USC.

The research was partially supported by National Science Foundation under Grant MIP-8710825, by DARPA under Contract MDA 972-90-C-0037, by DARPA under Contract N00140-87-C-9263, by Samsung Electronics Company and by TRW, Inc. Additional industrial support was provided by Meta-Software, Inc., and AT&T Bell Laboratories.

Table of Contents

List of Tables

List of Figures

Abstract

The BSIM_plus MOS transistor model is developed for design and simulation of analog and digital very large-scale integration (VLSI) circuits in sub-half-micron technologies for advanced signal processing, parallel computing, and telecommunication applications. A compact parameter set is created to characterize transistors and achieve continuity of the drain current and its derivatives. Advanced transistor modeling techniques are used for critical quantities including the threshold voltage and carrier mobility. Effects of non-uniform substrate doping and drain-induced barrier lowering are included in the threshold voltage expression, along with narrow-channel effects. Mobility reduction due to the transverse and lateral electric fields is also included. This model includes consistent charge and capacitance expressions that achieve charge conservation an high accuracy. A built-in substrate current expression serves the purposes of predicting circuit performance and reliability. Temperature and noise effects are included. The pseudo-boundary method is used to extend the use of a parameter set over the whole design space. This improves simulation results for circuits using large transistors such as digital drivers and analog voltage references, as well as for the prediction of circuit performance using next-generation technologies.

The BSIM_plus model is implemented in a modified version of the SPICE-3 circuit simulator from University of California, Berkeley. Parameter values can be extracted using a modified version of the SUXES extraction program from Stanford University. Simulation results agree well with

measurement data of transistors from sub-half-micron technologies of TRW Inc. and Samsung Electronics Co. Simulation results of VLSI circuits including self-timed adder, asynchronous master-slave latch, memory circuitry and operational amplifiers are presented. The required computing time and convergence properties of the simulation are compared by using the BSIM_plus model and various built-in MOS models in the SPICE circuit simulator. The convergence property of this is greatly enhanced due to the improved smoothness of the device characteristics. The BSIM_plus model functions as the cornerstone of an integrated simulation environment for advanced VLSI circuits.

Chapter 1

Introduction

Very large-scale integration (VLSI) circuits fabricated by metal-oxide-semiconductor (MOS) technologies are widely used in industry to implement high-performance computing, signal processing and telecommunication systems. The emergence of CMOS as the main fabrication technology over the past decade has been accompanied by a reduction in feature size from 2.0-μm to 0.5-μm, an increase in chip area from 50 mm^2 to 2000 mm^2, an increase in the number of transistors from 100,000 to 256 million for memories and from 50,000 to over 2 million in microprocessors, a drop in the on-chip gate delay from 1 nano-second to 10 pico-second and an increase in the chip clock frequency from 10 MHz to over 200 MHz [1.1]. In the competitive industrial environment, efficient design automation is invaluable in ensuring that high-quality products are developed within a short period of time. In such an environment, circuit and system designs can take place simultaneously with continuous technology improvement. This requires a closer relationship in the vertical direction from the device-level simulation through the circuit design level to the system-level simulation. In recent years, concurrent engineering has been replacing traditional isolated design and manufacture philosophies.

Fabrication technologies have progressed rapidly and the minimum feature sizes used in industrial processes have shrunk from 2 μm in the early 1980s to less than 0.4 μm in 1992, and 0.1-μm technologies will be available

by the year 2000 [1.2]. The level of circuit integration on a single chip has been greatly increased by new lithography and etching techniques [1.3-1.5]. The evolution of silicon integrated-circuit technologies used in the fabrication of semiconductor memories over the past decade and projected future direction are shown in Fig. 1.1.

Advanced signal-processing circuits and information-reasoning systems can now be implemented in sub-half-micron technologies to achieve high-speed performance [1.6-1.10]. A 0.4-μm double-poly double-metal CMOS technology was used to fabricate the 64-Mbit DRAM chip with 33-ns access time that was reported in 1991 [1.6]. Iino et al. [1.7] reported a single-chip microcomputer capable of 289 million floating-point operations-per-second (MFLOPS) that was fabricated using a 0.5-μm triple-metal CMOS technology. The chip could operate at a clock rate of 70 MHz, at a power supply of 3.3 V, and is constructed using a single instruction-stream multiple data-stream (SIMD) architecture. Toyokura et al. [1.8] presented a 2 giga-operations-per-second (GOPS), 60-MHz video digital signal processor with a vector-pipeline architecture for video coding/decoding (CODEC) systems, that was designed and fabricated in a 0.8-μm double-metal CMOS technology. In [1.9], Dobberpuhl et al. described a RISC-style microprocessor chip that operated at up to 200 MHz and implemented a 64-bit architecture that was fully pipelined and capable of issuing two instructions per clock cycle. The chip contained over 1.5 million transistors and was fabricated in a 0.5-μm double-metal CMOS technology. Innovative system-level technologies are being developed to integrate these high-performance components. Multi-chip

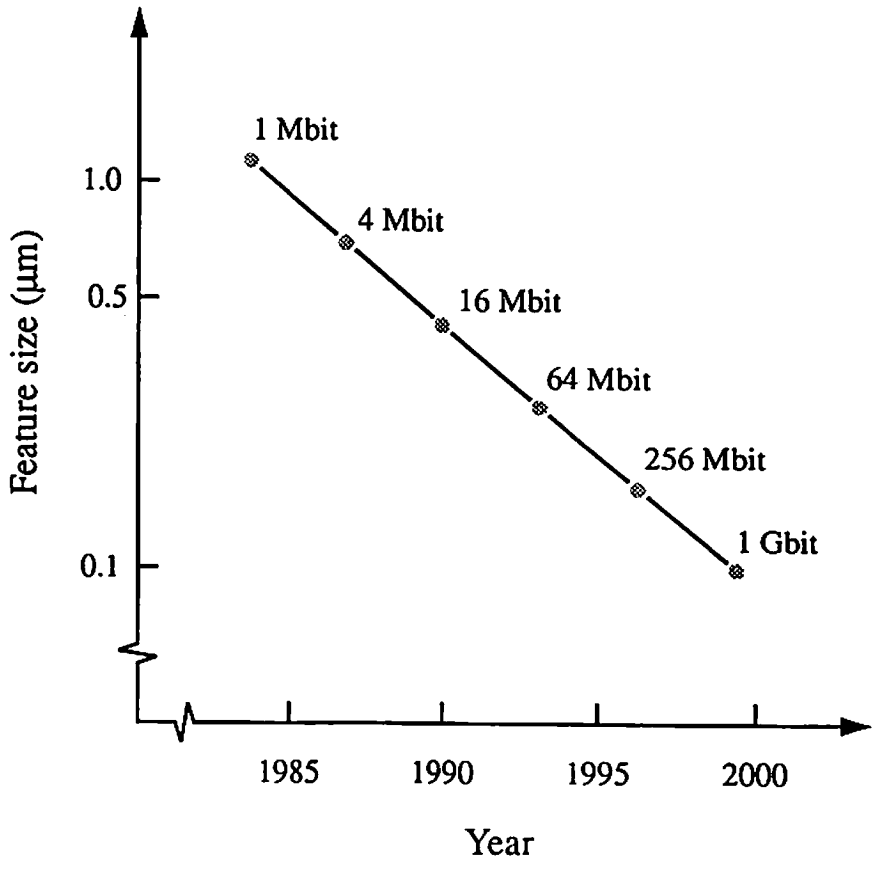


Fig. 1.1 Advances in fabrication technologies used for mass-production of CMOS dynamic memories [1.2].

modules can greatly reduce the noise and speed costs of communications between chips. Optical communication technologies are being heralded as the future of inter-processor communications, spurring considerable research into optoelectronic circuits using compound semiconductor materials [1.10, 1.11].

The increased use of sub-half-micron technologies has created new challenges for researchers in VLSI hardware design, high-performance circuit simulation, and microelectronic system design. At the transistor level, detailed investigation of small-geometry effects on the behavior of transistors is required. Effects of coupling between interconnections and neighboring devices can be more significant due to compactness of the circuit [1.12]. The degradation of device behavior with time of operation can be more significant due to higher electrical stresses in the channel region of MOS transistors. At the circuit design level, accurate modeling of transistors is urgently needed so that special features of advanced technologies can be exploited to the greatest extent. Desirable features of the model include a compact set of parameters, continuity of the drain current and its derivatives across different regions of operation, and the ability to use a single parameter set over a large geometric design space. BiCMOS technologies and circuits are being increasingly used because of the ability to exploit advantages of both bipolar and MOS transistors [1.13, 1.14]. At the system design level, new architectures are required in order to utilize advanced technologies effectively and extend boundaries of achievable performance. Advanced computer architectures are likely to use superpipelined multiprocessors with

distributed memories and optical interconnections [1.15-1.17]. Simultaneous efforts at the device, circuit and system levels are essential in order to achieve goals such as those outlined by the Committee on Physical, Mathematical and Engineering Sciences of the National Science Foundation [1.18], which are shown in Fig. 1.2.

The main components of an advanced VLSI design environment are shown in Fig. 1.3. Due to short prototype development time, device/process simulators such as SUPREM, SAMPLE and PISCES from Stanford University [1.19,1.20] can be used to analyze the effects of adjusting process variables, and to predict detailed device behavior. Device simulators can be used to generate circuit-level parameters so that simulation can be performed for prediction of circuit performance. This link between device and circuit simulators enables optimization of fabrication processes based on circuit performance. The core of the VLSI simulation environment contains circuit simulators such as SPICE from U.C. Berkeley [1.21,1.22], which use models of discrete devices such as transistors to predict the detailed electrical behavior of analog and digital circuits. The model expressions calculate the terminal voltage and current waveforms of devices based on model parameters. Several commercial circuit simulators are based upon the SPICE program including HSPICE from Meta-Software Inc. [1.23] and PSPICE from Microsim Corp. [1.24]. The use of macro-models increases the efficiency of these detailed circuit simulators. Some circuit simulators such as SPLICE from U.C. Berkeley [1.25] and iSPLICE from Univ. of Illinois [1.26], can perform simulation of mixed-signal circuits that contain substantial analog and digital

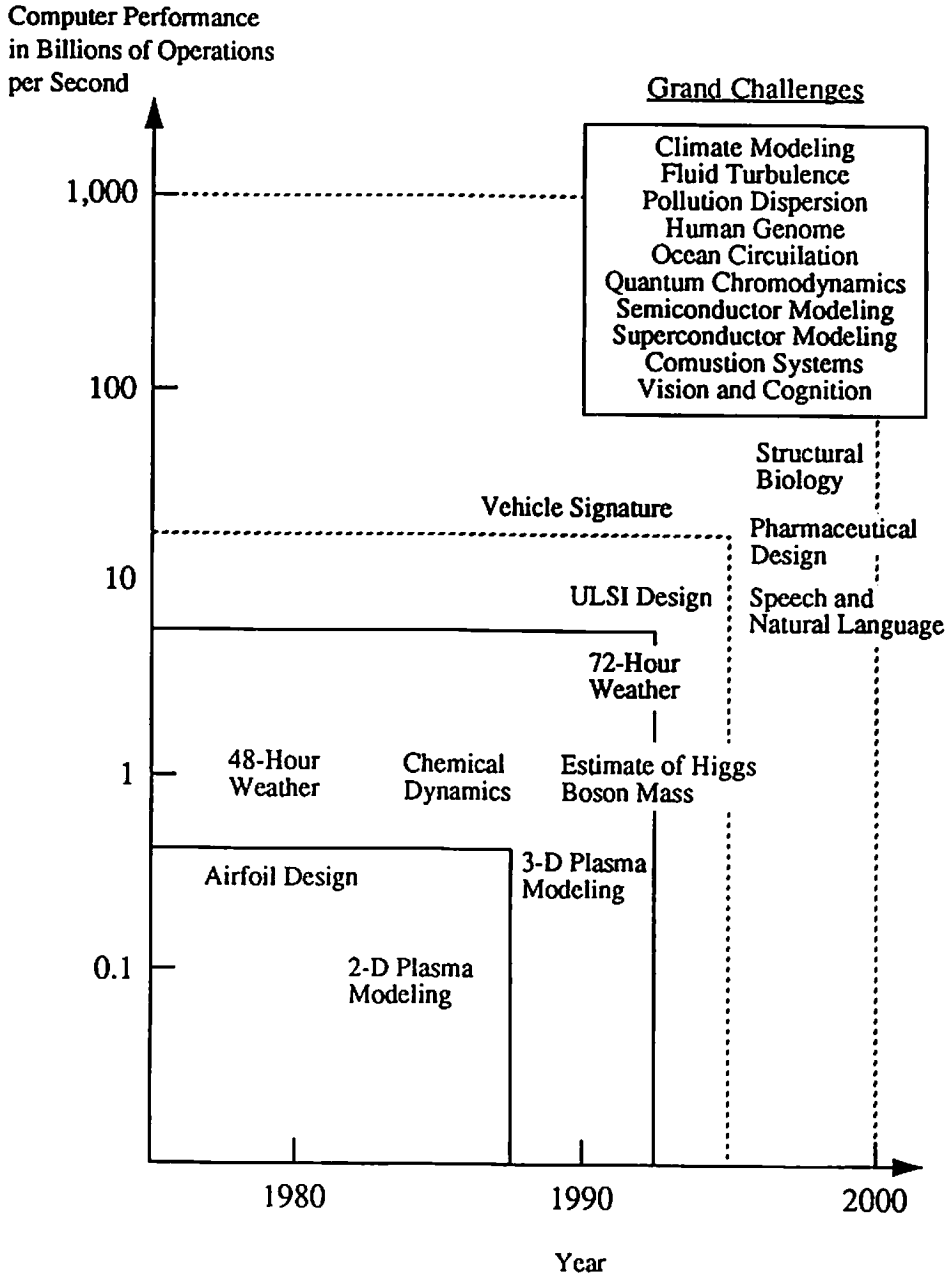


Fig. 1.2 Performance requirements for Grand Challenge problems [1.18].

circuitry. Other circuit simulators such as RELAX from U.C. Berkeley [1.27] and AWESIM from Carnegie Mellon University [1.28] use waveform relaxation techniques to speed up simulation tasks. In addition to simulation results of the freshly manufactured circuit, the designer may require information about the degraded performance of a circuit after it has operated for some period of time, since the use of extremely small feature sizes causes concerns of transistor and interconnection reliability. Reliability simulators such as RELY from University of Southern California [1.29], BERT from U.C. Berkeley [1.30], and iSMILE from Univ. of Illinois, can be used to predict the lifetime of circuits based on technology-dependent degradation parameters. Reliability simulation results can be used to modify circuit designs for reliability enhancement before actually committing the circuit to fabrication. Reliability predictions are also useful in determining warranties to be given to customers using electronic products. At the highest level of abstraction in the simulation environment, logic and timing simulators use behavioral models of the circuit to predict and verify the functionality and speed performance of electronic sub-systems or systems [1.32-1.34]. Behavioral models can be constructed from simulated data obtained by detailed circuit simulation. The circuit simulator at the core of the VLSI simulation environment and the individual device models that it contains are extremely important. Results from the circuit simulator affect crucial decisions that are made during architectural specification, circuit design, and chip fabrication. Accurate and efficient MOS transistor models are keys to the successful operation of such VLSI simulation environments.

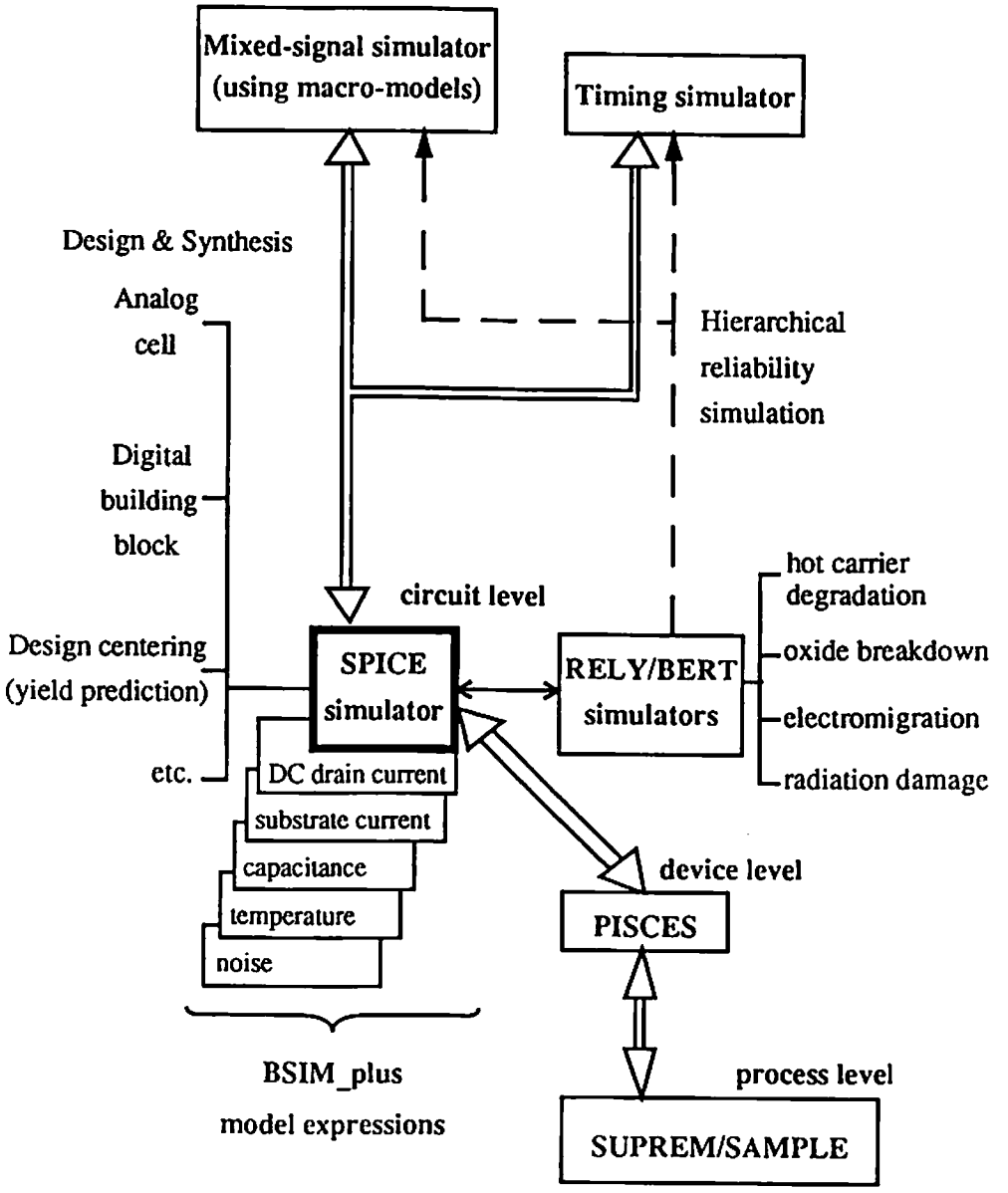


Fig. 1.3 An advanced VLSI design environment.

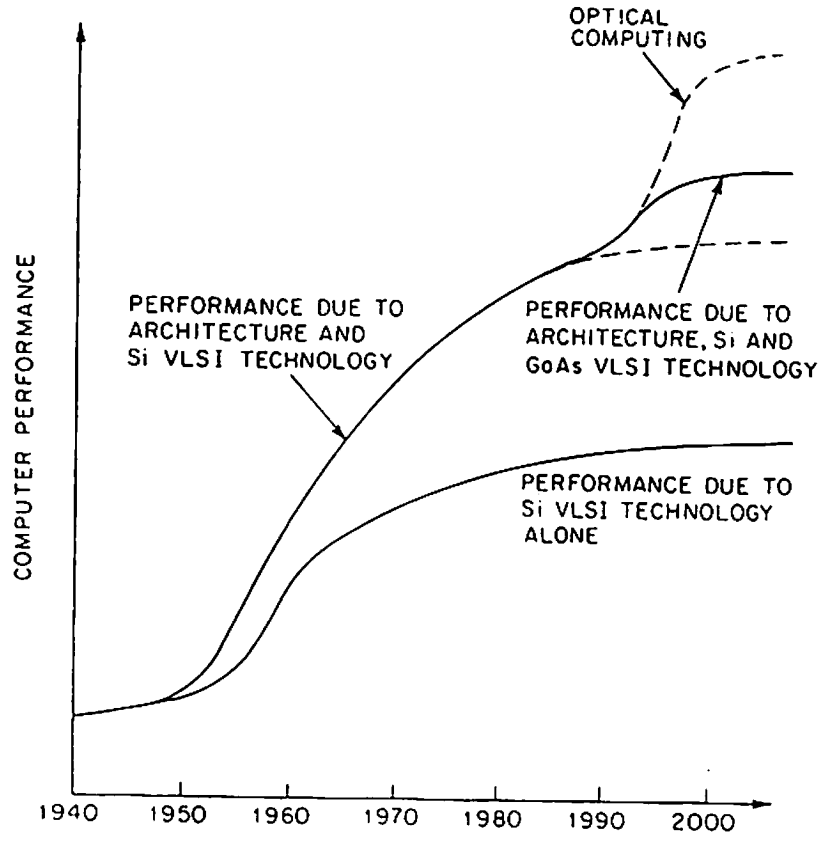


Fig. 1.4 Computing performance improves when advanced technologies are combined with innovative architectures [1.40].

We have developed an MOS transistor model that closely addresses the needs of circuit designers and device engineers. The BSIM_plus model is an enhanced version of the widely used BSIM model [1.35] and uses a compact set of physics-based parameters. Sub-half-micron modeling techniques have been used to achieve accuracy and continuity of the drain current and its derivatives in all regions of transistor operation. A new technique called the pseudo-boundary method is used to extend the applicability of a single set of transistor parameters over a large geometric design space. The BSIM_plus model contains a built-in substrate current expression which facilitates the use of SPICE circuit simulator for reliability simulation purpose. Temperature and noise effects on circuit performance can also be predicted by using the BSIM_plus model. The corresponding charge model for BSIM_plus has been derived. BSIM_plus has been implemented into a modified version of the SPICE-3e1 circuit simulation program. The new version of SPICE that contains BSIM_plus has been used to successfully simulate several analog and digital circuit examples.

Effective circuit design using an MOS transistor model depends upon the extracted model parameters. A significant part of the modeling effort is the extraction of transistor model parameters for characterization of fabrication technologies. Conventional parameter extraction programs include the SUXES program [1.36] for the SPICE Level-2 and Level-3 MOS transistor models, and a dedicated parameter extraction program [1.37] for the BSIM model. SUXES uses a modified gradient descent method to search over a constrained parameter space for a solution set of parameters. A global fit of

all data points is attempted. The dedicated parameter extraction program for BSIM selects closely related parameters and attempts to optimize them within a local set of data measured within specific bias ranges. The parameter extraction problem is NP-hard, since the complexity of finding an exact solution increases exponentially with problem size. The simulated annealing technique is suitable for such problems and has been used successfully in other engineering applications of a similar nature [1.38]. The objective function that is minimized during parameter extraction is usually the transistor drain current. Additional characteristics including the conductances and capacitances can be used in the objective function [1.39].

The MOS transistor modeling problem is described in Chapter 2. Literature publications in this area have been surveyed and significant results are briefly described. Sub-half-micron modeling techniques that are used in the development of the BSIM_plus model are described in Chapter 3. A detailed description of the BSIM_plus transistor model including the drain current expressions are given in this chapter. In Chapter 4, the organization of the SPICE circuit simulation program and the software implementation of BSIM_plus is described. The parameter extraction problem and new ways to solve it including the use of multiple-objective functions and simulated annealing techniques are described in Chapter 5. The implementation of the BSIM_plus model into the SUXES parameter extraction program is also described. Experimental results on parameter extraction and simulation of single transistors and circuit building blocks are presented in Chapter 6. The contribution of this research to current knowledge in the field of VLSI circuit

simulation and design is summarized in the conclusion in Chapter 7. A discussion of future directions for this research is also included. The appendices contain further details on the BSIM_plus model including the drain current derivatives and a numerical example for calculation of the drain current. User Guides for the software programs that are implemented are also given in the appendices along with example SPICE input decks, MOS transistor model parameter sets, and SUXES input files.

References

[1.1] M. I. Elmasry, "Preface," *Digital MOS Integrated Circuits with Applications to Processors and Memory Design*, vol. 2, Ed: M. I. Elmasry, p. xi, IEEE Press: Piscataway, NJ, 1992.

[1.2] D. Bursky, "Process advancements fuel IC developments," *Electronic Design* vol. 40, no. 1, p. 37, Jan. 9, 1992.

[1.3] L. G. Kang, Y. T. Kang, B. H. Roh, S. P. Kim, Y. W. Ha, K. M. Hang, C.-G. Hwang, "New transistor structure optimization for 0.25-μm CMOS technology," *Tech. Digest of IEEE/JSAP Symp. on VLSI Technology*, pp. 85-86, Osio, Japan, May 1991.

[1.4] A. Nitayama, H. Takato, N. Okabe, K. Sunouchi, K. Hieda, F. Horiguchi, F. Masuoka, "Multi-pillar surrounding gate transistor for compact and high-speed circuits," *IEEE Trans. on Electron Devices*, vol. 38, no. 3, pp. 579-583, Mar. 1991.

[1.5] J. Turner, "The half-micron apocalypse," *High-Speed Digital IC Technologies*, Editor: M. Rocchi, pp. 527-542, Artech House: Norwood, MA, 1990.

[1.6] Y. Oowaki, K. Tsuchida, Y. Watanabe, D. Takashima, H. Nakano, S. Watanabe, A. Nitayama, F. Horiguchi, K. Ohuchi, F. Masuoka, "A 33-ns 64-Mb DRAM," *IEEE Jour. of Solid-State Circuits*, vol. 26, no. 11, pp. 1498-1505, Nov. 1991.

[1.7] H. Iino, H. Takahashi, T. Sukemura, M. Kimura, K. Fujita, S. Mori, "A 289 MFLOPS single-chip supercomputer," *Tech. Digest of IEEE Int'l Solid-State Circuits Conf.*, San Francisco, CA, pp. 112-113, Feb. 1992.

[1.8] M. Toyokura, K. Okamoto, H. Kodama, A. Ohtani, T. Araki, K. Aono, "A video digital signal processor with a vector-pipeline architecture," *Tech. Digest of IEEE Int'l. Solid-State Circuits Conference*, pp. 72-73, San Francisco, CA, Feb. 1992.

[1.9] D. Dobberpuhl, R. Witek, R. Allmon, R. Anglin, S. Britton, L. Chao, R. Conrad, D. Dever, B. Gieseke, G. Hoeppner, J. Kowaleski, K. Kuchler, M. Ladd, M. Leary, L. Madden, E. McLellan, D. Meyer, J. Montanaro, D. Priore, V. Rajagopalan, S. Samudrala, S. Santhanam, "A 200-MHz 64-bit dual-issue microprocessor," *Tech. Digest of IEEE Int'l. Solid-State Circuits Conference*, pp. 106-107, San Francisco, CA, Feb. 1992.

[1.10] J. Choi, B. J. Sheu, S. Forrest, "A GaAs receiver module for optoelectronic computing and interconnection," *Proc. of IEEE Int'l. Conf. on Computer Design*, pp. 494-497, Cambridge, MA, Oct. 1991.

[1.11] C.-S. Li, H. S. Stone, C. M. Olsen, "Fully differential optical interconnects for high-speed digital systems," *Proc. of IEEE Int'l. Conf. on Computer Design*, pp. 190-193, Cambridge, MA, Oct. 1992.

[1.12] S.-Y. Oh, K.-J. Chang, N. Chang, K. Lee, "Interconnect modeling and design in high-speed VLSI/ULSI systems," *Proc. of IEEE Int'l. Conf. on Computer Design*, pp. 184-189, Cambridge, MA, Oct. 1992.

[1.13] P. G. Y. Tsui, S. W. Sun, J. R. Yeargain, B. Pappert, "A modular 0.5 micron BiCMOS technology for low voltage logic applications," *Proc. of IEEE Custom Integrated Circuits Conf.*, pp. 9.4.1-4, Boston, MA, May 1992.

[1.14] P. Raje, "Design and scaling of BiCMOS circuits," *Proc. of IEEE Int'l. Conf. on Computer Design*, pp. 234-238, Cambridge, MA, Oct. 1992.

[1.15] T. Tamura, S. Komori, F. Asai, H. Tsubota, H. Sato, H. Takata, Y. Seguchi, T. Tokuda, H. Terada, "A data driven architecture for distributed parallel processing," *IEEE Proc. of Int'l. Conf. on Computer Design*, pp. 218-224, Cambridge, MA, Oct. 1991.

[1.16] M. Johnson, *Superscalar Microprocessor Design*, Prentice Hall: Englewood Cliffs, NJ, 1991.

[1.17] J. L. Hennessy, D. A. Patterson, *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann: San Mateo, CA, 1990.

[1.18] Committee on Physical, Mathematical and Engineering Sciences, "Grand challenges: high-performance computing and communications, The FY 1992 U.S. Research and Development Program," *National Science Foundation*, Washington, D.C., 1991.

[1.19] D. A. Antoniadis, S. E. Hansen, R. W. Dutton, *SUPREM-II: A Program for IC Process Modeling and Simulation*, Tech. Report, Stanford Electronics Lab., Stanford University, Oct. 1979.

[1.20] M. R. Pinto, C. Rafferty, R. W. Dutton, *PISCES-II : Poisson Continuity Equation Solver*, Tech. Report, Stanford Electronics Lab., Stanford University, 1984.

[1.21] L. W. Nagel, *SPICE2: A Computer Program to Simulate Semiconductor Circuits*, Memo ERL-M520, Electronics Res. Lab., University of California, Berkeley, May 1975.

[1.22] B. Johnson, T. Quarles, A. R. Newton, D. O. Pederson, A. Sangiovanni-Vincentelli, *SPICE-3E1 User's Guide*, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, Apr. 1991.

[1.23] *HSPICE Users manual*, Meta-Software Inc., Campbell, CA, May 1991.

[1.24] *PSPICE User's Manual*, Microsim Corp., Irvine, CA, Jan. 1992.

[1.25] R. A. Saleh, A. R. Newton, *SPLICE User's Guide*, Dept. of Electrical Engineering and Computer Sciences, Univ. of California, Berkeley, CA, 1986.

[1.26] R. Saleh, R. Newton, *Mixed-Mode Simulation*, Kluwer Academic Publishers: Boston, MA, 1990.

[1.27] J. White, A. Sangiovanni-Vincentelli, "RELAX2: A new waveform relaxation approach for the analysis of LSI MOS circuits," *Proc. of IEEE Int'l. Symp. on Circuits and Systems*, pp. 756-759, Newport Beach, CA, May 1983.

[1.28] L. T. Pillage, R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. on Computer-Aided Design*, vol. 9, no. 4, pp. 352-366, Apr. 1990.

[1.29] B. J. Sheu, W.-J. Hsu, B. W. Lee, "An integrated-circuit reliability circuit simulator - RELY," *IEEE Jour. of Solid-State Circuits*, vol. 24, no. 2, pp. 473-477, Apr. 1989.

[1.30] R. H. Tu, E. Rosenbaum, C. C. Li, W. Y. Chan, P. M. Lee, B.-K. Liew, J. D. Burnett, P. K. Ko, C. Hu, *BERT - Berkeley Reliability Tools* University of California, Berkeley, CA, Feb. 1992.

[1.31] Y. Leblebici, S.-M. Kang, "Modeling of NMOS transistors for simulation of hot-carrier-induced device and circuit degradation," *IEEE Trans. on Computer-Aided Design*, vol. 11, no. 2, pp. 235-246, Feb. 1992.

[1.32] J. K. Ousterhout, "A switch-level timing verifier for digital MOS VLSI," *IEEE Trans. on Computer-Aided Design*, vol. 4, no. 3, pp. 336-348, Jul. 1985.

[1.33] D. D. Hill, D. R. Coelho, *Multi-Level Simulation for VLSI Design*, Kluwer Academic Publishers: Boston, MA, 1987.

[1.34] G. Gielen, W. Sansen, *Symbolic Analysis for Automated Design of Analog Integrated Circuits*, Kluwer Academic Publishers: Boston, MA, 1991.

[1.35] B. J. Sheu, D. L. Scharfetter, P. K. Ko, M.-C. Jeng, "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE Jour. of Solid-State Circuits*, vol. 22, no. 4, pp. 558-566, Aug. 1987.

[1.36] K. Doganis, R. W. Dutton, *SUXES-Stanford University Extractor of Model Parameters (User's Manual)*, Tech. Report, Stanford Electronics Lab., Stanford University, Nov. 1982.

[1.37] M.-C. Jeng, B. J. Sheu, P. K. Ko, *BSIM Parameter Extraction - Algorithms and User's Guide*, Memo ERL-M85/79, Electronics Res. Lab., Univ. of California, Berkeley, Oct. 1985.

[1.38] R. A. Rutenbar, "Simulated annealing algorithms: an overview," *IEEE Circuits and Devices Magazine*, vol. 5, no. 1, pp. 19-26, Jan. 1989.

[1.39] B. J. Sheu, C.-P. Wan, C.-C. Shih, W.-J. Hsu, M. C. Hsu, "Determination of process-dependent critical SPICE parameters for application-specific ICs," *Proc. of IEEE Int'l. Conf. on Microelectronic Test Structures*, pp. 73-78, Long Beach, CA, Feb. 1988.

[1.40] R. Sharma, "Impact of VLSI technology scaling on computer architectures," *Submicron Integrated Circuits*, Editor: R. K. Watts, Chapter 7, pp. 332-359, John Wiley: New York, NY, 1989.

Chapter 2

MOS Transistor Modeling for Circuit Simulation

Rapid advances in CMOS fabrication technologies have enabled the use of sub-half-micron devices to build high-speed VLSI circuits. The evolution of fabrication technologies has fueled the demand on research to further improve the MOS transistor models that are used by designers to simulate the circuits before fabrication. Three major criteria can be used to evaluate MOS transistor models for circuit simulation and circuit design:

- accuracy of performance predictions,
- computational efficiency, and
- usefulness of the model to circuit designers.

The accuracy of circuit performance prediction depends upon the ability of the model and the associated parameter set to simulate transistor characteristics including drain current, conductances, charges and capacitances over the ranges of terminal voltages and transistor geometries that occur in the circuit. There is usually a balance between the accuracy and computational efficiency of the model, and the clever handling of such a balance is a significant engineering task. The usefulness of the model to circuit designers depends upon several factors including the number and type of parameters, the different effects and features that are incorporated into the model, and how well the accuracy/efficiency balance is achieved.

Significant results have been reported over the past two decades from research on MOS transistor modeling. The tremendous progress achieved in improving the performance of these devices demands corresponding efforts and progress in modeling their behavior. Three main categories of MOS transistor modeling research include:

- type 1: investigation and modeling of specific important aspects of transistor behavior including threshold voltage, mobility, saturation velocity, and subthreshold conduction,
- type 2: development of highly accurate and computationally complex transistor drain current models that include many second-order and higher-order effects which are useful to device engineers, and
- type 3: development of accurate and computationally efficient transistor models with compact parameter sets that closely address the needs of VLSI circuit designers.

Research into detailed physical phenomena within the semiconductor device contributes significantly to understanding the physics of the device and the ability to predict these phenomena. Such research has resulted in a large volume of knowledge about semiconductor devices that is very useful in understanding MOS transistor operation and in the design and development of new devices [2.1-2.7]. In [2.8], Lee describes the universality and extraction of the mobility vs. gate-field curve in the inversion charge layer of MOSFETs. By using a simple, empirical mobility formulation, a single universal mobility curve is determined for seven different MOS technologies. In

[2.10], Conti et al. derive a rigorous analysis for the short-channel MOS transistor behavior on the basis of two-dimensional Poisson's equation, and attempt to predict a correct dependence of the threshold voltage on channel length and drain voltage. Ng et al. [2.11] summarize eleven different ways to determine the effective channel length based on resistance and capacitance measurement methods that have been proposed over the last 15 years. Sheu et al. [2.13] derive an expression for the source/drain resistance in the lightly-doped region of LDD MOSFETs and propose a method for the determination of this resistance. Wan et al. [2.14] identify a temperature-sensitive subset of BSIM (Berkeley Short-channel IGFET Model) parameters, and demonstrate the results on inverter transfer characteristics and the frequency response of a 31-stage ring oscillator. Hsu et al. [2.15] present a detailed study of the geometric dependence of MOSFET model parameters and propose methods to avoid adverse simulation results due to the modeling of narrow-channel and short-channel effects.

Several models have been proposed in the literature to provide circuit designers with the capability to predict behavior of circuit building blocks over the entire design space [2.16-2.26]. We have developed the BSIM_plus model with the objective of providing circuit designers with the enhanced capabilities needed to simulate sub-half-micron CMOS circuits. An overview of widely used MOS transistor models is presented here to provide the background of the BSIM_plus model development effort. The survey includes analytic models such as the MOS Level-1, Level-2, Level-3, Level-6 and BSIM models that are implemented in the SPICE-3e1 circuit simulator

Table 2.1 Comparison of MOS Level-2, Level-3 and BSIM transistor models.

MOS Model	MOS Level-2 [2.16]	MOS Level-3 [2.16]	BSIM [2.17]	BSIM_plus
Developers	Vladimirescu & Liu (1980)	Vladimirescu & Liu (1980)	Sheu, Scharfetter, Ko & Jeng (1985)	(this work)
Number of drain-current parameters	18	18	62	21
Variation of threshold voltage with substrate voltage	Monotonic	Monotonic	Possibly non-monotonic at high substrate voltages	Monotonic
Vertical field effect on carrier mobility	Not included	Due to gate voltage	Due to gate voltage	Due to gate voltage & substrate voltage
Conductance prediction accuracy for submicron technologies	Moderate	Moderate	Moderate	Good
Temperature/noise effects	Built-in	Built-in	External	Built-in
Charge/capacitance model	Conservation	Meyer model	Conservation	Conservation
Small-geometry effects	Complex expressions	Semi-empirical expressions	Globally fixed format	Locally adapted format
Applicability of parameter-set over a large geometric space	Very limited	Limited	Limited by abnormal second-order effects	Extended by pseudo-boundary method
Parameter extraction	Global optimization using SUXES	Global optimization using SUXES	Local optimization using BSIM extraction program	Combined local optimization with SUXES
Circuit type	Analog LSI	Digital VLSI	Digital VLSI	Analog LSI/Digital VLSI
Applicable technology	1.2 μm	1.0 μm	0.8 μm	Sub-half-micron

[2.16,2.17,2.19], the ASIM model from AT&T Bell Laboratories [2.18], and models that use the table look-up approach [2.25-2.28]. The BSIM is the MOS Level-4 model in the SPICE3 simulator and the subsequent BSIM2 is the MOS Level-5 model in the SPICE3 simulator. A comparison of the MOS Level-2, MOS Level-3, and BSIM transistor models that have been implemented in the SPICE circuit simulator is listed in Table 2.1.

2.1 MOS Level-1, Level-2 Transistor Models

The MOS Level-1 model is a first-order model that is useful for hand calculations when designing and analyzing new circuits. Simple expressions are used to describe the MOS drain current characteristics. The MOS Level-2 model, developed by Vladimirescu and Liu [2.16], used 18 parameters and included many second-order effects observed in devices with channel lengths down to 1.2 μm. An example MOS Level-2 model parameter set is listed in Table 2.2. The parameter values were provided by the MOSIS Service of USC/Information Sciences Institute, Marina del Rey, CA, and were extracted from a 2-μm P-well CMOS technology of Orbit Semiconductor, Inc., in Aug. 1992. The threshold voltage expression in the MOS Level-2 model included the substrate bias and narrow-channel effects. The body-effect coefficient due to the depletion charge at the drain and source was modified by correction factors. Depletion-layer widths near the source and drain were calculated from the source and drain voltages, respectively. The trapezoidal approximation shown in Fig. 2.1 was used in order to simplify

Table 2.2 MOS Level-2 transistor model parameters from a 2-μm P-well technology provided by the MOSIS Service in August 1992.

Name	Description	Unit	Value	
			NMOS	PMOS
LEVEL	selects model in SPICE	-	2	2
VTO	zero-bias threshold voltage	V	0.93	-0.75
KP	transconductance parameter	A/V^2	5.09E-5	1.93E-5
GAMMA	bulk threshold parameter	$V^{0.5}$	1.04	0.52
PHI	surface potential	V	0.6	0.6
LAMBDA	channel-length modulation	V^{-1}	1.3E-2	4.4E-2
TOX	oxide thickness	m	403E-8	403E-8
NSUB	substrate doping	cm^{-3}	2.4E+16	5.9E+15
NSS	surface state density	cm^{-2}	1.0E+10	1.0E+10
NFS	fast surface state density	cm^{-2}	3.9E+11	3.2E+11
TPG	type of gate material	-	1.0	-1.0
XJ	metallurgical junction depth	m	0.25E-6	0.25E-6
LD	lateral diffusion	m	0.25E-6	0.25E_6
UO	surface mobility	cm^2/Vs	595.4	225.3
UCRIT	critical field for mobility degradation	V/cm	1.38E+5	2.5E+4
UEXP	critical field exponent in mobility degradation	-	0.17	0.18
VMAX	maximum drift velocity of carriers	m/s	1.0E+5	4.7E+4
NEFF	total channel charge coeffient	-	1.0	1.0
DELTA	width effect on threshold voltage	-	1.68	0.93

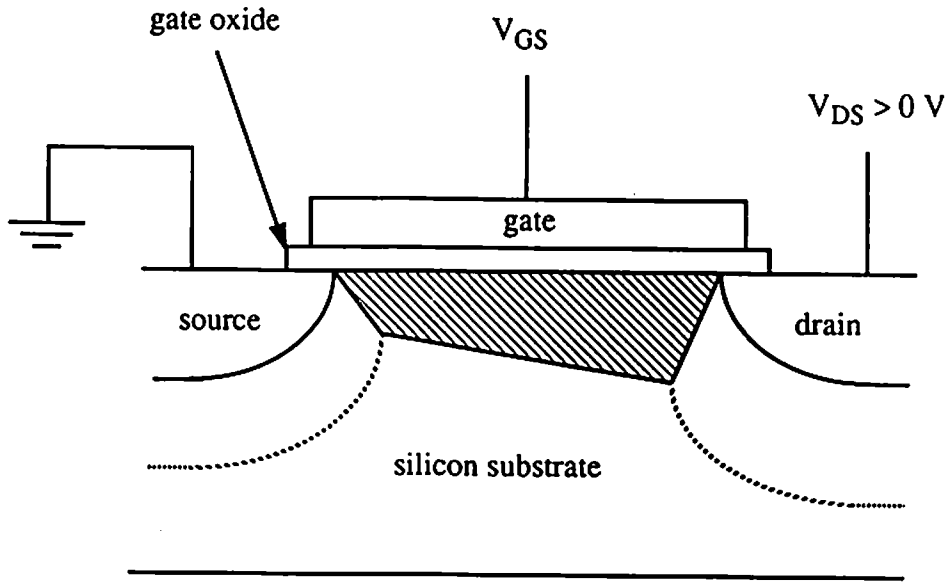


Fig. 2.1 Trapezoidal approximation for bulk charge depleted by gate electric field [2.16].

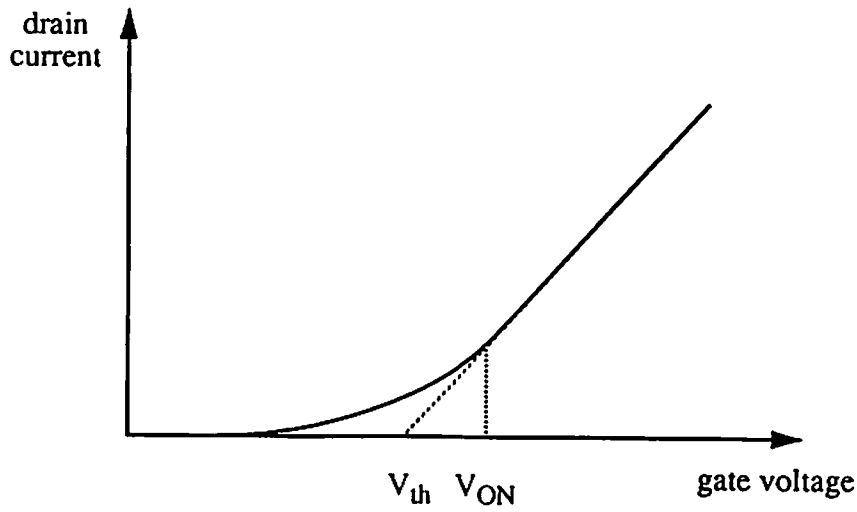


Fig. 2.2 Transition point between weak and strong inversion regions.

the computation. A single parameter with inverse width dependence is used to model the drain-induced barrier-lowering effect as well as the narrow-channel effect on the depletion charge-sharing coefficient. The channel length reduction was calculated from a complex expression that included the depletion layer width, the carrier mobility at the surface, and the maximum carrier drift velocity at velocity saturation. The transition point between the weak and strong inversion regions was defined to be above the threshold voltage by a multiple of the thermal voltage value. A graphical representation of the transition point is shown in Fig. 2.2. The multiplication factor was calculated from the bulk depletion capacitance and a curve-fitting parameter that was related to the fast surface states at the oxide/silicon interface. A complex expression modeled the weak-inversion drain current as an exponential function of the gate terminal voltage and the transition voltage. Continuity of drain current was achieved at the transition point between weak and strong inversion. However, continuity of the first derivative of the drain current was not achieved at this transition point.

2.2 MOS Level-3, Level-6 Transistor Models

The MOS Level-3 model, which was also developed by Vladimirescu and Liu [2.16], is a semi-empirical model and can be used for technologies with feature sizes down to 1.0 μm. The Level-3 model used 18 parameters in the drain current expressions that were mainly based on the curve fitting approach. The model took into account the two-dimensional nature of the

potential distribution in the channel region. Geometric dependent effects were included to a limited extent in order to increase the accuracy of the model for technologies below 1.5 μm. An example MOS Level-3 model parameter set is listed in Table 2.3. The parameters were provided by the MOSIS Service, and were extracted from a 1.2-μm N-well CMOS technology of Hewlett-Packard Co. in Jan. 1992.

The threshold voltage in the MOS Level-3 model was calculated from the flat-band voltage and the surface inversion potential, and included the drain-induced barrier-lowering effect and the non-uniform substrate-doping effect. The drain-induced barrier-lowering effect was modeled with an inverse dependence on the cubed channel length. The non-uniform substrate doping effect included correction terms for the short-channel and narrow-channel effects. The correction factor for short-channel effects was calculated from the junction depth by using a trapezoidal approximation. The correction factor of narrow-channel effect was calculated from an inverse width dependence and modeled the adjustment of depletion charge at the edge of the channel.

The surface carrier mobility was calculated from the intrinsic mobility in the channel region and an empirical fitting parameter. The effect of the vertical field on the intrinsic carrier mobility was modeled as a function of the gate voltage. The effective mobility also included the velocity saturation effect that was dependent upon the horizontal field in the channel and was calculated using the maximum carrier drift velocity parameter. The saturation of velocity due to the horizontal field is shown in Fig. 2.3. The channel

Table 2.3 MOS Level-3 transistor model parameters from a 1.2-μm N-well technology provided by the Mosis Service in January 1992.

Name	Description	Unit	Value	
			NMOS	PMOS
LEVEL	selects model in SPICE	-	3	3
VTO	zero-bias threshold voltage	V	0.77	-0.94
KP	transconductance parameter	A/V^2	9.99E-5	3.23E-5
GAMMA	bulk threshold parameter	$V^{0.5}$	0.46	0.45
PHI	surface potential	V	0.6	0.6
TOX	oxide thickness	m	2.1E-8	2.1E-8
NSUB	substrate doping	cm^{-3}	1.8E+16	1.8E+16
NSS	surface state density	cm^{-3}	-	-
NFS	fast surface state density	cm^{-2}	5.0E+12	4.9E+12
TPG	type of gate material	-	1.0	-1.0
XJ	metallurgical junction depth	m	0.20E-6	0.20E-6
LD	lateral diffusion	m	0.06E-6	0.03E_6
UO	surface mobility	cm^2/Vs	593.2	191.8
UTRA	transverse field coefficient	-	-	-
VMAX	maximum drift velocity of carriers	m/s	1.9E+5	3.7E+4
DELTA	width effect on threshold voltage	-	2.39	1.36
THETA	mobility modulation	V^{-1}	1.3E-1	1.7E-1
ETA	static feedback	-	1.1E-1	1.5E-1
KAPPA	saturation field factor	-	9.3E-2	9.8

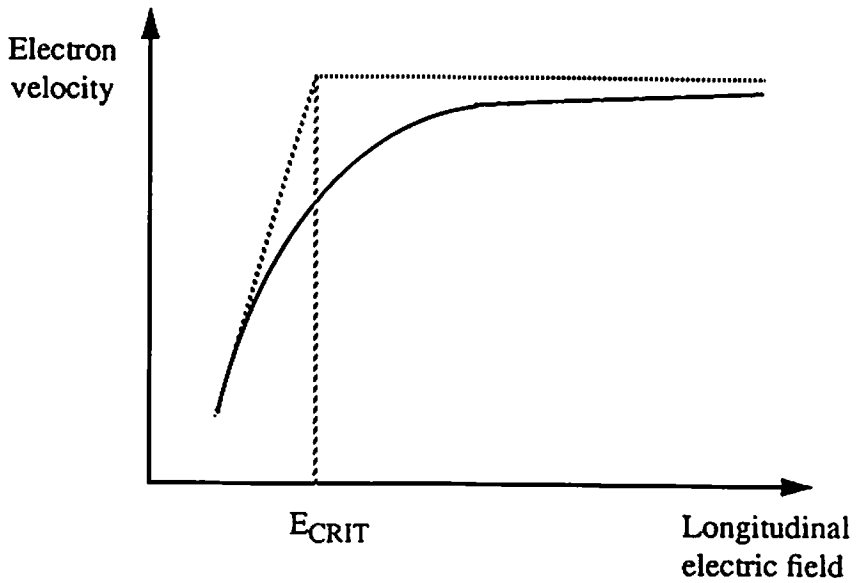


Fig. 2.3 Saturation of electron velocity due to high electric field [2.16].

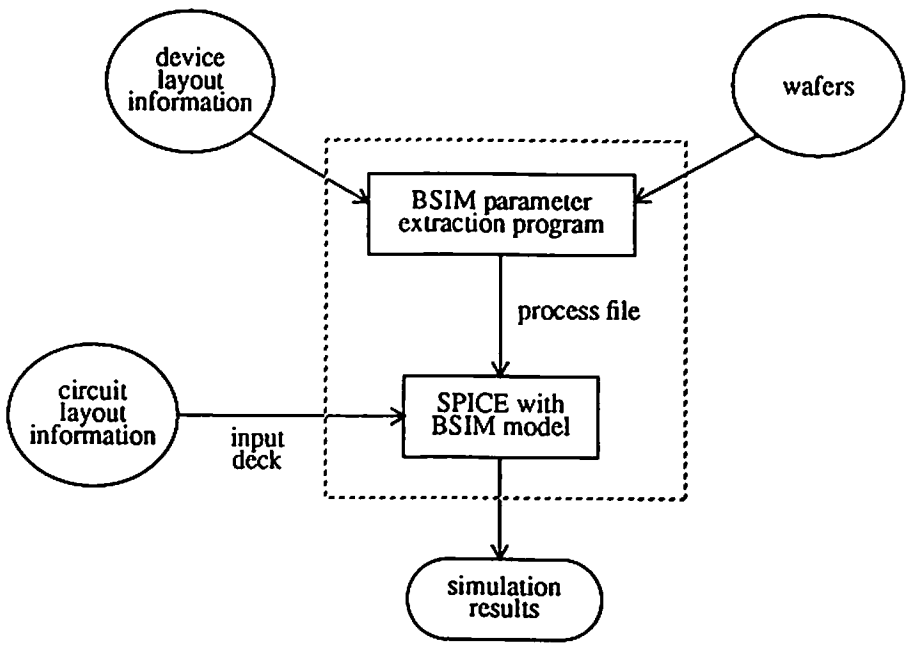


Fig. 2.4 The integrated parameter extraction and circuit simulation environment provided by the BSIM model [2.17].

length reduction was calculated from the lateral electric field at the channel pinch-off point. The coefficient of depletion layer width which was calculated from the substrate doping concentration, and an empirical fitting parameter, were also used to determine the channel length reduction. The drain current expression included a Taylor series expansion coefficient of bulk charge and the transconductance coefficient. The saturation voltage was defined as the drain voltage at which the carrier velocity approached the value of the maximum carrier drift velocity parameter. If this parameter was not given, the saturation voltage was determined from the maximum of the drain current equation. The weak-inversion drain current expression was similar to that used in the MOS Level-2 model.

The MOS Level-3 model used a compact set of parameters. This was convenient for circuit designers who used the model, and also eased the parameter extraction task in which device engineers characterized the technology in terms of the model parameters. Since many model parameters were empirical, integration of the circuit simulator with device-level simulators is quite difficult. Such integration includes determining the transistor parameter values from electronic quantities that are predicted by the device-level simulators. Empirical parameters are usually extracted to fit a limited voltage range or geometric space, while circuit designers could require simulations over a larger voltage range and extensive geometric design space. The use of cubic inverse-length dependence for the drain-induced barrier-lowering term of the threshold voltage could limit the range of channel lengths over which a single parameter set is applicable. The use of a square-root

dependence on ($V_{DS} - V_{DSAT}$) in the channel length modulation expression could cause discontinuity in drain current derivatives at the triode/saturation interface. Such discontinuities could lead to convergence problems in the circuit simulation procedure.

The MOS Level-6 model [2.19] was a simple model based on the n-th power law. The simulation times using this model were reported to be considerably better than the Level-3 model. Smooth drain current characteristics at the transition between the triode and saturation regions of operation improved the convergence of the circuit simulator. Parameters can be quickly calculated from a small number of data points. The model is general, and can also be applied to GaAs FETs.

2.3 BSIM, BSIM2, and BSIM3 Transistor Models

The BSIM transistor model was a circuit-level MOS model with strong device physics emphasis which can accurately predict drain current characteristics of transistors with channel lengths down to 0.8 μm [2.17]. The model used a total of 62 parameters in the drain current expressions. There were 24 electrical parameters, of which 19 were calculated from nominal, inverse-length and inverse-width coefficients. The simple framework of geometry dependence was an outstanding feature of the BSIM model. The parameter values were calculated by,

$$P = P_0 + \frac{P_L}{L} + \frac{P_W}{W} \tag{2.1}$$

Table 2.4 BSIM transistor model parameters from a 1.2-μm N-well technology provided by the MOSIS Service in January 1992.

Parameter Description	Unit	P_0			P_L			P_W		
		Name	NMOS	PMOS	Name	NMOS	PMOS	Name	NMOS	PMOS
flat-band voltage	V	VFB	-1.14E+0	-1.86E-1	LVFB	7.60E-2	1.45E-2	WVFB	3.29E-1	3.97E-2
surface inversion potential	V	PHI	8.09E-1	7.22E-1	LPHI	0.00E+0	2.15E-5	WPHI	0.00E+0	-3.22E-4
body-effect coefficient	V	K1	1.34E+0	4.20E-1	LK1	-6.02E-2	-3.24E-2	WK1	-3.09E-1	7.36E-2
depletion charge-sharing coefficient	-	K2	2.14E-1	-3.14E-2	LK2	3.07E-2	2.08E-2	WK2	-1.48E-1	-1.38E-3
zero-bias drain-induced barrier-lowering coeff.	-	ETA	-1.07E-2	-5.73E-3	LETA	1.58E-2	1.98E-2	WETA	1.96E-2	6.77E-3
zero-bias mobility	cm^2/Vs	MUZ	5.20E+2	1.75E+2	(DL)	4.05E-1	2.49E-1	(DW)	3.46E-1	3.74E-1
transverse field mobility degradation coeff.	V^{-1}	U0	9.88E-2	1.37E-1	LU0	1.49E-1	6.76E-2	WU0	-1.04E-1	-6.31E-2
zero-bias velocity saturation coefficient	μm/V	U1	3.89E-2	-3.45E-3	LU1	1.08E-1	9.28E-2	WU1	-7.65E-2	-1.45E-2
sensitivity of mobility to V_{BS} at V_{DS} = 0 V	cm^2/V^2s	X2MZ	4.70E+0	8.12E+0	LX2MZ	-2.90E+0	-1.69E+0	WX2MZ	4.64E+1	2.52E+0
sensitivity of ETA to V_{BS}	V^{-1}	X2E	-3.21E-3	1.20E-5	LX2E	-4.70E-3	-1.29E-3	WX2E	6.07E-3	-2.31E-3
sensitivity of ETA to V_{DS} at $V_{DS} = V_{DD}$	V^{-1}	X3E	1.64E-3	1.31E-4	LX3E	-1.32E-3	-1.07E-3	WX3E	-7.69E-3	-2.55E-3
sensitivity of U0 to V_{BS}	V^{-2}	X2U0	-4.25E-3	6.74E-3	LX2U0	2.11E-3	8.16E-5	WX2U0	3.59E-2	3.02E-3
sensitivity of velocity saturation to V_{BS}	$\mu m/V^2$	X2U1	-1.01E-2	-1.05E-3	LX2U1	7.94E-3	1.92E-3	WX2U1	2.44E-3	5.22E-3
mobility at V_{BS} = 0 V and $V_{DS} = V_{DD}$	cm^2/V^2s	MUS	6.74E+2	1.72E+2	LMUS	6.28E+1	5.20E+1	WMUS	-2.05E+2	-9.29E+0
sensitivity of mobility to V_{BS} at $V_{DS} = V_{DD}$	cm^2/V^2s	X2MS	-1.06E+0	6.20E+0	LX2MS	8.69E+0	1.66E+0	WX2MS	5.43E+1	5.88E+0
sensitivity of mobility to V_{DS} at $V_{DS} = V_{DD}$	cm^2/V^2s	X3MS	1.30E+1	-7.35E-2	LX3MS	1.50E+1	3.35E+0	WX3MS	-2.80E+1	-1.76E+0
sensit. of velocity satn. to V_{DS} at $V_{DS} = V_{DD}$	$\mu m/V^2$	X3U1	1.59E-2	-1.06E-2	LX3U1	5.44E-3	2.50E-3	WX3U1	-1.99E-2	-1.37E-3

where P_0, P_L and P_W were the nominal value, length-dependence coefficient and width-dependence coefficient of the parameter P, respectively. An example BSIM model parameter set provided by the MOSIS Service of USC/Information Sciences Institute is listed in Table 2.4. The parameters were extracted from a 1.2-μm N-well CMOS technology of Hewlett-Packard Co. in January 1992. The extracted parameters are in the form of a process file containing parameters for different layers including the NMOS and PMOS transistors, N-diffusion, P-diffusion, and metal layers. Figure 2.4 shows a fully-integrated approach for computer-aided parameter extraction and circuit design [2.17].

The threshold voltage expression in the BSIM model included the effect of non-uniform substrate doping on the depletion charge term. The effect of extra bulk charge at the edge of narrow transistor channels was not explicitly modeled in the threshold voltage expression. The drain-induced barrier-lowering coefficient was calculated using zero-bias, substrate-voltage and drain-voltage dependence parameters, each of which were geometry dependent. The reduction of carrier mobility in the triode region due to vertical and horizontal electric fields was modeled by terms that were dependent upon the gate and drain voltages. The vertical field effect included only the gate voltage contribution explicitly. A second-order dependence upon the substrate voltage was included in the parameter that was used to model the vertical field effect. The parameter that models the horizontal field effect was dependent upon the substrate and drain voltages. The drain current expression in the saturation region included a body-effect coefficient term and a

carrier saturation-velocity dependent term. The drain current and its first-order derivatives were continuous at the transition between the triode and saturation regions.

The subthreshold conduction expression in the BSIM model was dominated by the diffusion current component. The subthreshold slope was calculated using drain-voltage and substrate-voltage dependence coefficients. The diffusion component of the subthreshold current was modeled by using an exponential dependence on the gate and drain terminal voltages. The subthreshold current was limited in the strong-inversion region by clamping. The total drain current in all regions of transistor operations was expressed as the sum of weak-inversion and strong-inversion drain current terms.

The simple geometric dependence framework included in BSIM was intended to increase accuracy of the model over a large geometric range. However, the number of parameters that are to be extracted is quite large. As a result, only a small geometric region can be accurately characterized. The simulation of transistors beyond this characterized region can result in abnormal simulation results due to exaggeration of second-order geometry-dependent effects. The technique used to model the non-uniform substrate doping effect can cause non-monotonic threshold voltage variation at high substrate voltages, resulting in simulation convergence problems. This happens because the terminal voltages during intermediate circuit simulation iterations sometimes assume very high values beyond the power supply rails of the circuit. The drain current and first derivatives are continuous at the triode/saturation interface and this is critical for circuit simulation purpose.

However, the second derivative of the drain current is not continuous, resulting in poor output conductance behavior at the triode/saturation region interface and in the saturation region.

The BSIM2 model from U.C. Berkeley [2.20] was an extension of the BSIM model. Several additional empirical parameters were added to model second-order effects on transistor behavior. By increasing the number of parameters, the accuracy of the model in the submicron region was improved. However, additional problems of complexity in circuit simulation and parameter extraction were created due to the large parameter set. Extrapolating the process file from existing technologies to future technologies was also complicated. The same framework of geometry dependence for all parameters that was used in BSIM, was retained in BSIM2. The threshold voltage in BSIM2 was very similar to that used in BSIM. The drain-voltage dependence of the drain-induced barrier lowering coefficient was removed in order to prevent the occurrence of negative output resistance at low current levels. The effect of the vertical field on the carrier mobility included a quadratic dependence upon the gate voltage in order to model the effect of large electric fields that occur in devices with thin gate oxides. The velocity saturation effect was modeled using the critical electric field parameter, which was calculated from a second-order dependence on the drain and saturation voltages. The effect of source/drain parasitic resistances were lumped with the mobility term during parameter extraction. The horizontal and vertical field effects on the mobility were combined as a summation of terms rather than as a product. The subthreshold drain current was calculated using the charge-sheet

approximation. The depletion-layer capacitance and the surface potential at the channel/oxide interface were calculated as functions of the gate voltage. A transition region was defined around the threshold voltage and the effective gate voltage that was used in this region was generated using a cubic spline function in order to improve the transition between the weak-inversion and strong-inversion regions.

The BSIM3 model from U.C. Berkeley [2.21,2.22] used 20 to 25 parameters to model channel-length modulation, drain-induced barrier lowering and substrate-induced body effect. The threshold voltage reduction for short-channel transistors was modeled by an exponential term. The drain current expression in the saturation region included the Early voltage term. The subthreshold conduction was dominated by the diffusion expression. The weak-inversion and strong-inversion current were matched in a transition region that was defined around the threshold voltage.

2.4 ASIM Transistor Model

The ASIM transistor model was developed by Lee and Rennick [2.18], of AT&T Bell Laboratories, in 1988. A set of 89 parameters were used to model the drain current in all regions of transistor operation. The ASIM model was implemented in the circuit simulator ADVICE, and in the circuit/device simulator MEDUSA, both at AT&T Bell Laboratories. The

model used exponential dependencies on terminal voltages to model second-order effects and ensure smooth transitions between different regions of transistor operation.

The threshold voltage expression in the ASIM model used empirical terms to include the effects due to non-uniform substrate doping, narrow channel width, charge sharing, and drain-induced barrier lowering. Carrier mobility reduction was modeled primarily as a function of the effective gate field, which was described in terms of the field at the silicon/oxide interface and the field at the inversion region-depletion region interface. The saturation voltage was determined by calculating the drain voltage at which the horizontal field was equal to the critical electric field for velocity saturation. The critical electric field for velocity saturation was calculated by using an analytic expression that included gate-voltage and substrate-voltage dependencies. The channel-length modulation term was calculated by solving the one-dimensional Poisson's equation in the high field region. The resulting expression included the thickness of the inversion layer, saturation drain current, saturation drain voltage, and critical electric field for velocity saturation. The subthreshold drain current expression was calculated from the effective thickness of the inversion charge layer, the surface potential, and the carrier densities at the source and drain ends of the channel. Comparison of measured data with simulated drain current characteristics using the ASIM model were reported for transistors with channel lengths down to 1.75 μm [2.18].

2.5 Table Look-up Models

Table look-up models use data from devices of different geometries measured at different bias conditions. During circuit simulation, transistor voltage and current values for a specific point in the geometric and bias design spaces are calculated from the measurement data using various interpolation and extrapolation techniques. Various techniques are used to improve the accuracy of such models without greatly increasing the number of data points [2.25-2.30].

Shima et al. [2.25] proposed a three-dimensional table look-up modeling technique. Interpolation was done by using curve-shape fitting techniques. The data were stored in a three-dimensional table which consisted of a main table and several sub-tables, as shown in Fig. 2.5. The two-dimensional main table contained data at different drain and gate voltages at a substrate voltage of 0 V. The voltage intervals between data points in the main table were very small. In addition to the main table, the three-dimensional table contained sub-tables, each for a different constant bulk bias. Entries in the sub-tables were the deviations in drain current from the data in the main table. The number of sub-tables was small, since the drain current sensitivity to the substrate voltage was smaller than its sensitivity to drain and gate voltages. The number of data points in each sub-table was also reduced, upon the assumption that the variation of drain current with gate voltage was similar at different substrate voltages. In addition to the three-dimensional table, the variation of threshold voltage as a function of the substrate voltage was stored in a one-dimensional array. In order to calculate the D.C. current, the

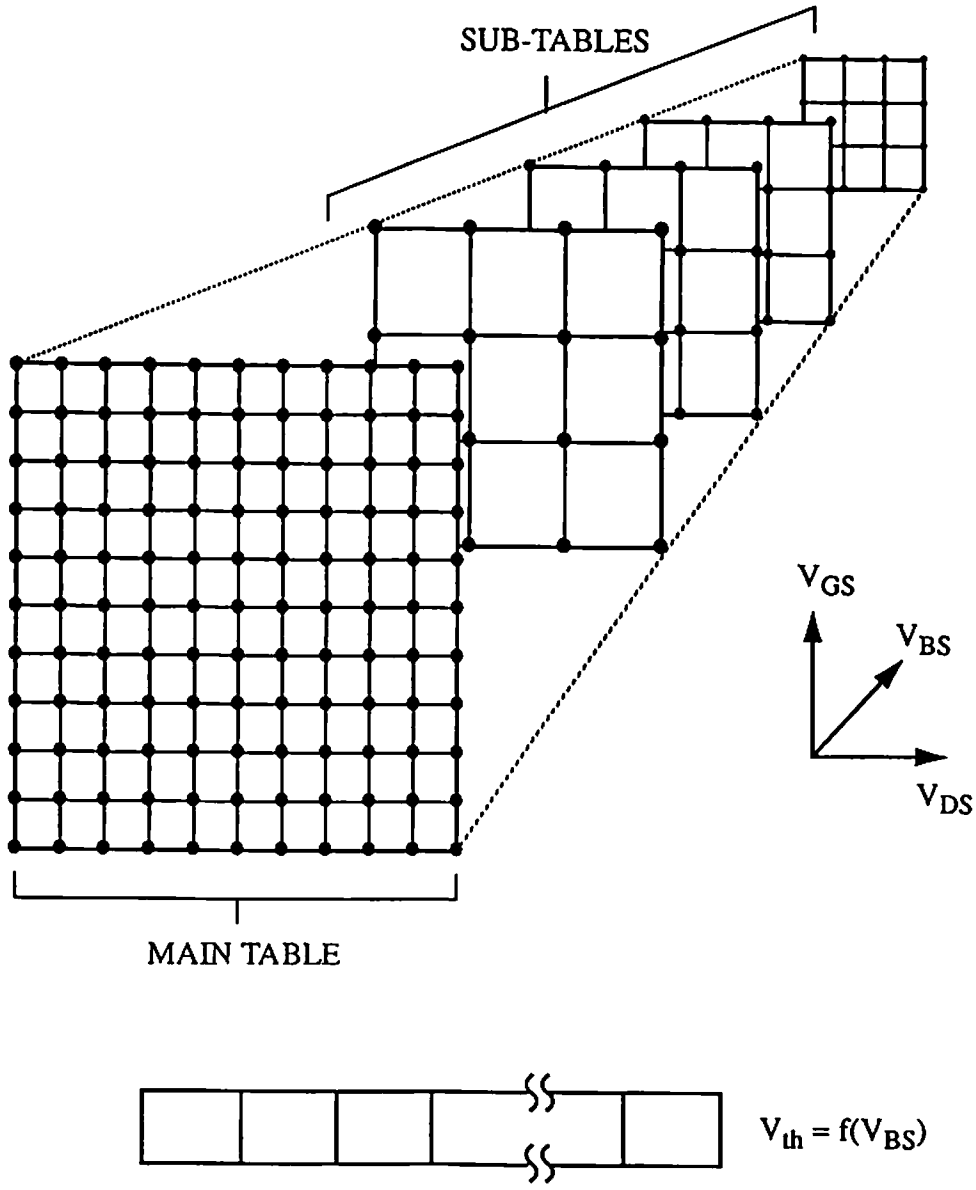


Fig. 2.5 Structure of main table and sub-tables in a table look-up MOS transistor model [2.23].

threshold voltage was first determined based upon the substrate bias using the stored data and second-order polynomial interpolation. Two sub-tables were selected, based upon the substrate voltage. A three-dimensional cell was constructed from eight points, four from each of the two sub-tables. The eight points were multiplied by the data in the main table, and this was called the curve-shape fitting technique. A single point was found on each sub-table, corresponding to the drain current at the drain and gate voltages specified. The drain current at the specified substrate voltage was calculated by interpolating between these points. Conductances were calculated from the differences in drain current and bias voltages in the table.

Shima et al. also used the table look-up method to simulate the capacitances of MOS transistors [2.29]. Measured gate-to-source and gate-to-drain capacitances and a calculated charge table were used to represent the MOS transistor capacitances. The bulk charge was formulated by an analytic expression and other charges were derived based on interpolation of measured capacitance data. Short-channel effects and subthreshold capacitance characteristics could be accurately simulated by using the experimental data in the table. The partitioning of the channel charge into the drain and source charges was done by using a partitioning factor.

Yoon et al. [2.26-2.28] proposed an adjustable accuracy table look-up model in which the user could determine the tradeoff point between table size and model accuracy. This method could be used to emphasize the accuracy of the model in a certain region of operation such as the weak-inversion, triode, or saturation region. Special attention was given to the

accurate calculation of small-signal quantities such as output conductance and transconductance, by considering both D.C. and A.C. error calculations in the table data extraction procedure. A multi-dimensional gradient data tracing methodology was used. The model was implemented within the framework of the SPICE program, and results on analog CMOS amplifiers using 1.6-μm CMOS technologies were demonstrated.

References

[2.1] S. M. Sze, *Physics of Semiconductor Physics*, 2nd Edition, John Wiley and Sons: New York, NY, 1981.

[2.2] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw-Hill: New York, NY, 1987.

[2.3] R. S. Muller, T. I. Kamins, *Device Electronics for Integrated Circuits*, 2nd ed., John Wiley: New York, NY, 1986.

[2.4] F. M. Klaassen, "Compact MOSFET modeling," *Process and Device Modeling*, Chapter 12, Editor: W. L. Engl, North-Holland: New York, NY, 1986.

[2.5] E. H. Nicollian, J. R. Brews, *MOS Physics and Technology*, John Wiley: New York, NY, 1982.

[2.6] P. Richman, *MOS Field-Effect Transistors and Integrated Circuits*, John Wiley, New York, NY, 1973.

[2.7] D. A. Divekar, *FET Modeling for Circuit Simulation*, Kluwer Academic Publishers: Boston, MA, p. 89, 1988.

[2.8] S.-W. Lee, "Universality of mobility-gate field characteristics of electrons in the inversion charge layer and its application in MOSFET modeling," *IEEE Trans. on Computer-Aided Design*, vol. 8, no. 7, pp. 724-730, Jul. 1989.

[2.9] G. M. Yeric, A. F. Tasch, S. K. Bannerjee, "A universal MOSFET mobility degradation model for circuit simulation," *IEEE Trans. on Computer-Aided Design*, vol. 9, no. 10, pp. 1123-1126, Oct. 1990.

[2.10] M. Conti, C. Turchetti, "On the short-channel theory for MOS transistor," *IEEE Trans. on Electron Devices*, vol. 38, no. 12, pp. 2657-2661, Dec. 1991.

[2.11] K. K. Ng, J. R. Brews, "Measuring the effective channel length of MOSFETs," *IEEE Circuits and Devices Magazine*, pp. 33-38, Nov. 1990.

[2.12] K. N. Ratnakumar, J. D. Meindl, "Short-channel MOST threshold voltage model," *IEEE Jour. of Solid-State Circuits*, vol. 17, no. 5, pp. 937-948, Oct. 1982.

[2.13] B. J. Sheu, C. Hu, P. K. Ko, F.-C. Hsu, "Source-and-drain series resistance of LDD MOSFETs," *IEEE Electron Device Letters*, vol. 5, no. 9, pp. 365-367, Sept. 1984.

[2.14] C.-P. Wan, B. J. Sheu, "Temperature dependence modeling for MOS VLSI circuit simulation," *IEEE Trans. on Computer-Aided Design*, vol. 8, no. 10, pp. 1065-1073, Oct. 1989.

[2.15] M. C. Hsu, B. J. Sheu, "Inverse-geometry dependence of MOS transistor electrical parameters," *IEEE Trans. on Computer-Aided Design*, vol. 6, no. 4, pp. 582-585, Jul. 1987.

[2.16] A. Vladimirescu, S. Liu, *The Simulation of MOS Integrated Circuits Using SPICE2*, Memo ERL-M80/7, Electronics Res. Lab., Univ. of California, Berkeley, Oct. 1980.

[2.17] B. J. Sheu, D. L. Scharfetter, P. K. Ko, M.-C. Jeng, "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE Jour. of Solid-State Circuits*, vol. 22, no. 4, pp. 558-566, Aug. 1987.

[2.18] S.-W. Lee, R. C. Rennick, "A compact IGFET model - ASIM," *IEEE Trans. on Computer-Aided Design*, vol. 7, no. 9, pp. 952-975, Sept. 1988.

[2.19] T. Sakurai, A. R. Newton, "A simple MOSFET model for circuit analysis," *IEEE Trans. on Electron Devices*, vol. 38, no. 4, pp. 887-894, Apr. 1991.

[2.20] M.-C. Jeng, P. K. Ko, C. Hu, "A deep-submicrometer MOSFET model for analog/digital circuit simulations," *Tech. Digest of IEEE Int'l. Electron Devices Meeting*, pp. 114-117, San Francisco, CA, Dec. 1988.

[2.21] J. H. Huang, et al. "A physical model for MOSFET output resistance," *Tech. Digest of IEEE Int'l. Electron Devices Meeting*, Dec. 1992.

[2.22] J. H. Huang, Z. H. Liu, M. C. Jeng, P. K. Ko, C. Hu, "A robust physical and predictive model for deep-submicrometer MOS circuit simulation," *submitted to IEEE Custom Integrated Circuits Conf.*, San Diego, CA, May 1993.

[2.23] K.-Y. Toh, P.-K. Ko, R. G. Meyer, "An engineering model for short-channel MOS devices," *IEEE Jour. of Solid-State Circuits*, vol. 23, no. 4, pp. 950-958, Aug. 1988.

[2.24] S. Karmalkar, K. N. Bhat, "A process-parameter-based circuit simulation model for ion-implanted MOSFETs and MESFETs," *IEEE Jour. of Solid-State Circuits*, vol. 24, no. 1, pp. 139-145, Jan. 1989.

[2.25] T. Shima, H. Yamada, R. L. M. Dang, "Table look-up MOSFET modeling system using a 2-D device simulator and monotonic piecewise cubic interpolation," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 2, no. 2, pp. 121-125, Apr. 1983.

[2.26] K. S. Yoon, P. E. Allen, "An adjustable accuracy model for VLSI analog circuits using lookup tables," *Jour. of Analog Integrated Circuits and Signal Processing*, Kluwer Academic Publishers, vol. 1, no. 1, pp. 45-64, Sept. 1991.

[2.27] K. S. Yoon, *Precision Analog Small-Signal Model for Submicron MOSFET Devices*, Ph.D. dissertation, School of Electrical Engineering, Georgia Institute of Technology, Jan. 1990.

[2.28] P. E. Allen, K. S. Yoon, "A table look-up MOSFET model for analog applications," *Tech. Digest of IEEE Int'l. Conf. on Computer-Aided Design*, pp. 124-127, Santa Clara, CA, Nov. 1988.

[2.29] T. Shima, "Table lookup MOSFET capacitance model for short-channel devices," *IEEE Trans. on Computer-Aided Design*, vol. 5, no. 4, Oct. 1986.

[2.30] M. G. Graham, J. J. Paulos, *to appear in IEEE Trans. on Computer-Aided Design*, 1993.

Chapter 3

The BSIM_plus MOS Transistor Model

List of Symbols

ε_{Si}	permittivity of silicon
μ_{eff}	effective carrier mobility
ϕ_{ms}	work-function difference between metal and semiconductor
ϕ_n	electron quasi-Fermi potential
C_{OX}	gate-oxide capacitance per unit area
E_y	lateral electric field
E_{eff}	effective transverse electric field
E_G	energy band gap
J_c	current density in the channel
k	Boltzmann constant
n	electron density in the channel
n_i	intrinsic carrier concentration
N_{SUB}	substrate impurity concentration
q	elementary charge
Q_b	bulk depletion charge density
Q_n	inversion charge density
Q_{OX}	oxide-semiconductor interface charge density
v	carrier velocity

v_{sat} carrier saturation velocity

V_T thermal voltage

V_{th} threshold voltage of an MOS transistor

Design of high-performance very large-scale integration (VLSI) systems is made possible by rapid advances in fabrication technologies that have enabled the use of deep-submicron devices. Circuit designers using advanced CMOS technologies require an accurate MOS transistor model for proper circuit simulation over the geometric and bias design spaces. An effective and efficient model will enable VLSI designers to fully exploit advantages of aggressive technologies. The following features are required to make the transistor model very useful to circuit designers:

- a compact parameter set,
- model expressions based on knowledge from device physics,
- accuracy of drain current, output conductance and capacitances,
- continuity of drain current and its derivatives across different regions of operation,
- the convenience to simulate transistors over the geometric design space, and
- the ability to simulate effects of temperature changes and noise.

The BSIM_plus model is based on the popular BSIM model [3.1,3.2]. The new model has been developed to address challenges posed by the rapid evolution of fabrication technologies and to enable accurate and efficient

Table 3.1 BSIM_plus drain current parameters and default values.

No.	Symbol	Name	Description	Default	Unit
1	ϕ_S	phis	surface inversion potential	0.7	V
2	V_{FB}	vfb	flat-band voltage	-0.875	V
3	γ_1	gamma1	zero-bias body-effect coeff.	0.8	$V^{0.5}$
4	γ_2	gamma2	high-bias body-effect coeff.	0.06	$V^{0.5}$
5	K_S	ks	depletion charge-sharing coeff.	1.1	-
6	K_{NZ}	knz	narrow-width threshold voltage coeff.	0.2	V µm
7	K_{NB}	knb	narrow-width thresh. volt. substrate coeff.	0.04	µm
8	η_Z	etaz	drain-induced barrier lowering coeff.	0.02	-
9	η_L	etal	short-channel barrier-lowering coeff.	0.01	µm
10	μ_0	mu0	intrinsic surface mobility	450	cm^2/Vs
11	ΔL	dl	channel length reduction	0.1	µm
12	ΔW	dw	channel width reduction	0.1	µm
13	U_{GSZ}	ugsz	gate-voltage mobility degradation coeff.	0.02	V^{-1}
14	U_{GSL}	ugsl	short-channel adjustment of ugsz	0.01	V^{-1}µm
15	U_{BS}	ubs	substrate-volt. mobility degradation coeff.	0.02	V^{-1}
16	E_{CRIT}	ecrit	critical electric field for velocity saturation	5.0	V/µm
17	H_0	h0	output conductance modulation prefactor	0.05	-
18	H_1	h1	output conductance modulation exponent	2.0	V
19	T_{OX}	tox	gate oxide thickness	25	nm
20	I_0	i0	subthreshold drain-current coefficient	1e-7	A
21	N	n	subthreshold drain current slope	1.5	-

simulation of submicron CMOS circuits by digital VLSI and analog LSI/VLSI circuit designers.

A compact set of parameters reduces the complexity of the parameter extraction problem and enhances the ability to extract an accurate parameter set. The BSIM_plus model uses 21 parameters for calculation of the D.C. drain current from the terminal voltages. The model parameters and their default values are listed in Table 3.1. The small number of parameters allows circuit designers to have a better understanding of the relationship between the circuit performance and behavior of its constituent transistors. A small set of physics-based parameters also facilitates linking detailed process/device simulators with circuit simulators. In the aggressive product development environment, designs are required to be fabricated by the most advanced technologies. In order to achieve this goal, circuit design and technology improvement can take place simultaneously. Convenient integration of process/device simulators with circuit simulators is required for this reason. By using a model with a compact set of physics-based parameters, transistor model parameters can be calculated from electronic quantities that are obtained from the solution of the underlying physical equations of the device [3.3,3.4].

3.1 Drain Current Formulation

Accuracy of the drain current expression is of primary interest in the computer simulation of digital VLSI circuits [3.5]. In addition, accurate output conductance and transconductance expressions are required in the design of analog LSI and VLSI circuits [3.6]. The drain current derivatives are also used in the intermediate iterations of circuit simulation in order to converge to a final solution. During these iterations, the terminal voltages of the transistor may take on a wide range of values. For example, the gate voltage may be as high as 20 V. Continuous and physically meaningful derivatives of the drain current with respect to the four terminal voltages over a wide range of bias conditions can facilitate convergence of the iteration process. Careful modeling of the threshold voltage and effective mobility help to achieve many of these criteria.

3.1.1 Threshold Voltage

The threshold voltage of an MOS transistor is the gate voltage separating the strong- and weak-inversion regions of operation. According to classical definition [3.7,3.8], this is the voltage at which there is significant inversion in the channel and the minority carrier concentration in the channel region at the surface of the semiconductor is equal to the majority carrier concentration in the bulk semiconductor. The threshold voltage expression in the BSIM_plus model for short-channel transistors includes the following terms:

- surface inversion potential,
- flat-band voltage,
- non-uniform substrate doping effect,
- drain-induced barrier lowering effect, and
- narrow-channel effect.

The surface inversion potential, ϕ_s, is a model parameter of the BSIM_plus model. It is related to the impurity concentration in the bulk semiconductor by,

$$|\phi_s| \approx 2V_T \ln\left[\frac{N_{SUB}}{n_i}\right]. \tag{3.1}$$

In the BSIM_plus model, the parameter V_{FB} is used to model the flat-band voltage. The flat-band voltage is applied between the gate and semiconductor in order to compensate for the difference between the work functions of the metal and semiconductor, resulting in "flat" energy bands. The flat-band voltage also accounts the effective interface charge which is the sum of the fixed and trapped oxide charges, mobile ionic charge and interface trapped charge. Although the flat-band voltage is a model parameter in the BSIM_plus model, it is closely related to the physics of the MOS device and can be calculated from the substrate doping and the interface charge density as given below [3.8],

$$V_{FB} = \phi_{ms} - \frac{Q_{OX}}{C_{OX}}. \tag{3.2}$$

ϕ_{ms} is the work function difference between the metal and the semiconductor.

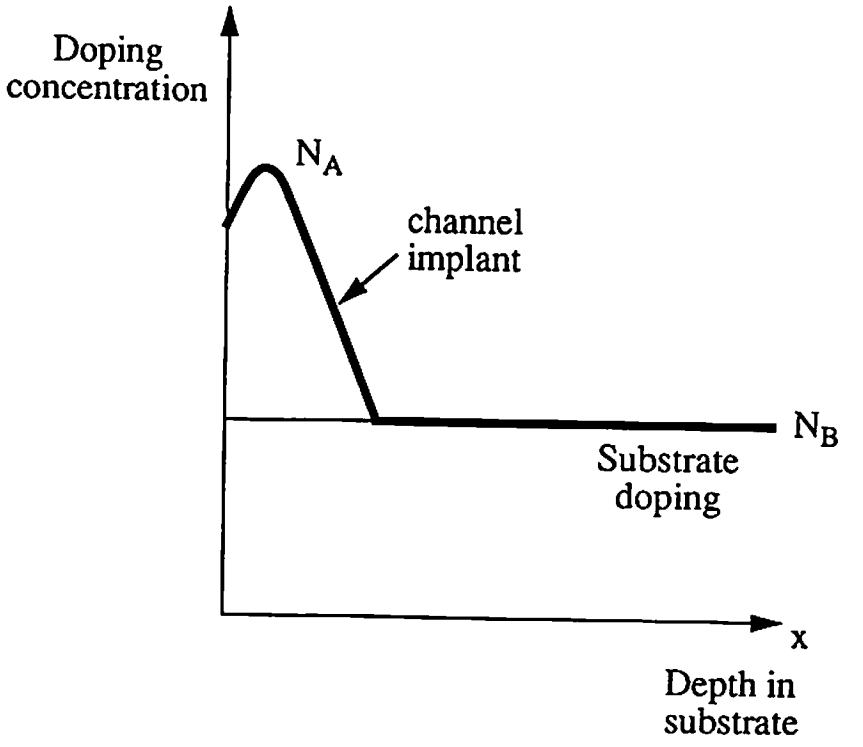


Fig. 3.1 Non-uniform substrate doping profile in ion-implanted CMOS technologies.

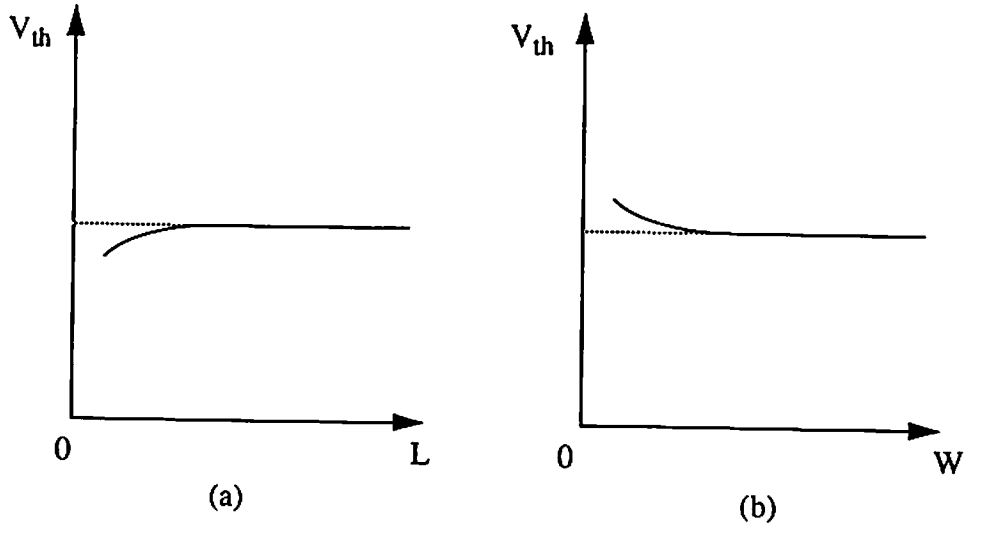


Fig. 3.2 Variation of threshold voltage with transistor geometry. (a) Length dependence. (b) Width dependence.

Q_{OX} is the effective interface charge which is directly proportional to the interface trap density.

The threshold voltage expression includes the effect of the substrate doping profile shown in Fig. 3.1. With increasing depth in the semiconductor from the oxide-semiconductor interface, the impurity concentration reaches a peak, N_A, very close to the interface and then decreases until it is equal to the constant impurity concentration, N_B, in the bulk semiconductor. The effect of such non-uniform substrate doping is included by using parameters γ_1, γ_2 and K_S. At high substrate biases, the derivative of the threshold voltage with respect to the substrate bias is maintained at a constant positive value. This ensures that the threshold voltage increases monotonically with increasing magnitude of the substrate bias. The transition point between low and high substrate bias voltages is marked by the point at which the depletion region extends into the substrate down to the region of uniform doping concentration. This transition voltage is calculated from ϕ_s, γ_1, γ_2, and K_S. The model parameter γ_1 is the slope of the threshold voltage with respect to the quantity $\sqrt{\phi_s - V_{BS}}$ at low substrate biases when the depletion region boundary is in the channel implant region. The parameter γ_1 is related to the implanted impurity concentration by,

$$\gamma_1 = \frac{1}{C_{OX}} \sqrt{2\, q\, \varepsilon_{Si}\, N_A}, \tag{3.3}$$

and,

$$\gamma_2 = \frac{1}{C_{OX}} \sqrt{2\, q\, \varepsilon_{Si}\, N_B}. \tag{3.4}$$

At high substrate biases, when the depletion region boundary is in the uniformly doped region of the substrate, the slope of the threshold voltage with respect to $\sqrt{\phi_s - V_{BS}}$ is a lower value corresponding to the parameter γ_2. As the depletion region boundary moves from point A to point B, the slope of the threshold voltage changes from γ_1 to γ_2 at a rate given by model parameter K_S. The parameter K_S can be calculated from the measured threshold voltage data by,

$$K_S = \frac{\partial^2 V_{th}}{\partial \sqrt{\phi_s - V_{BS}}^2}, \tag{3.5}$$

where V_{BS} is the voltage between the bulk and source terminals of the transistor.

The drain-induced barrier lowering effect describes the modification of the potential barrier in the channel region due to the influence of electric field lines from the drain region. This effect is modeled by changing the effective threshold voltage as a function of the drain voltage, using the parameters η_Z and η_L. An inverse length dependence parameter, η_L, has been included since the barrier lowering effect is more pronounced at shorter channel lengths.

Due to the fringe electric field on the two sides of the channel, there is depletion charge which is not directly under the thin gate oxide. In narrow-channel transistors, this extra depletion charge becomes significant when compared to the depletion charge that is directly under the gate oxide. The extra charge is a function of the substrate terminal voltage and results in increasing

threshold voltage with decreasing channel width as shown in Fig. 3.2(b) [3.9]. In the BSIM_plus model, the narrow-channel effects are included by using parameters K_{NZ} and K_{NB}.

The detailed expression for the threshold voltage is given by,

$$V_{th} = V_{FB} + \phi_s + \gamma_1(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s}) - \frac{K_S}{2}(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s})^2 + \frac{K_{NZ}}{W} + \frac{K_{NB}V_{BS}}{W} - \left[\eta_Z + \frac{\eta_L}{L}\right]V_{DS} \quad \text{for } |V_{BS}| \le |V_{BST}|, \tag{3.6}$$

and

$$V_{th} = V_{FB} + \phi_s + \gamma_1(\sqrt{\phi_s - V_{BST}} - \sqrt{\phi_s}) - \frac{K_S}{2}(\sqrt{\phi_s - V_{BST}} - \sqrt{\phi_s})^2 + \gamma_2(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s - V_{BST}}) + \frac{K_{NZ}}{W} + \frac{K_{NB}V_{BS}}{W} - \left[\eta_Z + \frac{\eta_L}{L}\right]V_{DS} \quad \text{for } |V_{BS}| > |V_{BST}|. \tag{3.7}$$

Here, V_{DS} is the voltage between the drain and source terminals of the transistor. The transition voltage, V_{BST}, at which the boundary of the depletion region touches the bulk semiconductor with the impurity concentration of N_B can be determined by,

$$V_{BST} = \phi_s - \left[\frac{\gamma_1 - \gamma_2}{K_S} + \sqrt{\phi_s}\right]^2. \tag{3.8}$$

The variation of threshold voltage with substrate bias was calculated by using expressions from the Level-3, BSIM, and the proposed BSIM_plus models, and results are compared with measurement data from an NMOS transistor

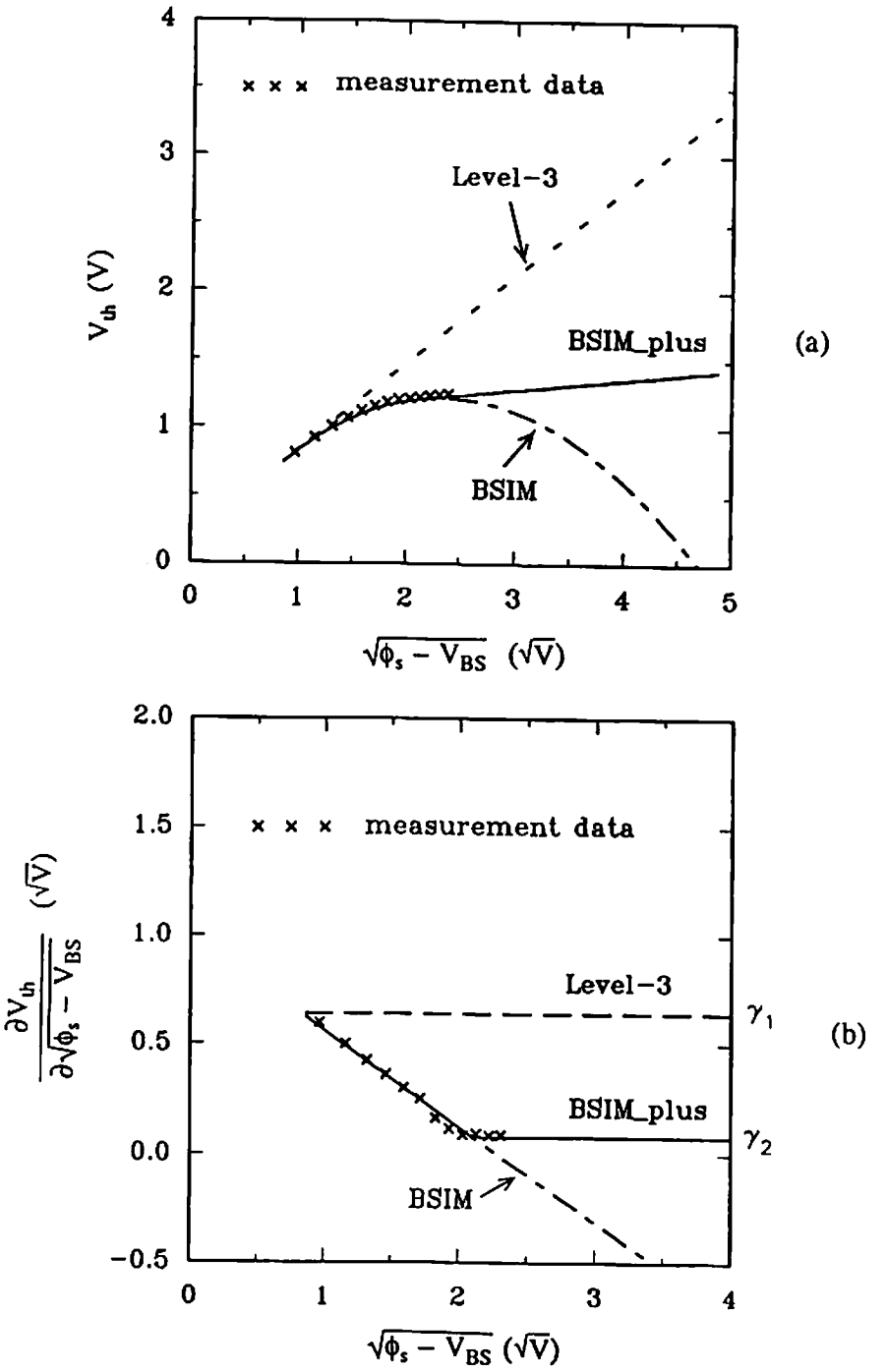


Fig. 3.3 Comparison of measured and simulated threshold voltages of an NMOS transistor with W/L = 50 μm/1 μm at V_{DS} = 0.1 V. (a) Threshold voltage. (b) Threshold voltage derivative.

with W/L = 50 μm/1 μm in Fig. 3.3(a). The derivatives of the threshold voltages with respect to $\sqrt{\phi_s - V_{BS}}$ as predicted by the three models are compared with measurement data in Fig. 3.3(b).

3.1.2 Effective Carrier Mobility

The intrinsic carrier mobility at the surface of the silicon is given by the model parameter μ_0. During device operation, the mobility of carriers is reduced due to the effect of the transverse and lateral fields. The effect of the transverse electric fields were previously modeled by universal mobility curves given by [3.10-3.12],

$$\mu_{eff} = \frac{A_1}{1 + A_2 \cdot E_{eff}}, \tag{3.9}$$

where E_{eff} was the effective transverse electric field. A_1 and A_2 were empirical parameters determined by least-square fitting of mobility vs. transverse field curves. The effective transverse electric field was calculated as,

$$E_{eff} = - \frac{\left[\frac{Q_n}{2} - Q_b\right]}{\varepsilon_{Si}}, \tag{3.10}$$

where Q_n is the inversion charge density, Q_b is the bulk depletion charge density, and ε_{Si} is the permittivity of the silicon substrate. These charges were calculated by,

$$Q_n = - C_{OX}(V_{GS} - V_{th}), \tag{3.11}$$

and,

$$Q_b = - C_{OX}\, \gamma_1 \sqrt{\phi_s - V_{BS}}. \tag{3.12}$$

Experimental data showing accurate characterization of mobility vs. transverse field curves for seven different technologies with oxide thicknesses ranging from 21 nm to 40 nm and surface impurity concentrations ranging from 6 x 10^{14} cm^{-3} to 1.4 x 10^{17} cm^{-3} were reported [3.10]. The transverse-field scattering effect on carrier mobility in the BSIM_plus model is based upon (3.9). In the BSIM_plus model, parameters U_{GSZ}, U_{GSL} and U_{BS} are used to model the reduction of mobility due to carrier scattering by the transverse electric field. The model parameter U_{GSZ} is used to include the gate-voltage contribution to the transverse field along with a short-channel correction parameter, U_{GSL}. The model parameter U_{BS} is used to include the substrate voltage contribution to the transverse electric field. The mobility reduction due to the effect of the transverse electric field is given by,

$$\mu'_{eff} = \frac{\mu_0}{\left[1 + (U_{GSZ} + \frac{U_{GSL}}{L})(V_{GS} - V_{th}) - U_{BS}V_{BS}\right]}. \tag{3.13}$$

The continuous velocity saturation effect due to the influence of the lateral field in the channel on the carrier mobility is also included. The critical field for velocity saturation is specified as a model parameter in the BSIM_plus model. The expression for the continuous velocity saturation is given by,

$$v = \frac{\mu_0 E_y}{\left[1 + \frac{E_y}{E_{CRIT}}\right]}, \tag{3.14}$$

where v is the carrier velocity and E_y is the lateral electric field in the channel. The terms describing the effects of the transverse and lateral fields are combined as a product in the expression for effective mobility. In the linear region the effective mobility expression is given by,

$$\mu_{eff} = \frac{\mu_0}{\left[1 + (U_{GSZ} + \frac{U_{GSL}}{L})(V_{GS} - V_{th}) - U_{BS}V_{BS}\right]\left[1 + \frac{V_{DS}}{E_{CRIT} \cdot L}\right]}. \quad (3.15)$$

3.1.3 Output Conductance Engineering

An exponential term is used in order to achieve output conductance matching in the transition from the triode to saturation regions of operation. Exponential terms were also used in the ASIM model [3.14] to improve drain current transition between these two regions. The linear- and saturation-region drain current expressions are multiplied by the factor F_S. In the linear region, this factor is defined as,

$$F_S = F_{S,triode} \equiv 1 - H_0 \cdot \left[1 - e^{\frac{V_{DS} - V_{DSAT}}{H_1}}\right], \quad (3.16)$$

and in the saturation region it is defined as,

$$F_S = F_{S,satn.} \equiv 1 + H_0 \cdot \left[1 - e^{\frac{V_{DSAT} - V_{DS}}{H_1}}\right]. \quad (3.17)$$

At the transition between the triode and saturation regions of operation, the triode and saturation drain current expressions are tangential even when the

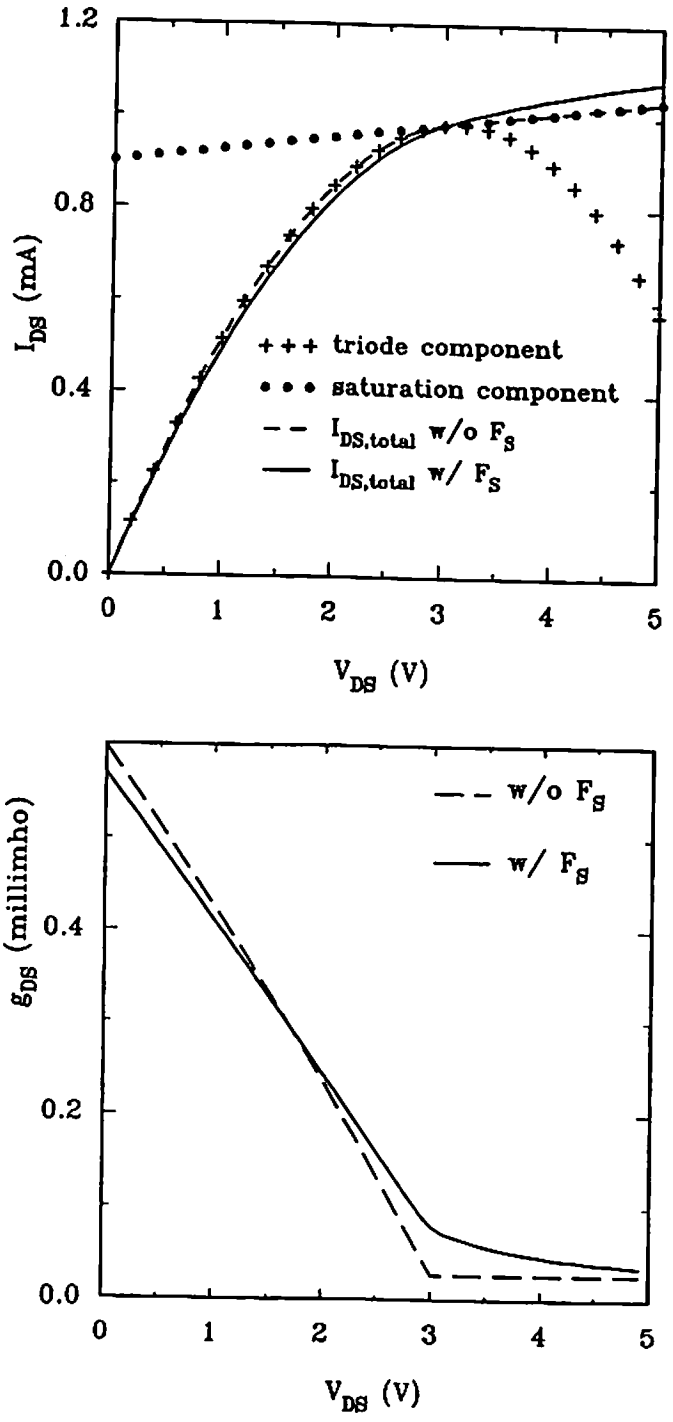


Fig. 3.4 Effect of the F_S term in triode and saturation regions. (a) Drain current. (b) Output conductance.

F_S factor is not used. Without the F_S factor, the drain current and output conductance are continuous at this transition point, but the output conductance has a sharp corner due to a discontinuity in the second derivative of the drain current. The inclusion of the F_S factor modifies the output conductance characteristic in the transition from linear to saturation regions by making the first derivative of the output conductance continuous. The output conductance in the saturation region is also more accurately modeled by the inclusion of the F_S term. The effects of the F_S term on the drain current and the output conductance are shown in Fig. 3.4.

3.1.4 Strong-Inversion Region

The transistor operates in the strong-inversion region if the gate-to-source voltage is greater than the threshold voltage. The electron current density due to carrier drift in the channel is written as,

$$J = -q\,\mu_0\,n\,\frac{d\phi_n}{dy}, \tag{3.18}$$

where n is the electron density and ϕ_n is the quasi-Fermi potential in the channel region. The drain current in the channel is written as,

$$I_{DS} = -\mu_0\,W\,q_c\,\frac{d\phi_n}{dy}. \tag{3.19}$$

The actual drain current expression is derived by integrating on both sides with limits extending from the source end of the channel to the drain end as in,

$$I_{DS}\int_0^L dy = -\mu_0 W \int_0^{V_{DS}} q_c \, d\phi_n. \tag{3.20}$$

The channel charge density, q_c, is written as [3.2],

$$q_c = -C_{OX}\left[(V_{GS} - \phi_s - V_{FB} - \phi_n) - \gamma_1\sqrt{\phi_s + \phi_n - V_{BS}}\right]. \tag{3.21}$$

Performing the integration given in (3.20), the drain current expression is derived as,

$$I_{DS} = \mu_{eff}C_{OX}\frac{W}{L}\left[(V_{GS} - \phi_s - V_{FB})V_{DS} - \frac{V_{DS}^2}{2} - \frac{2}{3}\gamma_1\left[(V_{DS} + \phi_s - V_{BS})^{\frac{3}{2}} - (\phi_s - V_{BS})^{\frac{3}{2}}\right]\right]. \tag{3.22}$$

The substrate-voltage dependent terms are approximated by a series expansion, and (3.22) can be written as,

$$I_{DS,triode} = \frac{\mu_0 C_{OX}\frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{a}{2}V_{DS}^2\right] F_S}{\left[1 + (U_{GSZ} + \frac{U_{GSL}}{L})(V_{GS} - V_{th}) - U_{BS}V_{BS}\right]\left[1 + \frac{V_{DS}}{E_{CRIT}\cdot L}\right]} \tag{3.23}$$

where the term "a" is defined as,

$$a \equiv 1 + \frac{g\gamma_1}{2\sqrt{\phi_s - V_{BS}}}, \tag{3.24}$$

and,

$$g \equiv 1 - \frac{1}{1.744 + 0.8364(\phi_s - V_{BS})}. \tag{3.25}$$

Notice that F_S is also included. The corresponding channel charge expression can be rewritten as,

$$q_c = - C_{OX}(V_{GS} - V_{th} - a\phi_n). \tag{3.26}$$

The saturation region is defined by the onset of velocity saturation, at which point $\phi_n = V_{DSAT}$. The channel charge at the onset of saturation is given by,

$$q_c = - \frac{I_{DSAT}}{Wv_{sat}} = - C_{OX}(V_{GS} - V_{th} - aV_{DSAT}). \tag{3.27}$$

Rearranging (3.27),

$$V_{DSAT} = \frac{1}{a}\left[(V_{GS} - V_{th}) - \frac{I_{DSAT}}{Wv_{sat}C_{OX}}\right]. \tag{3.28}$$

The drain current in the saturation region is obtained by integrating (3.26) with this new upper limit and is given by,

$$I_{DSAT} = \mu_0 C_{OX}\frac{W}{L}\left[\left[V_{GS} - V_{th} - \frac{I_{DSAT}}{Wv_{sat}C_{OX}}\right]V_{DSAT} - \frac{aV_{DSAT}^2}{2}\right]$$

$$= \frac{\mu_0 C_{OX}}{2a}\frac{W}{L}\left[V_{GS} - V_{th} - \frac{I_{DSAT}}{Wv_{sat}C_{OX}}\right]^2. \tag{3.29}$$

This expression can be written more conveniently as,

$$I_{DS,satn.} = \frac{\mu_0 C_{OX}\frac{W}{L}\left[V_{GS} - V_{th}\right]^2 F_S}{\left[1 + (U_{GSZ} + \frac{U_{GSL}}{L})(V_{GS} - V_{th}) - U_{BS}V_{BS}\right]2aK}. \tag{3.30}$$

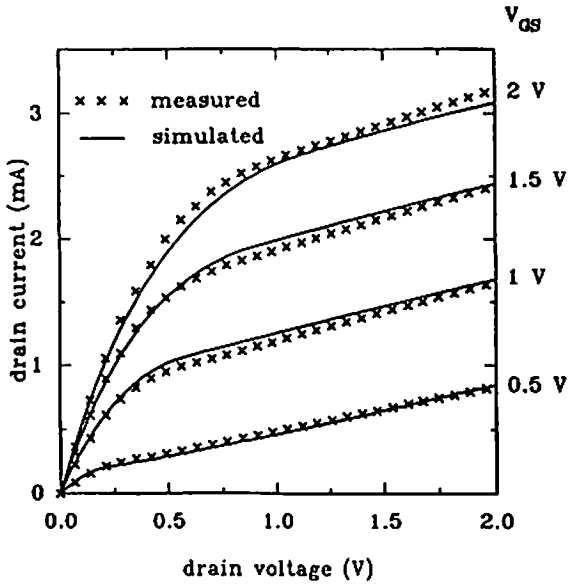
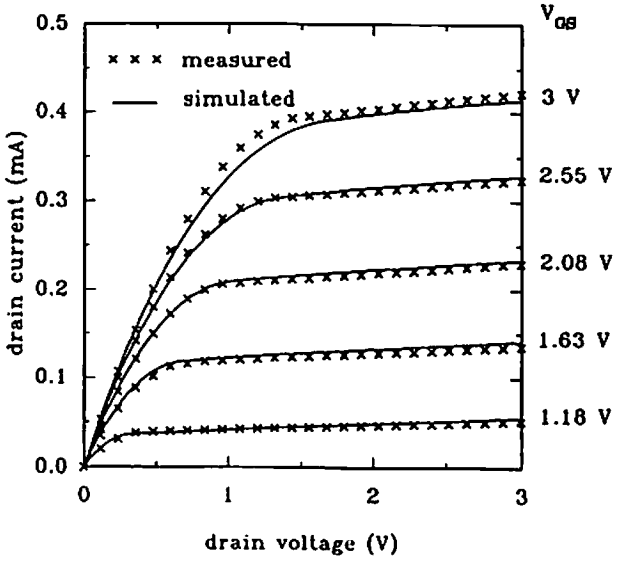
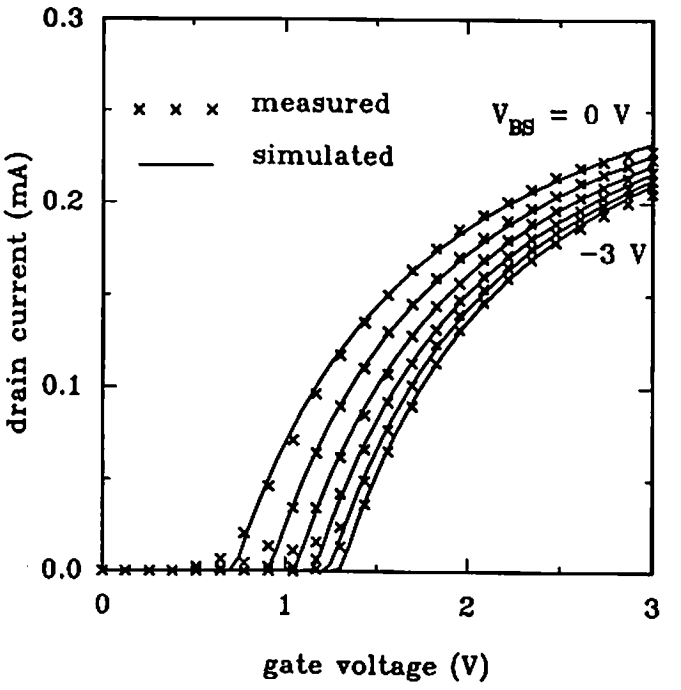


Fig. 3.5 BSIM_plus drain current characteristics for an NMOS transistor with W/L = 10 μm/0.15 μm [3.29].

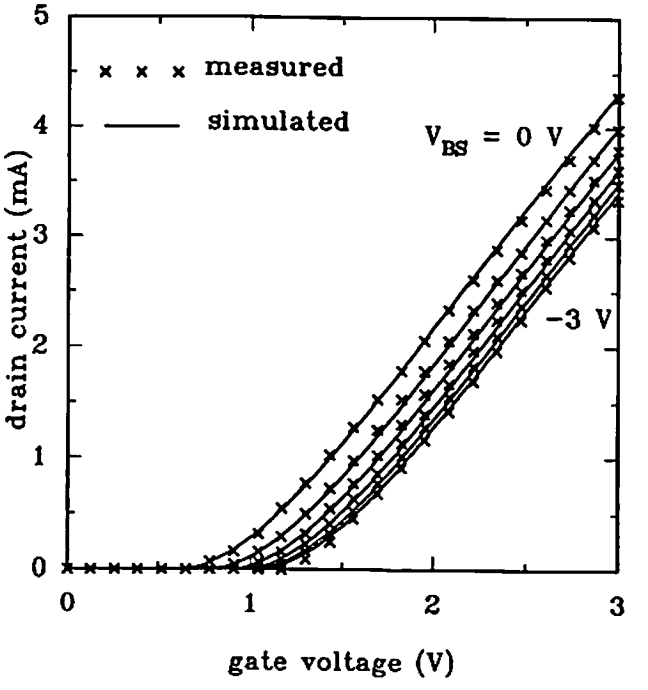


(a)

Fig. 3.6 BSIM_plus drain current characteristics for an NMOS transistor with W/L = 10 μm/0.25 μm [3.30]. (a) I_{DS} vs. V_{DS}



(b)



(c)

Fig. 3.6 (cont'd)
(b) I_{DS} vs. V_{GS} for V_{DS} = 0.05 V.
(c) I_{DS} vs. V_{GS} for V_{DS} = 3 V.

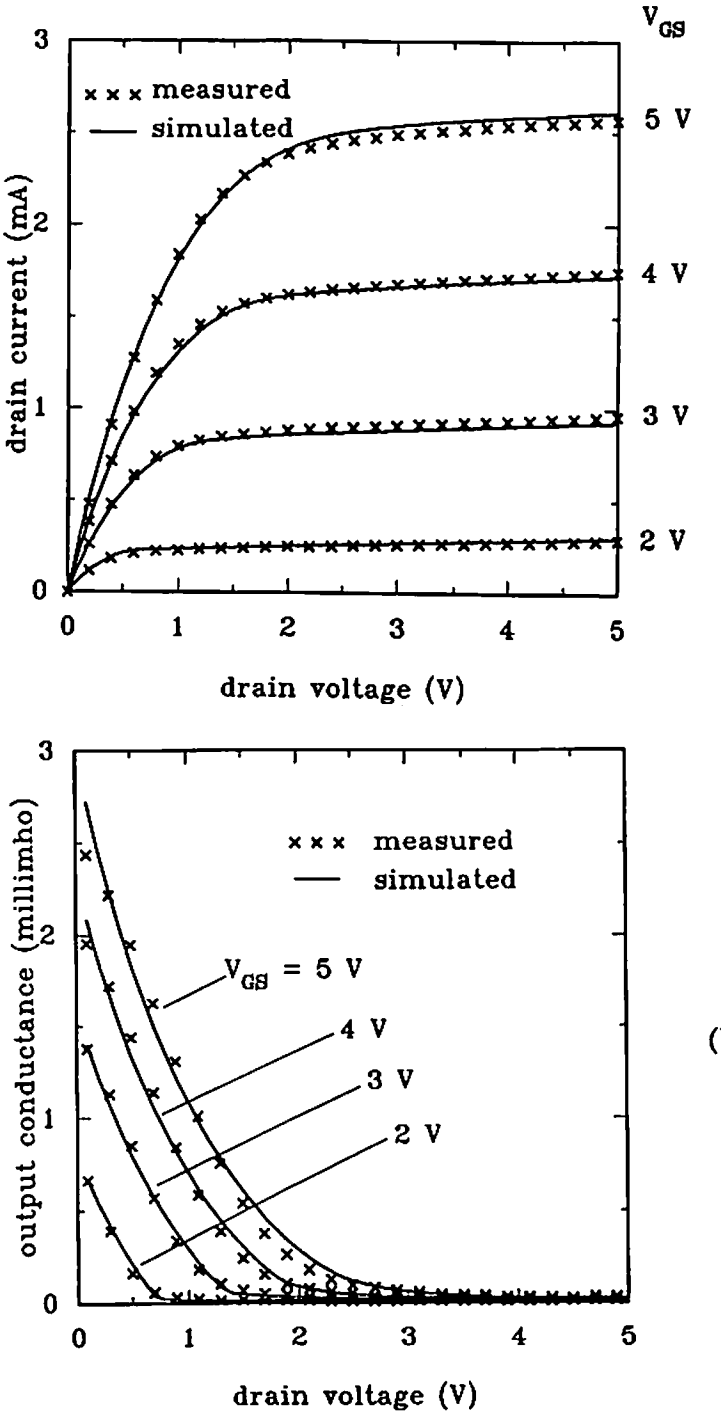


Fig. 3.7 BSIM_plus characteristics for an NMOS transistor with W/L = 10 μm/0.6 μm. (a) Drain current. (b) Output conductance.

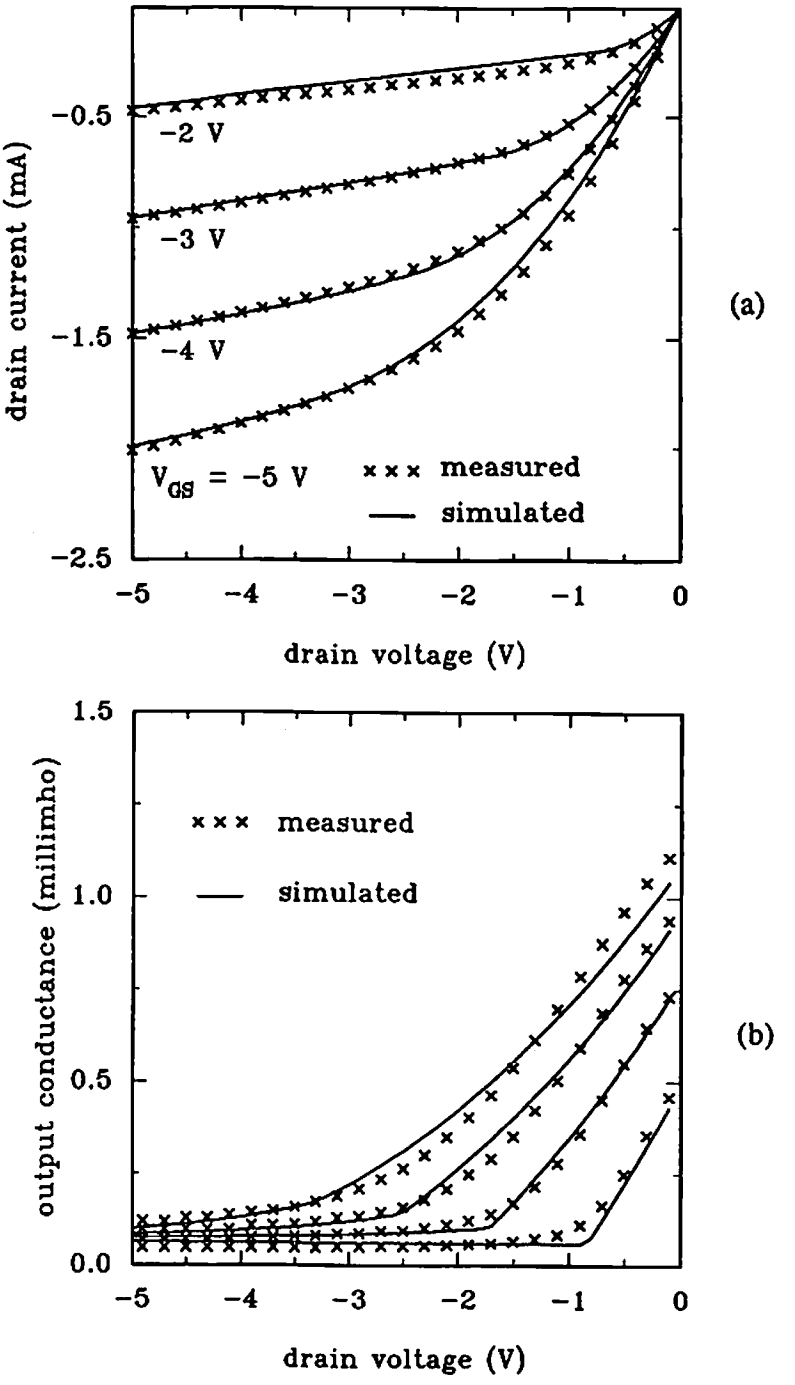


Fig. 3.8 BSIM_plus characteristics for a PMOS transistor with W/L = 10 μm/0.6 μm. (a) Drain current. (b) Output conductance.

By equating (3.29) and (3.30) the term K is defined as,

$$K \equiv \frac{1 + v_c + \sqrt{1 + 2v_c}}{2}, \tag{3.31}$$

where,

$$v_c \equiv \frac{V_{GS} - V_{th}}{aE_{CRIT}L}. \tag{3.32}$$

The saturation voltage given in (3.28) can be rewritten as,

$$V_{DSAT} = \frac{V_{GS} - V_{th}}{a\sqrt{K}}. \tag{3.33}$$

The saturation voltage is the drain voltage boundary between the linear and saturation regions of operation. The drain current characteristics vs. the drain voltage and gate voltage for sub-half-micron NMOS transistors with W/L = 10 μm/0.15 μm and 10 μm/0.25 μm are shown in Fig. 3.5 and Fig. 3.6, respectively. The drain current and output conductance characteristics of NMOS and PMOS transistors with W/L = 10 μm/0.6 μm are shown in Fig. 3.7 and Fig. 3.8, respectively.

3.1.5 Weak-Inversion Region

The MOS transistor operates in the weak-inversion region when $V_{GS} < V_{th}$. The design of low-power circuits using MOS transistors biased in the subthreshold region requires an accurate subthreshold drain current expression. Continuity of the drain current and its derivatives between the

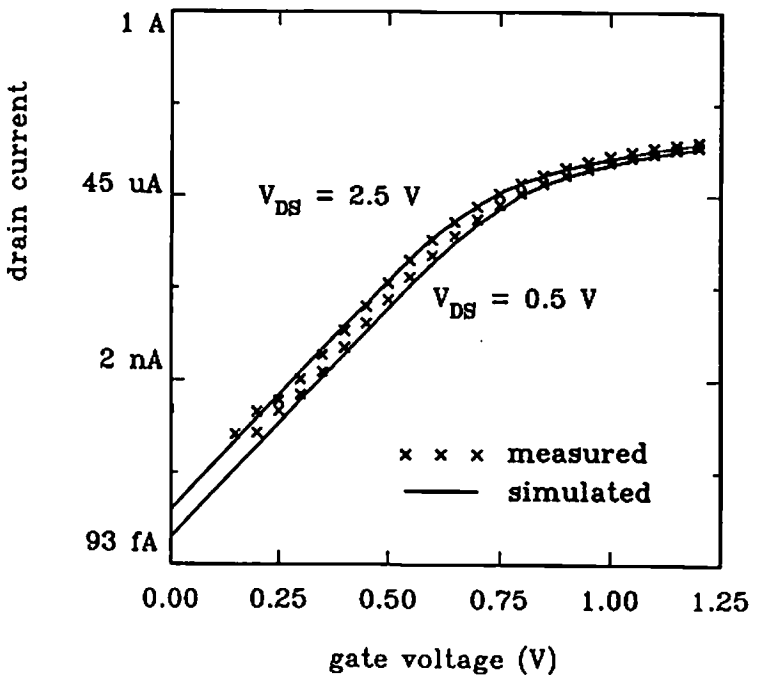


Fig. 3.9 Weak-inversion drain current characteristics of an NMOS transistor with W/L = 25 μm/0.4 μm.

weak-inversion and strong-inversion regions is also highly desirable. The drain current in the weak-inversion region is dominated by the diffusion component which is given by [3.2],

$$I_{EXP} = I_0 \frac{W}{L} e^{\frac{V_{GS} - V_{th}}{nV_T}} \left[1 - e^{-\frac{V_{DS}}{V_T}} \right] \tag{3.34}$$

This component increases exponentially with the gate voltage. At high gate biases close to the transition between the weak-inversion and strong-inversion regions and within the strong-inversion region, the exponentially increasing diffusion current is clamped by a limiting scheme which is given by,

$$I_{DS,weak} = \frac{I_{EXP}\, I_{LIM}}{I_{EXP} + I_{LIM}}. \tag{3.35}$$

The suggested limiting current is given by,

$$I_{LIM} = \frac{\mu_0 C_{OX}}{2} \cdot \frac{W}{L}. \tag{3.36}$$

The BSIM_plus weak-inversion drain current characteristics of an NMOS transistor with W/L = 25 μm/0.4 μm from TRW, Inc., are shown in Fig. 3.9.

3.1.6 Total Drain Current

If the subthreshold slope coefficient is specified, the total drain current that is calculated by the BSIM_plus model is obtained by summing the strong-inversion and weak-inversion components. If $V_{DS} \leq V_{DSAT}$, the transistor is in the triode region and the total drain current is calculated as,

$$I_{DS,total} = I_{DS,triode} + I_{DS,weak} \quad (3.37)$$

If $V_{DS} > V_{DSAT}$, the transistor is in the saturation region and the total drain current is calculated as,

$$I_{DS,total} = I_{DS,satn.} + I_{DS,weak} \quad (3.38)$$

Combining the weak-inversion and strong-inversion components by summation ensures the continuity of the drain current in the transition between these two regions of operation.

Another method of combining the drain current in the weak-inversion and strong-inversion regions is to define a transition region around the threshold voltage. The drain currents at the lower and upper boundaries of the transition region are given by the weak-inversion and strong-inversion expressions. Within the transition region the drain current values are obtained by a spline function that matches the boundary values.

3.2 Pseudo-Boundary Method

Advanced digital and analog VLSI circuits could require the use of transistors that are distributed over a large geometric space. In general, only a small region of the geometric design space is characterized in the laboratory in order to extract parameter values. The transistor model must enable circuit designers to explore the geometric space beyond the region of characterization. One conventional approach to providing transistor model parameter values over a large geometric space [3.15] involves partitioning the

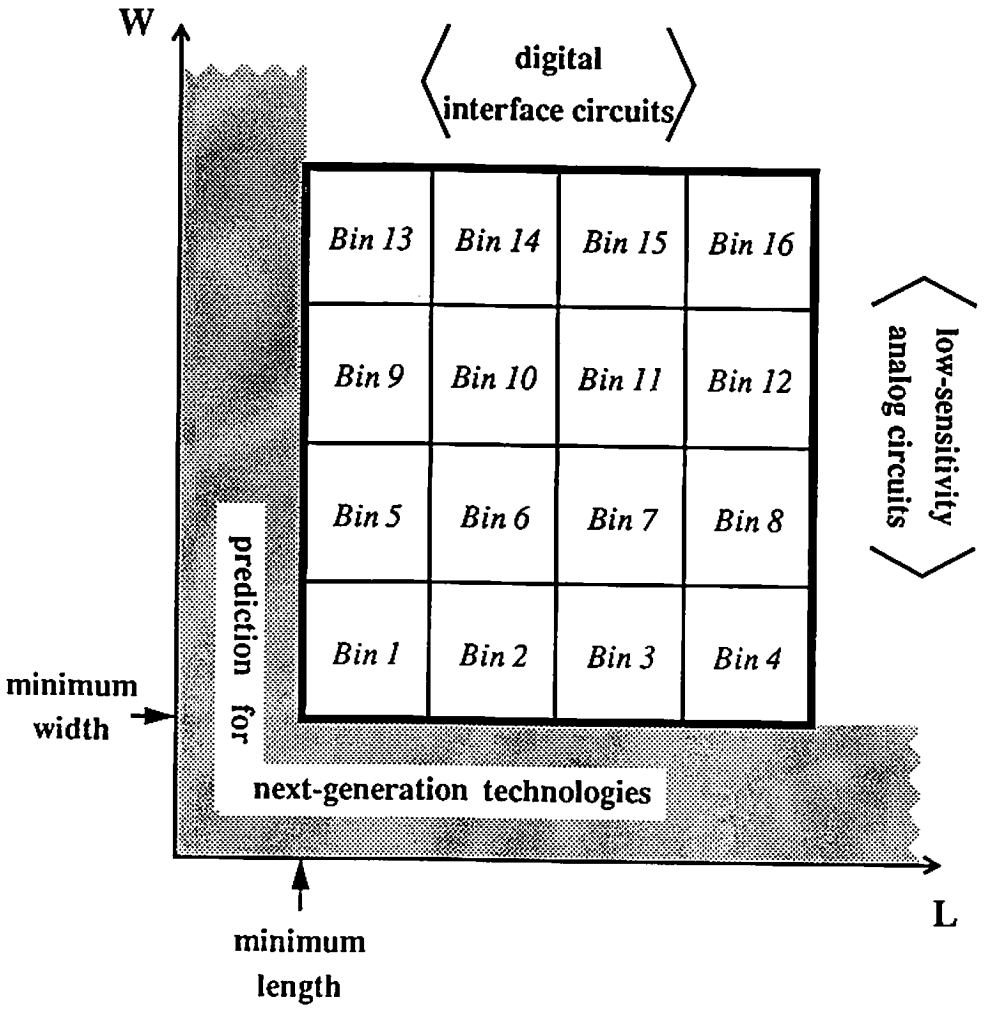


Fig. 3.10 Conventional multiple-bin technique to characterize a large geometric design space [3.15].

geometric space into several bins as shown in Fig. 3.10. In each bin, a parameter set is extracted with the intention of providing maximum accuracy within that bin. In this way, high accuracy can be achieved over a large geometric space without producing abnormal results in any of the bins where parameters are extracted. However, the problem in this approach lies in the transition from one geometric bin to another. Since the parameter sets used in two adjacent bins are extracted separately using data from different sets of transistors, the drain current may not vary monotonically across the boundary between the two bins. This is in contradiction to the principles of device operation and observations of measurement results. Such non-monotonicity can also cause convergence problems in automatic circuit synthesis programs [3.16,3.17] that use circuit simulation results to search across the geometric design space. The multiple-bin approach also fails to address the problem of modeling transistors beyond the periphery of the characterized region. These include long-channel transistors used in the design of analog circuits, wide-channel transistors used in special digital driver circuits, and small-geometry transistors that can be used to predict the effect of using next-generation technologies.

The pseudo-boundary method extends the use of a parameter set beyond the region of laboratory characterization [3.18]. The method involves clamping the evaluation of second-order effects at the boundaries of a primary region as shown in Fig. 3.11. The primary region is determined by using the criterion that abnormal drain current characteristics are not produced during simulation of transistors within this region. The upper and lower length

bounds of the primary region are L_{LNG} and L_{SHT}, while the corresponding width bounds are W_{WID} and W_{NRW}, respectively. The first-order scaling of the drain current with geometry is done by the $\frac{W}{L}$ term that is given in the following saturation drain current expression,

$$I_{DS,satn.} = \frac{\mu_0 C_{OX} \frac{W}{L} \left[V_{GS} - V_{th}\right]^2 F_S}{\left[1 + (U_{GSZ} + \frac{U_{GSL}}{L})(V_{GS} - V_{th}) - U_{BS} V_{BS}\right] 2aK}. \quad (3.39)$$

The effective width and length of the transistor are used in the calculation of this $\frac{W}{L}$ term over the entire geometric design space. In the evaluation of other second-order geometric dependencies, the length and width to be used are determined according to,

$$L = \begin{cases} L_{SHT} & \text{if } L \le L_{SHT}, \\ L_{LNG} & \text{if } L \ge L_{LNG}, \end{cases} \quad (3.40)$$

and

$$W = \begin{cases} W_{NRW} & \text{if } W \le W_{NRW}, \\ W_{WID} & \text{if } W \ge W_{WID}. \end{cases}$$

This is a set of conditional constraints that modifies the geometric dependence scheme in order to extend the use of a parameter set. For transistors beyond the primary region, the second-order effects are evaluated at the boundaries of the primary region. This is the central feature of the pseudo-boundary method.

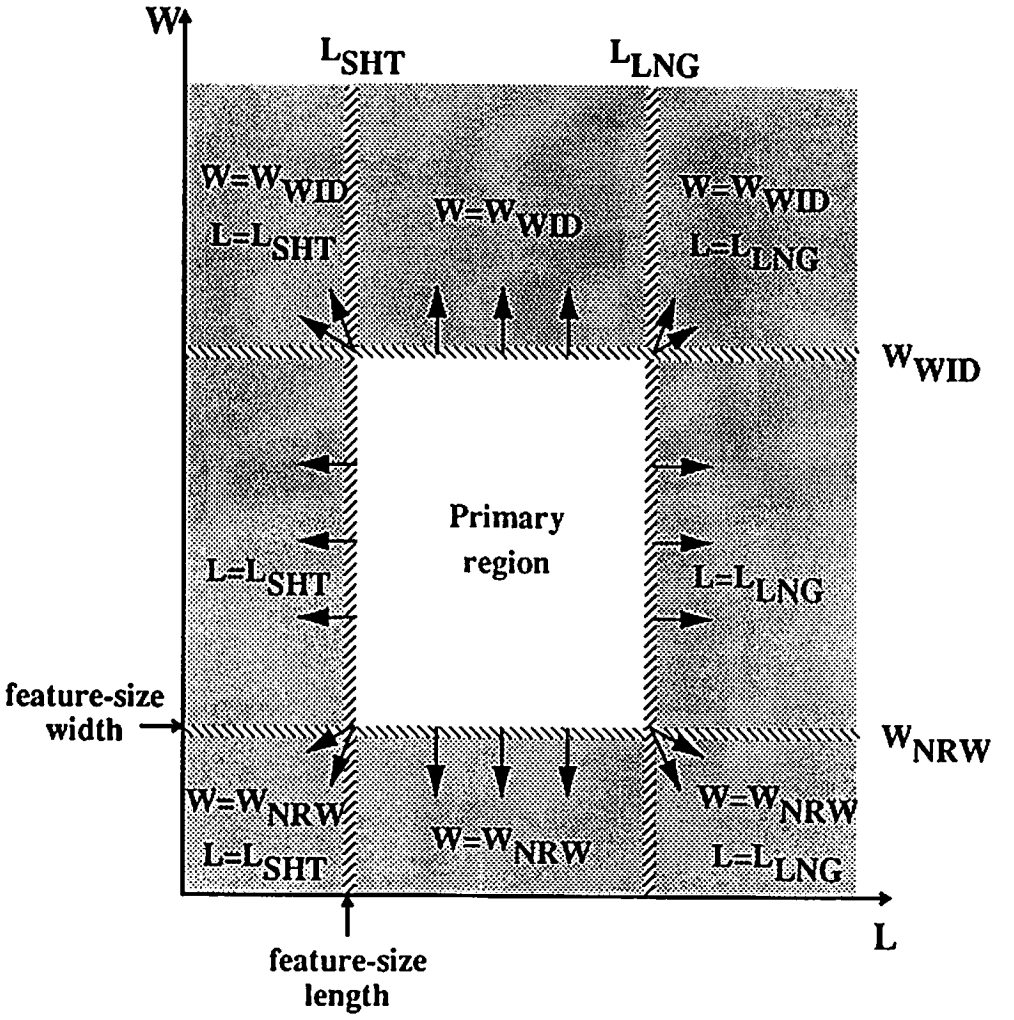


Fig. 3.11 The pseudo-boundary method extends the applicability of a single parameter set over the entire geometric design space.

The effectiveness of the pseudo-boundary method depends upon the suitable determination of the bounds L_{SHT}, L_{LNG}, W_{NRW}, and W_{WID}. The upper length and width bounds of the primary region, L_{LNG} and W_{WID}, can be defined as the longest length and widest width of the transistors used for actual parameter extraction. The lower length and width bounds, L_{SHT} and W_{NRW}, are determined in a systematic manner according to the search algorithm shown in Fig. 3.12. In the determination of L_{SHT}, for example, the algorithm is repeated for different widths within the primary region and the upper bound of the resulting length values is chosen as L_{SHT}. L_{SHT} and W_{NRW} represent the geometries at which physical constraints are violated and abnormal results are produced by the geometry dependence terms of the model. Choosing the lower bounds in this manner allows increased exploitation of the accuracy that is included in the small-geometry effect terms of the model.

3.3 Substrate Current Expression

As device geometries shrink with advances in fabrication technologies, the lateral electric field at the drain end of the channel increases. Impact ionization can occur in this high-field region, causing electron-hole pair generation within the bulk depletion region and resulting in a substrate current. The impact ionization region is shown in Fig. 3.13. The substrate current is important in submicron VLSI circuit design because it can affect the output conductance and it could be used as a monitor of transistor degradation. The

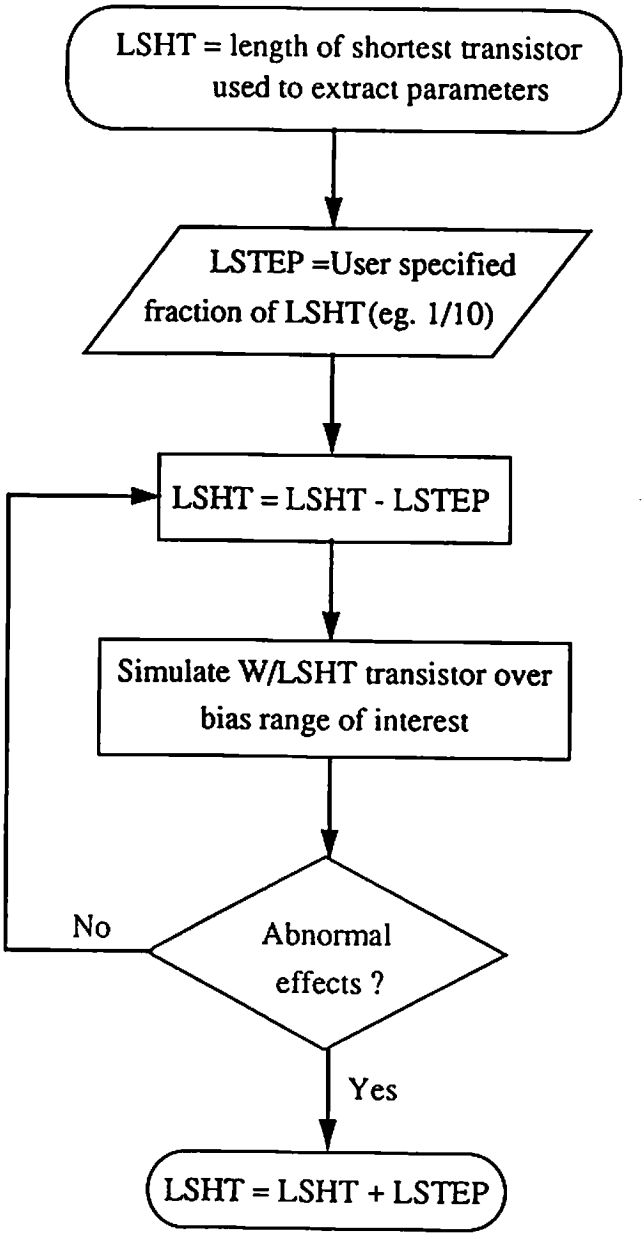


Fig. 3.12 Flowchart to determine the lower length bound of the primary region, L_{SHT}.

BSIM_plus model includes a built-in substrate current expression in order to enhance its capability in an integrated VLSI simulation environment. This expression for the substrate current is based on the model proposed by Mar et al. [3.19] and is given by,

$$I_{SUB} = I_{DS} \cdot \Delta L \cdot A \cdot e^{-\frac{B}{E_{max}}}, \tag{3.41}$$

where,

$$E_{max} = \frac{V_{DS} - V_P}{L - \Delta L}, \tag{3.42}$$

and,

$$V_P = \frac{L \cdot E_{CRIT} \cdot (V_{GS} - V_{th})}{L \cdot E_{CRIT} + V_{GS} - V_{th}}. \tag{3.43}$$

The impact ionization parameters, A and B, are the additional parameters required to calculate the substrate current. ΔL is a BSIM_plus model parameter and E_{max} can be calculated from the drain current parameters. Other substrate current expressions can also be linked to the BSIM_plus model. The D.C. substrate current that is calculated by the BSIM_plus model can be used by reliability simulation programs [3.20,3.21] in order to predict degradation in circuit performance and circuit lifetime under hot-carrier generation due to electrical stress. Measured and simulated data for an NMOS transistor with W/L = 10 μm/0.75 μm are compared in Fig. 3.14.

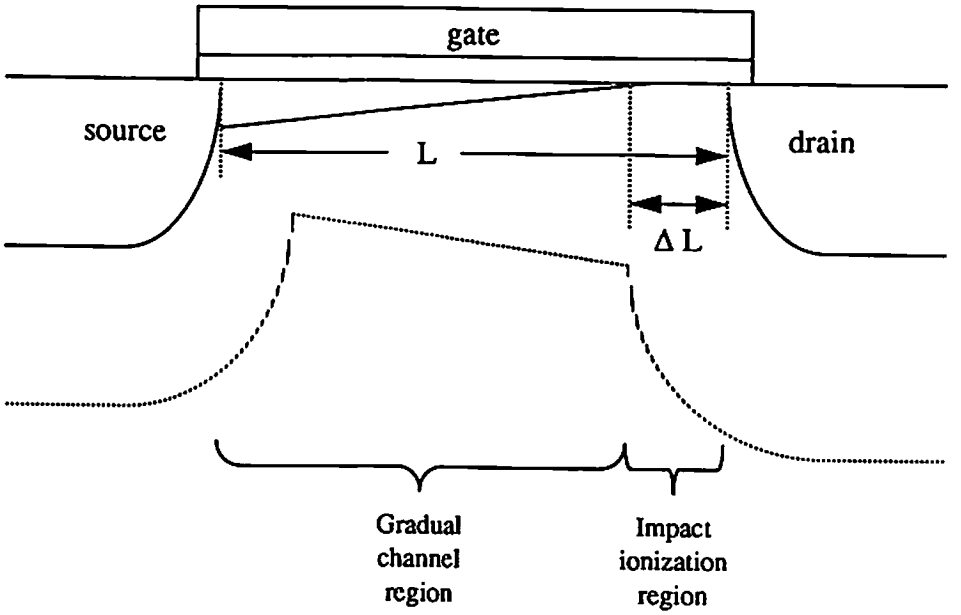


Fig. 3.13 Transistor channel under high electrical stress showing region of impact ionization.

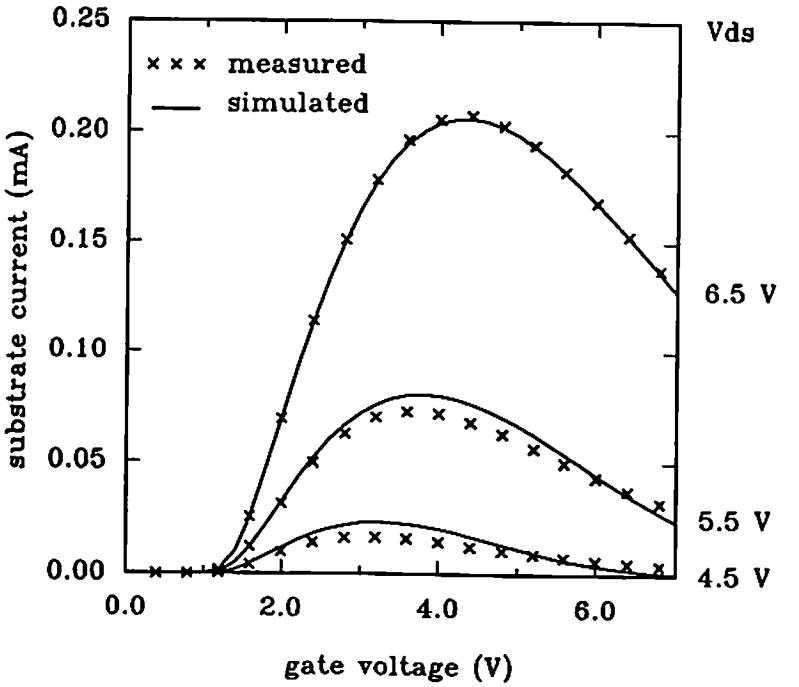


Fig. 3.14 Substrate current characteristics for an NMOS transistor with W/L = 10 μm/0.75 μm.

3.4 Parasitic Resistances

The drain current expressions that have been derived in the previous sections are used to model the drain current within the intrinsic region of the MOS transistor. In sub-half-micron transistors, the parasitic source and drain resistances contribute a significant voltage drop that can affect the performance of the transistor. The BSIM_plus model includes expressions to calculate the effect of these extrinsic parasitic resistances.

The different components of the parasitic resistance in the source/drain region are shown in Fig. 3.15 [3.22]. The components include,

- R_{co}: the contact resistance,
- R_{sh}: the diffusion sheet resistance,
- R_{sp}: the spreading resistance, and
- R_{ac}: the accumulation layer resistance.

The contact resistance, R_{co}, is the resistance between the metal contact and the diffusion layer under the contact window. When the length of the contact window is very small, the contact resistance is inversely proportional to this length. However, when the length of the contact window sufficiently large, the contact resistance saturates at a minimum value which is independent of the length of the window. The contact resistance is given by [3.22],

$$R_{co} \simeq \frac{\sqrt{\rho_{\square}\,\rho_c}}{W}, \tag{3.44}$$

where $\rho_{\square}$ is the sheet resistance per square of the source/drain diffusion layer, and ρ_c is the contact resistivity between the metal and diffusion layers.

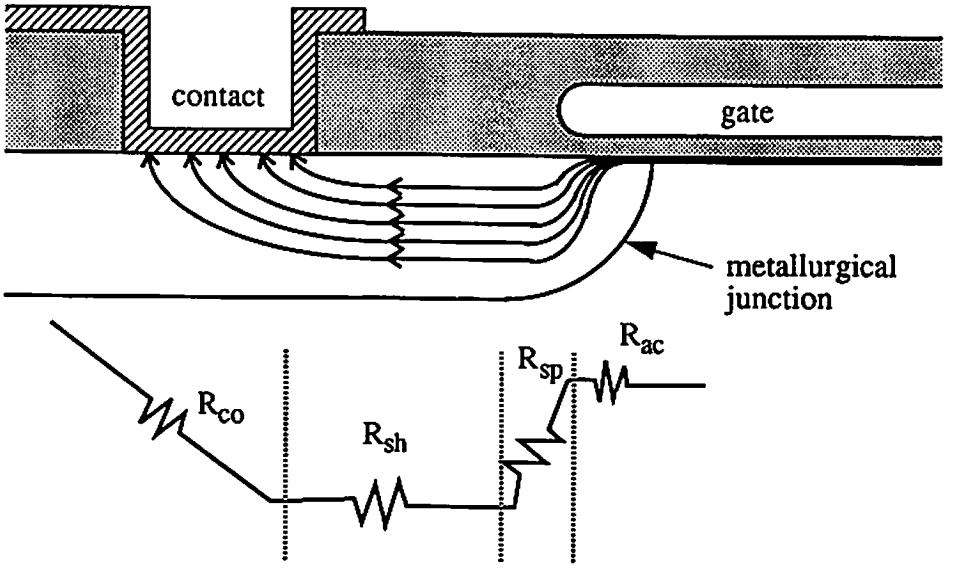


Fig. 3.15 Components of parasitic resistances in source/drain regions [3.22].

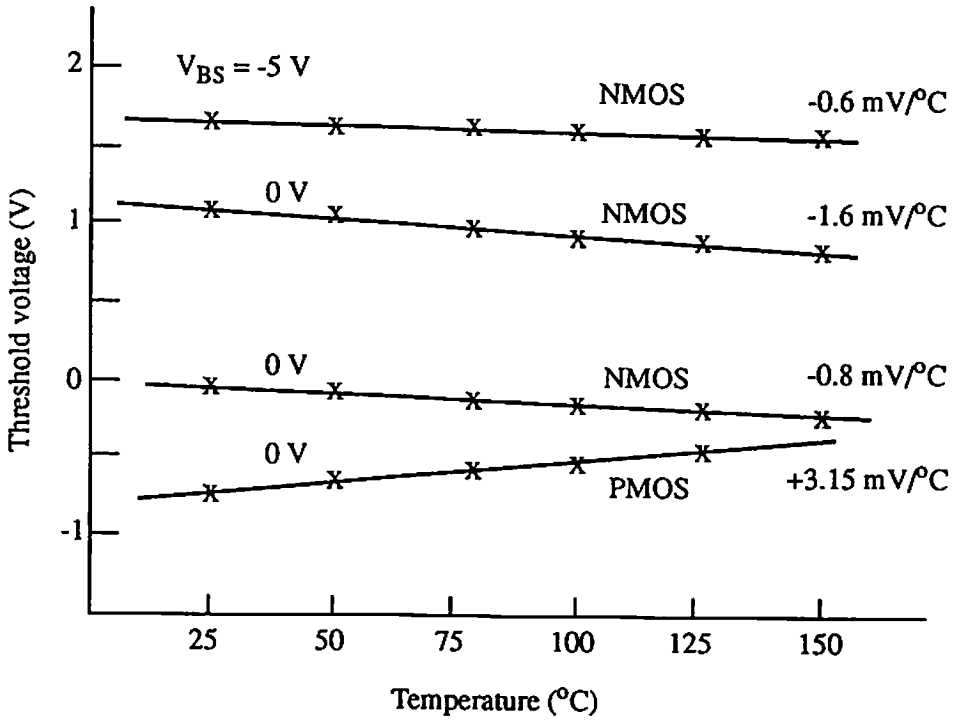


Fig. 3.16 Measured threshold voltage data for different MOS transistors [3.25].

The minimum length of the contact window that is required for the contact resistance to be independent of this length is frequently ensured by the design rules of the technology.

The diffusion sheet resistance, R_{sh}, of the source/drain diffusion region can be calculated from $\rho_{\square}$ and S, the spacing between the contact edge and the channel by,

$$R_{sh} = \frac{\rho_{\square}\, S}{W}. \tag{3.45}$$

The spreading resistance, R_{sp}, is due to the radially divergent pattern of the current as it flows from the thin channel region to the thicker source/drain diffusion layer. Assuming an abrupt doping profile at the edge of the source/drain diffusion layer, the spreading resistance s given by [3.22],

$$R_{sp} = \frac{0.64\ \rho_{s/d}}{W}\ \ln\left[\frac{0.37\ X_j}{X_c}\right], \tag{3.46}$$

where the resistivity and thickness of the source/drain diffusion layer are given by $\rho_{s/d}$ and X_j, respectively, and X_c is the thickness of the channel. The additional component due to resistance of the accumulation layer, R_{ac}, is significant only in the case of a gradual doping gradient at the edge of the source/drain diffusion layer and goes to zero under the assumption of a step junction.

Based upon this analysis, the extrinsic parasitic resistances in the source and drain regions are modeled in BSIM_plus with a constant term and an inverse width scaling term. The source parasitic resistance is given by,

$$R_S = R_{S0} + \frac{R_{SW}}{W}, \tag{3.47}$$

and the drain parasitic resistance is given by,

$$R_D = R_{D0} + \frac{R_{DW}}{W}. \tag{3.48}$$

3.5 Charge and Capacitance Model

MOS transistor capacitances include overlap capacitances, junction capacitances and intrinsic capacitances. Modeling the intrinsic capacitances in sub-half-micron transistors pose many challenges of charge conservation, channel-charge partition, distributed channel effect and other short-channel effects [3.31]. Researchers have proposed analytical and table look-up methods to simulate the intrinsic capacitances.

The charges in the MOS transistor are modeled in terms of the gate, bulk and channel charges. These charges are given by the following expressions [3.2],

$$q_g(y) = C_{OX}\left[V_{GS} - V_{FB} - \phi_s - V_y\right], \tag{3.49}$$

$$q_c(y) = -C_{OX}\left[V_{GS} - V_{th} - \alpha_x V_y\right], \tag{3.50}$$

and,

$$q_b(y) = -C_{OX}\left[V_{th} - V_{FB} - \phi_s - (1 - \alpha_x)V_y\right], \tag{3.51}$$

where,

$$\alpha_x = a\left[1 + \frac{V_{GS} - V_{th}}{E_{CRIT}\, L}\right]. \tag{3.52}$$

The electron quasi-Fermi potential with respect to the source is given by V_y. The constraint of charge neutrality in the one-dimensional MOS capacitor structure requires that,

$$q_g + q_c + q_b = 0. \tag{3.53}$$

The total charges that are stored in the bulk, gate and channel regions can be obtained by integrating the charge density expression over the active region giving,

$$Q_G = W\int_0^L q_g(y)dy, \tag{3.54}$$

$$Q_B = W\int_0^L q_b(y)dy, \tag{3.55}$$

and,

$$Q_C = W\int_0^L q_c(y)dy. \tag{3.56}$$

By substituting the expressions for the charge densities and performing the integration, the following expressions for the total charges can be obtained,

$$Q_G = WLC_{OX}\left[V_{GS} - V_{FB} - \phi_s - \frac{V_{DS}}{2} + \frac{V_{DS}}{12}\frac{\alpha_x V_{DS}}{\left[V_{GS} - V_{th} - \frac{\alpha_x}{2}V_{DS}\right]}\right], \tag{3.57}$$

$$Q_B = WLC_{OX}\left[- V_{th} + V_{FB} + \phi_s + \frac{(1 - \alpha_x)}{2}V_{DS} - \frac{(1 - \alpha_x)V_{DS}}{12}\frac{\alpha_x V_{DS}}{\left[V_{GS} - V_{th} - \frac{\alpha_x}{2}V_{DS}\right]}\right], \quad (3.58)$$

$$Q_C = - WLC_{OX}\left[V_{GS} - V_{th} - \frac{\alpha_x}{2}V_{DS} + \frac{\alpha_x V_{DS}}{12}\frac{\alpha_x V_{DS}}{\left[V_{GS} - V_{th} - \frac{\alpha_x}{2}V_{DS}\right]}\right]. \quad (3.59)$$

The total charges in the transistor also follow the charge neutrality constraint giving,

$$Q_G + Q_C + Q_B = 0. \quad (3.60)$$

Several schemes have been proposed in the literature for the partitioning of the channel charge between the source and drain terminals. A physically meaningful method developed by Ward et al. indicates that the point of partition is at 3/5 of the channel from the source end. According to this partioning scheme, the source and drain charges are given by the following expressions in the triode region,

$$Q_S = - WLC_{OX}\left[\frac{V_{GS} - V_{th}}{2} + \frac{\alpha_x V_{DS}}{12}\frac{\alpha_x V_{DS}}{\left[V_{GS} - V_{th} - \frac{\alpha_x}{2}V_{DS}\right]} - \frac{\alpha_x V_{DS}}{\left[V_{GS} - V_{th} - \frac{\alpha_x}{2}V_{DS}\right]^2}\left[\frac{(V_{GS} - V_{th})^2}{6}\right.\right.$$

$$- \frac{\alpha_x V_{DS}(V_{GS} - V_{th})}{8} + \frac{\alpha_x^2 V_{DS}^2}{40}\Bigg]\Bigg], \tag{3.61}$$

and,

$$Q_D = - WLC_{OX}\Bigg[\frac{V_{GS} - V_{th}}{2} - \frac{\alpha_x V_{DS}}{2} + \frac{\alpha_x V_{DS}}{\left[V_{GS} - V_{th} - \frac{\alpha_x}{2}V_{DS}\right]^2}$$

$$\left[\frac{(V_{GS} - V_{th})^2}{6} - \frac{\alpha_x V_{DS}(V_{GS} - V_{th})}{8} + \frac{\alpha_x^2 V_{DS}^2}{40}\right]\Bigg]. \tag{3.62}$$

In the saturation region, the charge expressions are given by,

$$Q_G = WLC_{OX}\left[V_{GS} - V_{FB} - \phi_s - \frac{V_{GS} - V_{th}}{3\alpha_x}\right], \tag{3.63}$$

$$Q_B = WLC_{OX}\left[V_{FB} + \phi_s - V_{th} + \frac{(1 - \alpha_x)(V_{GS} - V_{th})}{3\alpha_x}\right], \tag{3.64}$$

$$Q_S = - \frac{2}{5}WLC_{OX}(V_{GS} - V_{th}), \tag{3.65}$$

and,

$$Q_D = - \frac{4}{15}WLC_{OX}(V_{GS} - V_{th}). \tag{3.66}$$

The general capacitance expressions can be written as,

$$C_{ij} = \delta_{ij}\frac{\partial Q_i}{\partial V_j}, \tag{3.67}$$

where,

$$\delta_{ij} = \begin{cases} 1 & \text{if } i = j \\ -1 & \text{if } i \neq j \end{cases} \tag{3.68}$$

and i,j stand for the g, b, d and s, the gate, bulk, drain and source terminals. Charge neutrality in the transistor also implies that the sum of the terminal capacitive currents is zero, and the capacitances are constrained by the expressions,

$$C_{gg} + C_{bg} + C_{dg} + C_{sg} = 0, \tag{3.69}$$

$$C_{gb} + C_{bb} + C_{db} + C_{sb} = 0, \tag{3.70}$$

$$C_{gd} + C_{bd} + C_{dd} + C_{sd} = 0, \tag{3.71}$$

$$C_{gs} + C_{bs} + C_{ds} + C_{ss} = 0. \tag{3.72}$$

3.6 Temperature Dependence

Circuit designers require the ability to predict the variation of circuit performance with temperature. Typical temperature ranges used for performance verification are 0°C to 70°C for commercial applications and – 55°C to 125°C for military applications. The changes in temperature predominantly affect the threshold voltage and carrier mobility of the transistors [3.24]. The effect of temperature on circuit performance can be simulated using the BSIM_plus model. The BSIM_plus model uses the parameter B_{Vth} to calculate the temperature dependence of the threshold voltage, if this parameter is

provided by the user. Otherwise, the temperature dependence of the threshold voltage is calculated based upon device physics. The effect of temperature on the mobility is calculated by using the parameter B_μ and B_{VS}. The temperature dependence expressions for the BSIM_plus model are given in (3.81), (3.83), (3.84), (3.85), and (3.88).

3.6.1 Threshold Voltage Shift

The expression used to calculate the threshold voltage in the BSIM_plus model is given in (3.7). The threshold voltage changes with temperature because of changes in the energy required to move electrons into the conduction band in order to form the channel. Measurement data showing the variation of the threshold voltage with temperature for different types of MOSFETs are given in Fig. 3.16 [3.25]. In all cases the gates were n-type doped polysilicon. While the upper graphs refer to implanted n-channel transistors, the middle graphs refer to an unimplanted n-channel transistor and a p-channel transistor.

In the BSIM_plus model, the components of the threshold voltage expression that are highly sensitive to temperature include the flat-band voltage and the surface-inversion potential. The expression for the surface inversion potential of the p-type substrate of NMOS transistors that is given in (3.1) can be rewritten as,

$$|\phi_s| \simeq \frac{2kT}{q} \ln\left[\frac{N_{SUB}}{n_i}\right]. \tag{3.73}$$

The doping concentration in the substrate is given by N_{SUB}, and this is independent of the temperature. The relationship between the intrinsic carrier concentration and the temperature is given by [3.7],

$$n_i \alpha T^{\frac{3}{2}} e^{-\frac{E_G}{2kT}}. \tag{3.74}$$

The energy band-gap of silicon as a function of temperature is given by [3.7],

$$E_G(T) = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}. \tag{3.75}$$

This expression has a negative temperature coefficient.

The temperature dependence of the threshold voltage in the BSIM_plus model has been included by calculating the flat-band voltage and surface-inversion potential as temperature-dependent quantities. The nominal temperature, T_o, is the temperature at which the BSIM_plus drain current parameter values were extracted. From (3.73), we can write,

$$\frac{\phi_s(T)}{T} = \frac{2k}{q} \ln\left[\frac{N_{SUB}}{n_i(T)}\right], \tag{3.76}$$

and,

$$\frac{\phi_s(T_o)}{T_o} = \frac{2k}{q} \ln\left[\frac{N_{SUB}}{n_i(T_o)}\right]. \tag{3.77}$$

Subtracting (3.77) from (3.76) and rearranging terms, we can write,

$$\phi_s(T) = \phi_s(T_o)\left[\frac{T}{T_o}\right] - \frac{2kT}{q} \ln\left[\frac{n_i(T)}{n_i(T_o)}\right]. \tag{3.78}$$

Using the temperature dependence of the intrinsic carrier concentration given in (3.74), we can write,

$$\frac{n_i(T)}{n_i(T_o)} = \left[\frac{T}{T_o}\right]^{\frac{3}{2}} e^{-\frac{E_G(T)}{2kT} + \frac{E_G(T_o)}{2kT_o}}, \tag{3.79}$$

which can be rewritten as,

$$-\frac{2kT}{q}\ln\left[\frac{n_i(T)}{n_i(T_o)}\right] = -\frac{2kT}{q}\frac{3}{2}\ln\left[\frac{T}{T_o}\right] + E_G(T) - E_G(T_o)\left[\frac{T}{T_o}\right]. \tag{3.80}$$

Substituting (3.80) into (3.78) we get,

$$\phi_s(T) = \phi_s(T_o)\left[\frac{T}{T_o}\right] - \frac{3kT}{q}\ln\left[\frac{T}{T_o}\right] + E_G(T) - E_G(T_o)\left[\frac{T}{T_o}\right]. \tag{3.81}$$

For an NMOS transistor which has a p-type substrate and an n-type polysilicon gate, the flat-band voltage is given by,

$$V_{FB} = -\frac{E_G}{2} - \frac{\phi_s}{2} - \frac{Q_o}{2}. \tag{3.82}$$

Based upon this expression, the temperature dependence of the flat-band voltage is given by,

$$V_{FB}(T) = V_{FB}(T_o) + \frac{E_G(T_o)}{2} + \frac{\phi_s(T_o)}{2} - \frac{E_G(T)}{2} - \frac{\phi_s(T)}{2}. \tag{3.83}$$

The temperature dependence of the threshold voltage can also be simulated by using a threshold-voltage temperature-coefficient. Such a scheme is especially useful in cases where measured temperature-dependent threshold voltage data such as that shown in Fig. 3.16 are available. The user can specify the threshold-voltage temperature-coefficient as a parameter, B_{Vth}, and

the temperature-dependent threshold voltage can be calculated from,

$$V_{th}(T) = V_{th}(T_o) + B_{Vth}\left[T - T_o\right]. \tag{3.84}$$

3.6.2 Temperature Dependence of Carrier Mobility

Reported measurement data from several researchers indicate that the carrier mobility has a logarithmic dependence on temperature. Jacoboni et al. [3.26] reported that the electron mobility follows a $T^{-2.42}$ dependence, while the hole mobility follows a $T^{-2.2}$ dependence. In the BSIM_plus model, the intrinsic carrier mobility depends upon the temperature as given by,

$$\mu(T) = \mu(T_o)\left[\frac{T}{T_o}\right]^{-B_\mu}, \tag{3.85}$$

where B_μ is the slope of the log μ_0 vs. log T measurement data line.

It is reported that the saturation velocity has a $T^{-0.87}$ dependence for electrons and a $T^{-0.52}$ dependence for holes [3.26]. This can be written as,

$$v_{sat} \alpha T^{-B_{vs}}. \tag{3.86}$$

Since the saturation velocity, carrier mobility, and critical field for velocity saturation are related by,

$$E_{CRIT} \alpha \frac{v_{sat}}{\mu_{eff}}, \tag{3.87}$$

the temperature dependence of the saturation velocity can be incorporated into the critical field for velocity saturation. In the BSIM_plus model this is

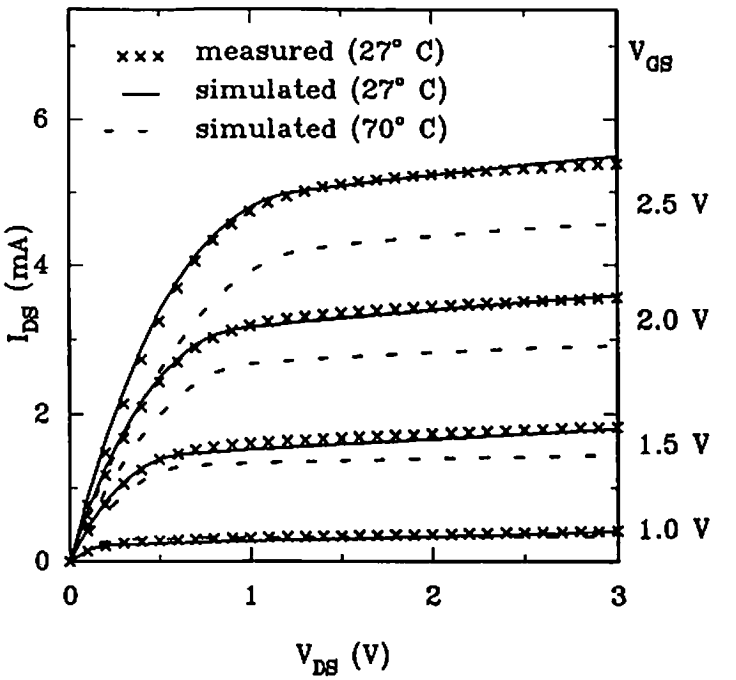


Fig. 3.17 Temperature-dependent drain current characteristics of an NMOS transistor with W/L = 25 μm/0.4 μm.

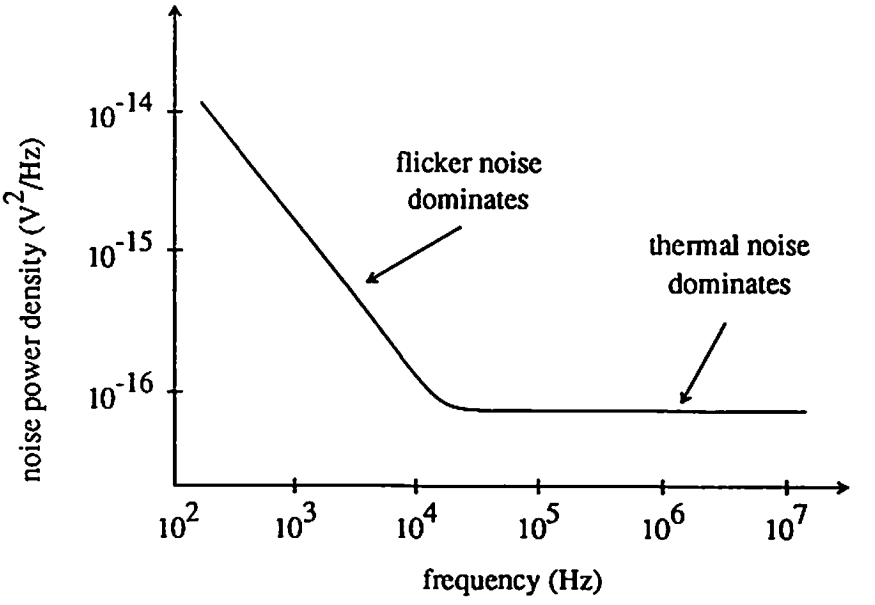


Fig. 3.18 Total noise power density of an MOS transistor.

included as,

$$E_{CRIT}(T) = E_{CRIT}(T_o)\left[\frac{T}{T_o}\right]^{-B_{VS}+B_{\mu}}, \tag{3.88}$$

where B_{vs} is the BSIM_plus model parameter for the temperature dependence of the saturation velocity. The temperature dependence effects on drain current predicted by the BSIM_plus model are shown in Fig. 3.17.

3.6.3 Temperature Dependence Based on Constant Drain Current

The discussion on temperature-dependent threshold voltage in Section 3.6.1 assumed the turn-on condition of the transistor to be defined as the point where surface inversion was achieved. The turn-on condition can also be defined as the voltage required to place a fixed quantity of charge in the channel which corresponds to a constant current in the channel. By using this condition, the temperature-dependent behavior of the MOS transistor can be analyzed differently.† The charge in the channel can be related to the quasi-Fermi potential in the channel by,

$$n = N_c\, e^{-\frac{E_c - q\phi_n}{kT}}. \tag{3.89}$$

where N_c is the effective density of states in the conduction band. Take the natural logarithms and then find derivatives with respect to temperature to

† This analysis was developed during discussions with Professor C. R. Crowell, Department of Electrical Engineering - Electrophysics, University of Southern California, in October, 1992.

get,

$$0 = \frac{\partial \ln[N_c]}{\partial T} - \frac{1}{kT}\frac{\partial (E_c - q\phi_n)}{\partial T} + \frac{(E_c - q\phi_n)}{kT^2}. \tag{3.90}$$

From (3.89),

$$-\frac{1}{T}\ln\left[\frac{n}{N_c}\right] = \frac{(E_c - q\phi_n)}{kT^2}. \tag{3.91}$$

Since N_c has a $T^{\frac{3}{2}}$ dependence on the temperature,

$$\frac{\partial \ln[N_c]}{\partial T} = \frac{3}{2}\frac{1}{T}. \tag{3.92}$$

Substituting (3.91) and (3.92) into (3.89),

$$\frac{\partial \phi_n}{\partial T} = \frac{k}{q}\ln\left[\frac{n}{N_c}\right] - \frac{3}{2}\frac{k}{q}. \tag{3.93}$$

The voltage change required to maintain a constant current in the channel is,

$$\frac{\partial \phi_n}{\partial T} = 0.086\ln\left[\frac{n}{N_c}\right] - 0.129\ \text{mV/°C}. \tag{3.94}$$

This analysis considers the turn-on condition of the transistor to be independent of physical quantities deep in the bulk semiconductor, and arrives at a temperature dependence that is independent of the energy band gap of the substrate.

3.7 Thermal and Flicker Noise Effects

Thermal noise is a physical phenomenon associated with any conductor. This noise is due to the random motion of electrons in the conductor and is directly proportional to the absolute temperature of the conductor. The spectral density of thermal noise is independent of frequency. The BSIM_plus model includes the contribution of thermal noise in the MOS transistor due to the source and drain conductances and the transconductance of the channel. The noise associated with these conductances can be represented as voltage sources in series with the conductances or current sources in parallel with the conductances.

Two theories have been proposed [3.27] to explain the source of flicker noise. The Carrier Number Fluctuation Theory attributes this noise to the random trapping and detrapping processes of charges near the oxide-semiconductor interface. The Mobility Fluctuation Theory proposes that the flicker noise is due to fluctuation in the bulk mobility of the carriers due to the scattering mechanism. In either case, the flicker noise is associated with the flow of current. The flicker noise also has an inverse dependence on the oxide capacitance since the time-varying component of the oxide interface charge causes changes in the threshold voltage that are inversely proportional to the oxide capacitance. The spectral density of flicker noise is found to have an inverse frequency dependence. Therefore it is frequently referred to as the 1/f noise [3.28].

The BSIM_plus model includes both thermal and flicker noise. The mean square noise current in BSIM_plus is given by,

$$\overline{i_N^2} = 2qI_{DS} + 4kT\frac{2}{3}g_m + 4kTg_D + 4kTg_S + \frac{K_F\, I_{DS}^{A_F}}{f\, WLC_{OX}}, \qquad (3.95)$$

where g_m is the transconductance of the transistor, g_D and g_S are the conductances of the source and drain regions, K_F is flicker noise coefficient and A_F is the flicker noise exponent. The total noise current can be calculated by adding the contribution of different components as given in (3.95) since the different noise sources are mutually independent and the average of their products cancels out. Figure 3.18 shows the total noise power density as a function of frequency. The noise generator may be represented as a voltage source in series with the gate of the transistor or as a current source in series with the transistor.

References

[3.1] B. J. Sheu, D. L. Scharfetter, P. K. Ko, M.-C. Jeng, "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE Jour. of Solid-State Circuits*, vol. 22, no. 4, pp. 558-566, Aug. 1987.

[3.2] B. J. Sheu, *MOS transistor modeling and characterization for circuit simulation*, Ph.D. Dissertation, Memo ERL-M85/22, Electronics Res. Lab., Univ. of California, Berkeley, Oct. 1985.

[3.3] C.-P. Wan, B. J. Sheu, S.-L. Lu, "Device and circuit simulation interface for an integrated VLSI design environment," *IEEE Trans. on Computer-Aided Design*, vol. 7, no. 9, pp. 998-1004, Sept. 1988.

[3.4] G. Chin, R. W. Dutton, "A tool towards integration of IC process, device, and circuit simulation," *IEEE Jour. of Solid-State Devices*, vol. 27, no. 3, pp. 265-273, Mar. 1992.

[3.5] L. A. Glasser, D. W. Dobberpuhl, *The Design and Analysis of VLSI Circuits*, Addison-Wesley: Reading, MA, 1985.

[3.6] P. R. Gray, R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley: New York, NY, 1984.

[3.7] S. M. Sze, *Physics of Semiconductor Physics*, 2nd Edition, New York, NY: John Wiley and Sons, 1981.

[3.8] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw-Hill: New York, NY, 1987.

[3.9] M. C. Hsu, B. J. Sheu, "Inverse-geometry dependence of MOS transistor electrical parameters," *IEEE Trans. on Computer-Aided Design*, vol. 6, no. 4, pp. 582-585, Jul. 1987.

[3.10] S.-W. Lee, "Universality of mobility-gate field characteristics of electrons in the inversion charge layer and its application in MOSFET modeling," *IEEE Trans. on Computer-Aided Design*, vol. 8, no. 7, pp. 724-730, Jul. 1989.

[3.11] G. M. Yeric, A. F. Tasch, S. K. Bannerjee, "A universal MOSFET mobility degradation model for circuit simulation," *IEEE Trans. on Computer-Aided Design*, vol. 9, no. 10, pp. 1123-1126, Oct. 1990.

[3.12] S.-W. Lee, T.-Y. Chan, "A closed-loop evaluation and validation of a method for determining the scattering limited carrier velocity in MOSFETs," *IEEE Trans. on Electron Devices*, vol. 37, no. 11, pp. 2388-2394, Nov. 1990.

[3.13] B. J. Sheu, D. L. Scharfetter, H. C. Poon, *Compact Short-Channel IGFET Model (CSIM)* Memo ERL-M84/20, Electronics Res. Lab., Univ. of California, Berkeley, CA, Mar. 1984.

[3.14] S.-W. Lee, R. C. Rennick, "A compact IGFET model - ASIM," *IEEE Trans. on Computer-Aided Design*, vol. 7, no. 9, pp. 952-975, Sept. 1988.

[3.15] D. A. Divekar, *FET Modeling for Circuit Simulation*, p. 89, Kluwer Academic Publishers: Boston, MA, 1988.

[3.16] B. J. Sheu, A. H. Fung, Y.-N. Lai, "A knowledge-based approach to analog integrated circuit design," *IEEE Trans. on Circuits and Systems*, vol. 35, no. 2, pp. 256-258, Feb. 1988.

[3.17] R. Harjani, R. A. Newton, L. R. Carley, "Analog circuit synthesis and exploration in OASYS," *Proc. of IEEE Int'l. Conf. on Computer Design*, pp. 44-47, Cambridge, MA, Oct. 1988.

[3.18] S. M. Gowda, B. J. Sheu, "Explicit geometry dependence of MOS transistor parameters by the pseudo-boundary method," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 2, no. 2, pp. 105-115, Kluwer Academic Publishers: Boston, MA, Apr. 1992.

[3.19] J. Mar, S.-S. Li, S.-Y. Yu, "Substrate current modeling for circuit simulation," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 1, no. 4, pp. 183-186, Oct. 1982.

[3.20] W.-J. Hsu, B. J. Sheu, S. M. Gowda, C.-G. Hwang, "Advanced integrated-circuit reliability simulation including dynamic stress effects," *IEEE Jour. of Solid-State Circuits*, vol. 27, no. 3, pp. 247-257, Mar. 1992.

[3.21] C. Hu, S. C. Tam, F.-C. Hsu, P.-K. Ko, T.-Y. Chan, K. W. Terrill, "Hot-electron-induced MOSFET degradation - model, monitor, and improvement," *IEEE Trans. on Electron Devices*, vol. 32, no. 2, pp. 375-385, Feb. 1985.

[3.22] K. K. Ng, W. T. Lynch, "The impact of intrinsic series resistance on MOSFET scaling," *IEEE Trans. on Electron Devices*, vol. 34, no. 3, pp. 503-511, Mar. 1987.

[3.23] K. K. Ng, W. T. Lynch, "Analysis of the gate-voltage-dependent series resistance of MOSFETs," *IEEE Trans. on Electron Devices*, vol. 33, no. 7, pp. 965-972, Jul. 1986.

[3.24] S. K. Tewksbury, "N-channel enhancement-mode MOSFET characteristics from 10 to 300 K," *IEEE Trans. on Electron Devices*, vol. 28, no. 12, pp. 1519-1529, Dec. 1981.

[3.25] F. M. Klaassen, W. Hes, "On the temperature coefficient of the MOSFET threshold voltage," *Solid-State Electronics*, vol. 9, no. 8, pp. 787-789, Aug. 1986.

[3.26] C. Jacoboni, C. Canali, G. Ottaviani, A. A. Quaranta, "A review of some charge transport properties of silicon," *Solid-State Electronics*, vol. 20, pp. 77-89, 1977.

[3.27] K. K. Hung, P. K. Ko, C. Hu, Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. on Electron Devices*, vol. 37, no. 3, pp. 654-665, Mar. 1990.

[3.28] P. R. Gray, R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd edition, John Wiley & Sons: New York, NY, 1984.

[3.29] J. E. Chung, M.-C. Jeng, J. E. Moon, P.-K. Ko, C. Hu, "Low-voltage hot-electron currents and degradation in deep- submicrometer MOSFETs", *IEEE Trans. on Electron Devices*, vol. 37, no. 2, pp. 1651-1657, Jul. 1990

[3.30] M.-C. Jeng, P.-K. Ko, C. Hu, "A deep-submicrometer MOSFET model for analog/digital circuit simulation," *IEEE IEDM Technical Digest*, pp. 114-117, San Francisco, CA, Dec. 1988.

[3.31] Y. Tsividis, G. Masetti, "Problems in precision modeling of the MOS transistor for analog applications," *IEEE Trans. on Computer-Aided Design*, vol. 3, no. 1, pp. 72-79, Jan. 1983.

[3.32] H. J. Park, P. K. Ko, C. Hu, "A non-quasi-static MOSFET model for SPICE-AC analysis," *IEEE Trans. on Computer-Aided Design*, vol. 11, no. 10, pp. 1247-1257, Oct. 1992.

Chapter 4

Implementation of BSIM_plus in SPICE-3e1P Circuit Simulator

The SPICE program was derived from an early general-purpose circuit simulation program called CANCER - Computer Analysis of Nonlinear Circuits Excluding Radiation [4.1]. An early version of the SPICE program was described by Nagel and Pederson [4.2]. A comparison of different versions of SPICE was reported in [4.3]. In the 1980s, the SPICE-2g6 program was used widely in the academic community and was the basis of many commercial circuit simulation programs. The SPICE-3e1 program [4.4] is the recent version of the SPICE program. Several new techniques are used to solve convergence problems and improve the performance of the simulator [4.5]. The SPICE-3e1 program contains several new utilities. These include,

- an interactive command interpreter,
- the ability to append an existing file to the simulation description,
- easy circuit modification between simulations, and
- improved convergence performance by using techniques such as adaptive timestep.

The SPICE-3e1 program also contained several new devices including,

- semiconductor capacitors,

- semiconductor resistors,
- n-channel and p-channel MESFETs,
- general non-linear sources,
- current controlled switches, and
- voltage controlled switches.

The BSIM_plus model was developed to enhance the capability of VLSI designers to simulate circuits in sub-half-micron technologies. In order to enable circuit designers to use the model, it was necessary to implement it into a popular circuit simulator. The SPICE-3e1 simulation program was selected for this implementation and the modified program with the BSIM_plus model is called SPICE-3e1P. The UNIX-based organization of the SPICE-3e1P program is shown in Fig. 4.1. A brief description of the primary functions served by the files contained in these directories follows.

The *conf/defaults* file contains several variables that are used during the compilation of the program which need to be set according to the environment in which the program is being compiled. These variables include the command to run the C-language compiler, the paths to the libraries that are required during compilation, the directories containing the source files, intermediate files and output files, the default editor when using SPICE interactively, the analyses that the program is to perform, and the device models that the program is to be capable of simulating. The *defaults* file was modified to include the BSIM_plus model as part of the *DEVICES* variable. In addition to the *defaults* file, the *conf* directory also contains files for

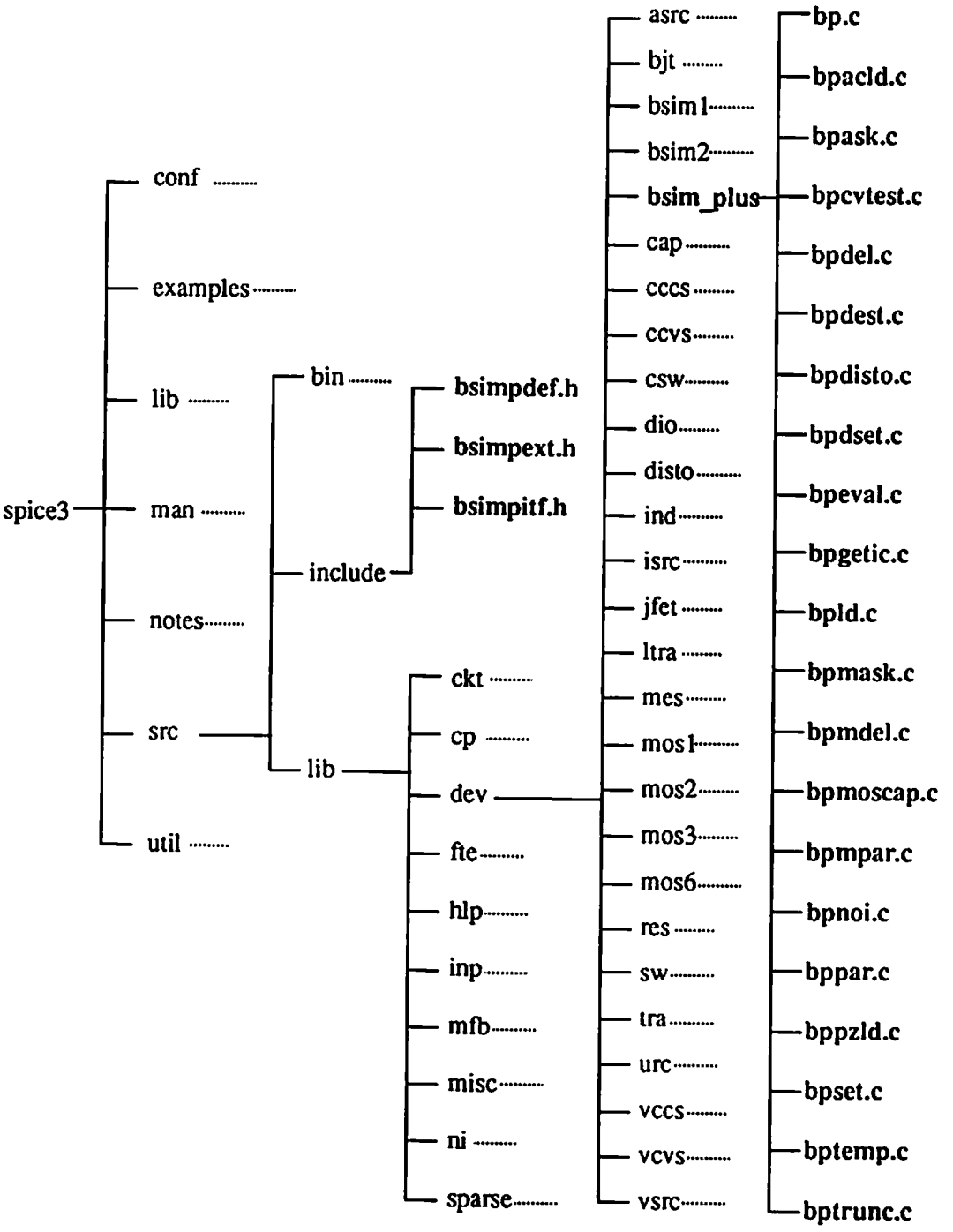


Fig. 4.1 Structure of the SPICE-3e1P program.

different computer systems that include special definitions that are required by the given system and which do not appear in the *defaults* file. The *util* directory contains the *build* command which is used to compile the program.

The *src/lib* directory contains the C-language files that constitute the program. The *src/include* directory contains C-language preprocessor files that are required by the program. Several variables including index numbers, values of physical constants, and sizes/types of data structures used by the programs are defined in files that are in this directory. These files are then included in the headers of the C-language program files by using the "*#include*" command. After the program is compiled, the executable file of the simulation program is placed in the *src/bin* directory.

The *ckt* directory contains routines that link the entire structure of the program and serve as interface points between different functions in the program. Some of these routines implement the front-end interface of the simulator. Other routines are used to bind the various components of the program together by stepping through device dependent subroutines and calling instances that have been defined or that are needed for the operations to be performed. Routines implementing the various analyses such as the D.C., A.C. and transient analyses that are to be performed by the program are contained in this directory. Simple utilities that are used to manipulate the data structures in SPICE are also contained in this directory.

The *ni* directory contains the numerical algorithms that are used by the SPICE program. These include routines that initialize and load matrices, compute timestep and integration-method dependent terms, and perform

voltage/current equation convergence tests. Routines that perform numerical integration, Newton-Raphson iterations, finding roots of complex polynomials, and computing determinants for the pole-zero analysis are also contained in this directory. The *sparse* directory contains functions of a specialized sparse matrix package that is use to manipulate the sparse matrices generated during simulation.

The *inp* directory contains the routines necessary to parse the input format and produce the subroutine calls that are required by the front-end to simulator interface. These include routines that parse the model definitions and descriptions of various active and passive elements in the input decks. The *fte* directory also contains files defining the front end of the simulator.

The *dev* directory contains routines that define and evaluate the different devices and models that have been implemented in SPICE. The subdirectories under *src/lib/dev* and the corresponding devices or models are listed below:

asrc: arbitrary voltage/current source

bjt: bipolar junction transistor

bsim1: original BSIM MOS transistor model (1985)

bsim2: BSIM2 MOS transistor model (1990)

bsim_plus: BSIM_plus MOS transistor model (1992)

cap: capacitor

cccs: current-controlled current source

ccvs: current-controlled voltage source

csw: current controlled switch

dio: diode

ind: inductor

isrc: current source

jfet: junction FET model

ltra: lossy transmission line

mes: MESFET model

mos1: MOS Level-1 transistor model

mos2: MOS Level-2 transistor model

mos3: MOS Level-3 transistor model

mos6: MOS Level-6 transistor model

res: resistor

sw: switch

tra: lossless transmission line

urc: uniform RC line

vccs: voltage-controlled current source

vcvs: voltage-controlled voltage source

vsrc: voltage source

The implementation of a new device model into the SPICE-3e1 program requires three types of changes:

- new routines written specifically to support the device,
- modifications of existing routines to include knowledge required for parsing, and

- changes to integrate the new device model into the main loops of the simulation algorithm.

Among the new files created to support the BSIM_plus model was *src/include/bsimpdef.h.* This file contains two data structures, one for the device model and one for a specific instance of the model. The *sBSIMP-model* structure contains the parameters that are specific to a model and which are common to different transistors associated with that model. This information usually describes that process technology used to fabricate the transistors. The *sBSIMPinstance* structure contains BSIM_plus parameters that are evaluated for a specific instance or transistor. The file *src/include/bsimpitf.h* contains pointers to routines that are used to interface with the device model, as well as a number of tables and constants. The different routines associated with the BSIM_plus model are declared in the file *src/include/bsimpext.h.*

The C-language files that were created to support the BSIM_plus model were placed in the *src/lib/dev/bsim_plus* directory. The main files and a brief description of the routines contained in them are listed below:

bp.c: This file contains two parameter descriptor arrays that list the parameters along with the type of values that can be assigned to the parameters, as well as integers that can be used to refer to the parameters in other routines. The *BSIMPpTable* array contains parameters, such as width and length, that describe a particular transistor, and the *BSIMPmPTable* array contains the BSIM_plus model parameters.

bpacld.c: This routine is used to load the sparse matrix during A.C. analysis where complex quantities may need to be loaded.

bpask.c: This routine allows users to access internal values of BSIM_plus devices instances. Certain parameters of instances can be passed to it in order to compute and return the values of such parameters.

bpcvtest.c: This routine performs the convergence test for each device.

bpdel.c: This routine deletes a single instance of the BSIM_plus model from the data structures, leaving everything else alone.

bpdest.c: This routine is used to dismantle the data structure and free all space used by BSIM_plus models and instances.

bpeval.c: This routine contains the BSIM_plus model expressions. The drain current, its derivatives and the charges associated with the gate, bulk and drain terminal are evaluated in this routine.

bpgetic.c: This routine gets the initial conditions of BSIM_plus devices from the node initial conditions.

bpld.c: This routine is used in the D.C. and transient analyses to load the sparse matrix.

bpmask.c: This routine allows users to access internal values of BSIM_plus model parameters.

bpmdel.c: This routine is used to dismantle data structures and free space occupied by a specific BSIM_plus model and all

instances of that model.

bpmoscap.c: This routine calculates and assigns values of equivalent conductances and total terminal charges.

bpmpar.c: This routine assigns a value to a specific BSIM_plus model parameter.

bpnoi.c: This routine calculates the thermal noise due to the source/drain and channel conductances, as well as the flicker noise.

bppar.c: This routine assigns a value to a specific parameter field of a device instance.

bppzld.c: This routine is used for evaluating and loading the matrix during pole-zero analysis.

bpset.c: This routine is called once during parameter preprocessing, and all the one-time operations such as allocating sparse matrix entries and getting pointers to them is done here.

bptemp.c: Most of the BSIM_plus parameter preprocessing takes place in this routine. It is called before simulation and whenever parameters or the simulation temperature have been changed.

bptrunc.c: Calculation of truncation errors on energy storage elements or components of elements is done here.

In order to enable the SPICE program to identify the BSIM_plus model in the input deck, the file *src/lib/inp/inp2m.c* was modified. No other changes were required to integrate the new model into the main

loop of the simulator since the new data structures used for BSIM_plus were closely related to those used for the other MOS transistor models.

The BSIM_plus model has been implemented in the SPICE-3e1P version of the circuit simulation program to give VLSI designers the ability to use the model for the design of high-performance circuit in advanced sub-half-micron technologies. This version is available from the Department of Electrical Engineering at the University of Southern California. An overview of the SPICE-3e1P circuit simulation program has been described. New files that were created in order to implement the BSIM_plus model have been listed, along with brief summaries of the routines contained in these files.

References

[4.1] R. A. Rohrer, L. W. Nagel, R. Meyer, L. Weber, "CANCER: Computer analysis of nonlinear circuits excluding radiation," *Tech. Digest of IEEE Int'l. Solid-State Circuits Conf.*, pp. 124-125, Philadelphia, PA, Feb. 1971.

[4.2] L. Nagel, D. O. Pederson, "Simulation program with integrated circuit emphasis," *IEEE Proc. of 16-th Midwest Symposium on Circuit Theory*, Waterloo, Canada, 1973.

[4.3] J. R. Hines, "A comparison of Berkeley SPICEs," *Design Automation Magazine*, pp. 28-32, Mar. 1991.

[4.4] B. Johnson, T. Quarles, A. R. Newton, D. O. Pederson, A. Sangiovanni-Vincentelli, *SPICE-3E1 User's Guide*, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, Apr. 1991.

[4.5] T. L. Quarles, *Analysis of Performance and Convergence Issues for Circuit Simulation*, Memo ERL-M89/42, Electronics Res. Lab., Univ. of California, Berkeley, Apr. 1989.

Chapter 5

Effective Parameter Extraction for MOS Transistor Models

Performance of the MOS transistor model during circuit simulation depends upon the parameter set that is used with the model. Parameter extraction for the MOS transistor model is a complicated task due to the large number of parameters that need to be optimized over a wide range of bias conditions for several transistor geometries. The important issues that must be resolved in the parameter extraction procedure include:

- number of transistors and transistor geometries for which data is required,
- terminal voltage biases for which data is required,
- choice of parameter extraction algorithm, and
- choice of transistor characteristics to be optimized.

5.1 Multiple-Objective Function in SUXES

The SUXES program is an extraction program that can be used to optimize model parameters from experimental data [5.1,5.2]. The program reads drain current data and searches through a constrained parameter space to find a nonlinear least-squares fit to the experimental data. The Levenberg-Marquardt and Gauss-Newton methods are augmented and used to solve this error-minimization problem [5.2]. The initial values and boundary

Table 5.1 Improvement in output conductance error obtained by using the multiple-objective function.

SUXES version	Weight (W_{GDS})	W/L = 2 μm/1.5 μm		W/L =3 μm/1.5 μm	
		I_{DS} error	g_{DS} error	I_{DS} error	g_{DS} error
single objective function	-	4 %	39 %	4 %	42 %
multiple objective function	1	19 %	36 %	26 %	40 %
	0.5	15 %	38 %	19 %	41 %
	0.1	4 %	28 %	9 %	32 %
	0.05	4 %	28 %	8 %	31 %
	0.01	4 %	26 %	4 %	29 %

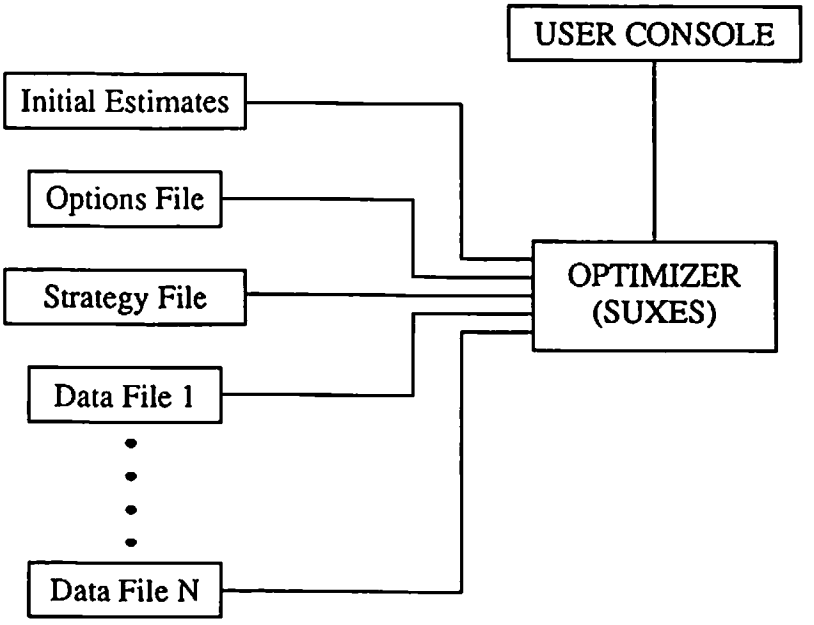


Fig. 5.1 Inputs to the SUXES program [5.1].

values of the model parameters are chosen by the user. The user can also determine an extraction strategy by specifying the order in which different sets of parameters are to be extracted.

The objective function that is minimized by the original SUXES program is given by,

$$\sum_i f_i^2(p) = \sum_i \left[\frac{I_{DSi}(p) - I^*_{DSi}}{\max(I^*_{DSi}, I_{DS0})} \right]^2, \tag{5.1}$$

where,

p = parameter vector being optimized,

$I_{DSi}(p)$ = calculated drain current value,

I^*_{DSi} = measured drain current value, and

I_{DS0} = normalization value to prevent very large errors at small drain current values.

The elements of the error vector are calculated at the i-th iteration and the parameter, "p", is adjusted to minimize the drain current error. The inputs and outputs of the SUXES program are shown in Fig. 5.1 and Fig. 5.2, respectively. The user provides initial estimates of parameters based on knowledge of the technology from which transistors are being characterized. The user also provides constraints on the parameter space that are specified as upper and lower bounds of individual parameter values. The options file contains parameters that determine convergence criteria of the numerical optimization procedure. The data files contain measured drain current data that are to be fitted in the parameter extraction procedure. The user also

specifies a strategy for the extraction of parameters. The strategy consists of selecting a few parameters to be optimized at the same time. When these parameters have been optimized to the extent possible, a few other parameters are selected for optimization. In order to properly optimize geometry-dependent parameters, transistors from a suitably large range of geometries must be chosen for the extraction procedure. The bias range over which measurement data is required in order to provide a parameter set suitable for real circuit simulation is also quite large. Due to this, the data set sometimes contains very high drain current values and very low drain current values. The difference between highest and lowest drain current values can sometimes be more than a few orders of magnitude. All these data points must be fitted simultaneously in order to obtain a single parameter set as the result of parameter extraction. The fitting results in such cases show less error for the larger data points and more error for the smaller data points. In order to perform parameter extraction such that the fitting error is more uniformly distributed over the entire range of drain current data, the data points of lower magnitude need to be given a weighting of more than 1.0. The flag indicating that weighting of the error is required is set in the options file. The actual value of the weight is set within the program, which needs to be edited in order to change the weight value or the data points to which the weight is to be applied. The data points to be weighted are specified in terms of the drain, gate, and substrate voltage ranges within which they fall. The voltage ranges, along with the weight values are specified in the *MODELx* subroutine, where *x* refers to a specific model. In the SUXES

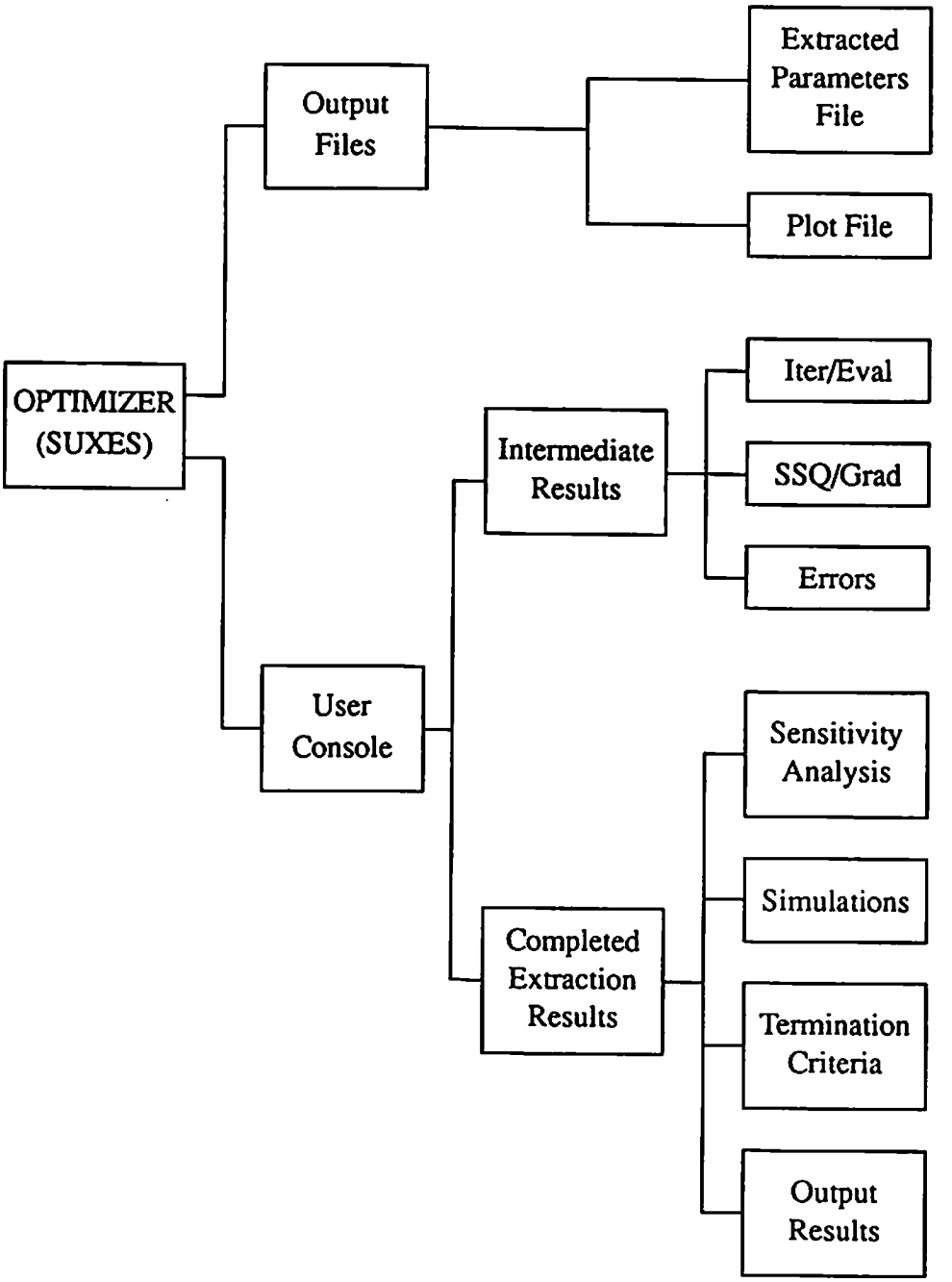


Fig. 5.2 Outputs of the SUXES program [5.1].

program, x=1 for MOS Levels 1 to 3 models. In the modified SUXES program, x=41 for the BSIM_plus model. The subroutine *MODELx* can be found in the file named *smodelx.f*, where *x* refers to a specific model as before. During the extraction procedure, the program displays information about the number of function evaluations, calculated errors, and intermediate parameter values. When the extraction is completed, the program displays sensitivity information of the transistor parameters, simulated results at specified bias points and termination criteria that were used to stop the extraction procedure. A file containing the extracted parameters and others containing measured and simulated data to be plotted for comparison are created.

The original SUXES program optimizes the I_{DS} values because digital circuit designers need to be able to accurately predict the drain current of transistors during circuit simulation. For analog designers the output conductance is also a critical quantity that needs to be accurately predicted by the extracted parameter set. Errors in the output conductance would affect accurate prediction of voltage gain and transient circuit behavior. In order to improve the quality of the parameter set that is extracted, a multiple objective function is used. The multiple objective function containing drain current and output conductance errors is given by,

$$\sum_i f_i^2(p) = \sum_i \left[\frac{I_{DSi}(p) - I^*_{DSi}}{\max(I^*_{DSi}, I_{DS0})} \right]^2 + W_{GDS} \sum_i \left[\frac{g_{DSi}(p) - g^*_{DSi}}{\max(g^*_{DSi}, g_{DS0})} \right]^2, \qquad (5.2)$$

where $g_{DSi}(p)$ is the output conductance value calculated from simulated data,

g^*_{DSi} is the output conductance value calculated from measured data, and g_{DS0} is a normalization factor to prevent very large errors at small output conductance values. The output conductance error can be weighted by a value, W_{GDS}, relative to the drain current error. The multiple objective function can also include other quantities such as the transconductance and capacitance values that may be critical to the circuit designer for simulation of special circuits.

The new objective function has been implemented in a modified version of the SUXES program. The new version of the program reads measured I_{DS} and g_{DS} data. The weight, W_{GDS} that is assigned to the output conductance error can be specified by the user. MOS Level-2 parameters were extracted from experimental data of two NMOS transistors, of geometries W/L = 2 μm/1.5 μm and 3 μm/1.5 μm. The errors that were obtained from different runs of SUXES are listed in Table 5.1. These include using the single objective function given in (5.1), as well as the multiple objective function given in (5.2) with different values of the weight, W_{GDS}. The data show that a considerable improvement in the output conductance errors can be obtained while maintaining the drain current accuracy. Although the numerical drain current error is the same even when the multiple objective function is used, the curve fitting is better since the shape of the curve is also better matched. The output conductance error is still significant since the model used for this demonstration is the MOS Level-2 model which contains limitations in the output conductance modeling. The multiple objective

function is better suited for use with models such as the BSIM_plus model which have better output conductance modeling.

5.2 BSIM_plus Model in SUXES Extractor

The SUXES program has also been modified to provide extraction capability for the BSIM_plus model. The SUXES program has variables that have been set to certain values that determine limits on the number of drain current parameters, the number of data points, and the number of bias data columns. These variable values are set in the file *parsize.f*. The number of parameters to be extracted was made consistent with the number of drain current parameters in the BSIM_plus model. The next step in implementing the BSIM_plus model was to update the subroutines that called upon the model file and include the name of the new BSIM_plus model-calculating subroutine. The third step involved writing a subroutine *MODEL41* which does the preprocessing and setting up of the model parameters and other variables containing data. The subroutine *MODEL41* was based on the existing subroutine *MODEL1* which corresponds to the MOS Level-1, -2 and, -3 models. Blocks of variables containing the model parameters that are passed between subroutines for evaluation of the BSIM_plus model are declared in *MODEL41*. The names of the BSIM_plus model parameters are stored in the array *prname()*. Some parameter preprocessing including conversion of units, assigning default values and calculation of the gate-oxide capacitance are also done. The width and length of the transistor are extracted from the

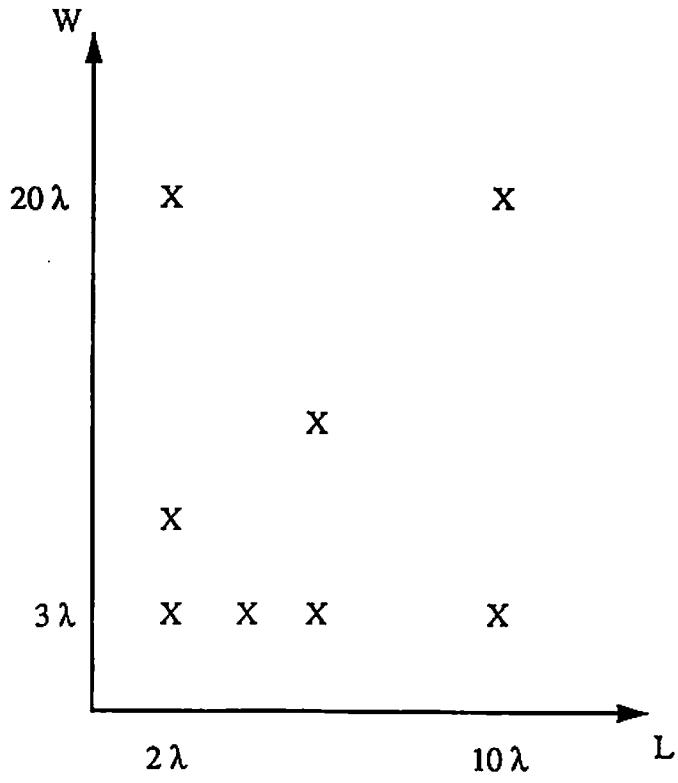


Fig. 5.3 Transistor geometries to be used for parameter extraction.

input data array in this subroutine. The original SUXES program could not handle submicron devices and this has been modified for extraction of BSIM_plus model parameters. The last step in the modification procedure was to write a new subroutine that contained the drain current expressions of the BSIM_plus model. This subroutine is called by the *MODEL41* subroutine when the calculation of drain current is required by the program. Extraction results using the modified SUXES program with the BSIM_plus model are presented in Chapter 6.

5.3 Simulated Annealing Techniques

The simulated annealing technique is used to solve complex optimization problems involving many variables [5.3]. The approach has been applied to several electronic engineering applications including chip floorplanning, cell placement, and circuit synthesis [5.4]. These problems are NP-complete since the time required for an exact solution increases exponentially with the size of the problem.

The simulated annealing technique consists of the following steps:

Step 1. Start with a high temperature and an initial state as the current state.

Step 2. Choose at random a new state from the neighborhood of the current state.

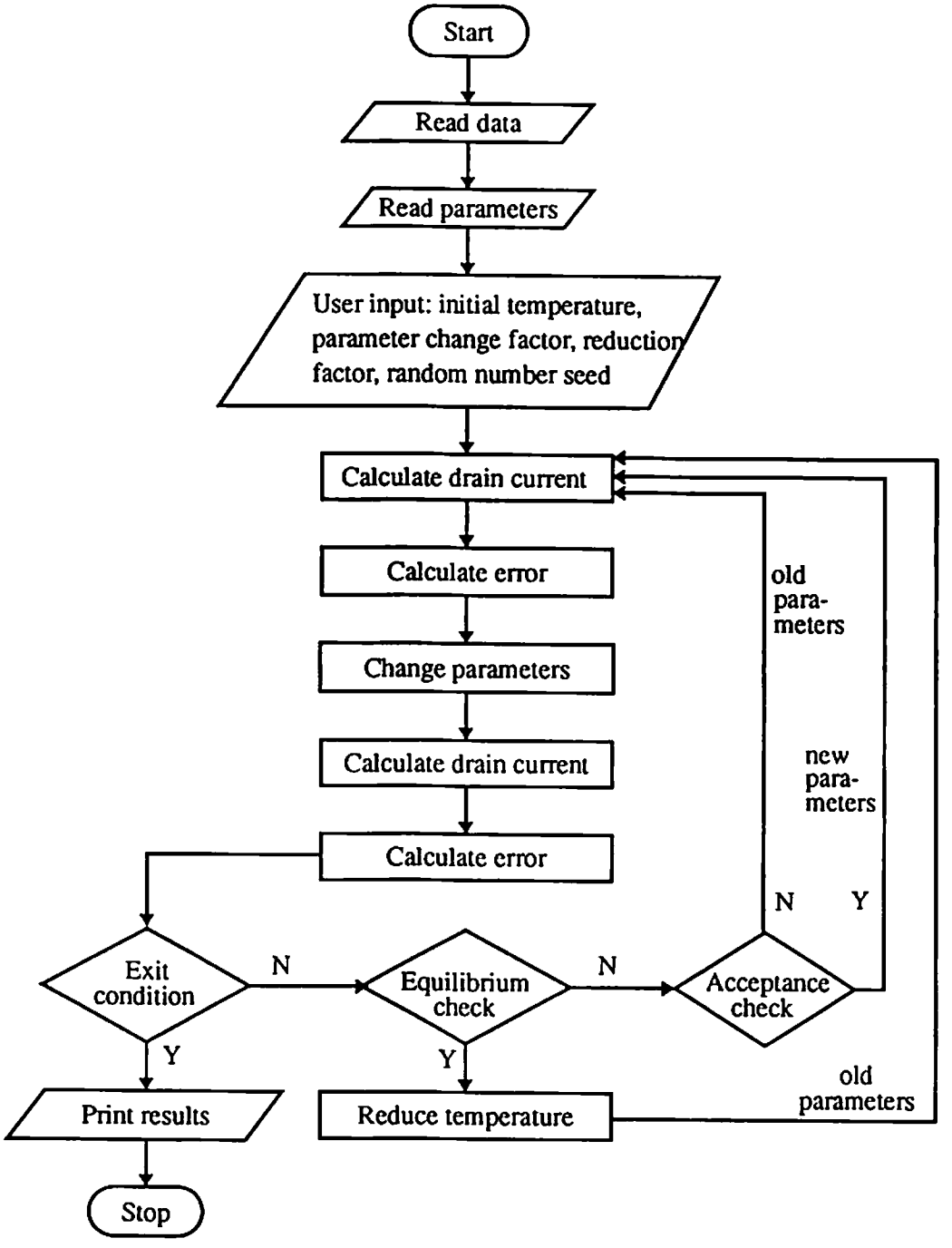


Fig. 5.4 Flowchart of the program using simulated annealing for MOSFET parameter extraction.

Step 3. Calculate the difference in energy, ΔE, between the new state and the current state.

Step 4. If ΔE is less or equal to zero, replace the current state by the new state.

Otherwise, accept the new state only if $e^{-\frac{\Delta E}{kT}}$ is greater than a random number drawn from a uniform distribution on [0,1].

Step 5. If equilibrium is not closely established at this temperature, go to Step 2.

Step 6. If the system is frozen, terminate the annealing process.

Otherwise, decrease the temperature and return to Step 2.

Since it usually takes a lot of time at "Step 2" to compare all possible states, a specific perturbation rule is often used. The perturbation is usually called artificial noise in software computation.

The parameter extraction problem is well suited for solution by the simualated annealing technique. The problem involves a large number of variables ranging from 20 to 60. The number of data points for which the model is evaluated and errors calculated is several hundreds. The extraction of MOS transistor parameters by using the simulated annealing procedure may take several hours. However, the parameter extraction task is not performed frequently, and the solution obtained through this procedure is of very high quality.

A parameter extraction program using the simulated annealing technique has been implemented in C-language. The flowchart of the program is

shown in Fig. 5.4. The input files that are read by the program include the set of initial parameters and the measurement data that is to be fitted. The measurement data file contains the geometry of the transistor, and four columns of data containing the drain voltage, gate voltage, substrate voltage and drain current values. The user also inputs parameters of the simulated annealing procedure. These include the initial temperature, the size of parameter variation that is allowed in each iteration, and a seed for the random number generator. The size of parameter variation limits the quantity by which the drain current error can change between iterations. The temperature is used to determine whether an increasing error change is accepted or not. Drain current values are calculated for input set of voltage biases using the initial parameter set. The root mean square error between simulated and measured data is calculated as given by (5.1). The parameters are changed in order to generate a new parameter set. The sign of the parameter change which determines whether the parameter increases or decreases is selected randomly for each parameter. The magnitude of parameter change is also determined randomly, but is limited by the user. By using the new parameter set, new drain current values are calculated and the new drain current error is calculated. The change in error is calculated as the difference between the new error and old error. If the error decreases, then the new parameter set is directly accepted. If the error increases, then the new parameter set is accepted only if the following condition is true:

$$e^{(-\frac{\Delta E}{T})} > R, \tag{5.3}$$

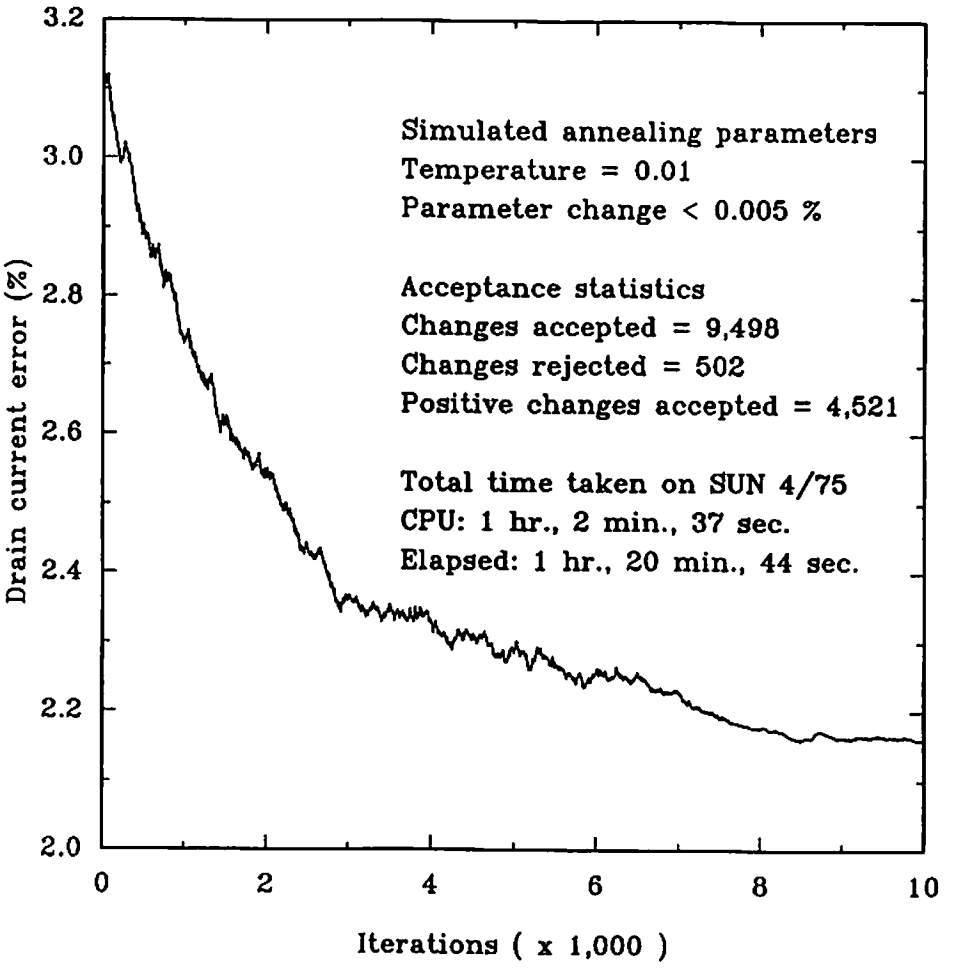


Fig. 5.5 Decreasing drain current error during parameter extraction using the simulated annealing procedure.

where ΔE is the difference between the new and old errors, T is the temperature and R is a random number in the interval [0,1]. On the next iteration the parameters are again changed and the new set of parameters are either accepted or rejected according to the comparison in (5.3). At every iteration, the system is checked for equilibrium. If equilibrium has been reached, the temperature is lowered and the cycle of parameter changes is repeated until equilibrium is reached at the new temperature. When the system remains at equilibrium even upon lowering the temperature, it is said to be frozen. The simulated annealing procedure has then been completed and the results of the parameter extraction are printed. Figure 5.5 shows the drain current error against number of iterations in the simulated annealing procedure applied to extraction of MOS Level-3 parameters. Measured drain current data from an NMOS transistor with W/L = 3.5 μm/1 μm are used for this extraction. The parameters of the simulated annealing procedure including the temperature and percentage limit on the parameter change per iteration are also given in Fig. 5.4. The CPU time required for 10,000 iterations of the program was 1 hour, 2 minutes and 37 seconds.

References

[5.1] K. Doganis, R.W. Dutton, *SUXES-Stanford University Extractor of Model Parameters (User's Manual)*, Tech. Report, Stanford Electronics Lab., Stanford University, Nov. 1982.

[5.2] K. Doganis, D. L. Scharfetter, "General optimization and extraction of IC device model parameters," *IEEE Trans. on Electron Devices*, vol. 30, no. 9, pp. 1219-1228, Sept. 1983.

[5.3] S. Kirkpatrick, C. D. Gelatt, Jr., M. P. Vecchi, "Optimization by simulated annealing," *Science*, vol. 220, no. 4598, pp. 671-680, May 1983.

[5.4] R. A. Rutenbar, "Simulated annealing algorithms: an overview," *IEEE Circuits and Devices Magazine*, vol. 5, no. 1, pp. 19-26, Jan. 1989.

Chapter 6

Experimental Results

Implementation of the BSIM_plus model in the SUXES parameter extraction program and SPICE circuit simulation program were applied to measurement data from industrial technologies from Samsung Electronics Co. and TRW Inc. The integrated parameter extraction and circuit simulation environment of the BSIM_plus model is shown in Fig. 6.1. The SPICE program was also used to simulate several conventional and advanced CMOS circuit blocks. Simulation performance using the BSIM_plus model was compared with other models including the MOS Level-2 and Level-3 models. Simulations were also performed to demonstrate the implementation of the temperature effects, as well as the charge conservation property of the capacitance model in BSIM_plus.

The wafers were set up in a probe station with electrostatic shielding. The device measurements were done using the HP 4145B semiconductor parameter analyzer. An HP-9000/310 desktop computer was used to control the HP-4145B semiconductor parameter analyzer. Control subroutines for the measurement procedure were written in HP-BASIC and HP-PASCAL languages. Communications between the computer, semiconductor analyzer and storage media were on the HP-IB interface bus. The measurement data was uploaded to SUN 4/75 SPARC Stations where the data processing was done.

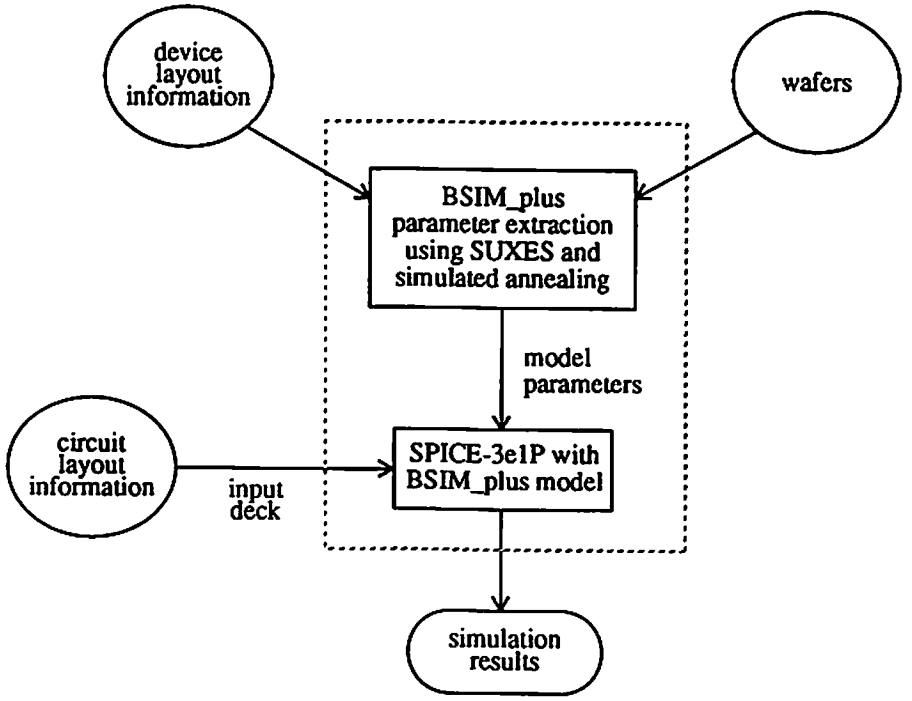


Fig. 6.1 The integrated parameter extraction and circuit simulation environment of the BSIM_plus model.

6.1 Individual Transistor Data

The BSIM_plus model can be used to simulate drain current and output conductance characteristics with high accuracy. The measured and simulated data for several submicron and sub-half-micron devices from industrial technologies are presented.

6.1.1 Determination of Effective Channel Length

The accurate estimation of reductions in channel length and width is essential in the simulation of VLSI circuits. In addition to the first-order dependence of the drain current on the geometric aspect ratio (W/L) of the transistor, there are numerous parameter dependencies on the effective transistor geometries [6.1,6.2]. Hence, an erroneous determination of the effective channel length and width will manifest itself in several parts of the transistor model, resulting in unacceptable inaccuracies. The accurate dependence of the effective channel length has been the topic of much research [6.3,6.4]. A simple method that can be used to measure the external resistance of the source and drain as well as measure the channel length reduction is described.

The determination of channel length reduction involves the measurement of the terminal resistance at different gate bias conditions for wide transistors with different lengths. The terminal resistance is measured as the ratio of the drain voltage applied across the terminals of the transistor to the drain current that passes through the transistor at that voltage. The determination

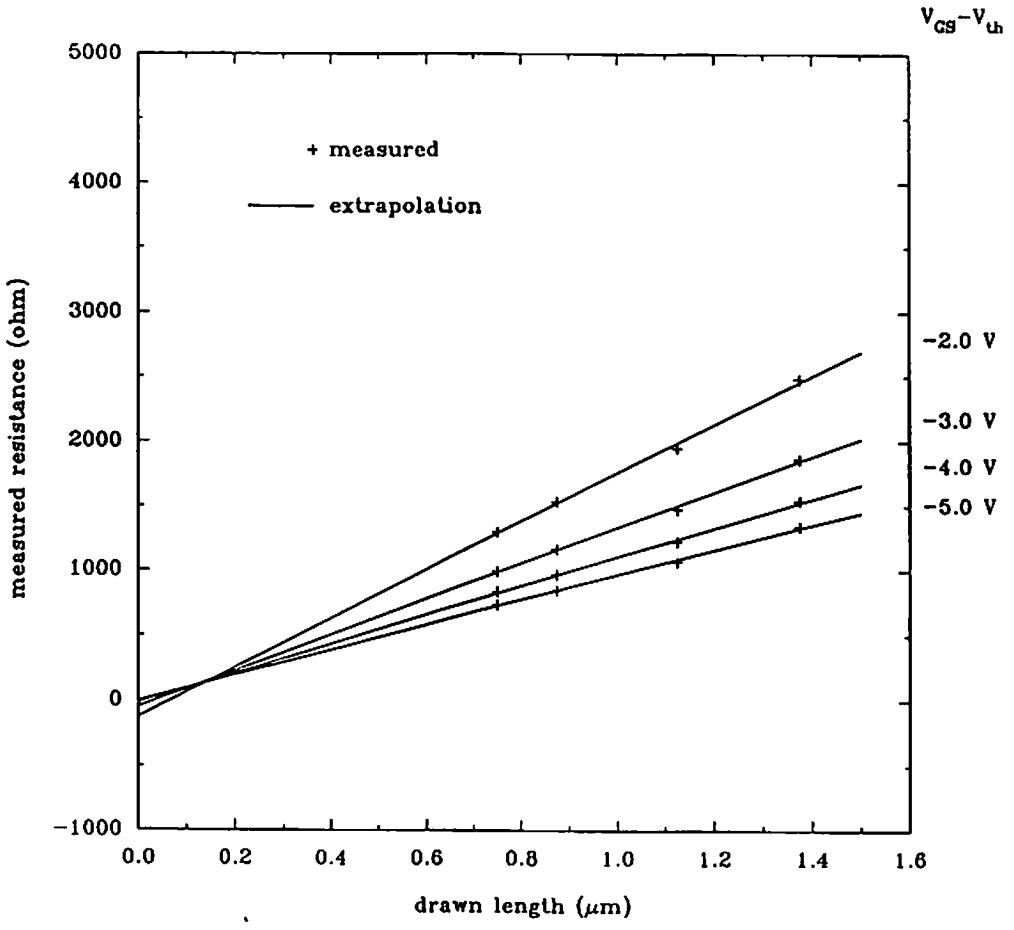


Fig. 6.2 Determination of channel length reduction of PMOS transistors.

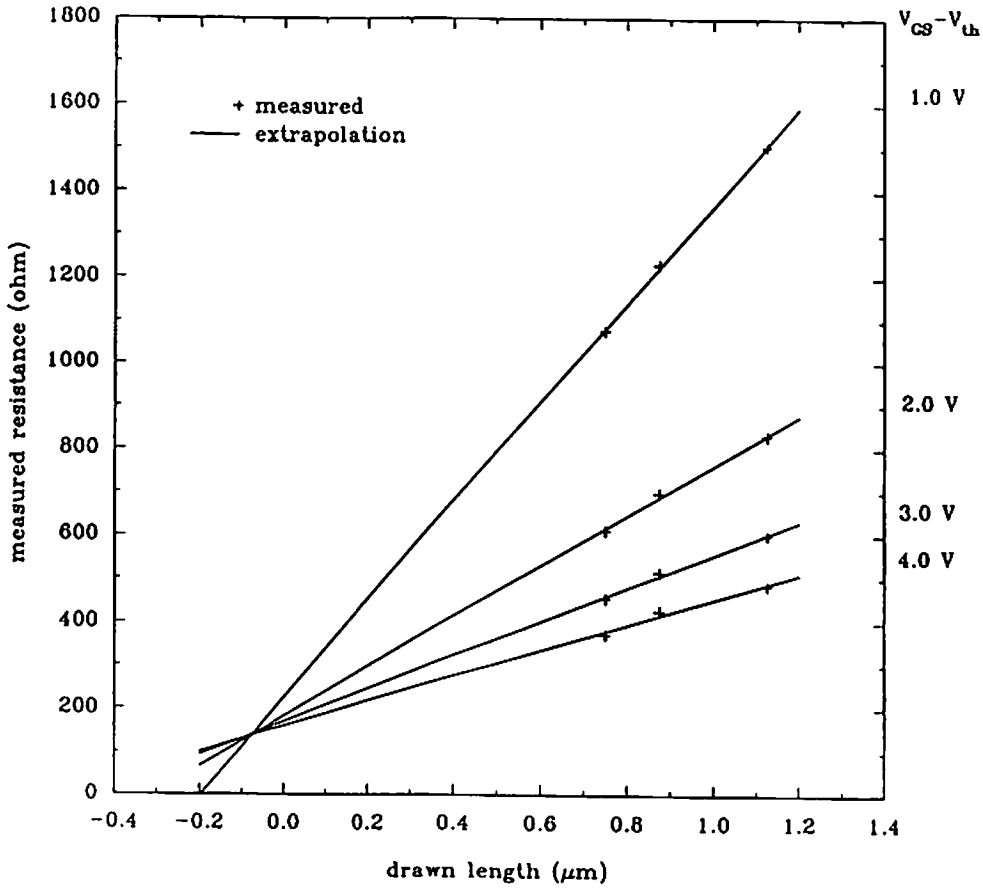


Fig. 6.3 Determination of channel length reduction of NMOS transistors.

method involves separating the terminal resistance into two components. These are the channel resistance and the source/drain series resistance. The separation of components is given by,

$$R_M = R_{EXT} + A \cdot (L_{MK} - \Delta L), \tag{6.1}$$

where R_M is the measured terminal resistance and R_{EXT} is the sum of the drain and source series resistances and the contact resistance. L_{MK} is the drawn (or mask) length of the transistor and ΔL is the channel length reduction. The channel resistance per unit length is given by A which is written as,

$$A = \left[\mu_s \, C_o \, W \, (V_{GS} - V_{th} - 0.5 \cdot V_{DS})\right]^{-1}. \tag{6.2}$$

μ_s is the carrier mobility in the channel, C_o is the gate oxide capacitance per unit area, W is the effective channel width, V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage and V_{th} is the threshold voltage of the transistor.

The drain current of each transistor is measured for a fixed V_{DS} at different values of $V_{GS} - V_{th}$. The drain voltage is fixed at a small value such as 0.05 V to ensure that the transistor is in the linear region for all the measurement. This is necessary to ensure the validity of the equations above that are the basis of this method. The $V_{GS} - V_{th}$ can be varied from 1 V to 4 V in steps of 0.5 V. The terminal resistance is calculated as the ratio of the drain voltage to the drain current. Such data is required from a set of wide transistors that have different lengths.

The extraction consists of plotting the terminal resistance against the drawn channel length for different $V_{GS} - V_{th}$. These lines intersect at a point. The x-coordinate of the point is the channel length reduction. The y-coordinate of the point of intersection gives the external resistance consisting of the source/drain series resistance and the contact resistance. The channel length reduction is a function of the gate voltage. Hence a perfect point of intersection is sometimes not achieved depending upon the range of gate voltages selected for measurements.

Figure 6.2 shows the method being used to determine the channel length reduction of PMOS transistors from TRW Inc. Four PMOS transistors with drawn lengths of 1.375 μm, 1.125 μm, 0.875 μm and 0.75 μm are used in this experiment. The channel length reduction and external resistance were determined to be 0.19 μm and 197 Ω, respectively. Results of a similar experiment using three NMOS transistors with drawn lengths of 1.125 μm, 0.875 μm, and 0.75 μm are shown in Fig. 6.3. The channel length reduction and external resistance were determined to be -0.08 μm and 132 Ω, respectively.

6.1.2 Transistors from TRW 1.0-μm Technology

Measurement data were obtained from several transistors of a 1.0-μm technology wafer from TRW Inc. The dedicated extraction program [6.5] was used to extract BSIM parameters from transistors with W/L = 3.5 μm/1 μm, 6 μm/1 μm, 11 μm/1 μm, 3.5 μm/4.75 μm, 11 μm/4.75 μm, and 3.5

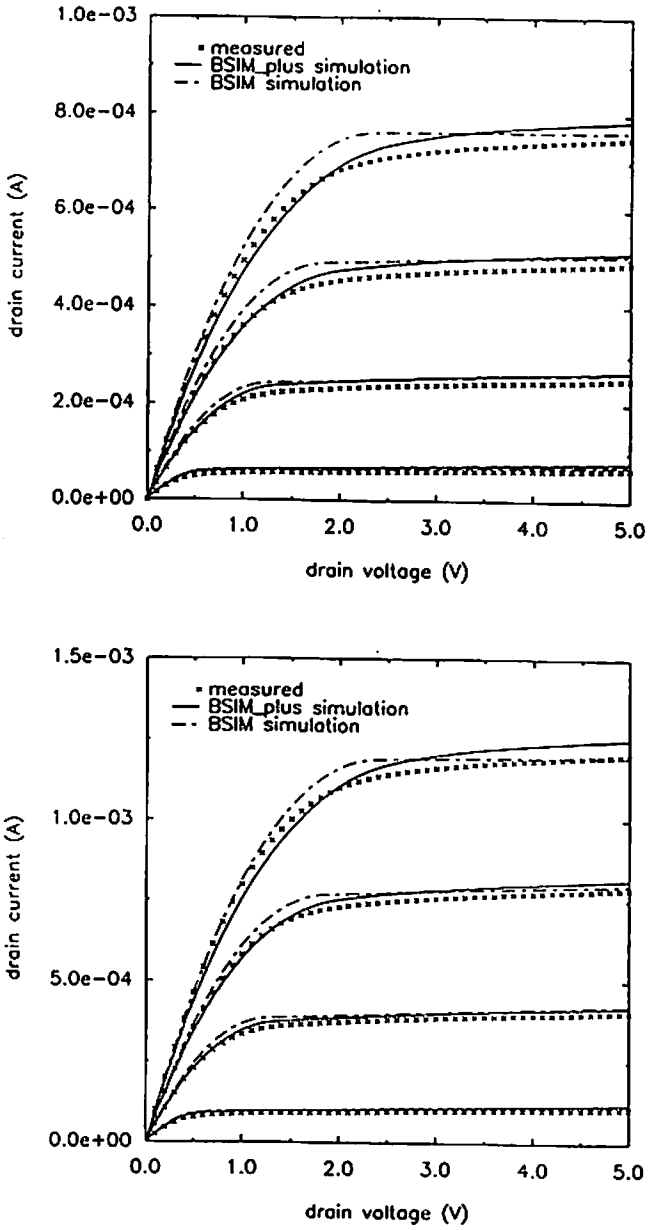


Fig. 6.4 Drain current characteristics from TRW 1.0-μm technology using the BSIM and BSIM_plus models. V_{GS}: 2 V to 5 V in steps of 1 V.
(a) W/L = 3.5 μm/1 μm. (b) W/L = 6 μm/1 μm.

Figure 6.4 (continued)

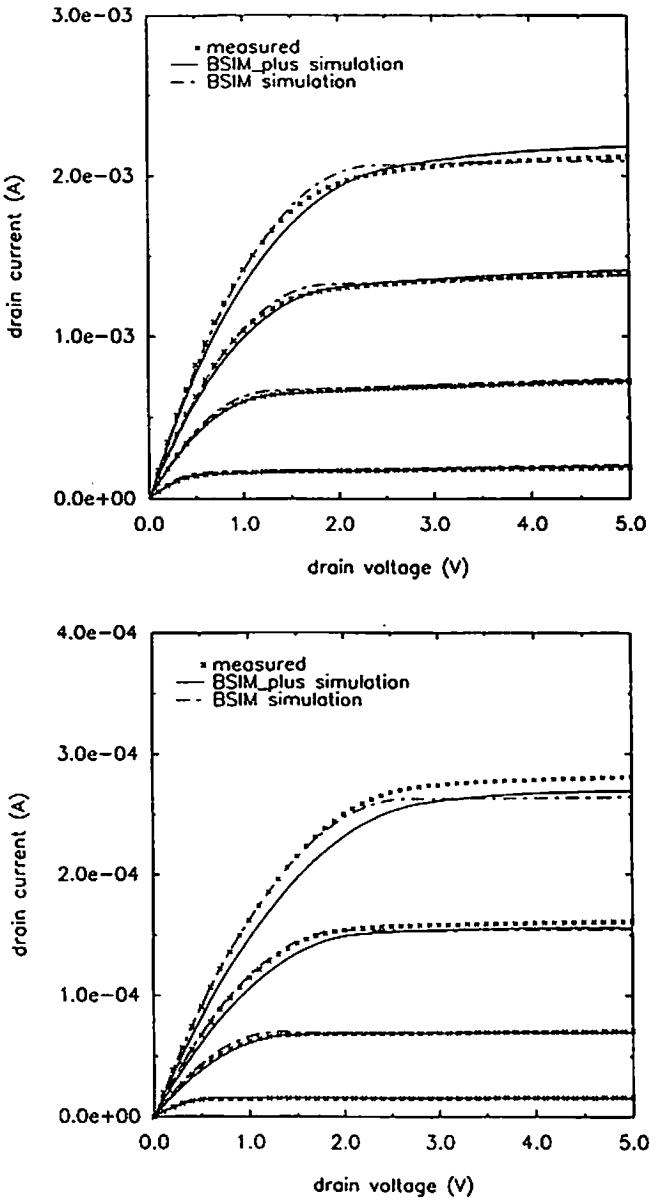
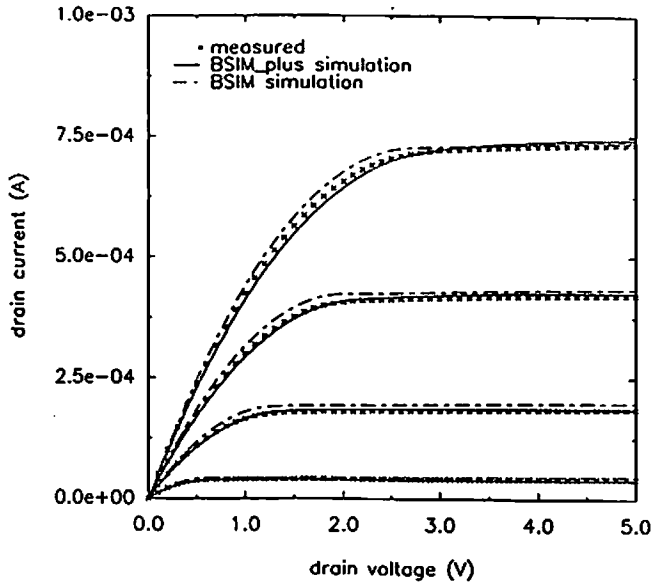
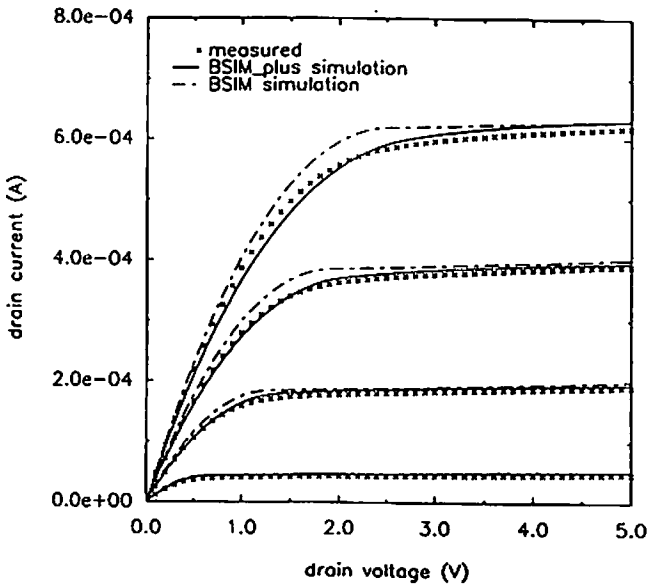


Fig. 6.4 (continued)
(c) W/L = 11 μm/1 μm. (d) W/L = 3.5 μm/4.75 μm.

Figure 6.4 (continued)



(e)



(f)

Fig. 6.4 (continued)
(e) W/L = 11 μm/4.75 μm. (f) W/L = 3.5 μm/1.5 μm.

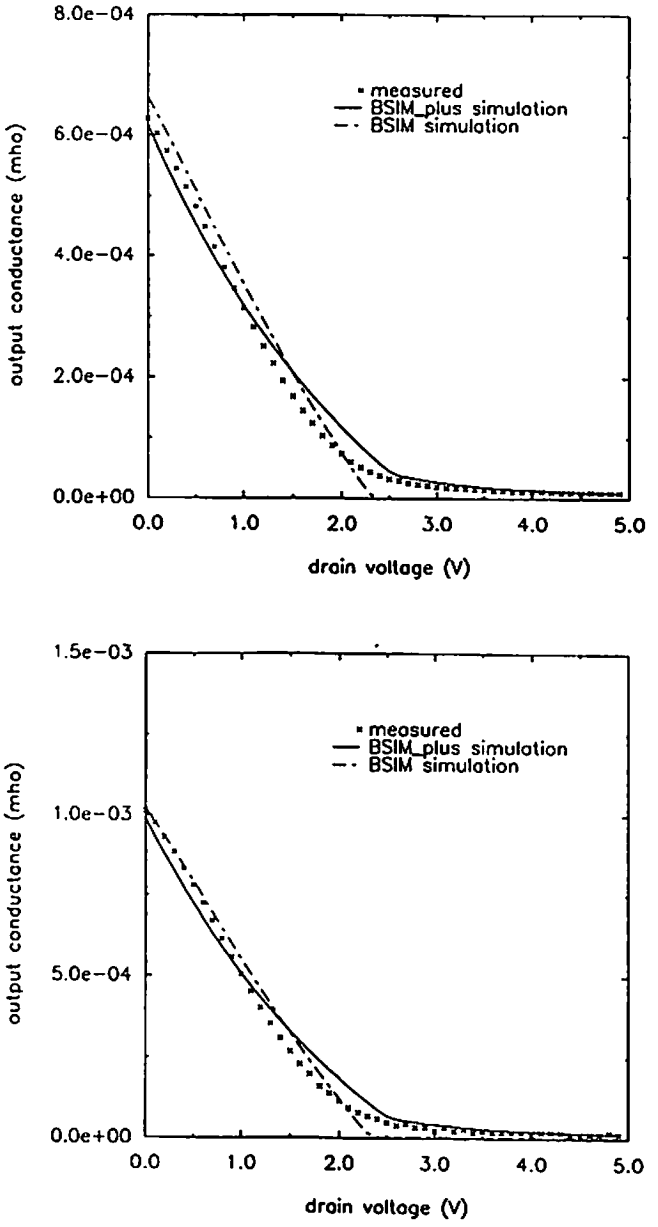
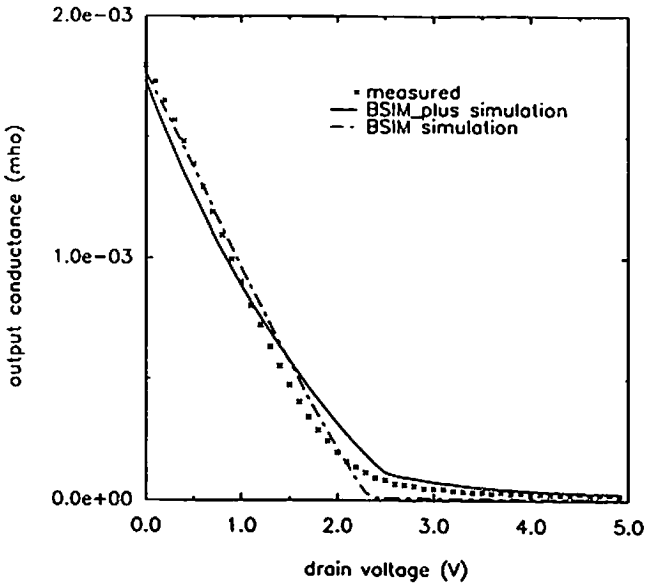
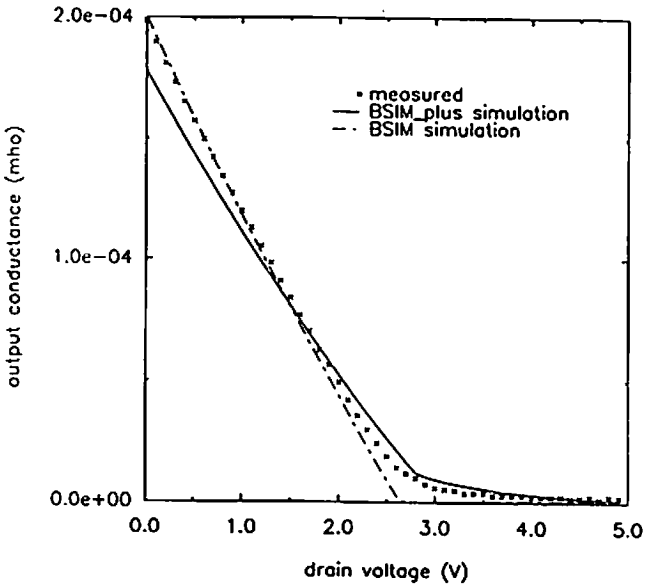


Fig. 6.5 Output conductance characteristics from TRW 1.0-μm technology using the BSIM and BSIM_plus models. (a) W/L = 3.5 μm/1 μm. (b) W/L = 6 μm/1 μm.

Figure 6.5 (continued)



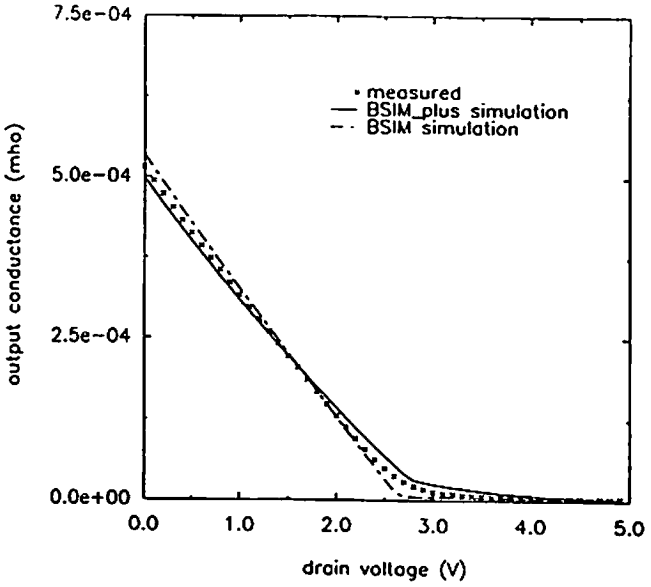
(c)



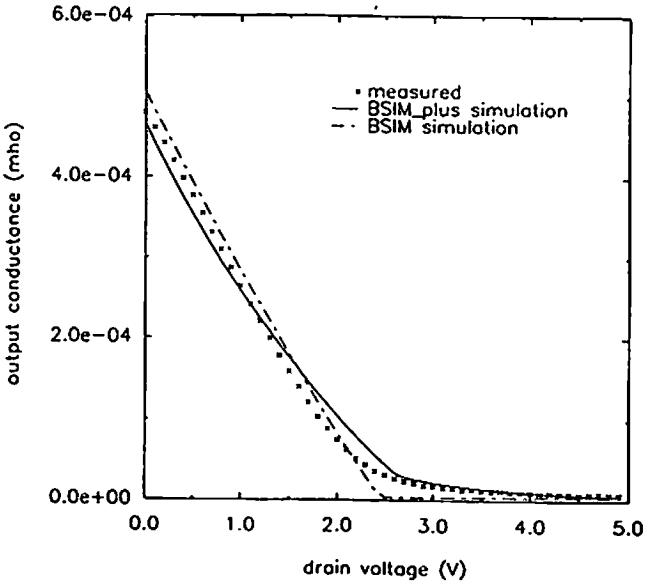
(d)

Fig. 6.5 (continued)
(c) W/L = 11 μm/1 μm. (d) W/L = 3.5 μm/4.75 μm.

Figure 6.5 (continued)



(e)



(f)

Fig. 6.5 (continued)
(e) W/L = 11 μm/4.75 μm. (f) W/L = 3.5 μm/1.5 μm.

μm/1.5 μm. The modified SUXES program was used to extract BSIM_plus parameters from these transistors. Comparison of measured and simulated drain current data obtained using the BSIM and BSIM_plus parameter sets are shown in Fig. 6.4. The output conductance characteristics for the same transistors are compared in Fig. 6.5.

6.1.3 Transistors from TRW 0.4-μm Technology

The modified SUXES program was also used to extract BSIM_plus parameter values for transistors from a 0.5-μm CMOS-fabricated wafer from TRW Inc. The geometries for NMOS transistors chosen for parameter extraction are W/L = 25 μm/0.4 μm, 1.75 μm/0.4 μm, 1.75 μm/0.6 μm, 1.75 μm/1.1 μm and 2 μm/0.4 μm. The parameters extracted from these transistors are listed in Table 6.1. Measured and simulated data are shown in Fig. 6.6.

6.1.4 Transistors from Samsung 0.4-μm Technology

Measurement data were also obtained from several transistors of a 0.4-μm technology for advanced DRAM memories from Samsung Electronics Co. The modified SUXES program was used to extract BSIM_plus parameters from the I_{DS} vs. V_{DS} data and I_{DS} vs. V_{GS} data. The transistors chosen for measurement were of W = 10 μm and L = 0.3 μm, 0.5 μm, 0.7 μm, 0.9 μm, 1.1 μm, 1.5 μm. The parameter set listed in Table 6.2 was used to

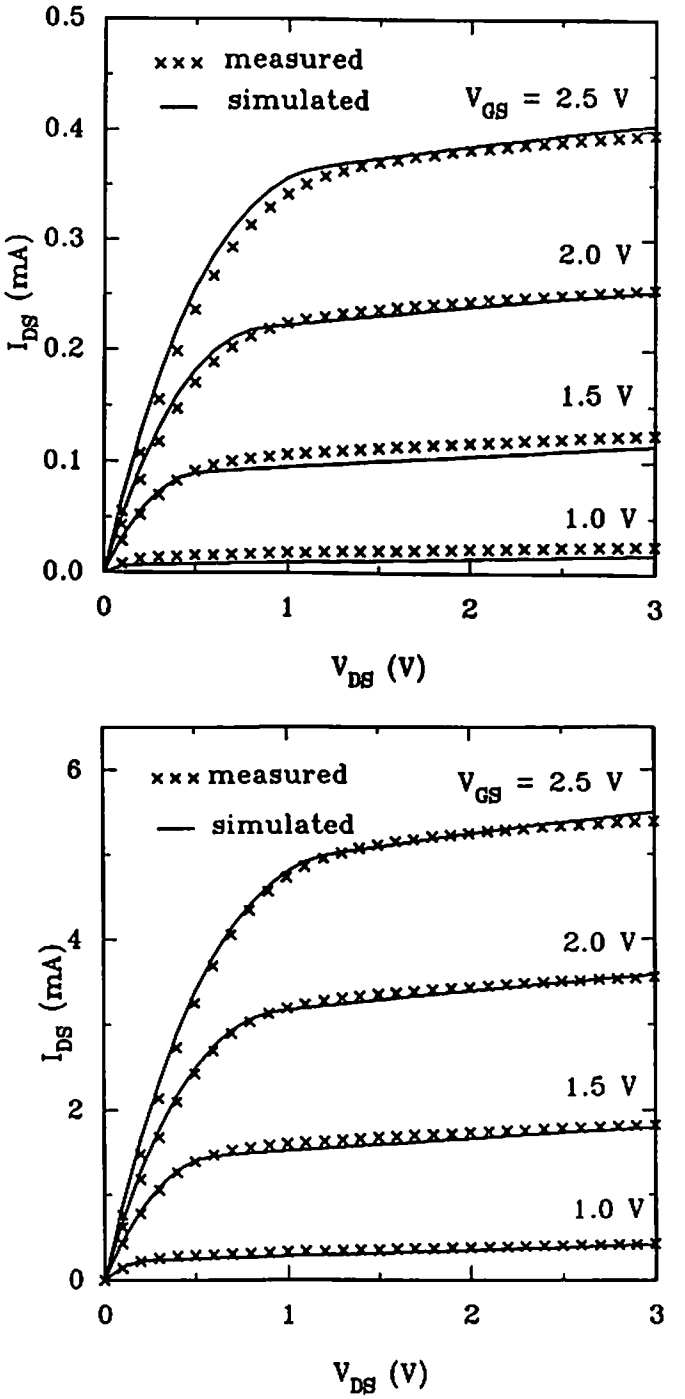


Fig. 6.6 Drain current characteristics of a 0.4-μm technology from TRW Inc.
(a) W/L = 2 μm/0.4 μm. (b) W/L = 25 μm/0.4 μm.

Figure 6.6 (continued)

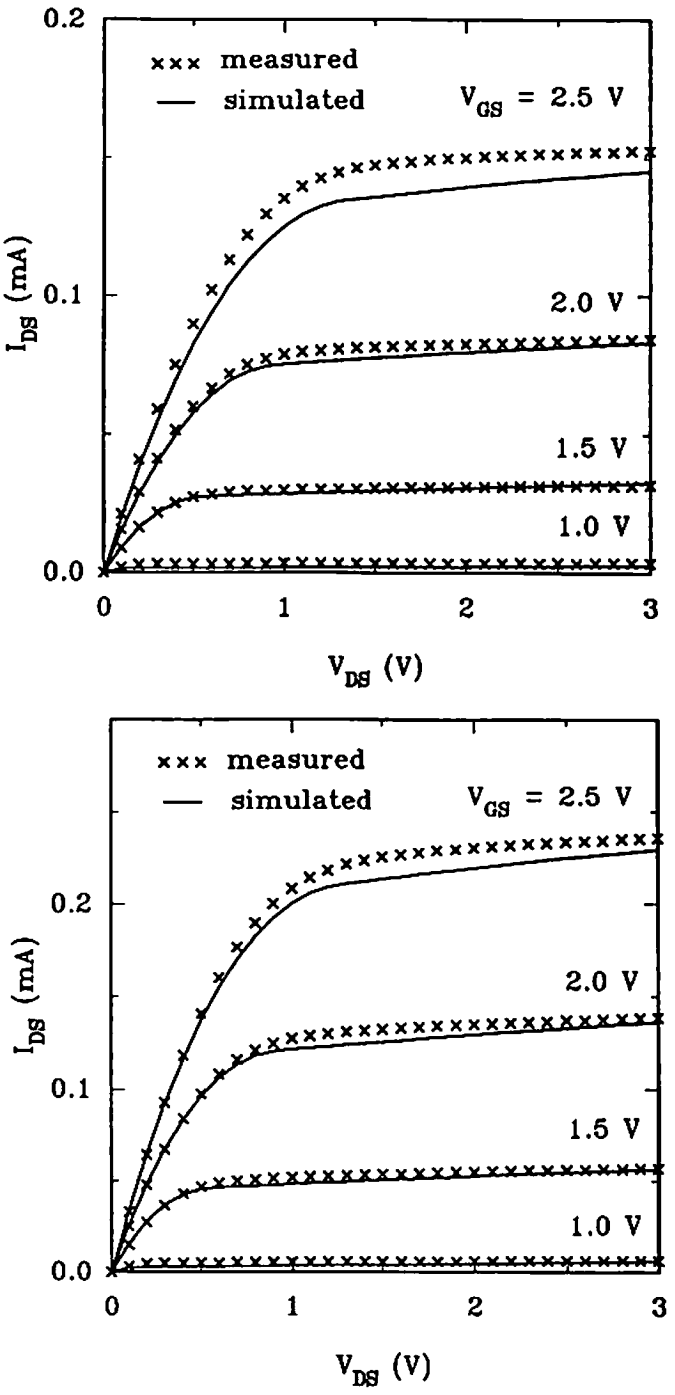


Fig. 6.6 (continued)
(c) W/L = 1.75 μm/1.1 μm. (d) W/L = 1.75 μm/0.6 μm.

Figure 6.6 (continued)

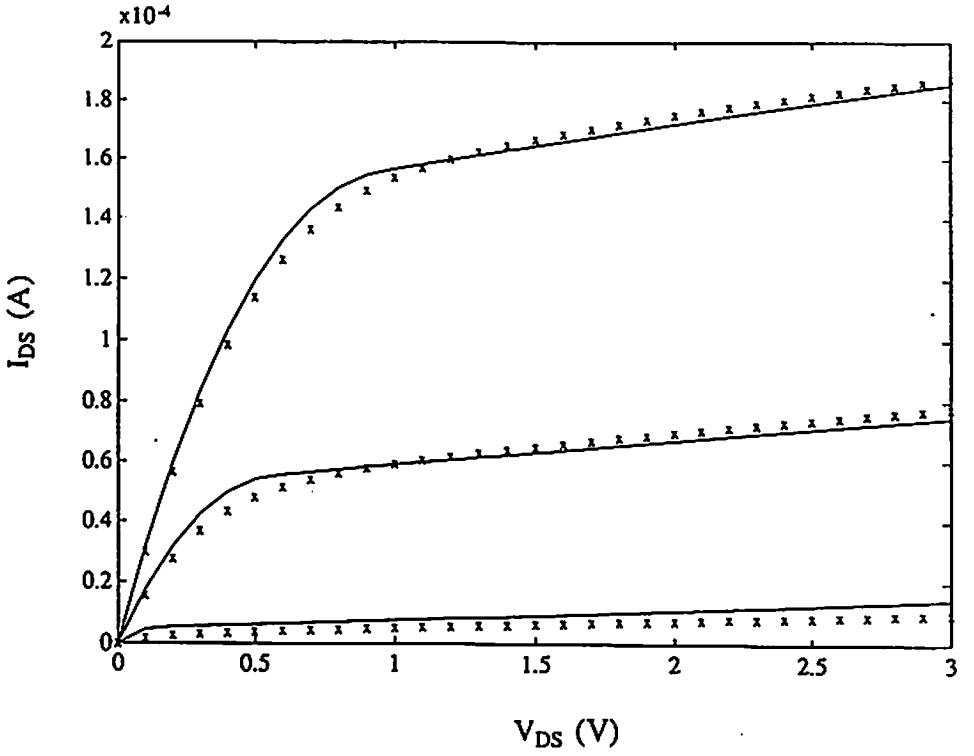


Fig. 6.6 (continued)
(e) W/L = 2.0 μm/0.5 μm, V_{BS} = -2.5 V.
V_{GS} = 1.5 V, 2 V, 2.5 V.

Table 6.1 BSIM_plus parameter set extracted from NMOS transistors of a 0.4-μm CMOS technology of TRW Inc.

Symbol	Value	Unit	Symbol	Value	Unit
ϕ_S	1.1	V	ΔL	0.1	μm
V_{FB}	-0.5	V	ΔW	0.003	μm
γ_1	0.89	$V^{0.5}$	U_{GSZ}	0.18	V^{-1}
γ_2	0.33	$V^{0.5}$	U_{GSL}	0.06	$V^{-1}\mu m$
K_S	1.2e-4	-	U_{BS}	0.005	V^{-1}
K_{NZ}	0.26	V μm	E_{CRIT}	14.1	V/μm
K_{NB}	3.6e-5	μm	H_0	0.14	-
η_Z	-0.67	-	H_1	2.1	V
η_L	0.18	μm	T_{OX}	12	nm
μ_0	400	cm^2/Vs			

Table 6.2 BSIM_plus parameter set extracted from NMOS transistors of a 0.4-μm CMOS technology of Samsung Electronics Co.

Symbol	Value	Unit	Symbol	Value	Unit
ϕ_S	1.64	V	ΔL	0.09	μm
V_{FB}	-1.29	V	ΔW	0.07	μm
γ_1	0.41	$V^{0.5}$	U_{GSZ}	-0.13	V^{-1}
γ_2	0.32	$V^{0.5}$	U_{GSL}	0.31	$V^{-1}\mu m$
K_S	4.3E-04	-	U_{BS}	6.2E-06	V^{-1}
K_{NZ}	0.24	V μm	E_{CRIT}	28.3	V/μm
K_{NB}	8.6E-05	μm	H_0	0.11	-
η_Z	-1.22	-	H_1	1.19	V
η_L	0.39	μm	T_{OX}	8	nm
μ_0	355.4	cm^2/Vs			

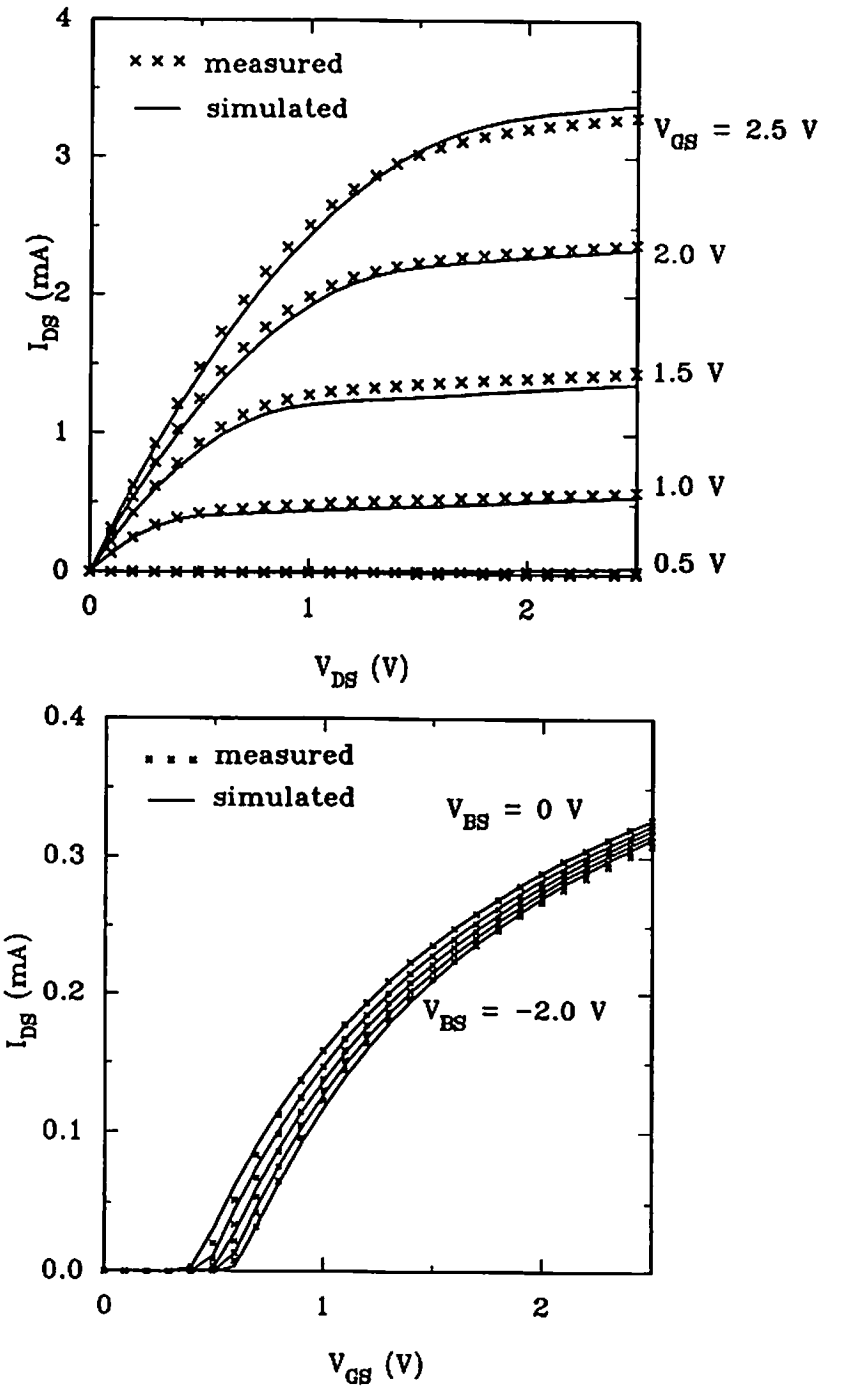


Fig. 6.7 Drain current characteristics obtained by fitting a single NMOS transistor with W/L = 10 μm/0.3 μm. (a) I_{DS} vs. V_{DS}. (b) I_{DS} vs. V_{GS}.

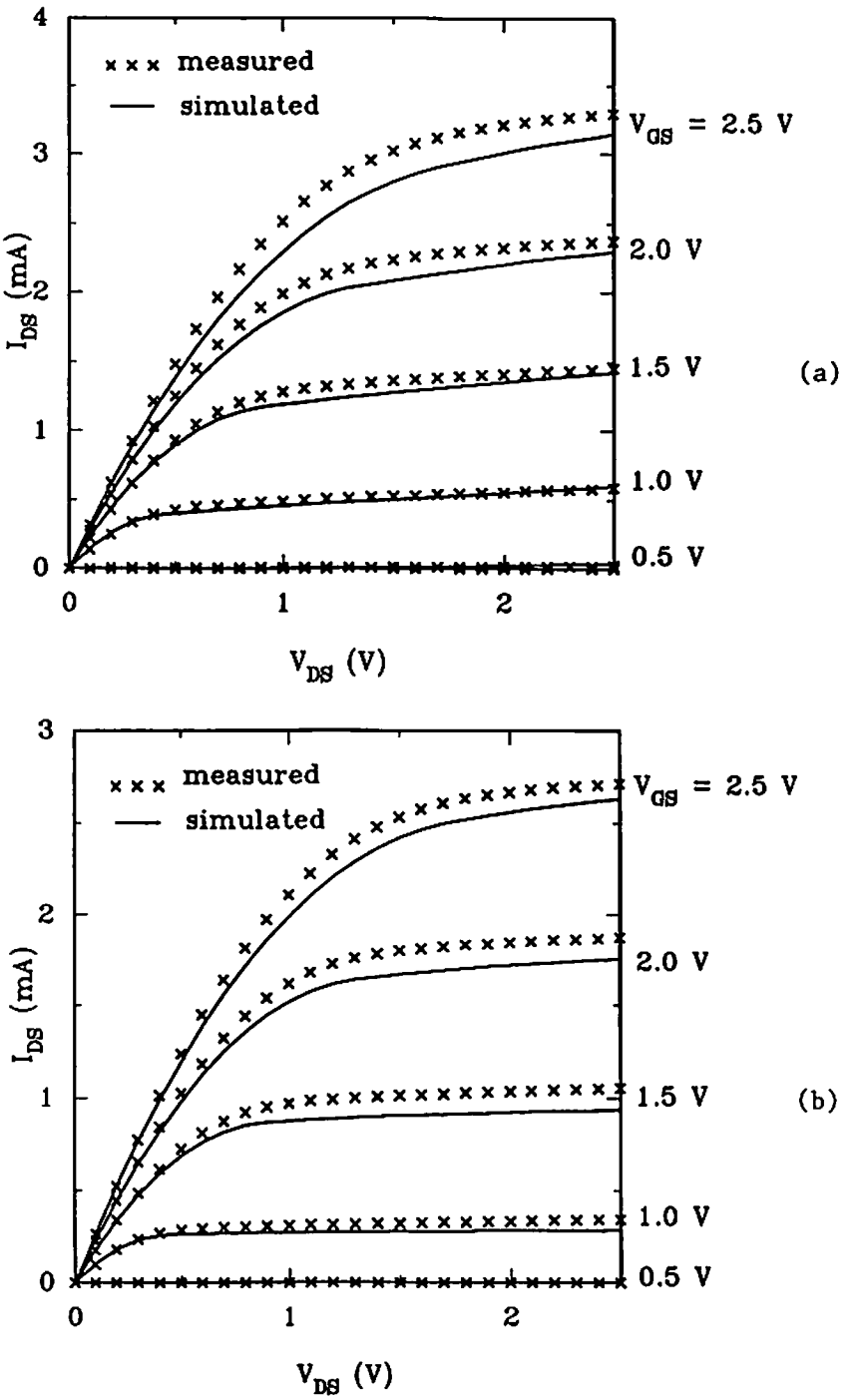


Fig. 6.8 I_{DS} vs. V_{DS} characteristics for NMOS transistors of a 0.4-μm technology from Samsung Electronics Co. (a) W/L = 10 μm/0.3 μm. (b) W/L = 10 μm/0.5 μm.

Figure 6.8 (continued)

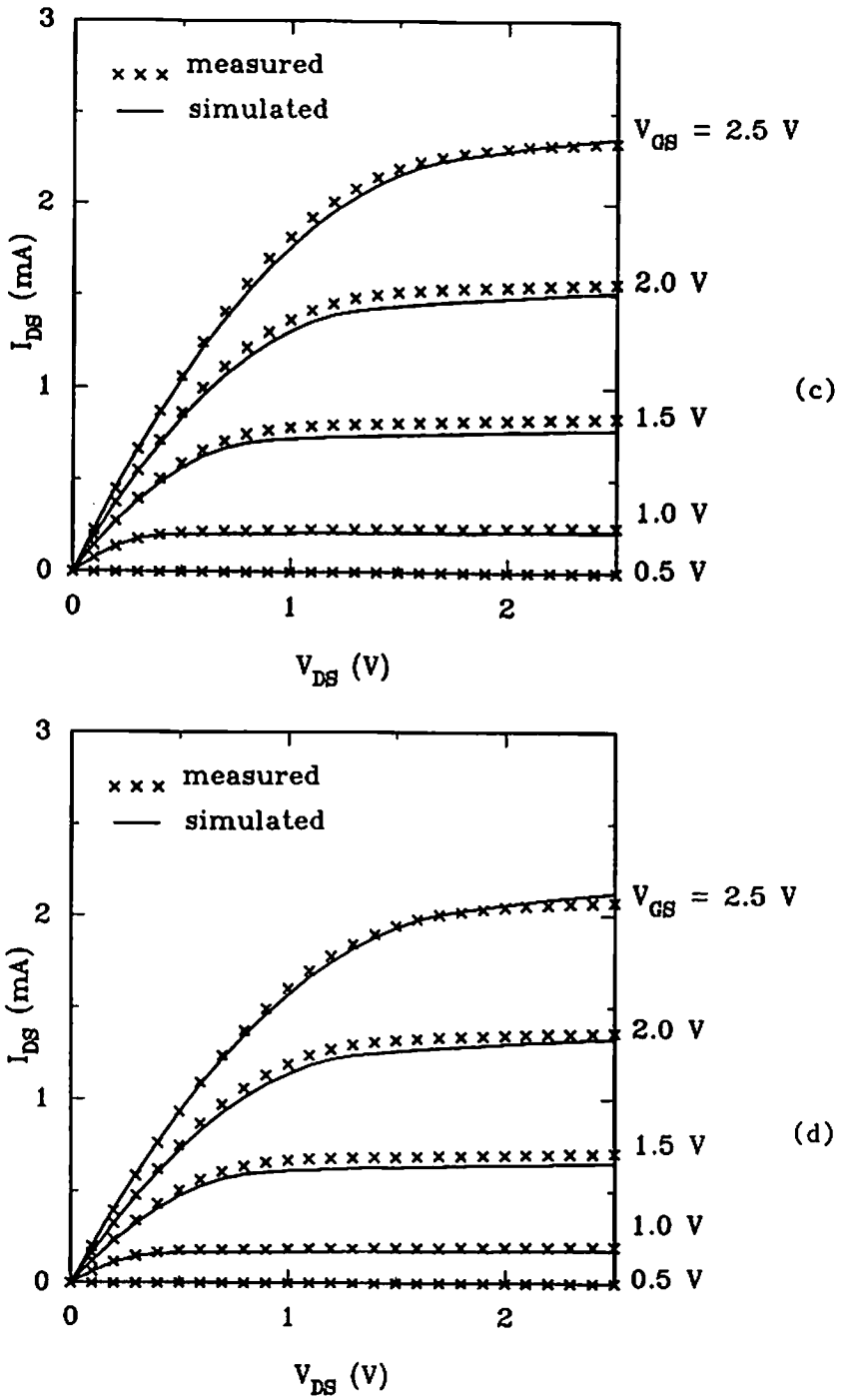


Fig. 6.8 (continued)
(c) W/L = 10 μm/0.7 μm. (d) W/L = 10 μm/0.9 μm.

Figure 6.8 (continued)

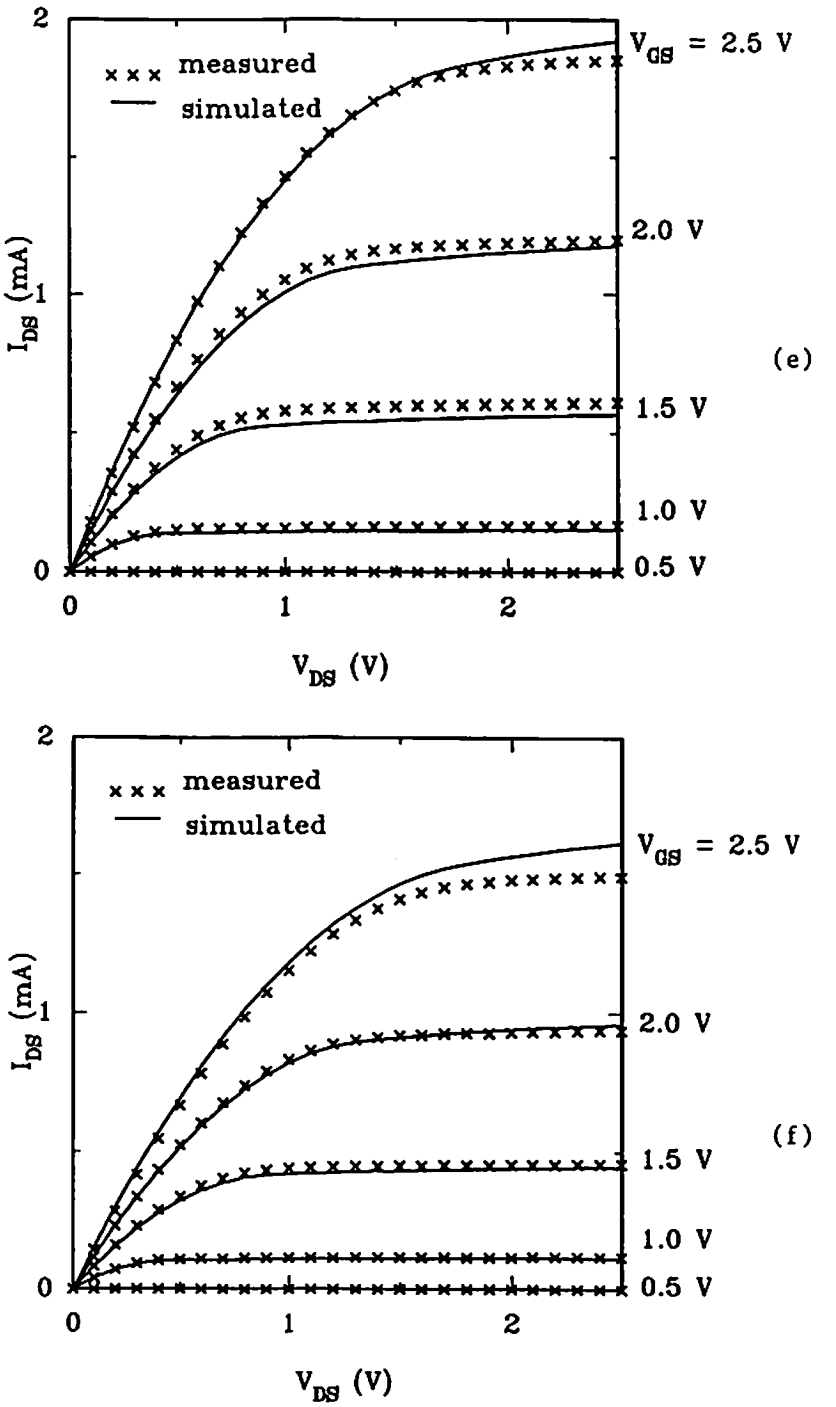


Fig. 6.8 (continued)
(e) W/L = 10 μm/1.1 μm. (f) W/L = 10 μm/1.5 μm.

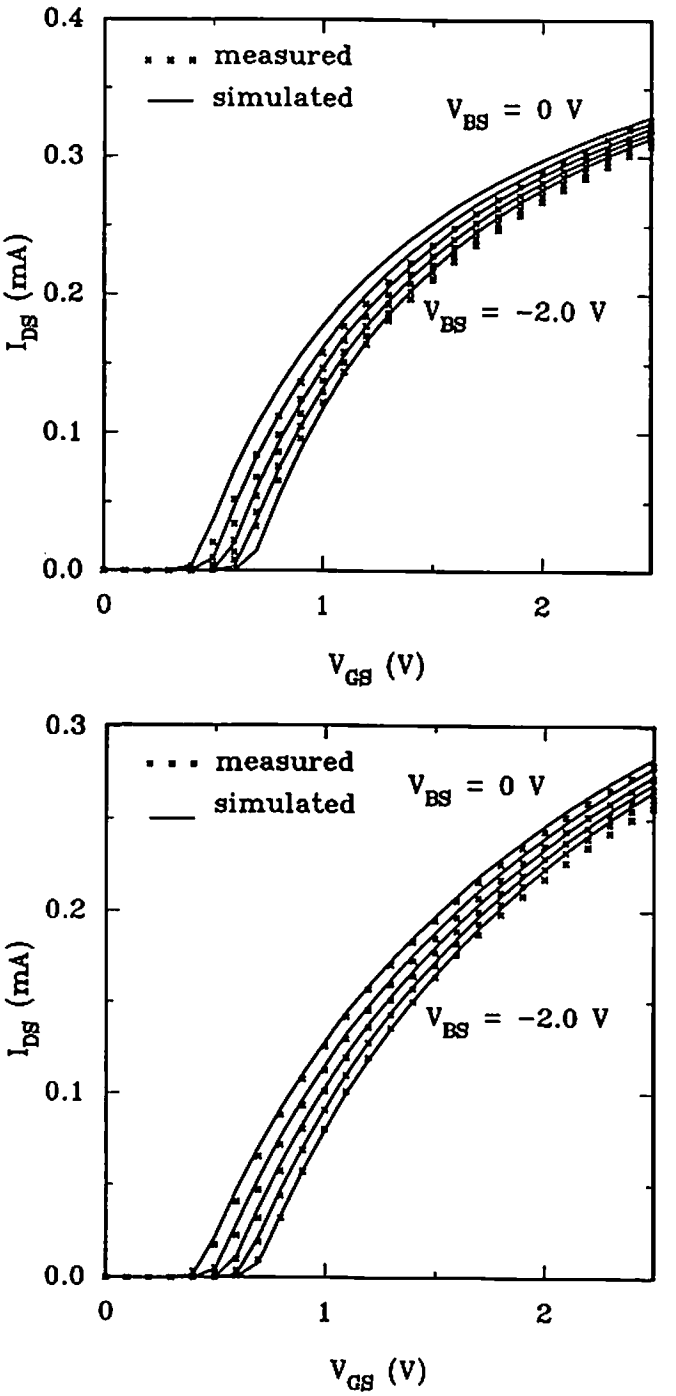


Fig. 6.9 I_{DS} vs. V_{GS} characteristics for NMOS transistors of a 0.4-μm technology from Samsung Electronics Co. (a) W/L = 10 μm/0.3 μm. (b) W/L = 10 μm/0.5 μm.

Figure 6.9 (continued)

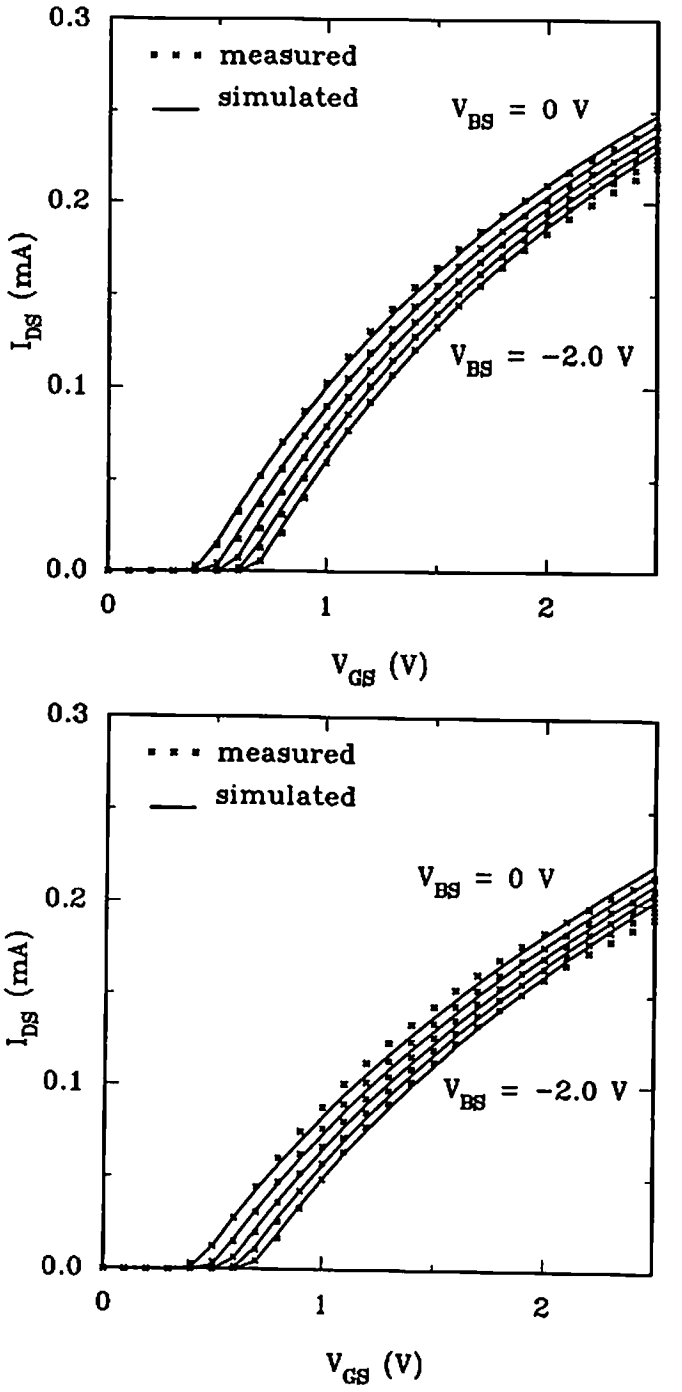
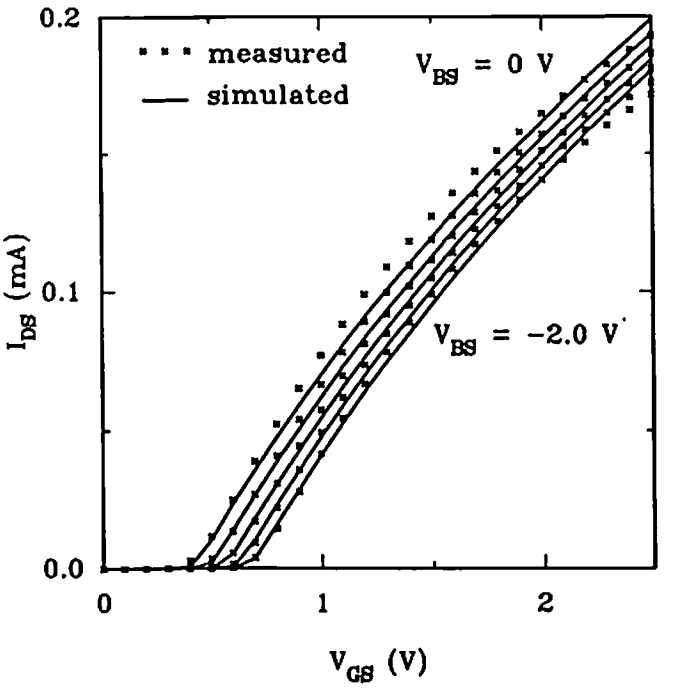
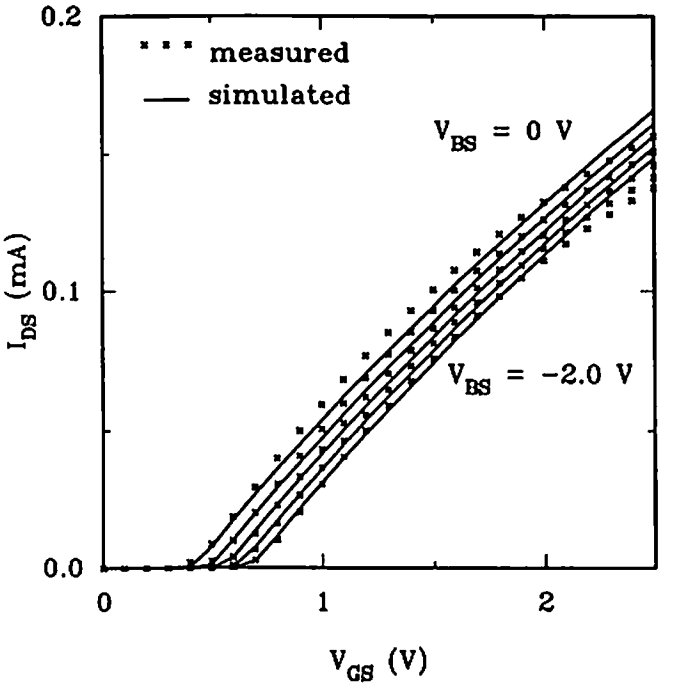


Fig. 6.9 (continued)
(c) W/L = 10 μm/0.7 μm. (d) W/L = 10 μm/0.9 μm.

Figure 6.9 (continued)



(e)



(f)

Fig. 6.9 (continued)
(e) W/L = 10 μm/1.1 μm. (f) W/L = 10 μm/1.5 μm.

Table 6.3 BSIM_plus parameter set extracted from PMOS transistors of a 0.4-μm CMOS technology of Samsung Electronics Co.

Symbol	Value	Unit	Symbol	Value	Unit
ϕ_S	0.89	V	ΔL	0.18	μm
V_{FB}	-0.33	V	ΔW	0.02	μm
γ_1	0.56	$V^{0.5}$	U_{GSZ}	-0.07	V^{-1}
γ_2	0.31	$V^{0.5}$	U_{GSL}	0.09	$V^{-1}\mu m$
K_S	3.4e-4	-	U_{BS}	1.5e-4	V^{-1}
K_{NZ}	0.22	V μm	E_{CRIT}	314	V/μm
K_{NB}	-3.9e-4	μm	H_0	1.61	-
η_Z	-0.04	-	H_1	42.3	V
η_L	0.04	μm	T_{OX}	8	nm
μ_0	90.0	cm^2/Vs			

Table 6.4 BSIM_plus parameter set extracted from a single NMOS transistor with W/L = 10 μm/0.3 μm.

Symbol	Value	Unit	Symbol	Value	Unit
ϕ_S	1.54	V	ΔL	8.4E-02	μm
V_{FB}	-1.21	V	ΔW	0.90	μm
γ_1	0.30	$V^{0.5}$	U_{GSZ}	-0.17	V^{-1}
γ_2	0.31	$V^{0.5}$	U_{GSL}	0.27	$V^{-1}\mu m$
K_S	4.7E-04	-	U_{BS}	8.6E-07	V^{-1}
K_{NZ}	0.29	V μm	E_{CRIT}	240.3	V/μm
K_{NB}	1.1E-04	μm	H_0	9.9E-03	-
η_Z	-1.46	-	H_1	0.24	V
η_L	0.48	μm	T_{OX}	8	nm
μ_0	316.0	cm^2/Vs			

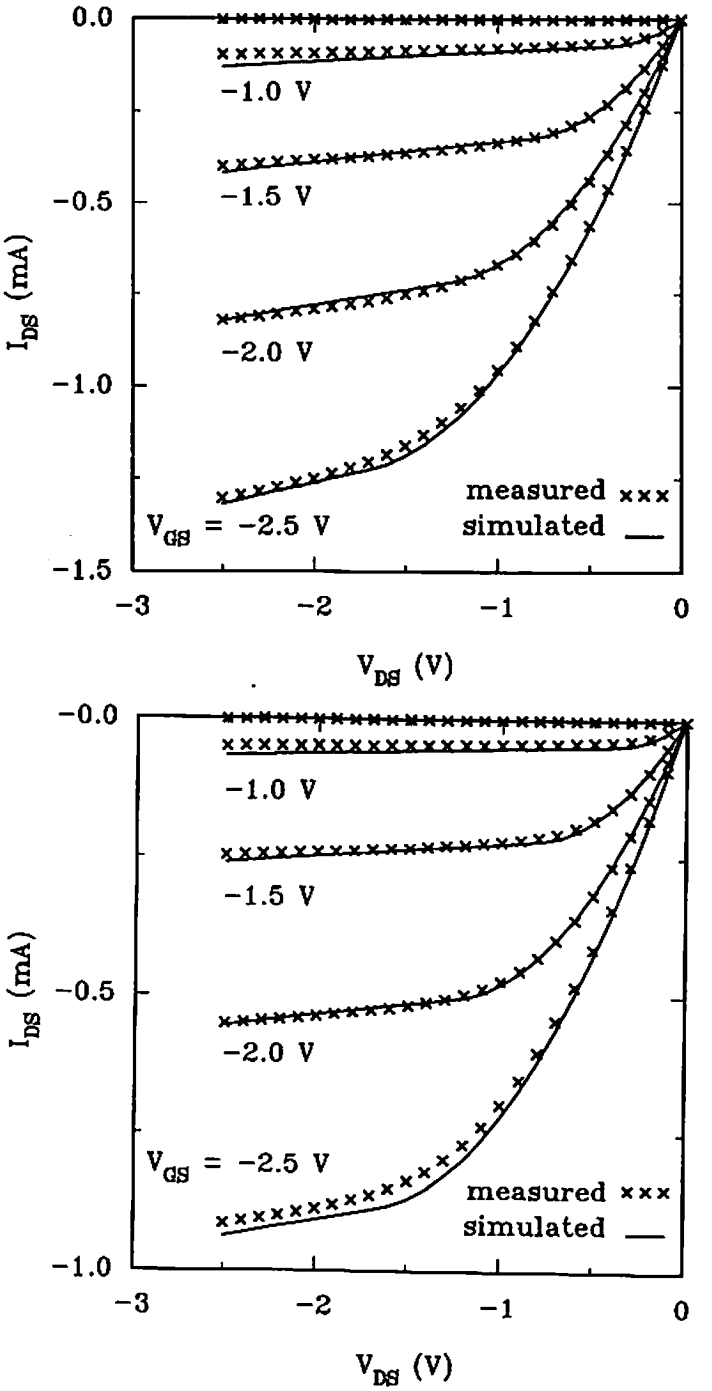


Fig. 6.10 I_{DS} vs. V_{DS} characteristics for PMOS transistors of a 0.4-μm technology from Samsung Electronics Co. (a) W/L = 10 μm/0.5 μm. (b) W/L = 10 μm/0.7 μm.

Figure 6.10 (continued)

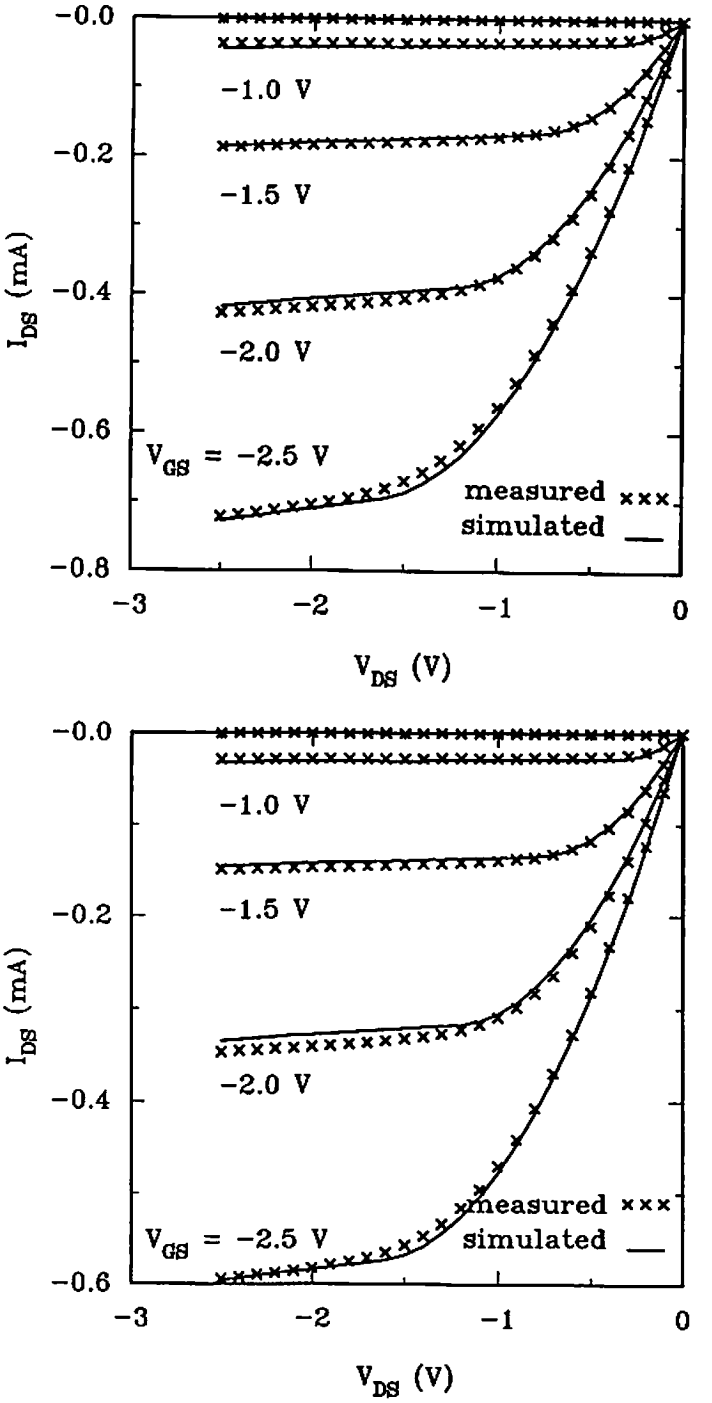
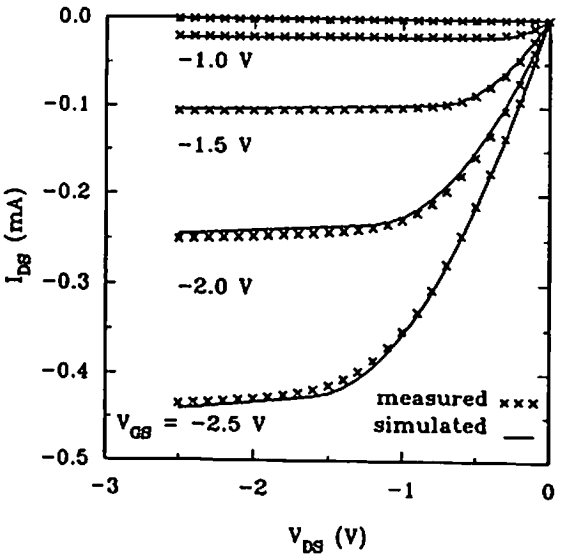


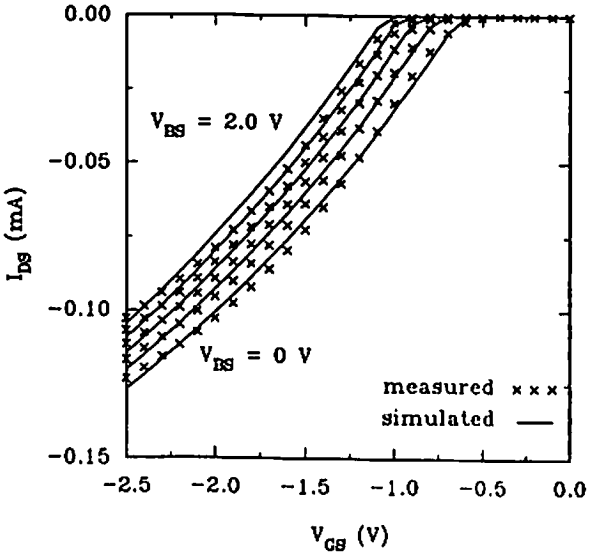
Fig. 6.10 (continued)
(c) W/L = 10 μm/0.9 μm. (d) W/L = 10 μm/1.1 μm.

Figure 6.10 (continued)



(e)

Fig. 6.10 (continued)
(e) W/L = 10 μm/1.5 μm.



(a)

Fig. 6.11 I_{DS} vs. V_{GS} characteristics for PMOS transistors of a 0.4-μm technology from Samsung Electronics Co.
(a) W/L = 10 μm/0.5 μm.

Figure 6.11 (continued)

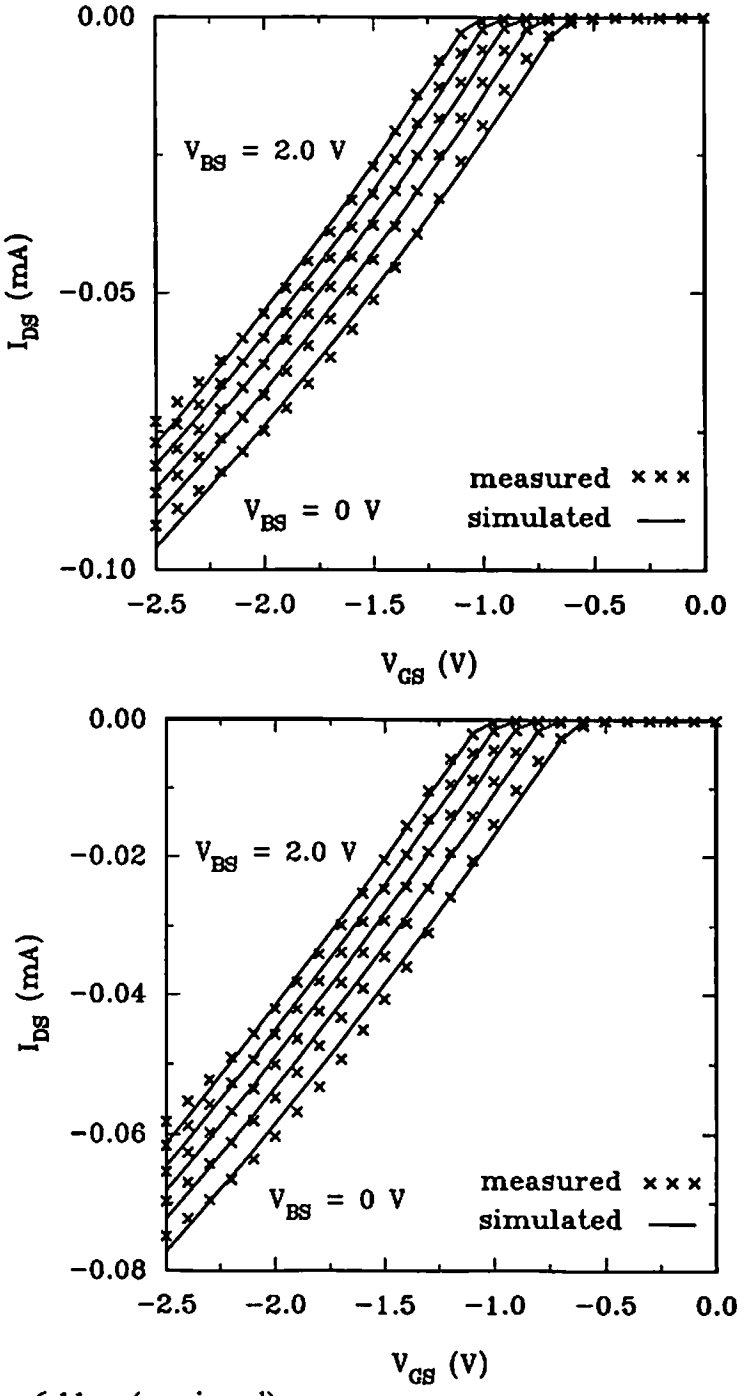
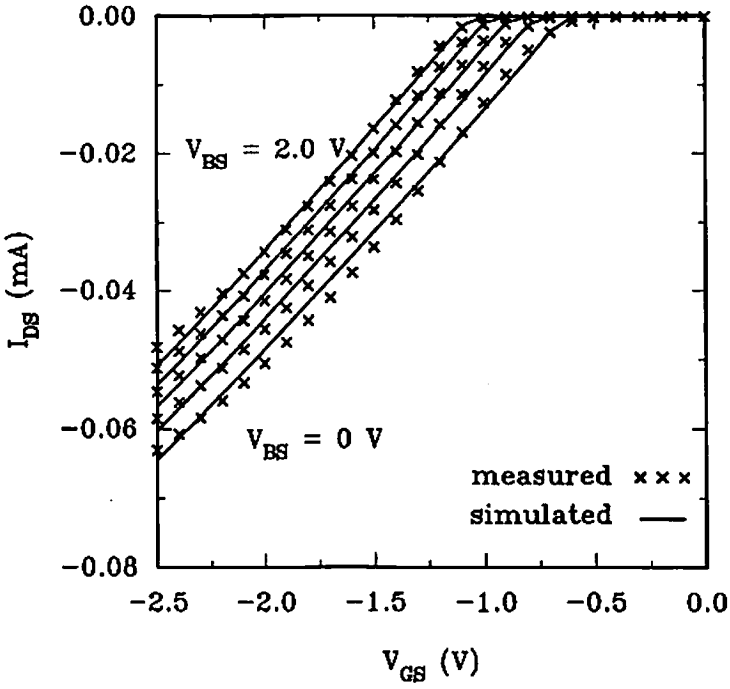
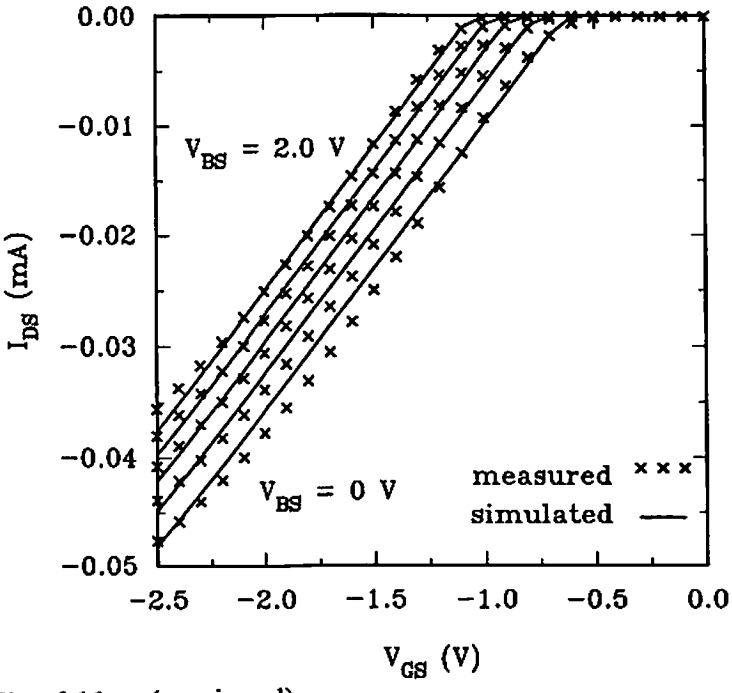


Fig. 6.11 (continued)
(b) W/L = 10 μm/0.7 μm. (c) W/L = 10 μm/0.9 μm.

Figure 6.11 (continued)



(d)



(e)

Fig. 6.11 (continued)
(d) W/L = 10 μm/1.1 μm. (e) W/L = 10 μm/1.5 μm.

obtain the results shown in Fig. 6.8 and Fig. 6.9. Results of fitting an NMOS transistor with W/L = 10 μm/0.3 μm separately with the parameters that are listed in Table 6.4, are shown in Fig. 6.7. A PMOS parameter set was also extracted from transistors of similar geometries. The parameter set is listed in Table 6.3, and drain current characteristics are shown in Fig. 6.10 and Fig. 6.11.

6.2 Demonstration of Charge Conservation Property

A single MOS transistor was simulated using the BSIM_plus, MOS Level-2 and Level-3 models [6.1] in order to compare the charge conservation property between these models based on methods reported in [6.6]. The transistor was connected to voltage sources, a capacitor and a resistor as shown in Fig. 6.12(a). The voltages to the drain, bulk and gate of the transistor were pulsed between 0 V and V_{DD}. The pulse waveforms of the voltage sources are shown in Fig. 6.12(b). Figure 6.12(c) shows the comparison of the simulated voltages across the capacitor using the BSIM_plus and Level-2 models. The SPICE option variables reltol = 0.5e-3, abstol = 1e-12, and chgtol = 1e-15 were used for this simulation. The value of X_{QC} was set to 0.4 in the Level-2 parameter set. This parameter value causes the channel charge to be partitioned between the source and drain in a 60/40 ratio when the transistor is biased in the saturation region. The same partitioning ratio is used in BSIM_plus. Figure 6.12(d) shows the comparison of the simulated voltages across the capacitor that are obtained using the

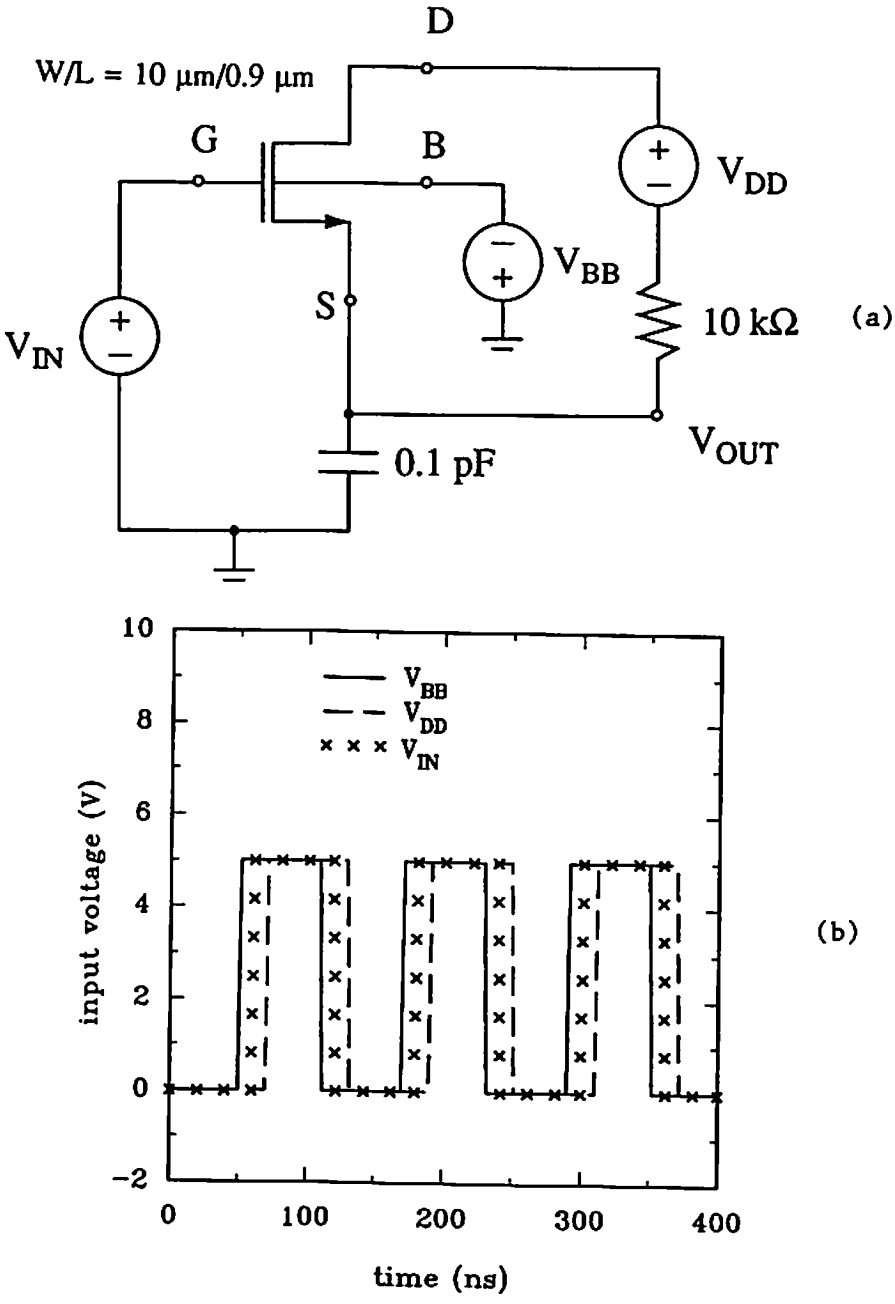
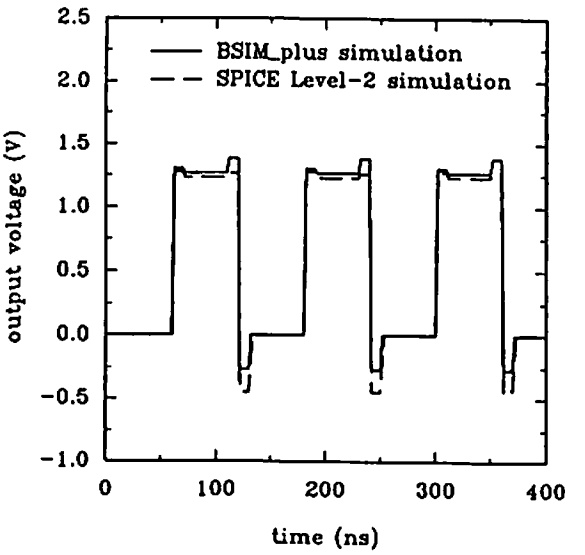
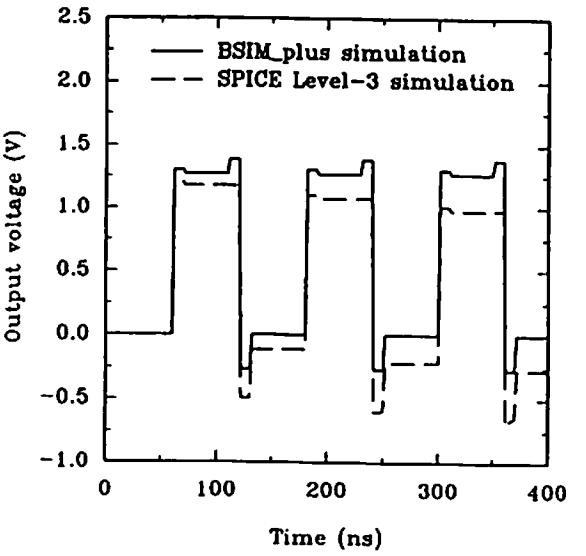


Fig. 6.12 Simulation to compare the charge conservation propertied of different MOS models.
(a) Circuit schematic. (b) Input waveforms.

Figure 6.12 (continued)



(c)



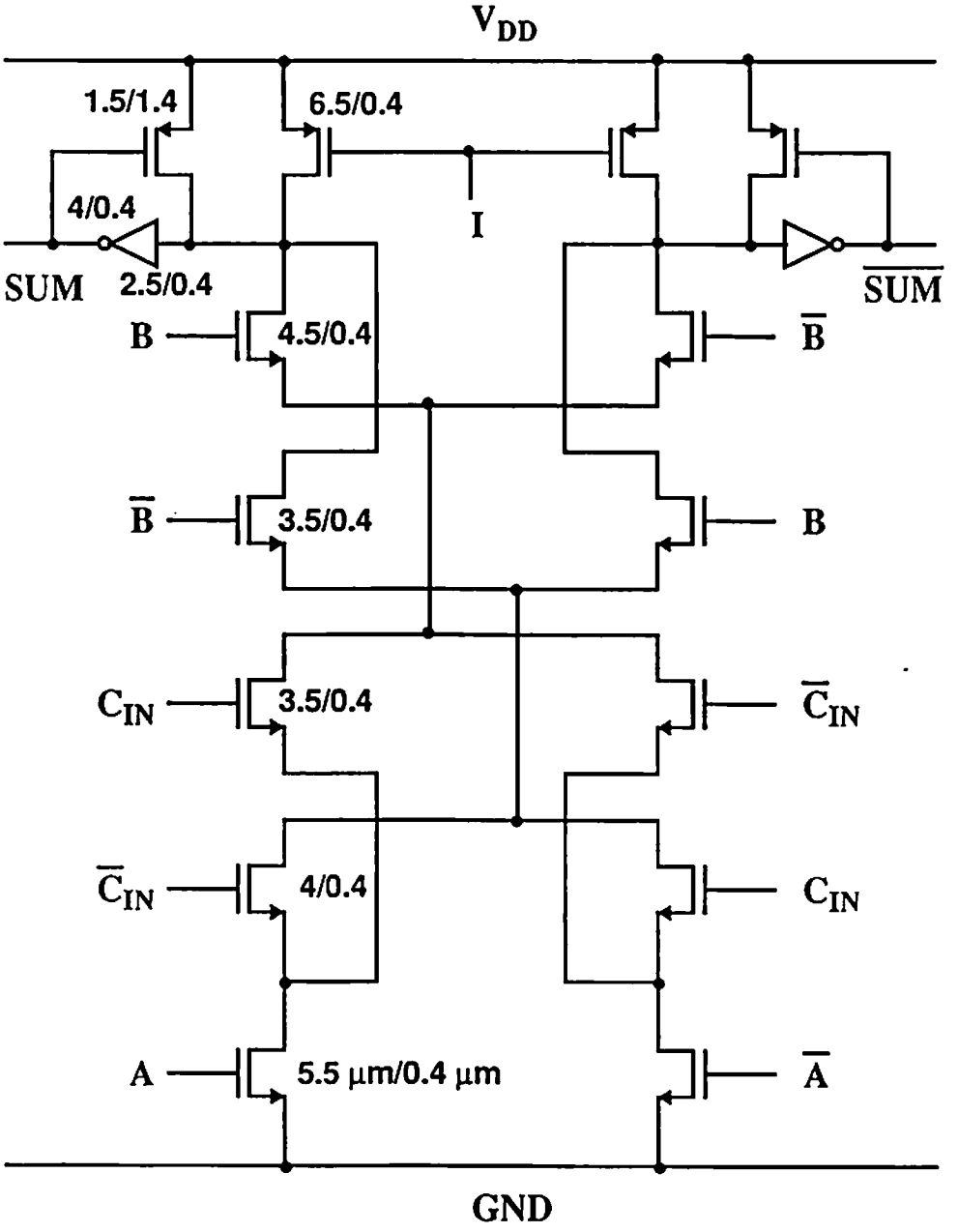
(d)

Fig. 6.12 (continued)
(c) Comparison of BSIM_plus and Level-2 simulation results.
(d) Comparison of BSIM_plus and Level-3 simulation results.

BSIM_plus and Level-3 models. The SPICE option variables reltol = 1e-5, abstol = 1e-11 and chgtol = 1e-15 were used in this simulation. The voltage across the capacitor that was obtained using the Level-3 model did not remain zero after several pulses but increased in magnitude. This was caused by an accumulation of charge on the capacitor. The Level-3 model uses the Meyer model for the transistor parasitic capacitances, in which charge is not conserved [6.7,6.8]. The charge that accumulates on the capacitor is generated due to the non-conservation effect in the simulated results. The Level-2 model uses the Ward-Dutton model in which charge is conserved [6.9]. The simulation results in Fig. 6.12(c) and Fig. 6.12(d) confirm that charge conservation is also achieved in the BSIM_plus model.

6.3 Self-Timed Adder Circuit

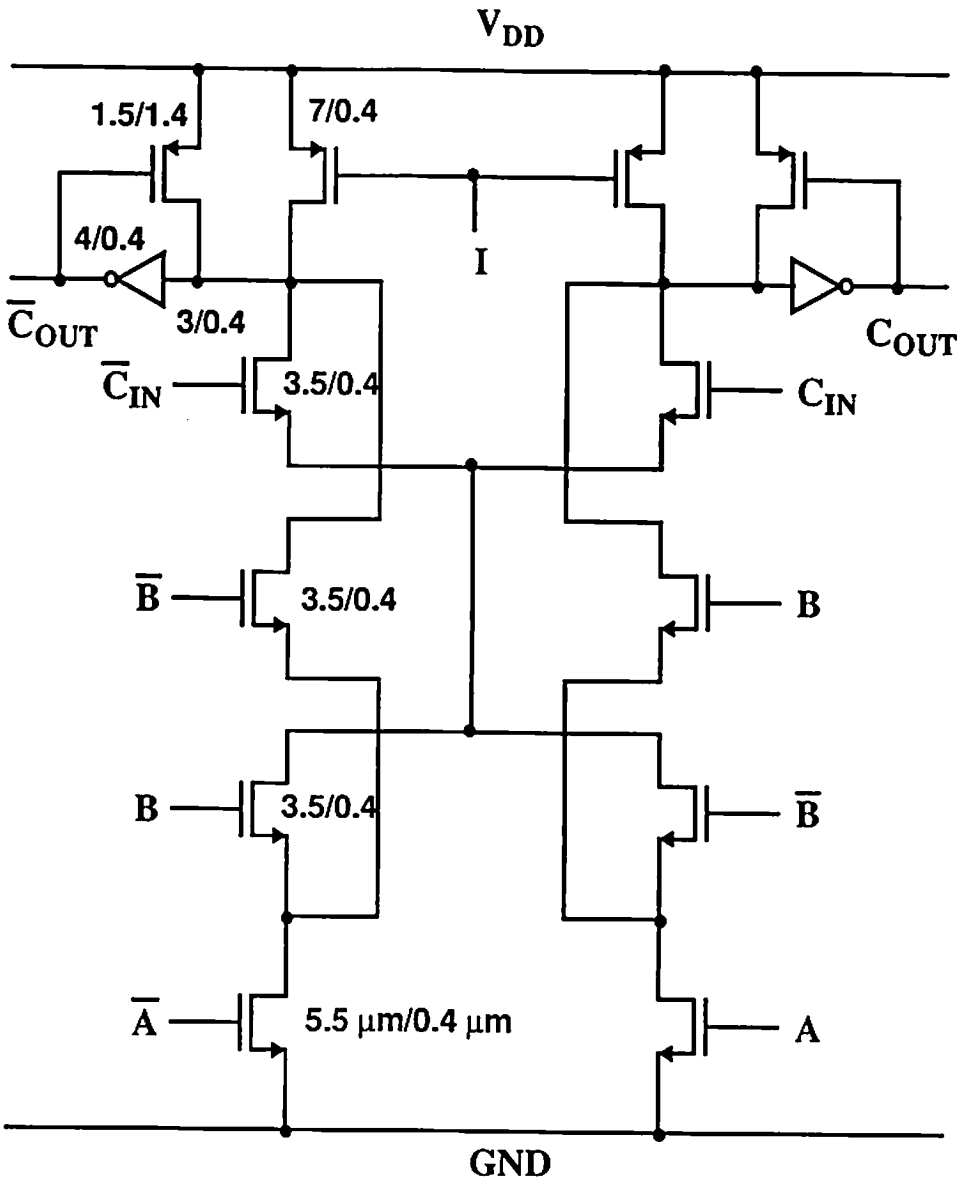
The distribution of a global clock to different circuits in a VLSI chip is a major problem in high-speed computing systems, since the latency required to accommodate the clock skew slows down the entire system. Self-timed circuits operate on the basis of initialization and completion signals, and communicate with each other using suitable handshake protocols. A self-timed adder circuit was designed in a 0.4-μm technology and simulated using the BSIM_plus model. The schematics of the SUM and CARRY stages of the adder are shown in Fig. 6.13(a) and Fig. 6.13(b) [6.10]. The initialization signal, I, triggers the operation of the circuit. For each circuit block, the output signal and its complement can be used to simply generate a



(a)

Fig. 6.13 BSIM_plus simulation results of a self-timed adder circuit [6.6]. (a) Sum stage.

Figure 6.13 (continued)



(b)

Fig. 6.13 (continued)
(b) Carry Stage.

Figure 6.13 (continued)

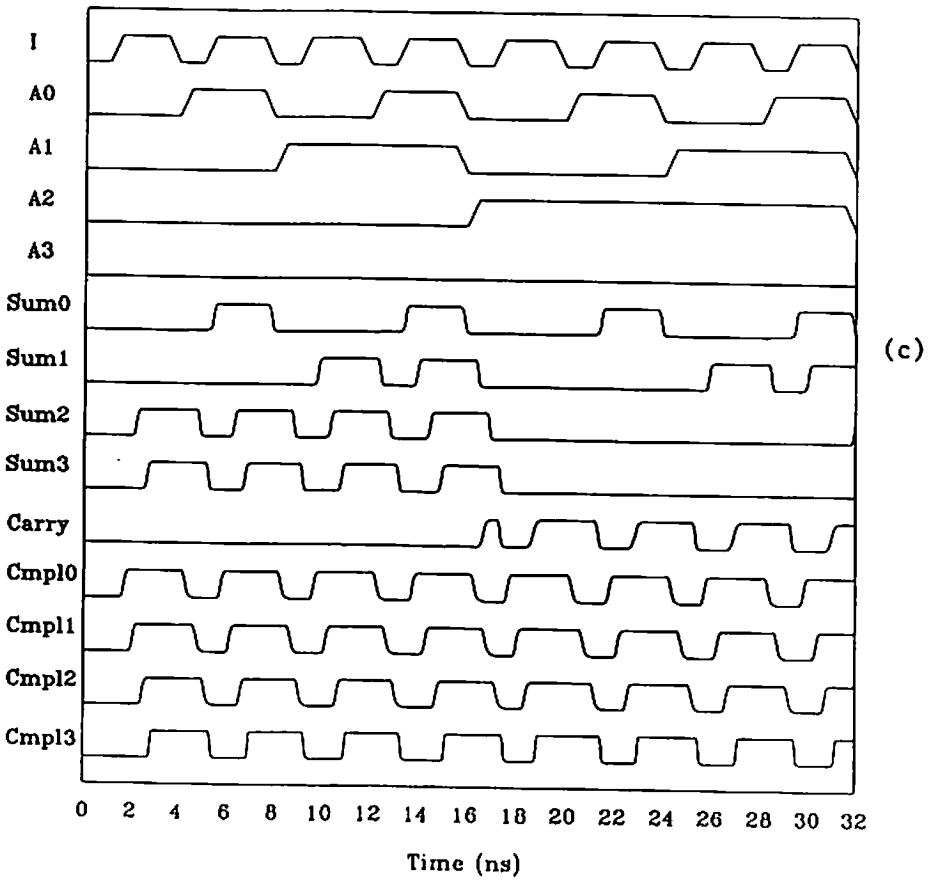


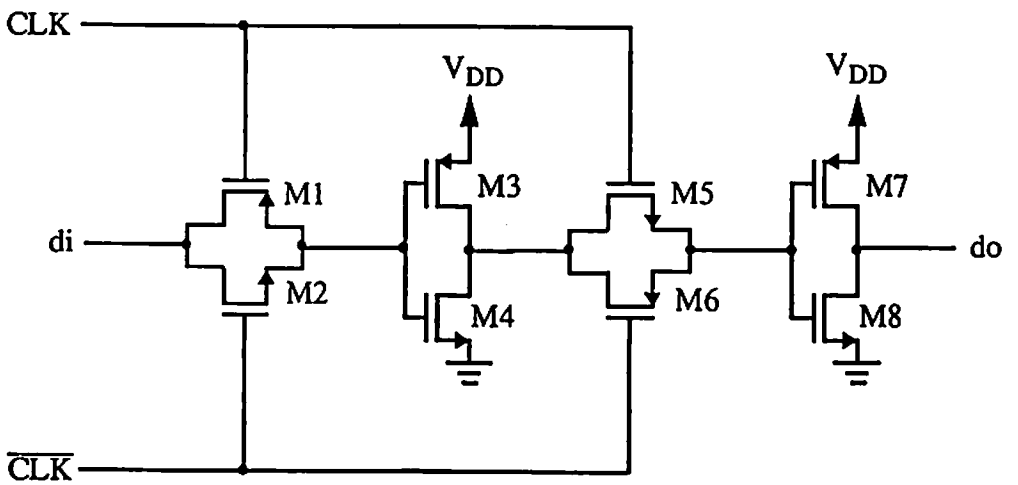
Fig. 6.13 (continued)
(c) Simulated waveforms.

completion signal, which in turn can be used to initialize the operation of another circuit building block. A four-bit adder was constructed and simulated. The input B_3 B_2 B_1 B_0 was set to 1100. The input and output voltage waveforms, along with the completion signals generated in each circuit block are shown in Fig. 6.13(c).

6.4 Clocked and Asynchronous Master-Slave Latches

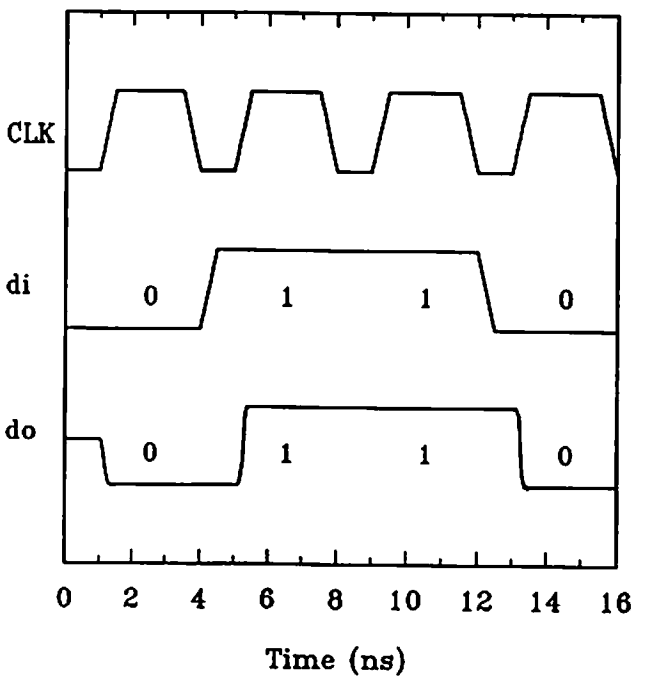
The schematic of a two-phase clocked master-slave latch designed using transmission gate logic is shown in Fig. 6.14(a). The circuit was simulated using the BSIM_plus model. The clock, input and output waveforms of the circuit are shown in Fig. 6.14(b). The use of this circuit in a VLSI chip requires careful distribution of the clock signal. The problem can be alleviated by using the single-phase master-slave latch whose schematic is shown in Fig. 6.15(a) [6.11]. However, this circuit also requires careful distribution of the clock signal and its complement, or local complementing of the clock signal. The simulated waveforms of this latch are shown in Fig. 6.15(b).

An asynchronous master-slave latch that uses four-state redundant logic was recently reported [6.12]. The circuit schematic is shown in Fig. 6.16(a). The four-state logic uses four bits to encode "0" and "1" values in two different phases. This helps to guarantee race-free and hazard-free operation of the latch. Although this type of latch occupies additional area, it can be



Transistor Size:
PMOS: 10 μm / 0.5 μm
NMOS: 5 μm / 0.5 μm

(a)



(b)

Fig. 6.14 BSIM_plus simulation results of a two-phase clocked master-slave latch. (a) Circuit schematic. (b) Waveforms.

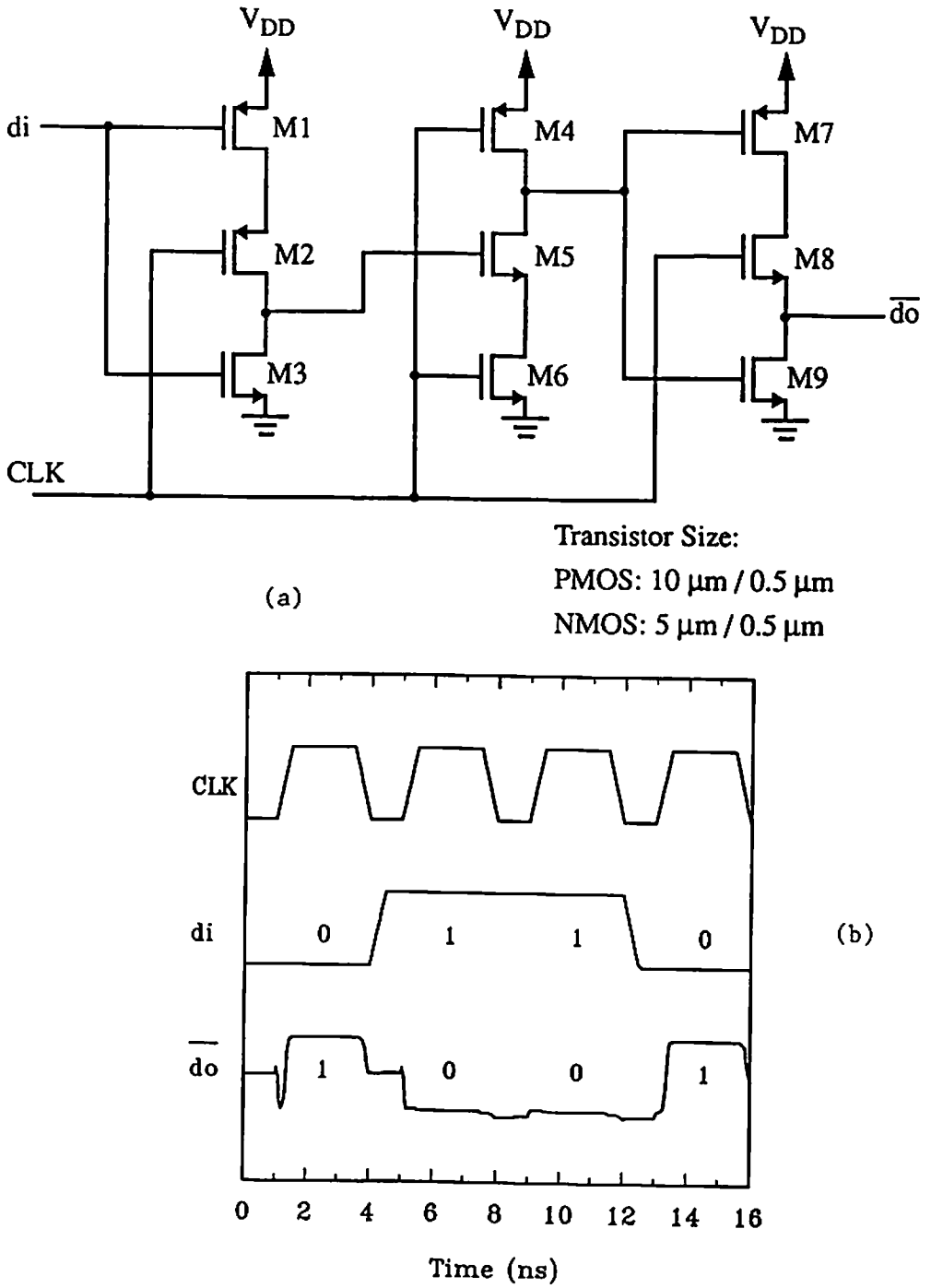


Fig. 6.15 BSIM_plus simulation results of a single-phase clocked master-slave latch. (a) Circuit schematic. (b) Waveforms.

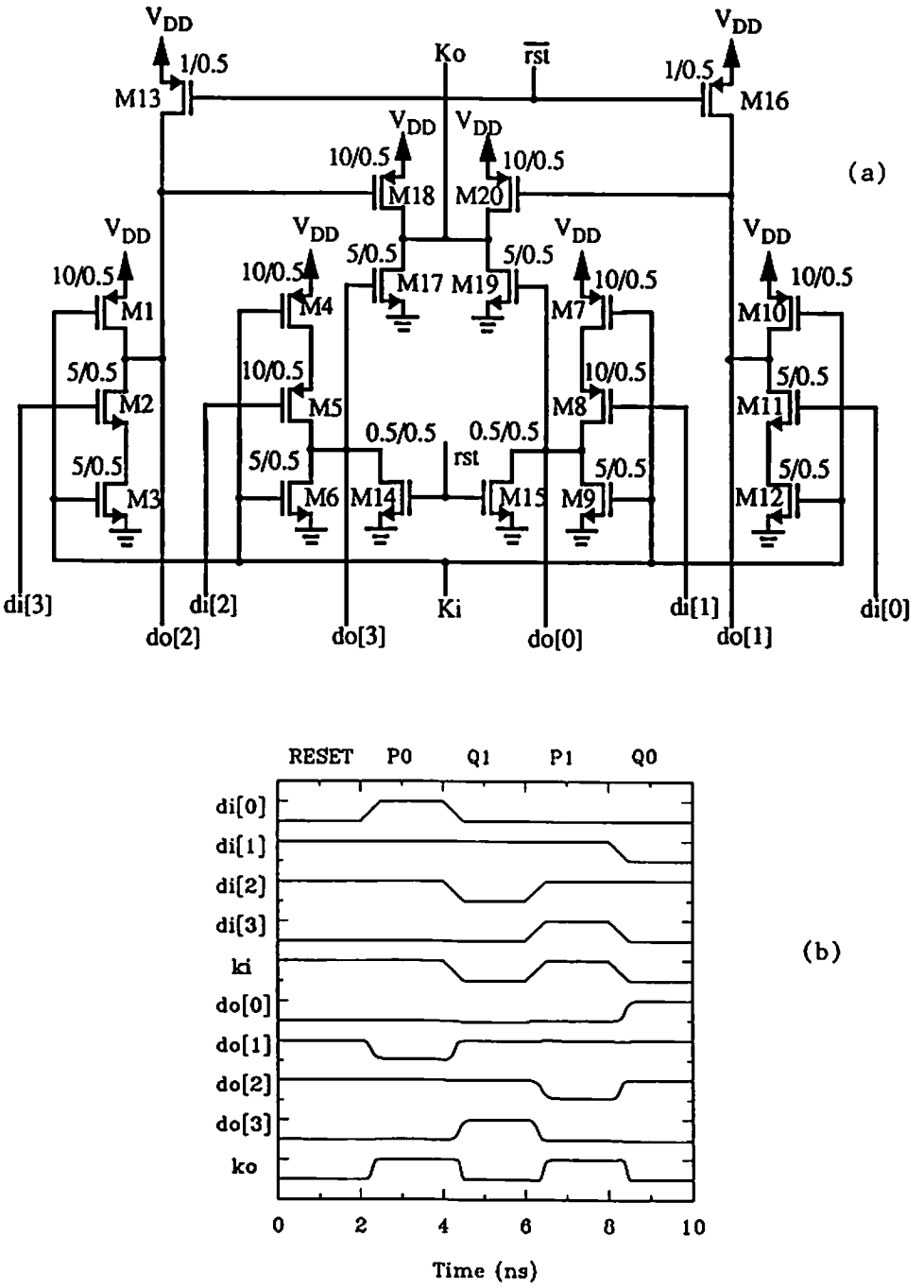


Fig. 6.16 BSIM_plus simulation results of an asynchronous master-slave latch. (a) Circuit schematic. (b) Waveforms.

used to speed up the overall performance of the system. The simulated waveforms of the asynchronous latch are shown in Fig. 6.16(b).

6.5 Dynamic Memory Circuit

A 16-word x 1-bit dynamic memory circuit was designed in a 0.4-μm CMOS technology and simulated using the BSIM_plus model. The circuit schematic of the memory circuit including the write circuitry, precharge circuitry, memory cell, sense amplifier and read circuitry is shown in Fig. 6.17(a). The simulated waveforms of control and data signals are shown in Fig. 6.17(b). Simulation was done for a single cycle containing Write-0, Read-0, Write-1 and Read-1 operations. The bit-line and dummy cell were first precharged using the PRECHARGE and PRECHARGE(dum) signal lines, respectively. The bit-line was precharged to 2.5 V while the dummy cell was precharged to 1.8 V. The precharging was then disabled and the WRITE signal was used to enable entry of data onto the BIT line. At the same time, the WORD line from the decoder allowed the writing of data from the BIT line to a specific memory cell. The data in the memory cell can be refreshed to V_{DD} by using the RESTORE signal. During the read operation, the WORD line was enabled and the data flow was from the memory cell onto the BIT line. The sense amplifier, which consists of a cross-coupled common-source transistor pair, drove the signal to V_{DD} or the power supply ground.

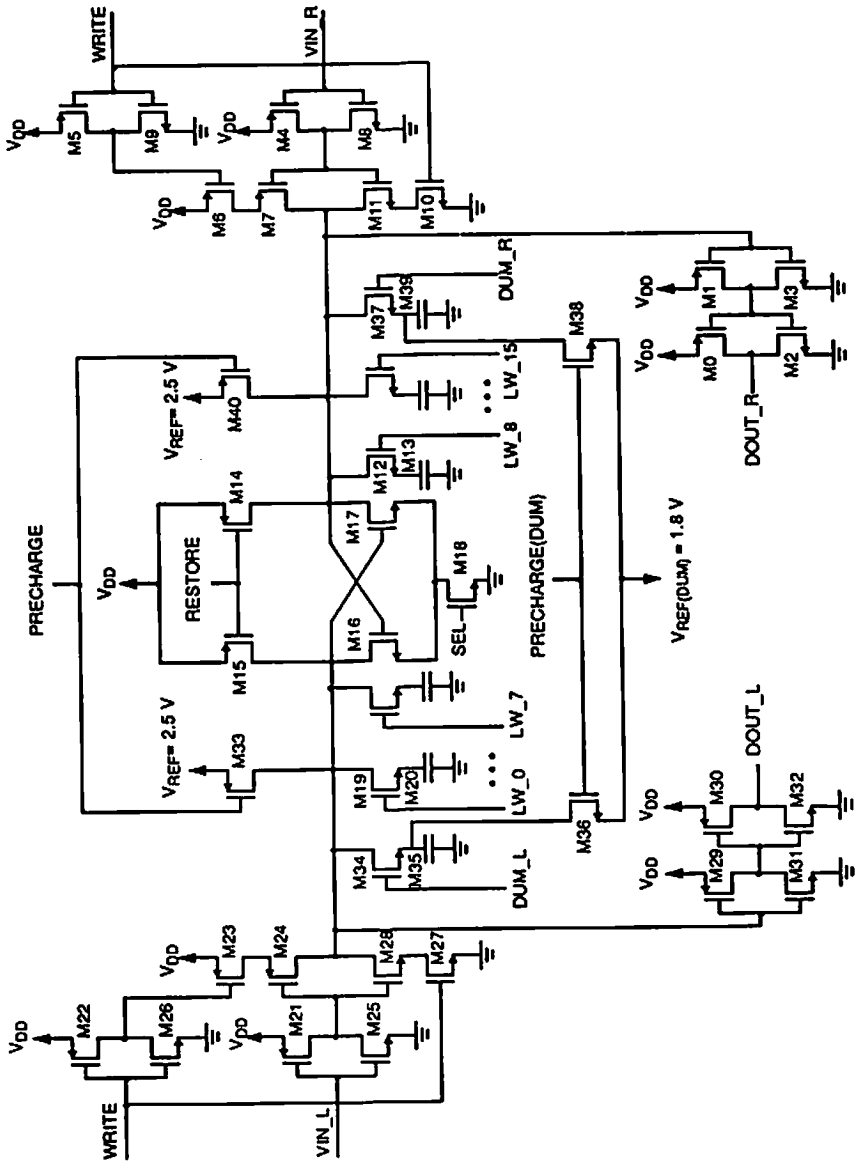


Fig. 6.17 BSIM_plus simulation results of a dynamic memory circuit.
(a) Circuit schematic.
For device size information, see Appendix C.

Figure 6.17 (continued)

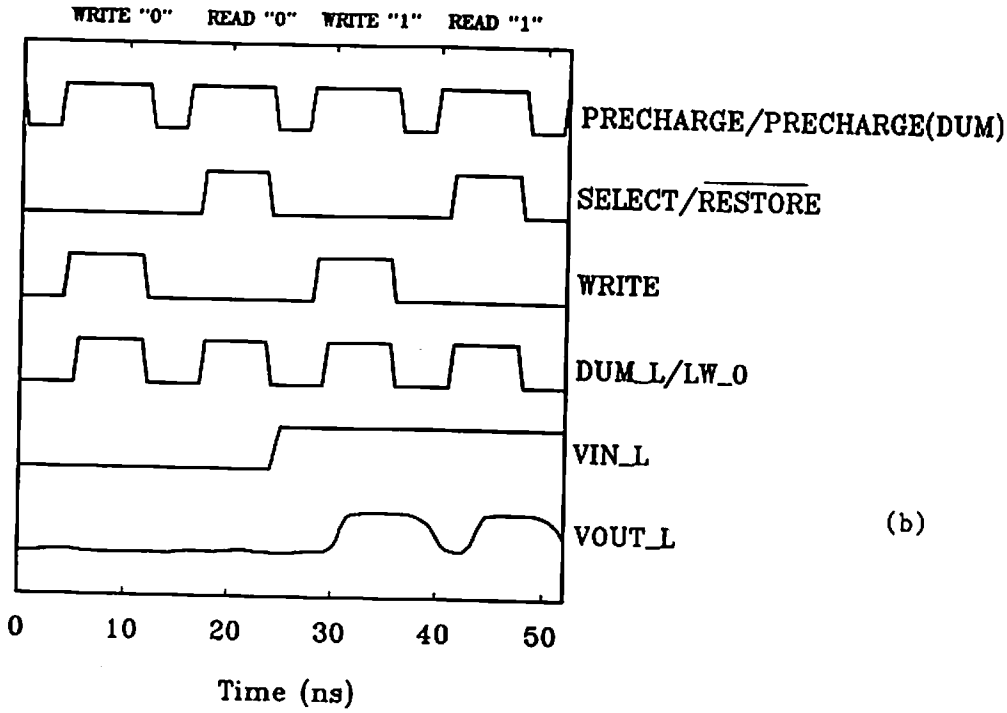


Fig. 6.17 (continued)
(b) Simulated waveforms.

6.6 Two-Stage and Single-Stage Amplifiers

A two-stage operational amplifier with frequency compensation was designed in a 0.5-μm CMOS technology. The circuit schematic of the amplifier is shown in Fig. 6.18(a) [6.13] and the transistor geometries that were used are listed in Table 6.5. The amplifier was designed to operate between power supply voltages of ± 2.5 V and a bias current of 28 μA was used in the simulations. For the determination of D.C. voltage gain and unity-gain frequency, the amplifier was simulated in the open-loop configuration. The systematic offset voltage and output range were also determined with the amplifier in the open-loop configuration. The slew rate and settling time were determined by simulating the amplifier in a unity-gain configuration and applying a step voltage to the input. Figure 6.18(b) shows the voltage gain characteristics of the amplifier. The configuration of the amplifier for the determination of the slew rate and settling time is shown in Fig. 6.18(c) along with the corresponding input and output waveforms. The common-mode rejection ratio was calculated from the differential-mode and common-mode gains. The common-mode gain was determined by connecting the inverting and non-inverting inputs of the amplifier together and simulating the amplifier using an A.C. analysis. The simulated results that were obtained by using the BSIM_plus model are listed in Table 6.6.

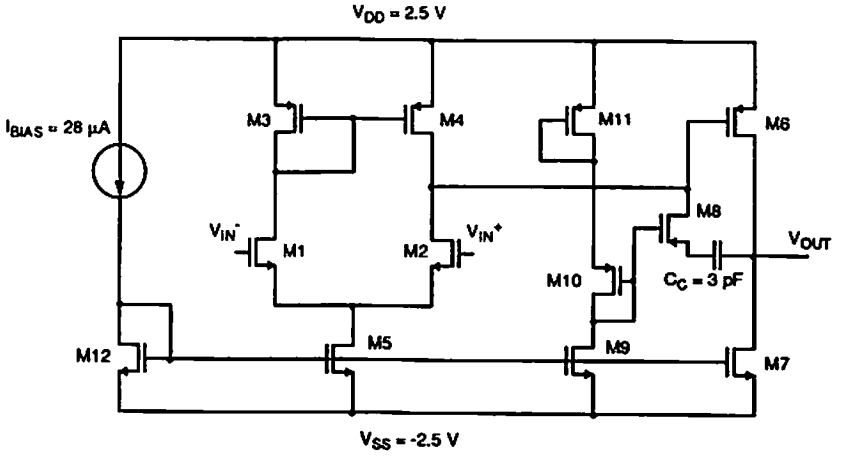
A single-stage folded-cascode amplifier [6.14] was designed in a 0.5-μm CMOS technology and simulated using the BSIM_plus model. The circuit schematic of the simulated amplifier is shown in Fig. 6.19(a). The transistor geometries that were used are listed in Table 6.7. Offset compensation was

Table 6.5 Transistor geometries used in the two-stage operational amplifier.

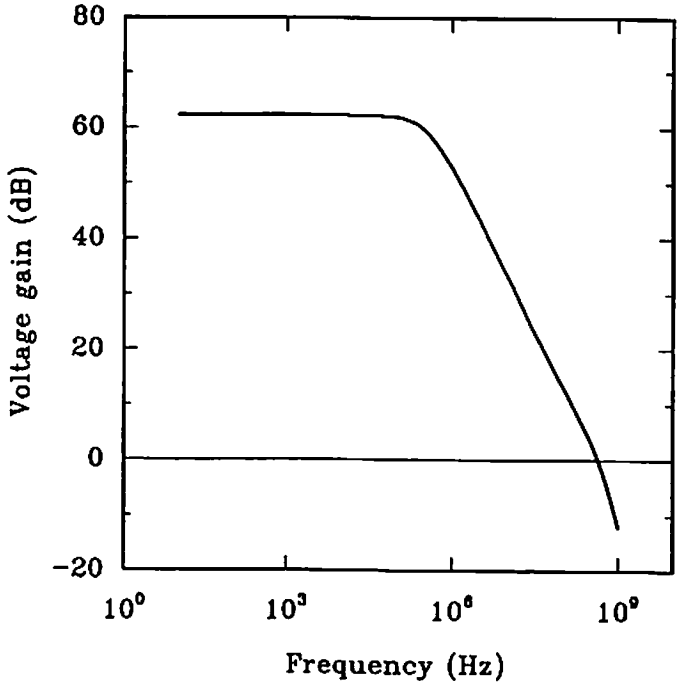
Transistor	W (μm)	L (μm)
M1,M2	250	0.5
M3,M4	25	0.75
M5	10	1
M6	250	0.75
M7	50	1
M8	27	0.75
M9	6	1
M10	3	0.75
M11	18	0.75

Table 6.6 Simulated performance characteristics of a two-stage operational amplifier.

Performance characteristic	Two-stage operational amplifier
Power supply	± 2.5 V
D. C. Gain	62.3 dB
Unity-gain freq. (1 pF load)	407 MHz
Systematic offset voltage	349.6 μV
Output range	-2.5 V to 2.22 V
Slew rate	0.3 V/ns (10 pF load)
Settling time (0.1 %)	27.5 ns (10 pF load)
CMRR @ 1 kHz	71 dB



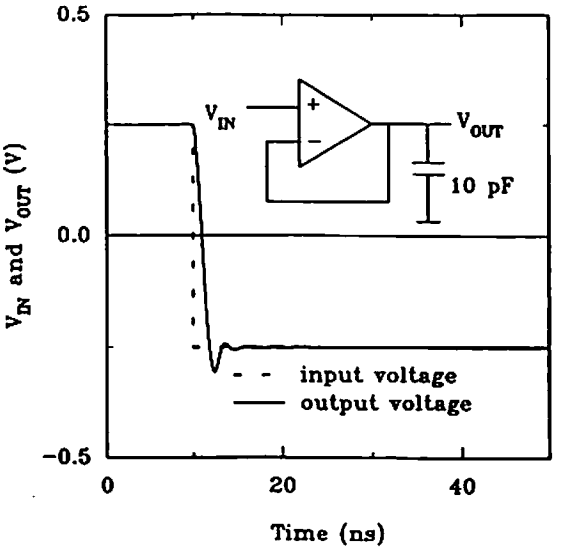
(a)



(b)

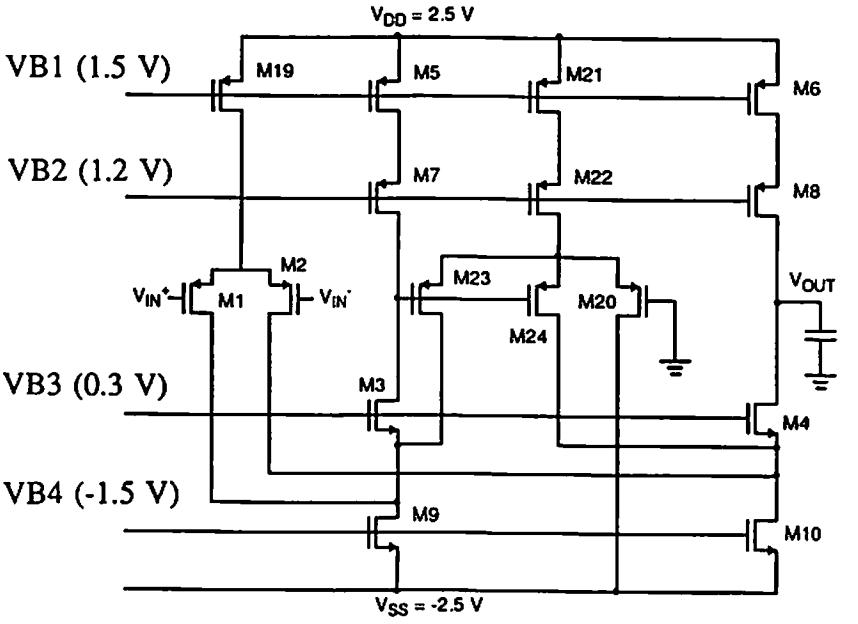
Fig. 6.18 BSIM_plus simulation results of a two-stage operational amplifier. (a) Circuit schematic. (b) Gain characteristics.

Figure 6.18 (continued)



(c)

Fig. 6.18 (continued)
(c) Determination of slew rate and settling time.



(a)

Fig. 6.19 BSIM_plus simulation results of a single-stage folded-cascode amplifier. (a) Circuit schematic.

Figure 6.19 (continued)

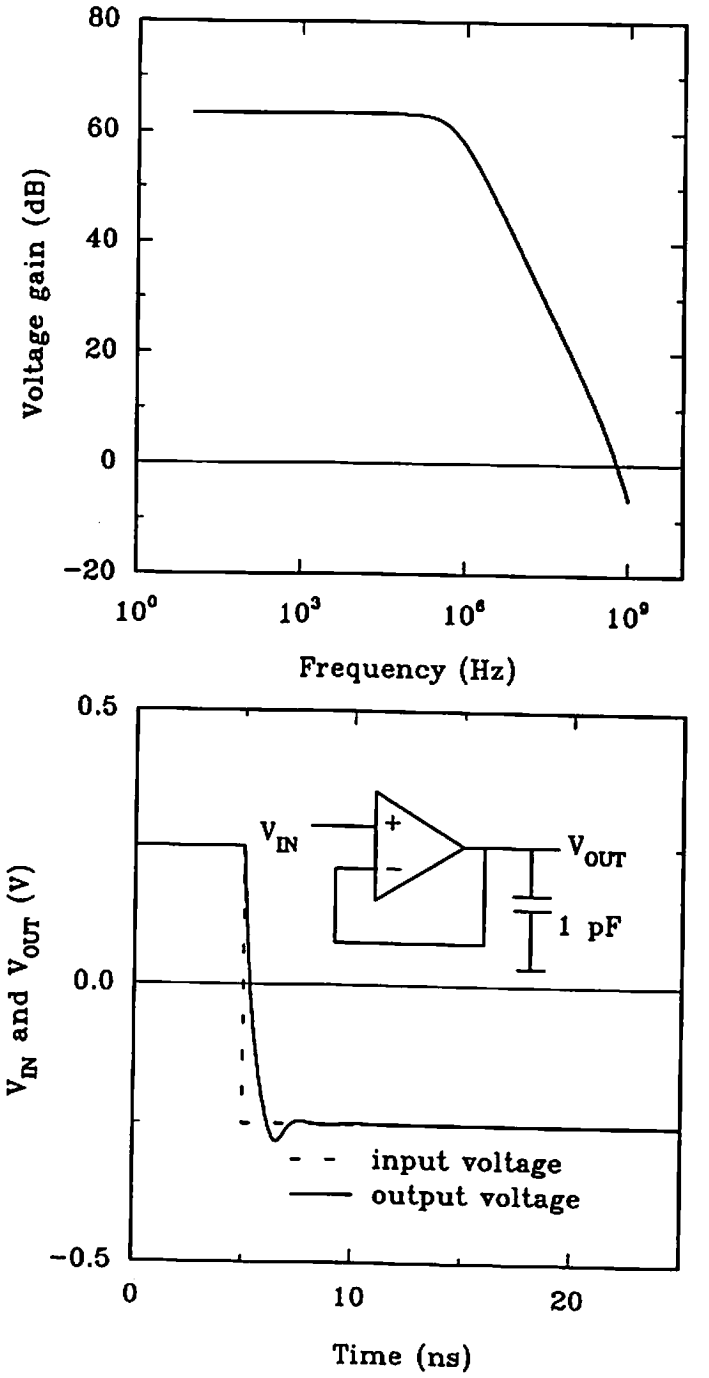


Fig. 6.19 (continued)
(b) Gain characteristics.
(c) Determination of slew rate and settling time.

Table 6.7 Transistor geometries used in the single-stage folded cascode amplifier.

Transistor	W (μm)	L (μm)
M1, M2, M20, M23, M24	100	0.5
M3, M4	112.5	0.75
M5, M6, M7,M8, M21, M22	200	0.5
M9, M10	125	0.75
M19	400	0.5

Table 6.8 Simulated performance characteristics of the single-stage folded-cascode amplifier.

Performance characteristic	Single-stage folded-cascode amplifier
Power supply	± 2.5 V
D. C. Gain	63.3 dB
Unity-gain freq. (1 pF load)	625 MHz
Systematic offset voltage	-568 μV
Output range	-0.54 V to 1.14 V
Slew rate	0.76 V/ns (1 pF load)
Settling time (0.1 %)	15.6 ns (1 pF load)
CMRR @ 1 kHz	67.4 dB

provided by transistors M20, M23, and M24. The simulated performance characteristics are listed in Table 6.8. The D.C. voltage gain, unity-gain frequency, output range, slew rate, settling time and common-mode rejection ratio were determined in the same manner as described for the two-stage operational amplifier. The gain characteristics are shown in Fig. 6.19(b) and the waveforms used to determine the slew rate and settling time are shown in Fig. 6.19(c).

6.7 Band-Gap Reference Circuit

Precision CMOS integrated circuits frequently require bias voltages that have a low sensitivity to temperature. Such circuits can be designed by assigning proper weights to voltages that have opposite temperature coefficients. Circuits using a composite of the V_{BE} of a parasitic bipolar transistor and the threshold voltage of an MOS transistor in a CMOS technology are described in [6.14]. The schematic of a circuit based on this principle is shown in Fig. 6.20(a). BSIM_plus simulation results of the circuit are shown in Fig. 6.20(b). By suitably adjusting the ratios of the resistors as well as the areas of the diodes, a null temperature coefficient is achieved at 30° C. In Fig. 6.20(a), the diodes D3 and D4 have 10 times larger areas than diodes D1 and D2.

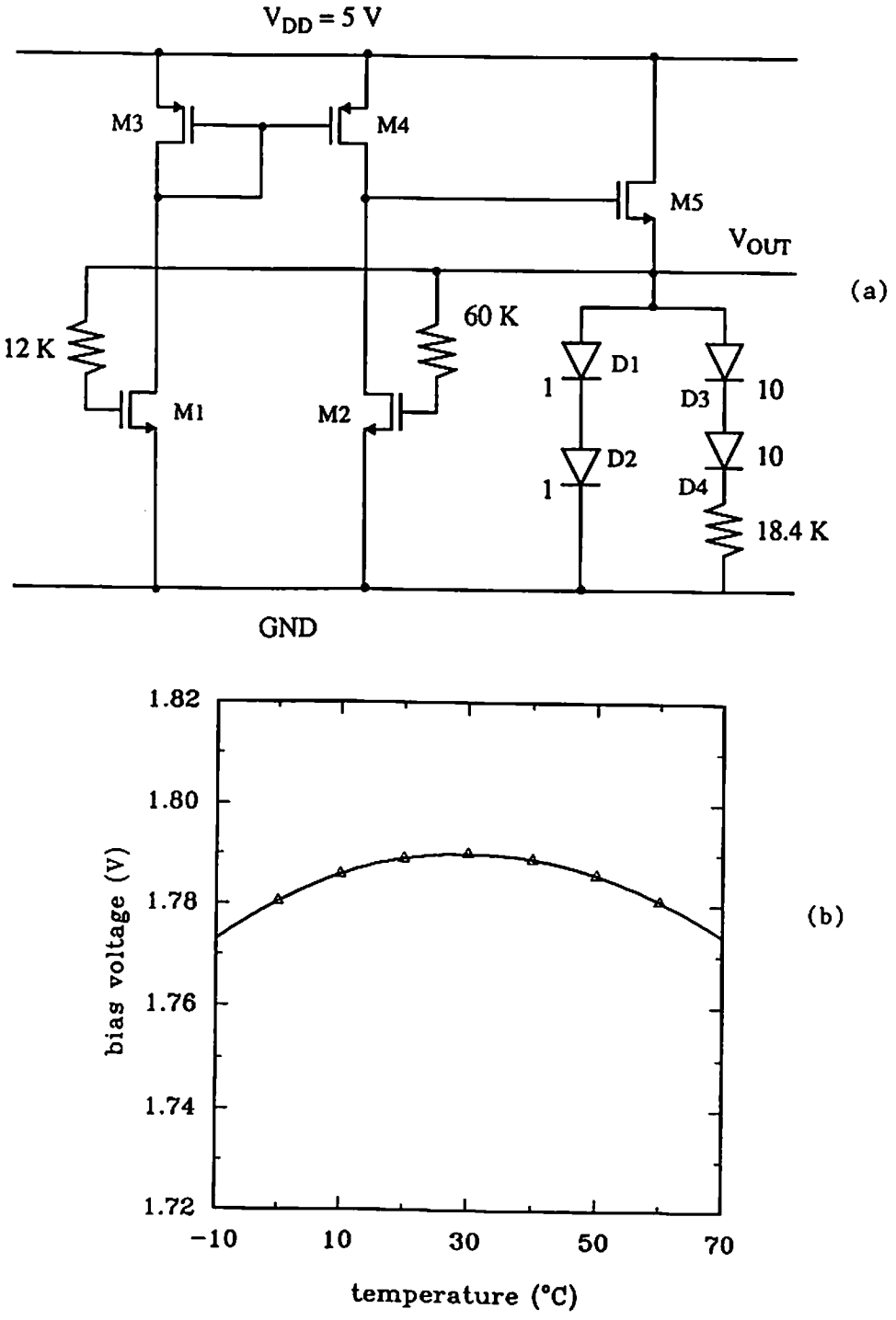


Fig. 6.20 Simulation results of a band-gap reference circuit. (a) Circuit schematic. (b) Simulated bias voltage.

6.8 Comparison of Simulation Performances

The BSIM_plus, MOS Level-2 and Level-3 models were used to simulate circuit including 31-stage ring oscillator, binary-to-octal decoder, 16-word x 1-bit DRAM, 4-bit neural A/D converter, 8-bit counter, 8-bit ripple-carry adder and 4-bit x 4-bit parallel multiplier.

A ring oscillator circuit can be constructed by taking the output signal of a chain of an odd number of inverters and feeding it back to the input. A ring oscillator circuit was constructed from a 31-stage inverter chain. The NMOS and PMOS transistors in the inverters had geometries of W/L = 20 μm/0.8 μm and 10 μm/0.8 μm, respectively. The simulated waveforms at the output nodes of the first, eleventh, and twenty-first inverters are plotted in Fig. 6.21. The ring-oscillator frequency was determined to be 227 MHz from these waveforms and the delay-per-stage of the inverter chain was calculated as 71 ps.

An asynchronous counter was designed based on 2-phase static D flip-flops [6.15]. The schematic of the individual latch is shown in Fig. 6.22(a) and the block diagram of the counter is shown in Fig. 6.22(b). The master-slave flip-flop was designed by cascading two individual latch stages and operating them on alternate clock phases. In the counter circuit, the clocking of each flip-flop was generated from the output of the previous flip-flop. The output waveforms of the counter for 4 cycles are shown in Fig. 6.22(c). The counter can cycle through 256 states.

Table 6.9 Truth table of the binary-to-octal decoder.

C	B	A	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Table 6.10 Computation times of different models in SPICE-3e1P.

Circuit	Number of transistors	Level-2 (sec)	Level-3 (sec)	BSIM_plus (sec)
31-stage ring oscillator	62	258	232	151
Binary-to-octal decoder	62	62	74	52
16 words x 1 bit DRAM	78	incorrect* results	incorrect* results	67
4-bit neural ADC	112	404	279	282
8-bit counter (1.2-μm)	128	timestep* error	62	73
8-bit counter (0.6-μm)	128	356	timestep* error	73
8-bit adder	224	incorrect* results	timestep* error	51
4 x 4 parallel multiplier	544	timestep* error	d.c. non-convergence*	635

*Note: See the explanations in Sec. 6.8.

A binary-to-octal decoder was designed using fully complementary CMOS logic gates [6.15]. The decoder reads a binary input word and indicates its value by setting one of eight output bits to zero. The gate-level schematic of the binary-to-octal decoder is given in Fig. 6.23(a). The decoder was constructed from NAND, NOR and inverter gates whose schematics are shown in Fig. 6.23(b). The truth table of the decoder is listed in Table 6.9.

An 8-bit ripple-carry-adder was designed using transistors with L = 0.5 μm. The adder was constructed by cascading eight single-bit adder cells and allowing the CARRY bit to ripple asynchronously across the array [6.15]. The functions generated by each adder cell were,

$$\overline{SUM}_{n+1} = \overline{CARRY}_{n+1} (A_{n+1} + B_{n+1} + CARRY_n) + A_{n+1} B_{n+1} CARRY_{n+1} , \quad (6.3)$$

and,

$$CARRY_{n+1} = A_{n+1} B_{n+1} + CARRY_n (A_{n+1} + B_{n+1}). \quad (6.4)$$

The circuit schematic of an individual adder cell, including the SUM and CARRY stages, is shown in Fig. 6.24(a). The cells were cascaded as shown in Fig. 6.24(b) to implement an 8-bit adder. The delay of such an adder is calculated from the sum of the carry propagation delays of each stage. The adder can be speeded up by omitting the inverter at the output of the carry gate and operating alternate stages on complement data.

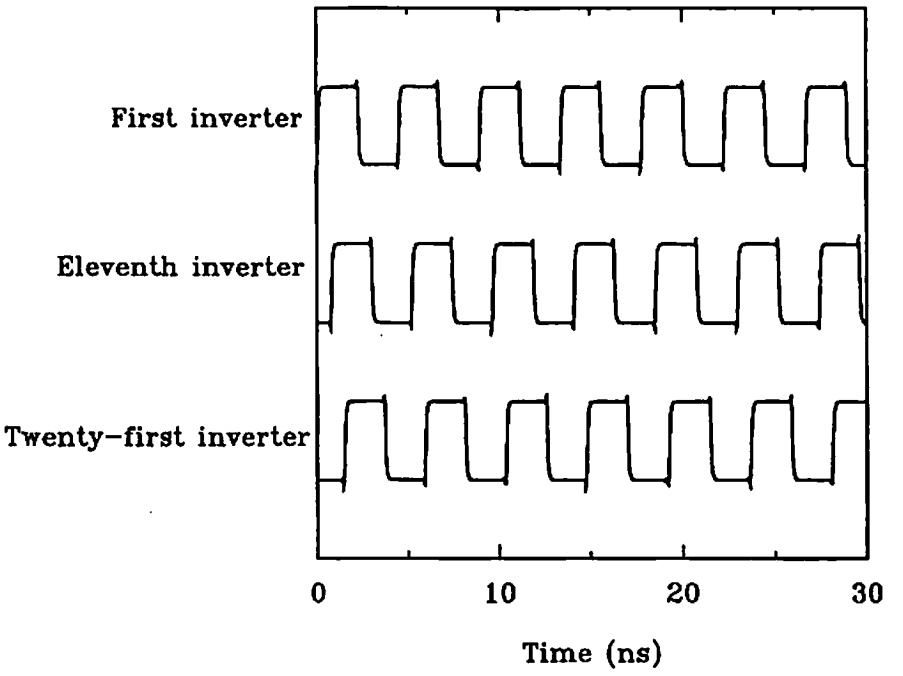


Fig. 6.21 Voltage waveforms at different stages of a 31-stage ring oscillator.

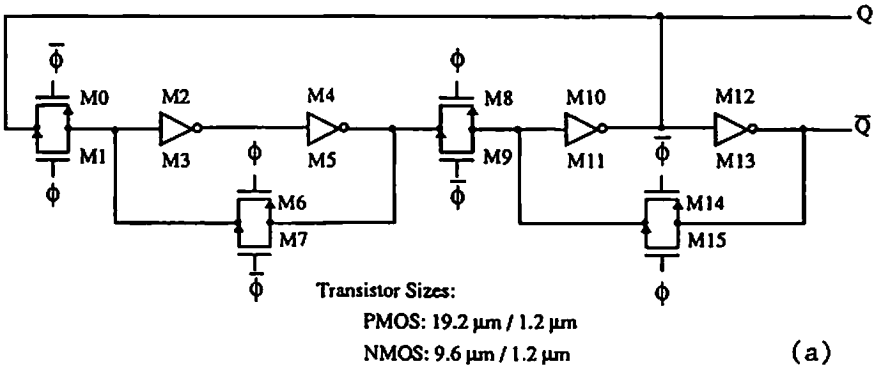
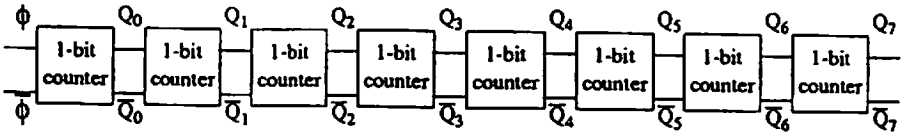
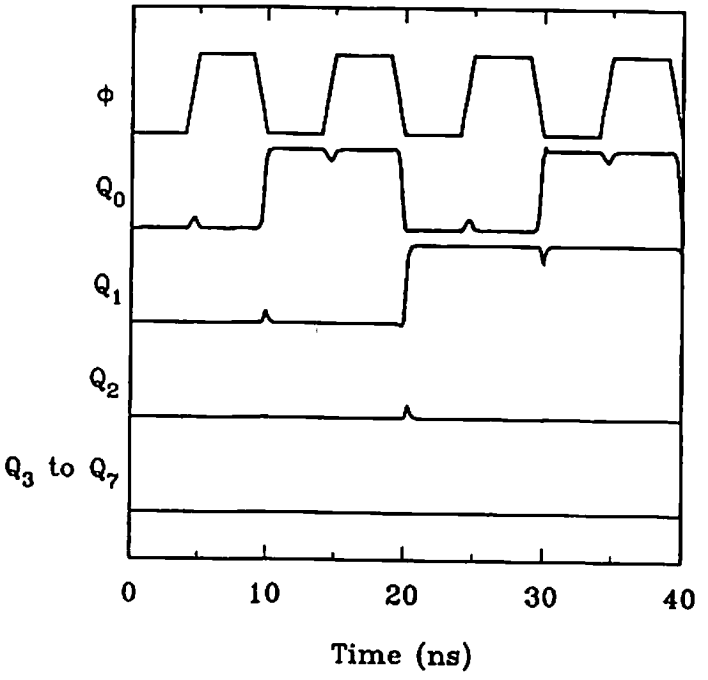


Fig. 6.22 Simulation of an 8-bit asynchronous counter. (a) Circuit schematic of the 2-phase static latch.

Figure 6.22 (continued)



(b)



(c)

Fig. 6.22 (continued)
(b) Block diagram of an 8-bit counter.
(c) Waveforms during operation of the counter.

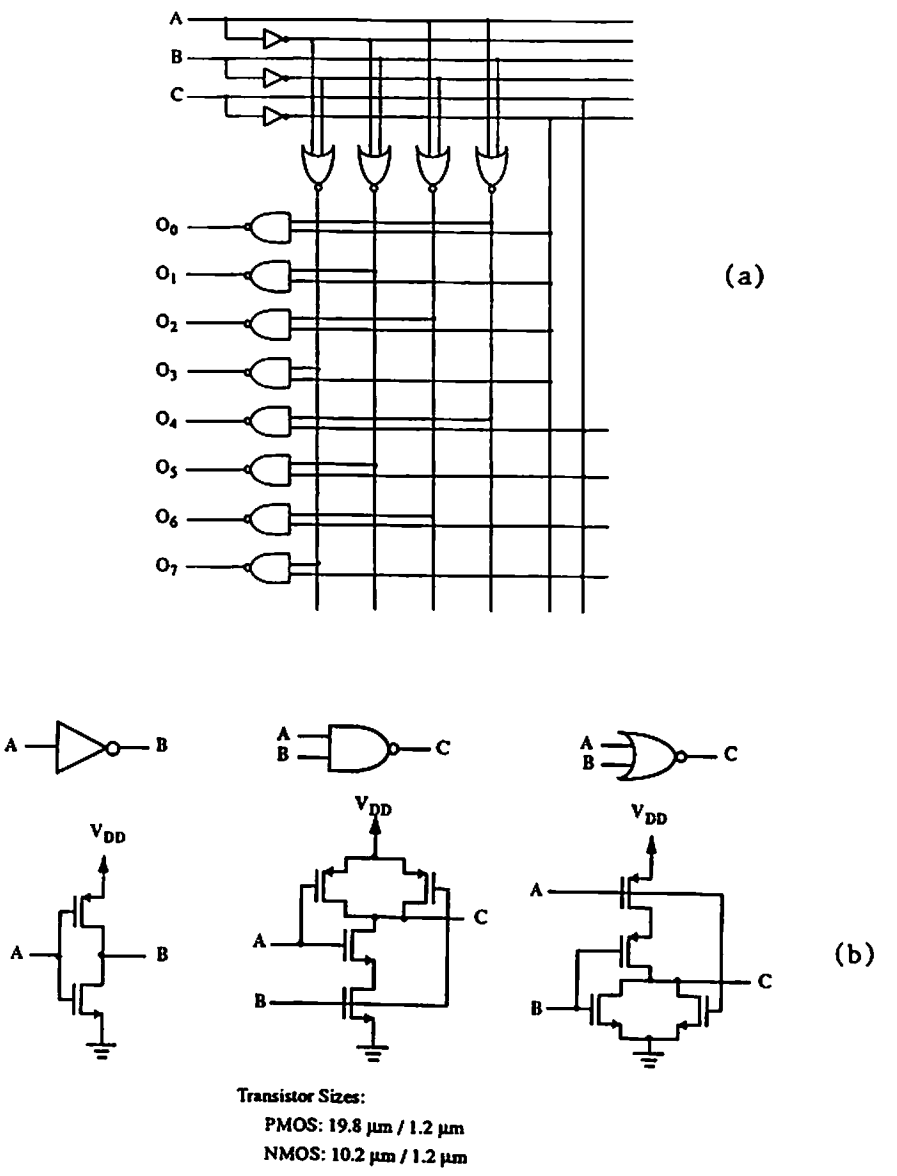
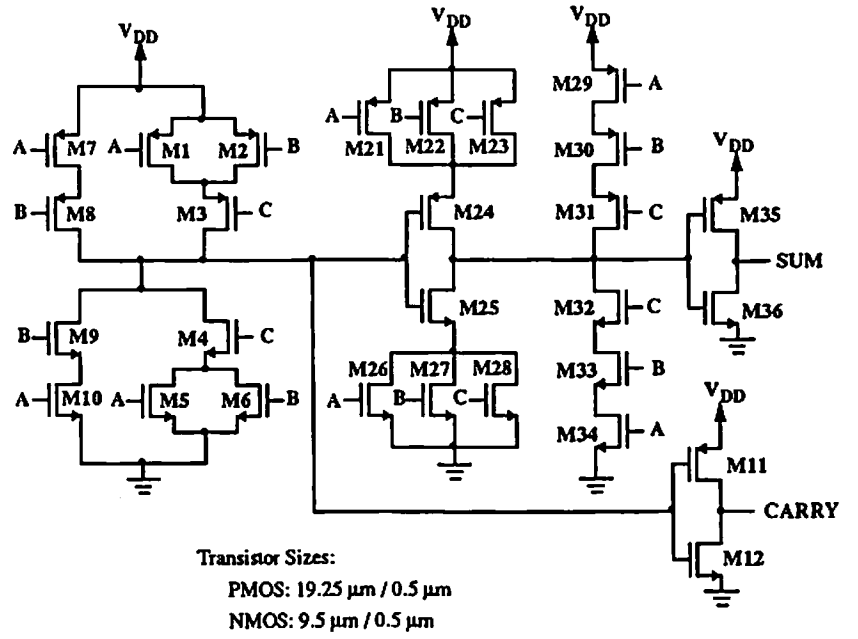
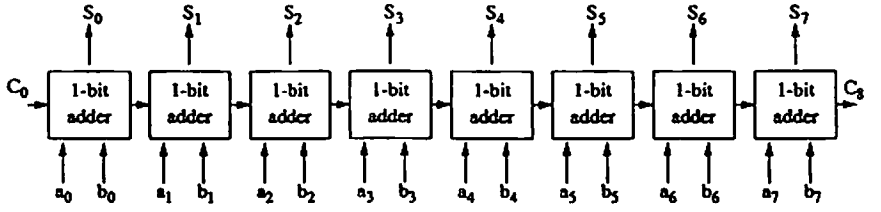


Fig. 6.23 Simulation of a binary-to-octal decoder.
(a) Gate-level schematic of the decoder.
(b) Schematics of circuit building blocks.



(a)



(b)

Fig. 6.24 Simulation of an 8-bit adder.
(a) Circuit schematic of a single-bit adder cell.
(b) Block diagram of 8-bit ripple-carry adder.

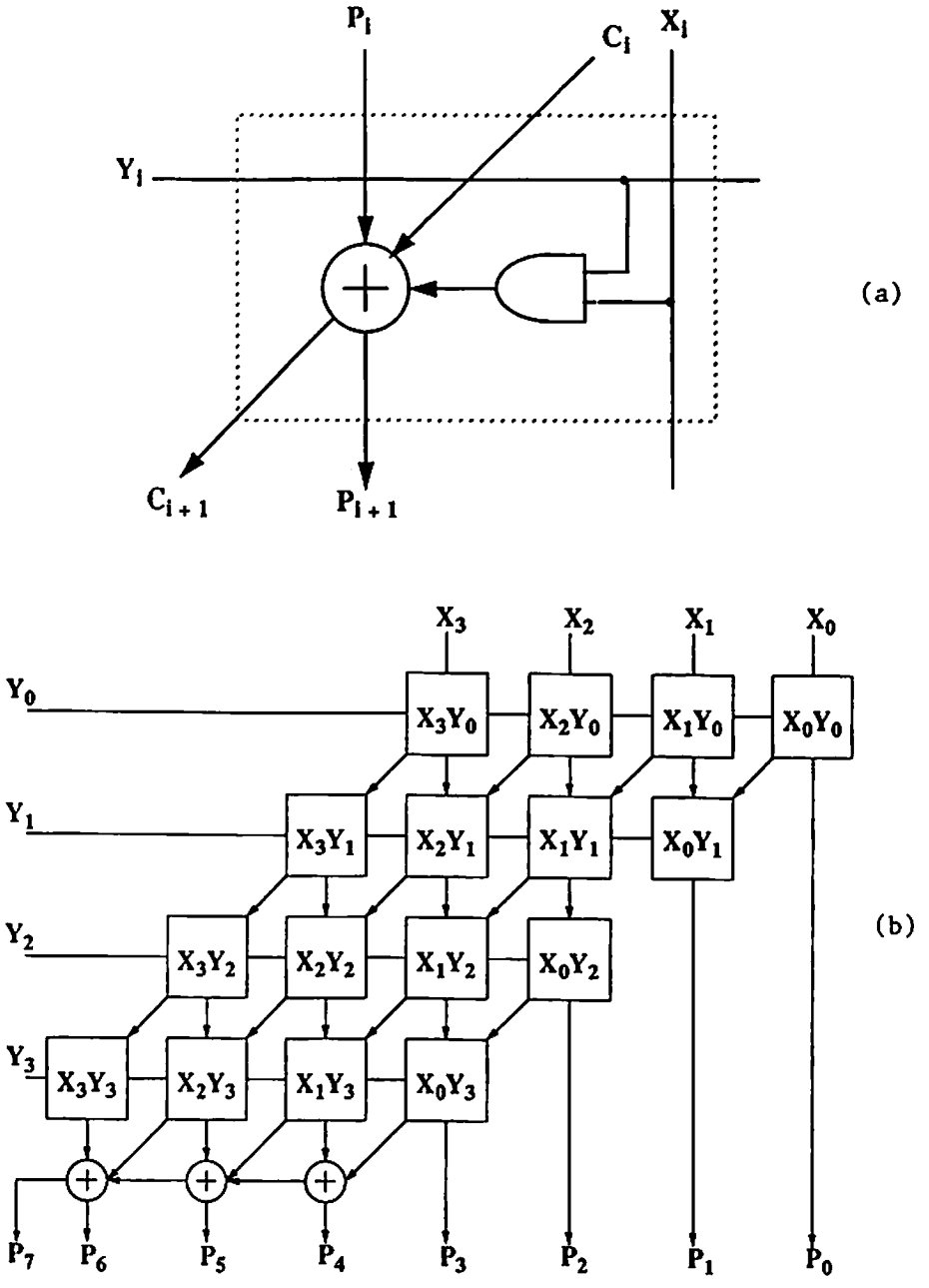


Fig. 6.25 Simulation of a 4-bit x 4-bit parallel multiplier.
(a) Individual multiplier cell.
(b) Block diagram of multiplier.

The 4-bit x 4-bit parallel multiplier can be constructed from AND gates and adder cells [6.15]. Sixteen AND gates were used to calculate the partial products of all pair-wise combinations of the input bits in parallel. Single-bit adder cells were then used for the accumulation of shifted partial-product terms. Figure 6.25(a) shows the individual multiplier cell containing the AND gate and the single-bit full-adder cell. The resulting sum and carry terms rippled across the array of multiplier cells shown in Fig. 6.25(b). The multiplier results were generated at the outputs of the adder cells on the boundary of the array. An n x n multiplier using this architecture can be constructed with n^2 AND gates, n x (n-2) full adders, and 2n - 1 half adders.

MOS Level-2 and Level-3 models were also used to simulate these circuits. The results of the simulations and how they compared with the simulations using the BSIM_plus model are described. The computation times taken for simulations of the different circuits using the BSIM_plus, Level-2, and Level-3 models are listed in Table 6.10. Simulations times using the BSIM_plus model compare favorably with those of the other two models. Convergence performance of the BSIM_plus model is better than the other two models.

In the cases of the 31-stage ring oscillator circuit and the binary-to-octal decoder circuit, the simulation results using the three models were similar. For both these circuits, the simulations using the BSIM_plus model were quicker than the simulations using the other two models.

When the 8-bit counter was simulated using the MOS Level-3 model, the simulations were unable to converge due to the transient timestep being

too small. The timestep error occurred during the transient analysis when time = 4.59 ns. The clock signal was rising from 0 V to 5 V in the first cycle of operation at this time. The design of the 8-bit counter was scaled up from a 0.6-μm to a 1.2-μm technology and simulated using Level-3 model parameters. The expected waveforms were obtained from this simulation. The 1.2-μm design of the 8-bit counter was also simulated using the Level-2 model. This simulation stopped at time = 34.57 ns in the transient analysis due to the internal timestep being too small. The clock signal was rising from 0 V to 5 V in the fourth cycle of operation when the simulation stopped.

When the 8-bit ripple-carry adder was simulated using the Level-2 model, incorrect results were obtained at time = 10 ns during the transient simulation. The fifth bit of the sum term from the LSB did not discharge to 0 V as expected but remained at 5 V. The Level-3 model simulations also gave incorrect results at time = 10.1 ns. The input B was rising from 0 V to 5 V at this time. When the design of the 8-bit adder was scaled up to 0.8-μm and 1.2-μm technologies and simulated using the Level-2 and Level-3 models, the expected results were obtained.

The 4-bit x 4-bit multiplier was also simulated using the Level-2 model. The internal timestep error occurred at time = 10.87 ns during the transient analysis. The input word was changing from 0000 to 1010 at this time. The simulations using the Level-3 model resulted in a D.C. convergence problem.

The Level-3 simulation of the DRAM circuit resulted in waveforms that were different from those expected. During the Level-2 simulation, the Write-0 step resulted in a low voltage being written onto the memory cell. However, when this value was read during the Read-0 step, a logic value of 1 was read at the output line.

References

[6.1] A. Vladimirescu, S. Liu, *The Simulation of MOS Integrated Circuits Using SPICE2*, Memo ERL-M80/7, Electronics Res. Lab., Univ. of California, Berkeley, Oct. 1980.

[6.2] B. J. Sheu, D. L. Scharfetter, P. K. Ko, M.-C. Jeng, "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE Jour. of Solid-State Circuits*, vol. 22, no. 4, pp. 558-566, Aug. 1987.

[6.3] K. Terada, H. Muta, "A new method to determine effective MOSFET channel length," *Japanese Jour. of Applied Physics*, vol. 18, no. 5, pp. 953-959, May 1979.

[6.4] J. G. J. Chern, P. Chang, R. F. Motta, N. Godinho, "A new method to determine MOSFET channel length," *IEEE Electron Device Letters*, vol. 1, no. 9, pp. 170-173, Sept. 1980.

[6.5] M.-C. Jeng, B. J. Sheu, P. K. Ko, *BSIM parameter extraction - algorithms and users guide*, Memo ERL-M85/79, Electronics Res. Lab., Univ. of California, Berkeley, Oct. 1985.

[6.6] P. Yang, B. D. Epler, P. K. Chatterjee, "An investigation of the charge conservation problem for MOSFET circuit simulation," *IEEE Jour. of Solid-State Circuits*, vol. 18, no. 1, pp. 128-138, Feb. 1983.

[6.7] J. E. Meyer, "MOS models and circuit simulation," *RCA Rev.*, vol. 32, pp. 42-63, 1971.

[6.8] M. A. Cirit, "The Meyer model revisited: why is charge not conserved?," *IEEE Trans. on Computer-Aided Design*, vol. 8, no. 10, pp. 1033-1037, Oct. 1989.

[6.9] D. E. Ward, R. W. Dutton, "A charge oriented model for MOS transistor capacitances," *IEEE Jour. of Solid-State Circuits*, vol. 13, pp. 703-707, 1978.

[6.10] G. M. Jacobs, R. W. Broderson, "A fully asynchronous digital signal processor using self-timed circuits," *IEEE Jour. of Solid-State Circuits*, vol. 25, no. 6, pp. 1526-1536, Dec. 1990.

[6.11] M. Afghahi, C. Svensson, "A unified single-phase clocking scheme for VLSI systems," *IEEE Jour. of Solid-State Circuits*, vol. 25, no. 1, pp. 225-232, Feb. 1990.

[6.12] A. J. McAuley, "Dynamic asynchronous logic for high-speed CMOS systems," *IEEE Jour. of Solid-State Circuits*, vol. 27, no. 3, pp. 382-388, Mar. 1992.

[6.13] W. C. Black, Jr., D. J. Allstot, R. A. Reed, "A high-performance low-power CMOS channel filter," *IEEE Jour. of Solid-State Circuits*, vol. 15, no. 6, pp. 929-938, Dec. 1980.

[6.14] P. R. Gray, R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd edition, John Wiley & Sons: New York, NY, 1984.

[6.15] N. Weste, K. Eshraghian, *Principles of CMOS VLSI Design*, Addison-Wesley: Reading, MA, 1985.

Chapter 7

Conclusion and Future Directions

The BSIM_plus model was developed to provide VLSI designers with an urgently needed tool to simulate high-performance circuits in sub-half-micron CMOS technologies. The key features of the model that make it very valuable in a modern design environment include,

- compact set of physics-based parameters,
- continuity of drain current and conductances in all regions of operation,
- improved threshold voltage and mobility expressions,
- better output conductance modeling in the saturation region,
- parasitic source/drain resistances with inverse-width scaling,
- single parameter set over all geometries using pseudo-boundary method,
- charge-conserving capacitance model,
- temperature dependent threshold voltage and carrier mobility,
- thermal and flicker noise effects, and
- built-in substrate current expression.

These features have resulted in many important properties of the BSIM_plus model which are summarized in Table 7.1.

Table 7.1 Important features of the BSIM_plus model.

MOS Model	BSIM2 (BSIM3)	BSIM_plus
Organization	U.C. Berkeley	University of Southern California
Number of drain-current parameters	104 (20-25)	21
Variation of threshold voltage with substrate voltage	Possibly non-monotonic at high V_{BS}	Monotonic
Vertical field effect on carrier mobility	Due to gate voltage & substrate voltage	Due to gate voltage & substrate voltage
Conductance prediction accuracy for submicron technologies	Moderate (Good)	Good
Temperature/noise effects	External	Built-in
Charge/capacitance model	Conservation	Conservation
Small-geometry effects	Globally fixed format	Locally adapted format
Applicability of parameter set over a large geometric design space	Limited by abnormal second-order effects	Extended by the Pseudo-Boundary method
Parameter extraction	Local optimization	Combined local optimization with SUXES
Circuit type	Digital VLSI	Analog LSI Digital VLSI
Applicable technology	Submicron	Sub-half-micron

The use of a compact set of 21 physics-based parameters for the drain current expressions greatly reduces the complexity of the parameter extraction procedure and facilitates linking with device/process simulators. The threshold voltage expression in BSIM_plus includes terms for the flat-band voltage, surface-inversion potential, non-uniform substrate doping effect, narrow width effects, and drain-induced barrier lowering effect. The mobility expression includes the effect of lateral and normal electric fields in the channel. The contribution of the normal electric field is modeled as a function of the gate and substrate voltages, while the contribution of the lateral electric field is modeled by the critical electric field for velocity saturation. An exponential term is included in the drain current expression to improve the output conductance matching in the transition from the triode to saturation regions of operation, and provide more accurate output conductance prediction in the saturation region. The weak-inversion drain current is dominated by the diffusion current, which is an exponential function of the gate voltage. The diffusion component is clamped in the strong-inversion region. The drain current in all regions of operation is expressed as the sum of strong- and weak-inversion components. The BSIM_plus model also includes the effect of temperature variations on circuit performance. Noise analysis of circuits includes thermal noise due to source/drain and transistor channel conductance, as well as flicker noise. A built-in substrate current expression facilitates linking the circuit simulator with reliability simulators in order to predict circuit performance degradation due to hot-carrier effects. The pseudo-boundary

method extends the use of a single parameter set over the entire geometric space.

The BSIM_plus model was implemented in the SPICE-3e1 circuit simulation program and the SUXES parameter extraction program in order to provide the capability to characterize new technologies and simulate circuits to be designed in these technologies. Parameter sets were extracted from different industrial sub-half-micron technologies from Samsung Electronics Co. and TRW Inc. Comparison of measured and simulated data from these technologies demonstrated the accuracy of the BSIM_plus drain current and output conductance expressions. Simulations of several circuit examples including self-timed adder circuit, clocked and asynchronous master-slave latches, DRAM circuit, two-stage and single-stage amplifiers, band-gap reference circuit, 31-stage ring oscillator, binary-to-octal decoder, 4-bit neural A/D converter, 8-bit counter, 8-bit ripple carry adder, and 4-bit x 4-bit parallel multiplier were done to observe the performance of the circuit simulator and the new model. Selected circuits among these were also simulated using the MOS Level-2 and Level-3 models to demonstrate the improved circuit simulation convergence properties of the BSIM_plus model. An experiment to demonstrate the charge conservation property of the BSIM_plus model was also described.

As fabrication technologies evolve, so must the tools available to circuit designers, in order to exploit advanced features of new technologies. This research is an important part of this evolution. While trying to address the challenges of circuit simulation today, we also strive to provide researchers

with a platform upon which to continue to address the new problems of upcoming generations of microelectronic circuits and systems.

The BSIM_plus model serves as the cornerstone of an integrated simulation environment which includes capabilities of statistical yield prediction, circuit reliability simulation, and macromodel/behavioral simulation. The prediction of yield in fabrication technologies is greatly facilitated by using the model with a compact set of physics-based parameters. Statistical distributions of circuit performance can be obtained by using different parameter sets which are generated by the introduction of stochastic variations or by results from process/device simulators.

The reliability of sub-half-micron VLSI circuits is of great concern to manufacturers of advanced electronic systems. Important degradation mechanisms include the high-field-induced hot-carrier generation, electromigration, time-dependent dielectric breakdown, and radiation damages. The BSIM_plus model is well suited for the analysis of circuit waveforms that can be used to predict the change in circuit behavior with time-of-operation. The BSIM_plus model can be used with reliability simulation programs including BERT, iSMILE, and RELY. In addition to reliability simulation, the BSIM_plus model can also be used in fault simulation for analog ICs.

Variations in fabrication processes can be correlated with changes in circuit performance by linking the process/device simulators with circuit simulators. Such statistical correlations are useful in the development of macromodels for sub-system level simulations. Mixed signal circuits with analog and digital portions also pose many challenges to VLSI designers. Simulation

tools for mixed-signal circuits can use state-space models or analytic expressions to model the interaction between the analog and digital signal domains. These tools must also account for substrate-induced noise in such circuits. The development of properly parameterized behavioral models is also essential in order to perform sub-system level simulations. Micropower and low-voltage circuits operating at 3.3 V are important for the realization of high-speed computing and signal processing circuits for portable electronic machines. Optical interconnection systems and optoelectronic interface circuits will contribute significantly to improving communication among VLSI chips and microelectronic systems.

Appendix A

User's Guide for Modified Program SPICE-3e1P

****

This User's Guide is to be used as a supplement to the original "SPICE3 Version 3e1 User's Manual" [1]. It is intended for SPICE users who have access to the modified program SPICE-3e1P with the BSIM_plus MOS transistor model. It contains the additional features supported by the BSIM_plus model and should be used together with the original User's Manual for completeness.

****

The "level=41" parameter is used to call the BSIM_plus model. The following parameters describe the BSIM_plus model:

name	parameter	units	default
level	model index	-	41
phis	surface inversion potential	V	0.7
vfb	flat-band voltage	V	-0.875
gamma1	zero-bias body-effect coeff.	$\sqrt{V}$	0.8
gamma2	high-bias body-effect coeff.	$\sqrt{V}$	0.06

ks	depletion charge-sharing coeff.	-	1.1
knz	narrow-width threshold voltage coeff.	Vμm	0.2
knb	narrow-width thresh. volt. substrate coeff.	μm	0.04
etaz	drain-induced barrier lowering coeff	-	0.02
etal	short-channel barrier-lowering coeff	μm	0.01
mu0	intrinsic surface mobility	cm^2/Vs	450
dl	channel-length reduction	μm	0.1
dw	channel-width reduction	μm	0.1
ugsz	gate-voltage mobility degradation coeff.	V^{-1}	0.02
ugsl	short-channel adjustment of ugsz	V^{-1}μm	0.01
ubs	substrate-volt. mobility degradation coeff.	V^{-1}	0.02
ecrit	critical electric field for velocity saturation	V/μm	5
h0	output conductance modulation prefactor	-	0.05
h1	output conductance modulation exponent	V	2
tox	gate-oxide thickness	nm	25
i0	subthreshold drain current coeff.	A	1e-7
n	subthreshold drain current slope	-	1.5
pb	bulk junction potential	V	0.8
cgso	gate-source overlap cap.	F/m	0.0
cgdo	gate-drain overlap cap.	F/m	0.0
cgbo	gate-bulk overlap cap.	F/m	0.0
cj	zero-bias bulk junction bottom cap.	F/m^2	0.0
mj	bulk junction bottom grading coeff.	-	0.5
cjsw	zero-bias bulk junction sidewall cap.	F/m	0.0

mjsw	bulk junction sidewall grading coeff.	-	0.33
tnom	parameter measurement temperature	°C	27
bvth	threshold-voltage temp. coeff.	V/°C	0.0
bmu0	mobility temp. coeff.	-	1.5
bvs	saturation velocity temp. coeff.	-	0.0
kf	flicker noise coefficient	-	0.0
af	flicker noise exponent	-	1.0

References

[1] B. Johnson, T. Quarles, A. R. Newton, D. O. Pederson, A. Sangiovanni-Vincentelli, *SPICE-3E1 User's Guide*, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, Apr. 1991.

Appendix B

User's Guide for Modified SUXES Program

****

This User's Guide is to be used as a supplement to the original "SUXES User's Manual" [1]. It is intended for SUXES users who have access to the modified SUXES program with the BSIM_plus MOS transistor model. It contains the input files that are required to extract BSIM_plus parameters and should be used together with the original User's Manual for completeness.

****

B.1 Initial Estimates File

Parameters	Initial	Lowbound	Upperbound
Vfbi	-0.875	-0.9	-0.8
Phii	0.7	0.6	0.8
xGamma1i	0.8	0.7	0.9
xGamma2i	0.06	0.05	0.07
xKsi	1.1	1.0	1.2
xKnzi	0.2	0.15	0.25

xKnbi	0.04	0.03	0.05
Etazi	0.02	0.01	0.03
Etali	0.01	0.005	0.015
xMuoi	450	425	475
Toxi	25	25	25
Ugszi	0.02	0.01	0.03
Ugsli	0.01	0.005	0.015
Ubsi	0.02	0.01	0.03
Ecriti	5	3	4
Dli	0.1	0.08	0.12
Dwi	0.1	0.08	0.12
Type	1.00000	1.00000	1.00000
H0i	0.05	0.0	0.1
H1i	2	1.8	2.2
Ni	1.5	1.4	1.6
I0i	1.0E-7	1.5E-7	0.5E-7

B.2 Options File

```
*    This is an options file for
*    CMOS N-Channel transistors.
*    date 10-25-92
*
   Criteria
```

```
    Nsign=3 Maxfn=200 Delta=1.0d-9 Epsil=1.d-6
    Linit=0.1 Lscal=2.0 Luppr=1000 Fcdsw=0.1
*
    RangVD     min=0       max=5.0    incr=0
*
    RangVG     min=0       max=5.0    incr=0
*
    RangVB     min=-5.0    max=0.0    incr=0
*
     Weight
*
```

B.3 Strategy File

Parameters	First	Second	Third
Vfb	1	0	0
Phi	1	0	0
Xgamma1	0	0	1
Xgamma2	0	0	1
Xks	0	0	1
Xknz	0	0	1
Xknb	0	0	1
Etaz	0	0	1
Etal	0	0	1

Xmuo	1	0	0
Tox	0	0	0
Ugsz	1	1	0
Ugsl	1	1	0
Ubs	0	1	0
Ecrit	1	1	0
Dl	0	1	0
Dw	0	1	0
Type	0	0	0
H0i	1	1	0
H1i	0	1	0
Xn	0	0	0
Xi0	0	0	0

References

[1] K. Doganis, R.W. Dutton, *SUXES-Stanford University Extractor of Model Parameters (User's Manual)*, Tech. Report, Stanford Electronics Lab., Stanford University, Nov. 1982.

Appendix C

SPICE Input Decks

C.1 Eight-Bit Counter

```
Eight-bit counter
*
* single bit counter
*
.subckt 1b_cou 2 3 4 5 1
* 2 = clock, 3 = clock_bar,
* 4 = input, 5 = output, 1 = vdd
m0 4 3 6 1 pfet w=9.6u l=0.6u
m1 4 2 6 0 nfet w=4.8u l=0.6u
m2 7 6 1 1 pfet w=9.6u l=0.6u
m3 7 6 0 0 nfet w=4.8u l=0.6u
m4 8 7 1 1 pfet w=9.6u l=0.6u
m5 8 7 0 0 nfet w=4.8u l=0.6u
m6 6 2 8 1 pfet w=9.6u l=0.6u
m7 6 3 8 0 nfet w=4.8u l=0.6u
m8 8 2 9 1 pfet w=9.6u l=0.6u
m9 8 3 9 0 nfet w=4.8u l=0.6u
m10 4 9 1 1 pfet w=9.6u l=0.6u
m11 4 9 0 0 nfet w=4.8u l=0.6u
m12 5 4 1 1 pfet w=9.6u l=0.6u
m13 5 4 0 0 nfet w=4.8u l=0.6u
m14 9 3 5 1 pfet w=9.6u l=0.6u
m15 9 2 5 0 nfet w=4.8u l=0.6u
.ends 1b_cou
*
* counter circuit
*
x0  2  3  4  5 1 1b_cou
x1  4  5  6  7 1 1b_cou
x2  6  7  8  9 1 1b_cou
x3  8  9 10 11 1 1b_cou
x4 10 11 12 13 1 1b_cou
x5 12 13 14 15 1 1b_cou
x6 14 15 16 17 1 1b_cou
x7 16 17 18 19 1 1b_cou
*
* Independent sources
*
* power supply
vdd 1 0 dc 5
```

```
* clock
vphi 2 0 dc 0 pulse(0 5 4ns 1ns 1ns 4ns 10ns)
* clock_bar
vphibar 3 0 dc 5 pulse(5 0 4ns 1ns 1ns 4ns 10ns)
*
* analysis
*
.ic v(0:6)=5 v(1:6)=5 v(2:6)=5 v(3:6)=5
+ v(4:6)=5 v(5:6)=5 v(6:6)=5 v(7:6)=5
.tran 0.5ns 40ns
.end
```

C.2 Static Four-Bit Adder

```
Four-bit Adder
*
* adder cell 1
*
m1  11 51  1 1 pfet w=19.2u l=0.5u as=69p ad=57.6p ps=7.2u pd=25.2u
m2  11 52  1 1 pfet w=19.2u l=0.5u as=69p ad=57.6p ps=7.2u pd=25.2u
m3  41 53 11 1 pfet w=19.2u l=0.5u as=57.6p ad=57.6p ps=25.2u pd=25.2u
m4  41 53 12 0 nfet w=9.6u  l=0.5u as=28.8p ad=28.8p ps=15.6u pd=15.6u
m5  12 51  0 0 nfet w=9.6u  l=0.5u as=34.6p ad=28.8p ps=7.2u pd=15.6u
m6  12 52  0 0 nfet w=9.6u  l=0.5u as=34.6p ad=28.8p ps=7.2u pd=15.6u
m7  13 52  1 1 pfet w=19.2u l=0.5u as=57.6p ad=23p ps=25.2u pd=2.4u
m8  41 51 13 1 pfet w=19.2u l=0.5u as=23p ad=57.6p ps=2.4u pd=25.2u
m9  41 51 14 0 nfet w=9.6u  l=0.5u as=10.5p ad=28.8p ps=2.4u pd=15.6u
m10 14 52  0 0 nfet w=9.6u  l=0.5u as=28.8p ad=10.5p ps=15.6u pd=2.4u
m11 153 41 1 1 pfet w=19.2u l=0.5u as=92.2p ad=80.6p ps=9.6u pd=27.6u
m12 153 41 0 0 nfet w=9.6u  l=0.5u as=46.1p ad=40.3p ps=9.6u pd=18u
m21 21 51  1 1 pfet w=19.2u l=0.5u as=57.6p ad=69p ps=25.2u pd=7.2u
m22 21 52  1 1 pfet w=19.2u l=0.5u as=69p ad=69p ps=7.2u pd=7.2u
m23 21 53  1 1 pfet w=19.2u l=0.5u as=69p ad=57.6p ps=7.2u pd=25.2u
m24 63 41 21 1 pfet w=19.2u l=0.5u as=57.6p ad=57.6p ps=25.2u pd=25.2u
m25 63 41 22 0 nfet w=9.6u  l=0.5u as=28.8p ad=28.8p ps=15.6u pd=15.6u
m26 22 51  0 0 nfet w=9.6u  l=0.5u as=28.8p ad=34.6p ps=15.6u pd=7.2u
m27 22 52  0 0 nfet w=9.6u  l=0.5u as=34.6p ad=34.6p ps=7.2u pd=7.2u
m28 22 53  0 0 nfet w=9.6u  l=0.5u as=34.6p ad=28.8p ps=7.2u pd=15.6u
m29 23 51  1 1 pfet w=19.2u l=0.5u as=57.6p ad=23p ps=25.2u pd=2.4u
m30 24 52 23 1 pfet w=19.2u l=0.5u as=23p ad=23p ps=2.4u pd=2.4u
m31 63 53 24 1 pfet w=19.2u l=0.5u as=23p ad=57.6p ps=2.4u pd=25.2u
m32 63 53 25 0 nfet w=9.6u  l=0.5u as=10.5p ad=28.8p ps=2.4u pd=15.6u
m33 25 52 26 0 nfet w=9.6u  l=0.5u as=10.5p ad=10.5p ps=2.4u pd=2.4u
m34 26 51 0  0 nfet w=9.6u  l=0.5u as=28.8p ad=10.5p ps=15.6u pd=2.4u
m35 64 63 1  1 pfet w=19.2u l=0.5u as=92.2p ad=80.6p ps=9.6u pd=27.6u
m36 64 63 0  0 nfet w=9.6u  l=0.5u as=46.1p ad=40.3p ps=9.6u pd=18u
* adder cell 2
```

```
m101 111 151 1   1 pfet w=19.2u l=0.5u as=69p ad=57.6p ps=7.2u pd=25.2u
m102 111 152 1   1 pfet w=19.2u l=0.5u as=69p ad=57.6p ps=7.2u pd=25.2u
m103 141 153 111 1 pfet w=19.2u l=0.5u as=57.6p ad=57.6p ps=25.2u pd=25.2u
m104 141 153 112 0 nfet w=9.6u  l=0.5u as=28.8p ad=28.8p ps=15.6u pd=15.6u
m105 112 151 0   0 nfet w=9.6u  l=0.5u as=34.6p ad=28.8p ps=7.2u pd=15.6u
m106 112 152 0   0 nfet w=9.6u  l=0.5u as=34.6p ad=28.8p ps=7.2u pd=15.6u
m107 113 152 1   1 pfet w=19.2u l=0.5u as=57.6p ad=23p ps=25.2u pd=2.4u
m108 141 151 113 1 pfet w=19.2u l=0.5u as=23p ad=57.6p ps=2.4u pd=25.2u
m109 141 151 114 0 nfet w=9.6u  l=0.5u as=10.5p ad=28.8p ps=2.4u pd=15.6u
m110 114 152 0   0 nfet w=9.6u  l=0.5u as=28.8p ad=10.5p ps=15.6u pd=2.4u
m111 253 141 1   1 pfet w=19.2u l=0.5u as=92.2p ad=80.6p ps=9.6u pd=27.6u
m112 253 141 0   0 nfet w=9.6u  l=0.5u as=46.1p ad=40.3p ps=9.6u pd=18u
m121 121 151 1   1 pfet w=19.2u l=0.5u as=57.6p ad=69p ps=25.2u pd=7.2u
m122 121 152 1   1 pfet w=19.2u l=0.5u as=69p ad=69p ps=7.2u pd=7.2u
m123 121 153 1   1 pfet w=19.2u l=0.5u as=69p ad=57.6p ps=7.2u pd=25.2u
m124 163 141 121 1 pfet w=19.2u l=0.5u as=57.6p ad=57.6p ps=25.2u pd=25.2u
m125 163 141 122 0 nfet w=9.6u  l=0.5u as=28.8p ad=28.8p ps=15.6u pd=15.6u
m126 122 151 0   0 nfet w=9.6u  l=0.5u as=28.8p ad=34.6p ps=15.6u pd=7.2u
m127 122 152 0   0 nfet w=9.6u  l=0.5u as=34.6p ad=34.6p ps=7.2u pd=7.2u
m128 122 153 0   0 nfet w=9.6u  l=0.5u as=34.6p ad=28.8p ps=7.2u pd=15.6u
m129 123 151 1   1 pfet w=19.2u l=0.5u as=57.6p ad=23p ps=25.2u pd=2.4u
m130 124 152 123 1 pfet w=19.2u l=0.5u as=23p ad=23p ps=2.4u pd=2.4u
m131 163 153 124 1 pfet w=19.2u l=0.5u as=23p ad=57.6p ps=2.4u pd=25.2u
m132 163 153 125 0 nfet w=9.6u  l=0.5u as=10.5p ad=28.8p ps=2.4u pd=15.6u
m133 125 152 126 0 nfet w=9.6u  l=0.5u as=10.5p ad=10.5p ps=2.4u pd=2.4u
m134 126 151 0   0 nfet w=9.6u  l=0.5u as=28.8p ad=10.5p ps=15.6u pd=2.4u
m135 164 163 1   1 pfet w=19.2u l=0.5u as=92.2p ad=80.6p ps=9.6u pd=27.6u
m136 164 163 0   0 nfet w=9.6u  l=0.5u as=46.1p ad=40.3p ps=9.6u pd=18u
* adder cell 3
m201 211 251 1   1 pfet w=19.2u l=0.5u as=69p ad=57.6p ps=7.2u pd=25.2u
m202 211 252 1   1 pfet w=19.2u l=0.5u as=69p ad=57.6p ps=7.2u pd=25.2u
m203 241 253 211 1 pfet w=19.2u l=0.5u as=57.6p ad=57.6p ps=25.2u pd=25.2u
m204 241 253 212 0 nfet w=9.6u  l=0.5u as=28.8p ad=28.8p ps=15.6u pd=15.6u
m205 212 251 0   0 nfet w=9.6u  l=0.5u as=34.6p ad=28.8p ps=7.2u pd=15.6u
m206 212 252 0   0 nfet w=9.6u  l=0.5u as=34.6p ad=28.8p ps=7.2u pd=15.6u
m207 213 252 1   1 pfet w=19.2u l=0.5u as=57.6p ad=23p ps=25.2u pd=2.4u
m208 241 251 213 1 pfet w=19.2u l=0.5u as=23p ad=57.6p ps=2.4u pd=25.2u
m209 241 251 214 0 nfet w=9.6u  l=0.5u as=10.5p ad=28.8p ps=2.4u pd=15.6u
m210 214 252 0   0 nfet w=9.6u  l=0.5u as=28.8p ad=10.5p ps=15.6u pd=2.4u
m211 353 241 1   1 pfet w=19.2u l=0.5u as=92.2p ad=80.6p ps=9.6u pd=27.6u
m212 353 241 0   0 nfet w=9.6u  l=0.5u as=46.1p ad=40.3p ps=9.6u pd=18u
m221 221 251 1   1 pfet w=19.2u l=0.5u as=57.6p ad=69p ps=25.2u pd=7.2u
m222 221 252 1   1 pfet w=19.2u l=0.5u as=69p ad=69p ps=7.2u pd=7.2u
m223 221 253 1   1 pfet w=19.2u l=0.5u as=69p ad=57.6p ps=7.2u pd=25.2u
m224 263 241 221 1 pfet w=19.2u l=0.5u as=57.6p ad=57.6p ps=25.2u pd=25.2u
m225 263 241 222 0 nfet w=9.6u  l=0.5u as=28.8p ad=28.8p ps=15.6u pd=15.6u
m226 222 251 0   0 nfet w=9.6u  l=0.5u as=28.8p ad=34.6p ps=15.6u pd=7.2u
m227 222 252 0   0 nfet w=9.6u  l=0.5u as=34.6p ad=34.6p ps=7.2u pd=7.2u
```

```
m228 222 253 0   0 nfet w=9.6u  l=0.5u as=34.6p ad=28.8p ps=7.2u pd=15.6u
m229 223 251 1   1 pfet w=19.2u l=0.5u as=57.6p ad=23p ps=25.2u pd=2.4u
m230 224 252 223 1 pfet w=19.2u l=0.5u as=23p ad=23p ps=2.4u pd=2.4u
m231 263 253 224 1 pfet w=19.2u l=0.5u as=23p ad=57.6p ps=2.4u pd=25.2u
m232 263 253 225 0 nfet w=9.6u  l=0.5u as=10.5p ad=28.8p ps=2.4u pd=15.6u
m233 225 252 226 0 nfet w=9.6u  l=0.5u as=10.5p ad=10.5p ps=2.4u pd=2.4u
m234 226 251 0   0 nfet w=9.6u  l=0.5u as=28.8p ad=10.5p ps=15.6u pd=2.4u
m235 264 263 1   1 pfet w=19.2u l=0.5u as=92.2p ad=80.6p ps=9.6u pd=27.6u
m236 264 263 0   0 nfet w=9.6u  l=0.5u as=46.1p ad=40.3p ps=9.6u pd=18u
* adder cell 4
m301 311 351 1   1 pfet w=19.2u l=0.5u as=69p ad=57.6p ps=7.2u pd=25.2u
m302 311 352 1   1 pfet w=19.2u l=0.5u as=69p ad=57.6p ps=7.2u pd=25.2u
m303 341 353 311 1 pfet w=19.2u l=0.5u as=57.6p ad=57.6p ps=25.2u pd=25.2u
m304 341 353 312 0 nfet w=9.6u  l=0.5u as=28.8p ad=28.8p ps=15.6u pd=15.6u
m305 312 351 0   0 nfet w=9.6u  l=0.5u as=34.6p ad=28.8p ps=7.2u pd=15.6u
m306 312 352 0   0 nfet w=9.6u  l=0.5u as=34.6p ad=28.8p ps=7.2u pd=15.6u
m307 313 352 1   1 pfet w=19.2u l=0.5u as=57.6p ad=23p ps=25.2u pd=2.4u
m308 341 351 313 1 pfet w=19.2u l=0.5u as=23p ad=57.6p ps=2.4u pd=25.2u
m309 341 351 314 0 nfet w=9.6u  l=0.5u as=10.5p ad=28.8p ps=2.4u pd=15.6u
m310 314 352 0   0 nfet w=9.6u  l=0.5u as=28.8p ad=10.5p ps=15.6u pd=2.4u
m311 453 341 1   1 pfet w=19.2u l=0.5u as=92.2p ad=80.6p ps=9.6u pd=27.6u
m312 453 341 0   0 nfet w=9.6u  l=0.5u as=46.1p ad=40.3p ps=9.6u pd=18u
m321 321 351 1   1 pfet w=19.2u l=0.5u as=57.6p ad=69p ps=25.2u pd=7.2u
m322 321 352 1   1 pfet w=19.2u l=0.5u as=69p ad=69p ps=7.2u pd=7.2u
m323 321 353 1   1 pfet w=19.2u l=0.5u as=69p ad=57.6p ps=7.2u pd=25.2u
m324 363 341 321 1 pfet w=19.2u l=0.5u as=57.6p ad=57.6p ps=25.2u pd=25.2u
m325 363 341 322 0 nfet w=9.6u  l=0.5u as=28.8p ad=28.8p ps=15.6u pd=15.6u
m326 322 351 0   0 nfet w=9.6u  l=0.5u as=28.8p ad=34.6p ps=15.6u pd=7.2u
m327 322 352 0   0 nfet w=9.6u  l=0.5u as=34.6p ad=34.6p ps=7.2u pd=7.2u
m328 322 353 0   0 nfet w=9.6u  l=0.5u as=34.6p ad=28.8p ps=7.2u pd=15.6u
m329 323 351 1   1 pfet w=19.2u l=0.5u as=57.6p ad=23p ps=25.2u pd=2.4u
m330 324 352 323 1 pfet w=19.2u l=0.5u as=23p ad=23p ps=2.4u pd=2.4u
m331 363 353 324 1 pfet w=19.2u l=0.5u as=23p ad=57.6p ps=2.4u pd=25.2u
m332 363 353 325 0 nfet w=9.6u  l=0.5u as=10.5p ad=28.8p ps=2.4u pd=15.6u
m333 325 352 326 0 nfet w=9.6u  l=0.5u as=10.5p ad=10.5p ps=2.4u pd=2.4u
m334 326 351 0   0 nfet w=9.6u  l=0.5u as=28.8p ad=10.5p ps=15.6u pd=2.4u
m335 364 363 1   1 pfet w=19.2u l=0.5u as=92.2p ad=80.6p ps=9.6u pd=27.6u
m336 364 363 0   0 nfet w=9.6u  l=0.5u as=46.1p ad=40.3p ps=9.6u pd=18u
* signal inputs
vc0  53 0 dc 0
va0  51 0 dc 0 pulse(0 5 10n 2n 2n 6n 20n)
vb0  52 0 dc 0
va1 151 0 dc 5 pulse(0 5 20n 2n 2n 16n 40n)
vb1 152 0 dc 0
va2 251 0 dc 5 pulse(0 5 40n 2n 2n 36n 80n)
vb2 252 0 dc 5
va3 351 0 dc 5 pulse(0 5 80n 2n 2n 76n 160n)
vb3 352 0 dc 0
```

```
* power supply
vdd 1 0 dc 5
* load capacitors
cs0  64 0 2f
cs1 164 0 2f
cs2 264 0 2f
cs3 364 0 2f
cc  453 0 2f
* initial conditions
.ic v(12)=0 v(14)=0 v(25)=0 v(26)=0 v(22)=4.17 v(125)=0 v(212)=0
+ v(214)=0 v(225)=0 v(226)=0 v(222)=4.2 v(321)=4.2 v(323)=5
.tran 1n 160n
.end
```

C.3 DRAM Circuit

```
2-word x 1-bit DRAM circuit
*
* read circuits
*
m0 101 100 1 1 pfet l=0.4u w=1.2u
m1 102 101 1 1 pfet l=0.4u w=3.2u
m2 101 100 0 0 nfet l=0.4u w=0.6u
m3 102 101 0 0 nfet l=0.4u w=1.6u
*
m29 122 112 1 1 pfet l=0.4u w=1.2u
m30 123 122 1 1 pfet l=0.4u w=3.2u
m31 122 112 0 0 nfet l=0.4u w=0.6u
m32 123 122 0 0 nfet l=0.4u w=1.6u
*
* write circuits
*
m4 104 103 1 1    pfet l=0.4u w=1.2u
m5 105 106 1 1    pfet l=0.4u w=1.2u
m6 107 105 1 1    pfet l=0.4u w=1.2u
m7 100 104 107 1  pfet l=0.4u w=1.2u
m8 104 103 0 0    nfet l=0.4u w=0.6u
m9 105 106 0 0    nfet l=0.4u w=0.6u
m10 108 106 0 0   nfet l=0.4u w=0.6u
m11 100 104 108 0 nfet l=0.4u w=0.6u
*
m21 118 117 1 1   pfet l=0.4u w=1.2u
m22 119 106 1 1   pfet l=0.4u w=1.2u
m23 120 119 1 1   pfet l=0.4u w=1.2u
m24 112 118 120 1 pfet l=0.4u w=1.2u
m25 118 117 0 0   nfet l=0.4u w=0.6u
m26 119 106 0 0   nfet l=0.4u w=0.6u
```

```
m27 121 106 0 0   nfet l=0.4u w=0.6u
m28 112 118 121 0 nfet l=0.4u w=0.6u
*
* precharging transistors
*
m33 112 125 124 1 pfet l=0.4u w=3.0u
m36 128 129 127 0 nfet l=0.4u w=0.6u
m38 128 129 131 0 nfet l=0.4u w=0.6u
m40 100 125 124 1 pfet l=0.4u w=3.0u
*
* sense amplifier and restoring circuit
*
m14 100 111 1 1   pfet l=0.4u w=1.2u
m15 112 111 1 1   pfet l=0.4u w=1.2u
m16 112 100 113 0 nfet l=0.4u w=2.8u
m17 100 112 113 0 nfet l=0.4u w=2.8u
m18 113 114 0 0   nfet l=0.4u w=2.4u
*
* memory cells
*
m12 100 109 110 0 nfet l=0.4u w=0.6u
m13 0 110 0 0 nfet l=2.0u w=2.0u
m19 112 115 116 0 nfet l=0.4u w=0.6u
m20 0 116 0 0 nfet l=2.0u w=2.0u
m34 112 126 127 0 nfet l=0.4u w=0.6u
m35 0 127 0 0 nfet l=2.0u w=1.0u
m37 100 130 131 0 nfet l=0.4u w=0.6u
m39 0 131 0 0 nfet l=2.0u w=1.0u
*
* parasitic capacitance
*
c0 131 0 37f
c1 128 0 248f
** node: 128 = vdum
c2 129 0 200f
** node: 129 = pre0
c3 127 0 37f
c4 130 0 13f
** node: 130 = dumr
c5 126 0 13f
** node: 126 = duml
c6 124 0 461f
** node: 124 = vref
c7 125 0 335f
** node: 125 = pre
c8 123 0 117f
** node: 123 = vol
c9 122 0 66f
```

```
c10 121 0 12f
c11 120 0 23f
c12 118 0 63f
c13 119 0 57f
c14 117 0 17f
** node: 117 = vinl
c15 116 0 28f
c16 115 0 13f
c17 114 0 11f
** node: 114 = sel
c18 113 0 152f
c19 112 0 369f
** node: 112 = bitl
c20 111 0 12f
** node: 111 = restore
c21 110 0 28f
c22 109 0 13f
c23 108 0 12f
c24 107 0 23f
c25 104 0 63f
c26 105 0 57f
c27 106 0 276f
** node: 106 = write
c28 103 0 18f
** node: 103 = vinr
c29 102 0 117f
** node: 102 = vor
c30 101 0 66f
c31 100 0 378f
c32 1 0 666f
*
* voltage signals
*
vref 124 0 dc 2.5
vinl 117 0 dc 0 pwl(0 0 24ns 0 25ns 5)
vinr 103 0 dc 0
vpre 125 0 dc 5
+ pulse(5 0 0ns 0.5ns 0.5ns 3ns 12ns)
vpredum 129 0 dc 0
+ pulse(0 5 0ns 0.5ns 0.5ns 3ns 12ns)
vlw0 115 0 dc 0
+ pulse(0 5 5ns 0.5ns 0.5ns 6ns 12ns)
vdumr 130 0 dc 0
+ pulse(0 5 5ns 0.5ns 0.5ns 6ns 12ns)
vwrite 106 0 dc 0
+ pulse(0 5 4ns 0.5ns 0.5ns 7ns 24ns)
vsel 114 0 dc 0
+ pulse(0 5 17ns 0.5ns 0.5ns 6ns 24ns)
```

```
vrestore 111 0 dc 0
+ pulse(5 0 17.5ns 0.5ns 0.5ns 5.5ns 24ns)
vdum 128 0 dc 1.8v
vlw1 109 0 dc 0
vduml 126 0 dc 0
* power supply
vdd 1 0 dc 5
*
* analysis
*
.nodeset v(1)=5 v(100)=1.52 v(101)=4.87
+ v(102)=1.25e-8 v(103)=0 v(104)=5
+ v(105)=5 v(106)=0 v(107)=5 v(108)=1.52
+ v(109)=0 v(110)=4.45e-7
+ v(111)=5 v(112)=1.52 v(113)=8.83e-1
+ v(114)=0 v(115)=0 v(116)=4.45e-7
+ v(117)=0 v(118)=5 v(119)=5 v(120)=5
+ v(121)=1.52 v(122)=4.87
+ v(123)=1.25e-8 v(124)=2.5 v(125)=5
+ v(126)=0 v(127)=4.51e-7 v(128)=1.8
+ v(129)=0 v(130)=0 v(131)=4.51e-7
.tran 0.2ns 48ns
.end
```

C.4 Single-Stage Folded-Cascode Amplifier

```
Single-stage folded-cascode amplifier
*
* gain stage
*
m1   12 5 4 4     cmosp w=100u l=0.5u
m2   13 3 4 4     cmosp w=100u l=0.5u
m3   16 7 12 12   cmosn w=112.5u l=0.75u
m4   17 7 13 12   cmosn w=112.5u l=0.75u
m5   14 10 105 1 cmosp w=200u l=0.5u
m6   15 10 106 1 cmosp w=200u l=0.5u
m7   16 11 14 14 cmosp w=200u l=0.5u
m8   17 11 15 15 cmosp w=200u l=0.5u
m9   12 6 2 2     cmosn w=125u l=0.75u
m10 13 6 2 2     cmosn w=125u l=0.75u
m19 4 10 119 1   cmosp w=400u l=0.5u
*
* offset compensation
*
m20 2 0 19 19    cmosp w=100u l=0.5u
m21 18 10 121 1 cmosp w=200u l=0.5u
m22 19 11 18 18 cmosp w=200u l=0.5u
```

```
m23 12 16 19 19 cmosp w=100u l=0.5u
m24 13 16 19 19 cmosp w=100u l=0.5u
* power supply
vdd 1 0 dc 2.5
vss 2 0 dc -2.5
vin+ 5 0 dc 0 ac 1
vin- 3 0 dc dc 0
* current monitoring sources
vm5 1 105 dc 0
vm6 1 106 dc 0
vm19 1 119 dc 0
vm21 1 121 dc 0
*
* Bias voltages
*
vb10 10 0 dc 1.5
vb11 11 0 dc 1.2
vb7  7  0 dc 0.3
vb6  6  0 dc -1.5
*
cl 17 0 2p
*
.ac dec 5 10 10meg
.end
```

C.5 Four-Bit Self-Timed Adder

```
Four-bit Adder circuit
*
* Single bit adder
*
* 2 = A, 3 = Ab, 4 = B, 5 = Bb, 6 = C, 7 = Cb,
* 8 = Carry, 9 = Carryb, 10 = Initialize, 30 = Completion
.subckt 1b_add 2 3 4 5 6 7 8 9 20 21 10 30 1
* Carry circuit
M1  11  9  1  1 cmosp w=1.5u l=1.5u as=4.5p ad=4.5p ps=7.5u pd=7.5u
M2  11 10  1  1 cmosp w=7.0u l=0.5u as=21p  ad=21p  ps=13u  pd=13u
M3  12 10  1  1 cmosp w=7.0u l=0.5u as=21p  ad=21p  ps=13u  pd=13u
M4  12  8  1  1 cmosp w=1.5u l=1.5u as=4.5p ad=4.5p ps=7.5u pd=7.5u
M5   9 11  1  1 cmosp w=4.0u l=0.5u as=12p  ad=12p  ps=10u  pd=10u
M6   9 11  0  0 cmosn w=3.0u l=0.5u as=9p   ad=9p   ps=9u   pd=9u
M7   8 12  1  1 cmosp w=4.0u l=0.5u as=12p  ad=12p  ps=10u  pd=10u
M8   8 12  0  0 cmosn w=3.0u l=0.5u as=9p   ad=9p   ps=9u   pd=9u
M9  11  7 13  0 cmosn w=3.5u l=0.5u as=10.5p ad=10.5p ps=9.5u pd=9.5u
M10 12  6 13  0 cmosn w=3.5u l=0.5u as=10.5p ad=10.5p ps=9.5u pd=9.5u
M11 11  5 15  0 cmosn w=3.5u l=0.5u as=10.5p ad=10.5p ps=9.5u pd=9.5u
M12 12  4 16  0 cmosn w=3.5u l=0.5u as=10.5p ad=10.5p ps=9.5u pd=9.5u
```

```
M13 13  4 15  0 cmosn w=3.5u l=0.5u as=10.5p ad=10.5p ps=9.5u pd=9.5u
M14 13  5 16  0 cmosn w=3.5u l=0.5u as=10.5p ad=10.5p ps=9.5u pd=9.5u
M15 15  3  0  0 cmosn w=5.5u l=0.5u as=16.5p ad=16.5p ps=11.5u pd=11.5u
M16 16  2  0  0 cmosn w=5.5u l=0.5u as=16.5p ad=16.5p ps=11.5u pd=11.5u
*
* Sum circuit
M21 22 20  1  1 cmosp w=1.5u l=1.5u as=4.5p ad=4.5p ps=7.5u pd=7.5u
M22 22 10  1  1 cmosp w=6.5u l=0.5u as=19.5p ad=19.5p ps=12.5u pd=12.5u
M23 23 10  1  1 cmosp w=6.5u l=0.5u as=19.5p ad=19.5p ps=12.5u pd=12.5u
M24 23 21  1  1 cmosp w=1.5u l=1.5u as=4.5p ad=4.5p ps=7.5u pd=7.5u
M25 20 22  1  1 cmosp w=4.0u l=0.5u as=12p  ad=12p  ps=10u  pd=10u
M26 20 22  0  0 cmosn w=2.5u l=0.5u as=7.5p ad=7.5p  ps=8.5u pd=8.5u
M27 21 23  1  1 cmosp w=4.0u l=0.5u as=12p  ad=12p  ps=10u  pd=10u
M28 21 23  0  0 cmosn w=2.5u l=0.5u as=7.5p ad=7.5p  ps=8.5u pd=8.5u
M29 22  4 24  0 cmosn w=4.5u l=0.5u as=13.5p ad=13.5p ps=10.5u pd=10.5u
M30 23  5 24  0 cmosn w=4.5u l=0.5u as=13.5p ad=13.5p ps=10.5u pd=10.5u
M31 22  5 25  0 cmosn w=3.5u l=0.5u as=10.5p ad=10.5p ps=9.5u pd=9.5u
M32 23  4 25  0 cmosn w=3.5u l=0.5u as=10.5p ad=10.5p ps=9.5u pd=9.5u
M33 24  6 26  0 cmosn w=3.5u l=0.5u as=10.5p ad=10.5p ps=9.5u pd=9.5u
M34 24  7 27  0 cmosn w=3.5u l=0.5u as=10.5p ad=10.5p ps=9.5u pd=9.5u
M35 25  7 26  0 cmosn w=4.0u l=0.5u as=12p  ad=12p  ps=10u  pd=10u
M36 25  6 27  0 cmosn w=4.0u l=0.5u as=12p  ad=12p  ps=10u  pd=10u
M37 26  2  0  0 cmosn w=5.5u l=0.5u as=16.5p ad=16.5p ps=11.5u pd=11.5u
M38 27  3  0  0 cmosn w=5.5u l=0.5u as=16.5p ad=16.5p ps=11.5u pd=11.5u
*
* DV/PV OR gate circuit
M40 31  8  1  1 cmosp w=4.0u l=0.5u as=12p  ad=12p  ps=10u  pd=10u
M41 32  9 31  1 cmosp w=4.0u l=0.5u as=12p  ad=12p  ps=10u  pd=10u
M42 32  8  0  0 cmosn w=3.0u l=0.5u as=9p   ad=9p   ps=9u   pd=9u
M43 32  9  0  0 cmosn w=3.0u l=0.5u as=9p   ad=9p   ps=9u   pd=9u
M44 30 32  1  1 cmosp w=4.0u l=0.5u as=12p  ad=12p  ps=10u  pd=10u
M45 30 32  0  0 cmosn w=3.0u l=0.5u as=9p   ad=9p   ps=9u   pd=9u
.ends 1b_add
*
x0   2   3   4   5   6   7   8   9  20  21  10  30 1 1b_add
x1 102 103 104 105   8   9 108 109 120 121  30 130 1 1b_add
x2 202 203 204 205 108 109 208 209 220 221 130 230 1 1b_add
x3 302 303 304 305 208 209 308 309 320 321 230 330 1 1b_add
*
* voltage sources
*
vini 10 0 pulse (0 5 1n 1n 1n 1n 4n)
va0   2 0 dc 0
va0b  3 0 dc 5
vb0   4 0 dc 0 pwl (0 0 9n 0 10n 5 16n 5)
vb0b  5 0 dc 5 pwl (0 5 9n 5 10n 0 16n 0)
vc0   6 0 dc 0 pwl (0 0 5n 0 6n 5 9n 5 10n 0 13n 0 14n 5 16n 5)
vc0b  7 0 dc 5 pwl (0 5 5n 5 6n 0 9n 0 10n 5 13n 5 14n 0 16n 0)
```

```
va1   102 0 dc 0 pwl (0 0 5n 0 6n 5 9n 5 10n 0 13n 0 14n 5 16n 5)
va1b  103 0 dc 5 pwl (0 5 5n 5 6n 0 9n 0 10n 5 13n 5 14n 0 16n 0)
vb1   104 0 dc 0 pwl (0 0 5n 0 6n 5 9n 5 10n 0 13n 0 14n 5 16n 5)
vb1b  105 0 dc 5 pwl (0 5 5n 5 6n 0 9n 0 10n 5 13n 5 14n 0 16n 0)
va2   202 0 dc 0 pwl (0 0 9n 0 10n 5 16n 5)
va2b  203 0 dc 5 pwl (0 5 9n 5 10n 0 16n 0)
vb2   204 0 dc 0 pwl (0 0 9n 0 10n 5 16n 5)
vb2b  205 0 dc 5 pwl (0 5 9n 5 10n 0 16n 0)
va3   302 0 dc 5 pwl (0 5 9n 5 10n 0 16n 0)
va3b  303 0 dc 0 pwl (0 0 9n 0 10n 5 16n 5)
vb3   304 0 dc 0 pwl (0 0 9n 0 10n 5 16n 5)
vb3b  305 0 dc 5 pwl (0 5 9n 5 10n 0 16n 0)
*
vdd 1 0 dc 5
.tran 0.5n 16n
.end
```

C.6 Four-State Asynchronous Master-Slave Latch

```
Asynchronous D-Flip-Flop
*
* four-state dynamic asynchronous master-slave latch
*
* 11 = di[0], 12 = di[1], 13 = di[2], 14 = di[3],
* 15 = ki, 16 = rst, 17 = rstb,
* 51 = do[0], 52 = do[1], 53 = do[2], 54 = do[3], 55 = ko
.subckt dff 11 12 13 14 15 16 17 51 52 53 54 55
m1  53 15 1  1  cmosp w=10u l=0.5u
m2  53 14 21 0  cmosn w=5u  l=0.5u
m3  21 15 0  0  cmosn w=5u  l=0.5u
m4  22 15 1  1  cmosp w=10u l=0.5u
m5  54 13 22 1  cmosp w=10u l=0.5u
m6  54 15 0  0  cmosn w=5u  l=0.5u
m7  23 15 1  1  cmosp w=10u l=0.5u
m8  51 12 23 1  cmosp w=10u l=0.5u
m9  51 15 0  0  cmosn w=5u  l=0.5u
m10 52 15 1  1  cmosp w=10u l=0.5u
m11 52 11 24 0  cmosn w=5u  l=0.5u
m12 24 15 0  0  cmosn w=5u  l=0.5u
m13 53 17 1  1  cmosp w=1u  l=0.5u
m14 54 16 0  0  cmosn w=0.5u l=0.5u
m15 51 16 0  0  cmosn w=1u  l=0.5u
m16 52 17 1  1  cmosp w=0.5u l=0.5u
m17 55 54 0  0  cmosn w=5u  l=0.5u
m18 55 53 1  1  cmosp w=10u l=0.5u
m19 55 51 0  0  cmosn w=5u  l=0.5u
m20 55 52 1  1  cmosp w=10u l=0.5u
```

```
vdd 1 0 dc 5
.ends dff
x1 11 12 13 14 15 16 17 51 52 53 54 55 dff
r51 51 0 10meg
r52 52 0 10meg
r53 53 0 10meg
r54 54 0 10meg
r55 55 0 10meg
vdi0 11 0 pwl ( 0n 0 2n 0 2.5n 5 4n 5 4.5n 0 6n 0 8n 0 10n 0 )
vdi1 12 0 pwl ( 0n 5 2n 5 4n 5 6n 5 8n 5 8.5n 0 10n 0)
vdi2 13 0 pwl ( 0n 5 2n 5 4n 5 4.5n 0 6n 0 6.5n 5 8n 5 10n 5 )
vdi3 14 0 pwl ( 0n 0 2n 0 4n 0 6n 0 6.5n 5 8n 5 8.5n 0 10n 0 )
vki   15 0 pulse ( 5 0 4n 0.5n 0.5n 1.5n 4n )
vrst  16 0 pulse ( 5 0 4n 0.5n 0.5n 1.5n 4n )
vrstb 17 0 pulse ( 0 5 4n 0.5n 0.5n 1.5n 4n )
.tran 0.1n 10n
.end
```

C.7 Band-gap Reference Circuit

```
Bandgap Voltage Reference
*
m1  3  1  60 60  cmosn  w=40u  l=6u
m2  4  2  60 60  cmosn  w=40u  l=6u
m3  3  3  50 50  cmosp  w=20u  l=6u
m4  4  3  50 50  cmosp  w=20u  l=6u
m6  59 4  6  6   cmosn  w=100u l=3u
vm 50 59 dc 0
*
r1  6 1  12k
r2  6 2  60k
re  9 60 18.4k
d1  1 7  diode1 1
d2  7 60 diode1 1
d3  2 8  diode1 10
d4  8 9  diode1 10
vdd 50 0 dc 5
vss 60 0 dc 0
*
m7  51 6  50 50  cmosp  w=4u   l=10u
m8  51 51 52 52  cmosn  w=6u   l=6u
m9  52 52 60 60  cmosn  w=19u  l=6u
*
.op
.width in=80 out=80
.option gmin=1e-10 temp=80
.end
```

Appendix D

Example Parameter Sets for SPICE Models

D.1 BSIM_plus Parameter Set

The following parameter set was extracted from a 0.4-μm CMOS technology of Samsung Electronics Co., in Jul. 1992.

```
.model cmosn nmos level = 41
+    vfb     =    -1.299
+    phis    =     1.631
+    gamma1  =     0.421
+    gamma2  =     0.328
+    ks      =     2.7e-4
+    knz     =     0.244
+    knb     =     5.4e-05
+    etaz    =    -0.699
+    etal    =     0.185
+    mu0     =     350.35
+    tox     =     8.0
+    ugsz    =    -0.12
+    ugsl    =     0.313
```

```
+    ubs     =     4.9e-3
+    ecrit   =     70
+    dl      =     0.1
+    dw      =     0.04
+    h0      =     0.142
+    h1      =     2.238
+    wwid = 20 wnrw = 0.2
+    llng = 20 lsht = 0.2
+    cgdo = 5.98e-10 cgso = 5.98e-10
+    cgbo = 5.92e-10 rsh = 0 cj = 2.9e-4
+    cjsw = 4.54e-10 js = 1e-08 pb = 0.8
+    pbsw = 0.8 mj = 0.91 mjsw = 0.163
.model cmosp pmos level=41
+    vfb     =    -0.330
+    phis    =     0.889
+    gamma1  =     0.563
+    gamma2  =     0.309
+    ks      =     3.4e-04
+    knz     =     0.217
+    knb     =    -3.9e-04
+    etaz    =    -3.7e-02
+    eta1    =     4.2e-02
+    mu0     =     90.0
+    tox     =     8.0
```

```
+    ugsz    =    -7.1e-02
+    ugsl    =     9.3e-02
+    ubs     =     1.5e-04
+    ecrit   =     314
+    dl      =     0.186357
+    dw      =     2.0e-02
+    h0      =     1.61
+    h1      =     42.25
+    wwid = 20 wnrw = 0.2
+    llng = 20 lsht = 0.2
+    cgdo = 2.23e-10 cgso = 2.23e-10
+    cgbo = 6.6e-10 rsh = 0 cj = 4.77e-4
+    cjsw = 1.41e-10 js = 1e-08 pb = 0.85
+    pbsw = 0.85 mj = 0.499 mjsw = 0.198
```

D.2 BSIM Parameter Set

The following parameter set was provided by the MOSIS Service of the USC/Information Sciences Institute, Marina del Rey, CA, in Sept. 1992, for a 1.2-µm N-well CMOS technology from Hewlett-Packard Co.

```
.model n28p_nm1_du1 nmos level=4
+ vfb = -1.09268 lvfb = 0.145976 wvfb = -0.18062
```

+ phi = 0.81773 lphi = 1.5388e-25 wphi = 0

+ k1 = 1.24109 lk1 = -0.147884 wk1 = 0.311637

+ k2 = 0.171956 lk2 = 0.00789554 wk2 = 0.0409508

+ eta = -0.00856825 leta = 0.0156111 weta = 0.00657144

+ muz = 545.594 dl = 0.364296 dw = 0.326307

+ u0 = 0.0804435 lu0 = 0.121767 wu0 = -0.040991

+ u1 = -0.00894358 lu1 = 0.173892 wu1 = -0.0135661

+ x2mz = 4.45009 lx2mz = -1.30542 wx2mz = 34.1889

+ x2e = -0.00334242 lx2e = -0.00244882 wx2e = -0.00376562

+ x3e = 0.00107654 lx3e = -0.000837026 wx3e = -0.00702102

+ x2u0 = -0.00248138 lx2u0 = 0.00202559 wx2u0 = 0.0208494

+ x2u1 = -0.00214153 lx2u1 = 0.00226659 wx2u1 = 0.00500715

+ mus = 619.09 lmus = 94.7385 wmus = -15.4818

+ x2ms = -3.9388 lx2ms = 6.86882 wx2ms = 62.6617

+ x3ms = 4.37592 lx3ms = 19.5844 wx3ms = -8.86701

+ x3u1 = 0.00140679 lx3u1 = 0.016155 wx3u1 = -0.00698885

+ tox = 0.021 temp = 27 vdd = 5

+ cgdo = 4.49274e-10 cgso = 4.49274e-10 cgbo = 3.30355e-10

+ xpart = 1

+ n0 = 1 ln0 = 0 wn0 = 0

+ nb = 0 lnb = 0 wnb = 0

+ nd = 0 lnd = 0 wnd = 0

+ rsh = 94.8 cj = 0.00039182 cjsw = 1.33e-10

+ js = 0 pb = 0.8 pbsw = 0.8

```
+ mj = 0.688329 mjsw = 0.119521 wdf = 0
+ dell = 0
.model n28p_pm1_du2 pmos level=4
+ vfb = -0.259516 lvfb = 0.0507676 wvfb = 0.0835717
+ phi = 0.720766 lphi = 3.61782e-25 wphi = 0
+ k1 = 0.651893 lk1 = -0.419673 wk1 = 0.525431
+ k2 = 0.0706889 lk2 = -0.190061 wk2 = 0.278352
+ eta = 0.00590856 leta = -0.0130801 weta = 0.0556095
+ muz = 175.801 dl = 0.123481 dw = 0.270397
+ u0 = 0.158352 lu0 = 0.0192455 wu0 = -0.0229639
+ u1 = -0.0116846 lu1 = 0.13276 wu1 = 0.00272628
+ x2mz = 10.0075 lx2mz = -5.0057 wx2mz = 5.82096
+ x2e = 0.00702262 lx2e = -0.0204754 wx2e = 0.0268249
+ x3e = 0.00213282 lx3e = -0.00371037 wx3e = 0.000394245
+ x2u0 = 0.0101004 lx2u0 = -0.00671065 wx2u0 = 0.0105184
+ x2u1 = -0.00197964 lx2u1 = 0.005204 wx2u1 = 0.00412466
+ mus = 198.447 lmus = 42.3116 wmus = 0.882657
+ x2ms = 9.68845 lx2ms = -2.6516 wx2ms = 10.9009
+ x3ms = 1.08978 lx3ms = 2.27222 wx3ms = 2.00229
+ x3u1 = 0.000591917 lx3u1 = -0.00926292 wx3u1 = 0.000399501
+ tox = 0.021 temp = 27 vdd = 5
+ cgdo = 1.52285e-10 cgso = 1.52285e-10 cgbo = 3.12479e-10
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
```

```
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 118.4 cj = 0.00049439 cjsw = 1.8372e-10
+ js = 0 pb = 0.85 pbsw = 0.85
+ mj = 0.50403 mjsw = 0.241211 wdf = 0
+ dell = 0
```

D.3 MOS Level-3 Parameter Set

The following parameter set was provided by the MOSIS Service of the USC/Information Sciences Institute, Marina del Rey, CA, in Sept. 1992, for a 1.2-μm N-well CMOS technology from Hewlett-Packard Co.

```
.model cmosn nmos level=3 phi=0.600000 tox=2.1000e-08
+ xj=0.200000u tpg=1 vto=0.8190 delta=8.8120e-01
+ ld=1.6000e-07 kp=9.9549e-05 uo=605.4 theta=8.6960e-02
+ rsh=9.4800e+01 gamma=0.5785 nsub=2.7260e+16
+ nfs=1.9800e+12 vmax=1.7400e+05 eta=4.8300e-02
+ kappa=1.0750e-01 cgdo=3.9465e-10 cgso=3.9465e-10
+ cgbo=3.4612e-10 cj=3.9182e-04 mj=0.6883
+ cjsw=1.3284e-10  mjsw=0.119521 pb=0.800000
* weff = wdrawn - delta_w
* the suggested delta_w is 3.7560e-07
```

```
.model cmosp pmos level=3 phi=0.600000 tox=2.1000e-08
+ xj=0.200000u tpg=-1 vto=-0.9202 delta=1.1620e+00
+ ld=1.9470e-08 kp=2.9845e-05 uo=181.5 theta=1.1970e-01
+ rsh=1.1840e+02 gamma=0.5592 nsub=2.5470e+16
+ nfs=3.4600e+12 vmax=3.8140e+05 eta=1.7250e-01
+ kappa=1.0000e+01 cgdo=4.8023e-11 cgso=4.8023e-11
+ cgbo=3.3294e-10 cj=4.9439e-04 mj=0.5040
+ cjsw=1.8372e-10 mjsw=0.241211 pb=0.850000
* weff = wdrawn - delta_w
* the suggested delta_w is 3.3440e-07
```

D.4 MOS Level-2 Parameter Set

The following parameter set was provided by the MOSIS Service of the USC/Information Sciences Institute, Marina del Rey, CA, in Aug. 1992, for a 2-μm double-poly P-well CMOS technology from Orbit Semiconductor Inc.

```
* n26e/scpe/august 1992
.model cmosn nmos level=2 ld=0.250000u
+ tox=403.000000e-10 nsub=2.385409e+16
+ vto=0.930789 kp=5.098000e-05 gamma=1.0384
+ phi=0.6 uo=595.348 uexp=0.170172
+ ucrit=138498 delta=1.68804 vmax=100000
```

```
+ xj=0.250000u lambda=1.273190e-02
+ nfs=3.91e+11 neff=1 nss=1.000000e+10
+ tpg=1.000000 rsh=28.080000 cgdo=3.213223e-10
+ cgso=3.213223e-10 cgbo=3.502129e-10
+ cj=3.777700e-04 mj=0.445282 cjsw=5.017100e-10
+ mjsw=0.365853 pb=0.80
* weff = wdrawn - delta_w
* the suggested delta_w is 0.02 um
.model cmosp pmos level=2 ld=0.247291u
+ tox=403.000000e-10 nsub=5.919569e+15
+ vto=-0.746341 kp=1.928000e-05 gamma=0.5173
+ phi=0.6 uo=225.229 uexp=0.182046
+ ucrit=25792.2 delta=0.927627 vmax=47097.2
+ xj=0.250000u lambda=4.440734e-2
+ nfs=3.23e+11 neff=1.001 nss=1.000000e+10
+ tpg=-1.000000 rsh=72.640000 cgdo=3.178405e-10
+ cgso=3.178405e-10 cgbo=3.826468e-10
+ cj=2.075600e-04 mj=0.464141 cjsw=1.870000e-10
+ mjsw=0.073070 pb=0.70
* weff = wdrawn - delta_w
* the suggested delta_w is -0.23 um
```

APPENDIX E

BSIM_plus Model Expressions

E.1 Drain Current Expressions

E.1.1 Threshold Voltage:

$$V_{BST} = \frac{\gamma_1 - \gamma_2}{K_S} + \sqrt{\phi_S}$$

$$V_{th} = V_{FB} + \phi_S + \gamma_1(\sqrt{\phi_S - V_{BS}} - \sqrt{\phi_S}) - \frac{K_S}{2}(\sqrt{\phi_S - V_{BS}} - \sqrt{\phi_S})^2$$

$$+ \frac{K_{NZ}}{W} + \frac{K_{NB}V_{BS}}{W} - \left[\eta_Z + \frac{\eta_L}{L}\right]V_{DS} \quad \text{for } |V_{BS}| \le |V_{BST}|,$$

and

$$V_{th} = V_{FB} + \phi_S + \gamma_1(\sqrt{\phi_S - V_{BST}} - \sqrt{\phi_S}) - \frac{K_S}{2}(\sqrt{\phi_S - V_{BST}} - \sqrt{\phi_S})^2$$

$$+ \gamma_2(\sqrt{\phi_S - V_{BS}} - \sqrt{\phi_S - V_{BST}}) + \frac{K_{NZ}}{W} + \frac{K_{NB}V_{BS}}{W}$$

$$- \left[\eta_Z + \frac{\eta_L}{L}\right]V_{DS} \quad \text{for } |V_{BS}| > |V_{BST}|.$$

E.1.2 Triode Region Drain Current Expression

$$I_{DS,T} = \frac{\mu_0 C_{OX}\frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{a}{2}V_{DS}^2\right]F_{S,triode}}{\left[1 + \left[U_{GSZ} + \frac{U_{GSL}}{L}\right](V_{GS} - V_{th}) + U_{BS}V_{BS}\right]\left[1 + \frac{V_{DS}}{E_{CRIT}\cdot L}\right]}$$

$$a = 1 + \frac{g\gamma_1}{2\sqrt{\phi_S - V_{BS}}}$$

$$g = 1 - \frac{1}{1.744 + 0.8364(\phi_S - V_{BS})}$$

$$F_{S,triode} = 1 - H_0\left[1 - e^{\frac{V_{DS} - V_{DSAT}}{H_1}}\right]$$

E.1.3 Saturation Region Drain Current Expression:

$$I_{DS,S} = \frac{\mu_0 C_{OX}\frac{W}{L}(V_{GS} - V_{th})^2 F_{S,satn.}}{\left[1 + \left[U_{GSZ} + \frac{U_{GSL}}{L}\right](V_{GS} - V_{th}) + U_{BS}V_{BS}\right]2aK}$$

$$K = \frac{1 + V_C + \sqrt{1 + 2V_C}}{2}$$

$$V_C = \frac{1}{E_{CRIT}\cdot L}\frac{(V_{GS} - V_{th})}{a}$$

$$F_{S,satn.} = 1 + H_0\left[1 - e^{\frac{V_{DSAT} - V_{DS}}{H_1}}\right]$$

E.1.4 Saturation Voltage:

$$V_{DSAT} = \frac{V_{GS} - V_{th}}{a\sqrt{K}}$$

E.1.5 Weak Inversion Drain Current Expression:

$$I_{EXP} = I_0 \frac{W}{L} e^{\frac{V_{GS} - V_{th}}{nV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right)$$

$$I_{DS,W} = \frac{I_{EXP} \cdot I_{LIM}}{I_{EXP} + I_{LIM}}$$

$$I_{LIM} = \frac{I_0}{2} \cdot \frac{W}{L}$$

E.1.6 Total Drain Current:

1. The summation method:

For $|V_{DS}| \leq |V_{DSAT}|$,

$$I_{DS} = I_{DS,T} + I_{DS,W}$$

For $|V_{DS}| > |V_{DSAT}|$,

$$I_{DS} = I_{DS,S} + I_{DS,W}$$

2. The spline method:

Use spline function to ensure continuous values in I_{DS}, G_m, and G_{DS} at the strong-inversion to weak-inversion transition point.

E.2 Drain Current Derivatives and Conductance Expressions:

$$\frac{\partial g}{\partial V_{BS}} = \frac{-0.8364}{\left[1.744 + 0.8364(\phi_S - V_{BS})\right]^2}$$

$$\frac{\partial g}{\partial V_{DS}} = 0$$

$$\frac{\partial g}{\partial V_{GS}} = 0$$

$$\frac{\partial a}{\partial V_{BS}} = \frac{0.25\gamma_1}{\sqrt{\phi_S - V_{BS}}}\left[2\frac{\partial g}{\partial V_{BS}} + \frac{g}{\phi_S - V_{BS}}\right]$$

$$\frac{\partial a}{\partial V_{DS}} = 0$$

$$\frac{\partial a}{\partial V_{GS}} = 0$$

$$\frac{\partial (V_{GS} - V_{th})}{\partial V_{BS}} = -\frac{\partial V_{th}}{\partial V_{BS}}$$

$$\frac{\partial (V_{GS} - V_{th})}{\partial V_{DS}} = \eta_Z + \frac{\eta_L}{L}$$

$$\frac{\partial (V_{GS} - V_{th})}{\partial V_{GS}} = 1$$

$$ARG1 = 1 + \left[U_{GSZ} + \frac{U_{GSL}}{L}\right](V_{GS} - V_{th}) + U_{BS}V_{BS}$$

$$\frac{\partial ARG1}{\partial V_{BS}} = -\left[U_{GSZ} + \frac{U_{GSL}}{L}\right]\frac{\partial V_{th}}{\partial V_{BS}} + U_{BS}$$

$$\frac{\partial ARG1}{\partial V_{DS}} = \eta\left[U_{GSZ} + \frac{U_{GSL}}{L}\right]$$

$$\frac{\partial ARG1}{\partial V_{GS}} = \left[U_{GSZ} + \frac{U_{GSL}}{L}\right]$$

$$\frac{\partial V_C}{\partial V_{BS}} = \frac{1}{E_{CRIT} \cdot L \cdot a^2}\left[- a\frac{\partial V_{th}}{\partial V_{BS}} - (V_{GS} - V_{th})\frac{\partial a}{\partial V_{BS}}\right]$$

$$\frac{\partial V_C}{\partial V_{DS}} = \frac{\eta_Z + \frac{\eta_L}{L}}{E_{CRIT} \cdot L \cdot a}$$

$$\frac{\partial V_C}{\partial V_{GS}} = \frac{1}{E_{CRIT} \cdot L \cdot a}$$

$$\beta_{EFF} = \frac{\mu_0 \, C_{OX} \, \frac{W}{L}}{ARG1}$$

$$\frac{\partial \beta_{EFF}}{\partial V_{BS}} = - \frac{\beta_{EFF}}{ARG1}\left[- \left[U_{GSZ} + \frac{U_{GSL}}{L}\right]\frac{\partial V_{th}}{\partial V_{BS}} + U_{BS}\right]$$

$$\frac{\partial \beta_{EFF}}{\partial V_{DS}} = - \frac{\beta_{EFF}}{ARG1}\left[U_{GSZ} + \frac{U_{GSL}}{L}\right]\left[\eta_Z + \frac{\eta_L}{L}\right]$$

$$\frac{\partial \beta_{EFF}}{\partial V_{GS}} = - \beta_{EFF} \, \frac{U_{GSZ} + \frac{U_{GSL}}{L}}{ARG1}$$

$$ARG2 = (V_{GS} - V_{th}) - \frac{aV_{DS}}{2}$$

$$\frac{\partial ARG2}{\partial V_{BS}} = - \frac{\partial V_{th}}{\partial V_{BS}} - \frac{V_{DS}}{2} \cdot \frac{\partial a}{\partial V_{BS}}$$

$$\frac{\partial ARG2}{\partial V_{DS}} = \left[\eta_Z + \frac{\eta_L}{L}\right] - \frac{a}{2}$$

$$\frac{\partial ARG2}{\partial V_{GS}} = 1$$

$$\frac{\partial K}{\partial V_{BS}} = \frac{1}{2}\left[\frac{\partial V_C}{\partial V_{BS}} + \frac{2}{2\sqrt{1 + 2V_C}} \cdot \frac{\partial V_C}{\partial V_{BS}}\right]$$

$$\frac{\partial K}{\partial V_{DS}} = \frac{1}{2}\left[\frac{\partial V_C}{\partial V_{DS}} + \frac{1}{\sqrt{1 + 2V_C}} \cdot \frac{\partial V_C}{\partial V_{DS}}\right]$$

$$\frac{\partial K}{\partial V_{GS}} = \frac{1}{2}\left[\frac{\partial V_C}{\partial V_{GS}} + \frac{1}{\sqrt{1 + 2V_C}} \cdot \frac{\partial V_C}{\partial V_{GS}}\right]$$

$$\frac{\partial V_{DSAT}}{\partial V_{BS}} = -\frac{V_{DSAT}}{(V_{GS} - V_{th})} \cdot \frac{\partial V_{th}}{\partial V_{BS}} - \frac{V_{DSAT}}{2K} \cdot \frac{\partial V_{th}}{\partial V_{BS}} - \frac{V_{DSAT}}{a} \cdot \frac{\partial a}{\partial V_{BS}}$$

$$\frac{\partial V_{DSAT}}{\partial V_{DS}} = \left[\eta_Z + \frac{\eta_L}{L}\right] \frac{V_{DSAT}}{(V_{GS} - V_{th})} - \frac{V_{DSAT}}{2K} \cdot \frac{\partial K}{\partial V_{DS}}$$

$$\frac{\partial V_{DSAT}}{\partial V_{GS}} = \frac{V_{DSAT}}{(V_{GS} - V_{th})} - \frac{V_{DSAT}}{2K} \cdot \frac{\partial K}{\partial V_{GS}}$$

$$ARG3 = 1 + \frac{V_{DS}}{E_{CRIT} \cdot L}$$

$$\frac{\partial ARG3}{\partial V_{BS}} = 0$$

$$\frac{\partial ARG3}{\partial V_{DS}} = \frac{1}{E_{CRIT} \cdot L}$$

$$\frac{\partial ARG3}{\partial V_{GS}} = 0$$

$$ARG4 = \frac{(V_{GS} - V_{th})^2}{aK}$$

$$\frac{\partial ARG4}{\partial V_{BS}} = ARG4 \left[-\frac{2}{(V_{GS} - V_{th})} \cdot \frac{\partial V_{th}}{\partial V_{BS}} - \frac{1}{K} \cdot \frac{\partial K}{\partial V_{BS}} - \frac{1}{a} \cdot \frac{\partial a}{\partial V_{BS}}\right]$$

$$\frac{\partial ARG4}{\partial V_{DS}} = ARG4\left[\frac{2\left(\eta_Z + \frac{\eta_L}{l}\right)}{(V_{GS} - V_{th})} - \frac{1}{K}\cdot\frac{\partial K}{\partial V_{DS}}\right]$$

$$\frac{\partial ARG4}{\partial V_{GS}} = ARG4\left[\frac{2}{(V_{GS} - V_{th})} - \frac{1}{K}\frac{\partial K}{\partial V_{GS}}\right]$$

$$\frac{\partial F_{S,triode}}{\partial V_{BS}} = -\frac{\partial V_{DSAT}}{\partial V_{BS}}\left[\frac{-1 + H_0 + F_{S,triode}}{H_1}\right]$$

$$\frac{\partial F_{S,triode}}{\partial V_{DS}} = \left[1 - \frac{\partial V_{DSAT}}{\partial V_{DS}}\right]\left[\frac{-1 + H_0 + F_{S,triode}}{H_1}\right]$$

$$\frac{\partial F_{S,triode}}{\partial V_{GS}} = -\frac{\partial V_{DSAT}}{\partial V_{GS}}\left[\frac{-1 + H_0 + F_{S,triode}}{H_1}\right]$$

$$\frac{\partial F_{S,satn.}}{\partial V_{BS}} = \frac{\partial V_{DSAT}}{\partial V_{BS}}\left[\frac{F_{S,satn.} - 1 - H_0}{H_1}\right]$$

$$\frac{\partial F_{S,satn.}}{\partial V_{DS}} = \left[\frac{\partial V_{DSAT}}{\partial V_{DS}} - 1\right]\left[\frac{F_{S,satn.} - 1 - H_0}{H_1}\right]$$

$$\frac{\partial F_{S,satn.}}{\partial V_{GS}} = \frac{\partial V_{DSAT}}{\partial V_{GS}}\left[\frac{F_{S,satn.} - 1 - H_0}{H_1}\right]$$

$$W_{GS} = e^{\frac{(V_{GS} - V_{th})}{nV_T}}$$

$$\frac{\partial W_{GS}}{\partial V_{BS}} = -\frac{\partial V_{th}}{\partial V_{BS}}\cdot\frac{W_{GS}}{nV_T}$$

$$\frac{\partial W_{GS}}{\partial V_{DS}} = \left[\eta_Z + \frac{\eta_L}{L}\right]\frac{W_{GS}}{nV_T}$$

$$\frac{\partial W_{GS}}{\partial V_{GS}} = \frac{W_{GS}}{nV_T}$$

$$W_{DS} = 1 - e^{-\frac{V_{DS}}{V_T}}$$

$$WARG1 = e^{-\frac{V_{DS}}{V_T}}$$

$$\frac{\partial W_{DS}}{\partial V_{BS}} = 0$$

$$\frac{\partial W_{DS}}{\partial V_{DS}} = \frac{WARG1}{V_T}$$

$$\frac{\partial W_{DS}}{\partial V_{GS}} = 0$$

$$\frac{\partial I_{EXP}}{\partial V_{BS}} = -\frac{\partial V_{th}}{\partial V_{BS}} \cdot \frac{I_{EXP}}{nV_T}$$

$$\frac{\partial I_{EXP}}{\partial V_{DS}} = \frac{I_{EXP}}{nV_T}\left(\eta_Z + \frac{\eta_L}{L}\right) + I_0 \frac{W}{L} W_{GS} \frac{WARG1}{V_T}$$

$$\frac{\partial I_{EXP}}{\partial V_{GS}} = \frac{I_{EXP}}{nV_T}$$

$$WARG2 = \frac{I_{LIM}}{I_{EXP} + I_{LIM}}$$

$$G_{M,T} = I_{DS}\left(- \frac{\left(U_{GSZ} + \frac{U_{GSL}}{L}\right)}{ARG1} + \frac{1}{ARG2} + \frac{1}{F_{S,triode}} \frac{\partial F_{S,triode}}{\partial V_{GS}} \right)$$

$$G_{DS,T} = I_{DS}\left(- \frac{\left(U_{GSZ} + \frac{U_{GSL}}{L}\right)\left(\eta_Z + \frac{\eta_L}{L}\right)}{ARG1} + \frac{\left(\eta_Z + \frac{\eta_L}{L}\right) - \frac{a}{2}}{ARG2} \right.$$

$$+ \frac{1}{V_{DS}} + \frac{1}{F_{S,triode}} \frac{\partial F_{S,triode}}{\partial V_{DS}} - \frac{1}{E_{CRIT} LARG3} \Bigg]$$

$$G_{MB,T} = I_{DS} \Bigg[- \frac{1}{ARG1} \Bigg[- \left[U_{GSZ} + \frac{U_{GSL}}{L} \right] \frac{\partial V_{th}}{\partial V_{BS}} + U_{BS} \Bigg]$$

$$- \frac{1}{ARG2} \left[\frac{\partial V_{th}}{\partial V_{BS}} + \frac{V_{DS}}{2} \frac{\partial a}{\partial V_{BS}} \right] + \frac{1}{F_{S,triode}} \frac{\partial F_{S,triode}}{\partial V_{BS}} \Bigg]$$

$$G_{M,S} = I_{DS} \Bigg[- \frac{\left[U_{GSZ} + \frac{U_{GSL}}{L} \right]}{ARG1} + \frac{2}{(V_{GS} - V_{th})}$$

$$- \frac{1}{K} \frac{\partial K}{\partial V_{GS}} + \frac{1}{F_{S,satn.}} \frac{\partial F_{S,satn.}}{\partial V_{GS}} \Bigg]$$

$$G_{DS,S} = I_{DS} \Bigg[- \frac{\left[U_{GSZ} + \frac{U_{GSL}}{L} \right] \left[\eta_Z + \frac{\eta_L}{L} \right]}{ARG1} + \frac{2 \left[\eta_Z + \frac{\eta_L}{L} \right]}{(V_{GS} - V_{th})}$$

$$- \frac{1}{K} \frac{\partial K}{\partial V_{DS}} + \frac{1}{F_{S,satn.}} \frac{\partial F_{S,satn.}}{\partial V_{DS}} \Bigg]$$

$$G_{MB,S} = I_{DS} \Bigg[- \frac{1}{ARG1} \Bigg[- \left[U_{GSZ} + \frac{U_{GSL}}{L} \right] \frac{\partial V_{th}}{\partial V_{BS}} + U_{BS} \Bigg]$$

$$- \frac{2}{(V_{GS} - V_{th})} \frac{\partial V_{th}}{\partial V_{BS}} - \frac{1}{K} \frac{\partial K}{\partial V_{BS}} - \frac{1}{a} \frac{\partial a}{\partial V_{BS}} + \frac{1}{F_{S,satn.}} \frac{\partial F_{S,satn.}}{\partial V_{BS}} \Bigg]$$

$$G_{M,W} = WARG2^2 \frac{I_{EXP}}{nV_T}$$

$$G_{DS,W} = WARG2^2 \left[\frac{I_{EXP}}{nV_T} \left(\eta_Z + \frac{\eta_L}{L} \right) + I_0 \frac{W}{L} W_{GS} \frac{WARG1}{V_T} \right]$$

$$G_{MB,W} = WARG2^2 \frac{I_{EXP}}{nV_T} \left(- \frac{\partial V_{th}}{\partial V_{BS}} \right)$$

APPENDIX F

Numerical Example

In order to relate the BSIM_plus model to hand calculations, the following numerical example is presented. Consider an NMOS transistor with W/L = 5 um/0.4 um where the p-type substrate has a bulk doping of N_B = 1.5 x 10^{16} cm^{-3}. The peak doping concentration near the oxide-semiconductor interface is N_A = 2 x 10^{17} cm^{-3} due to the channel implant. The total drain current is calculated for the following terminal voltage conditions: V_{GS} = 1.5 V, V_{DS} = 3 V, V_{BS} = -2 V. The fermi-level in the semiconductor near the oxide-semiconductor interface is calculated by,

$$\phi_F = V_T \ln\frac{N_A}{n_i} \tag{F.1}$$

$$= 0.026 \ln\frac{7 \times 10^{16}}{1.5 \times 10^{10}} = 0.4 \text{ V}.$$

where n_i = 1.5 x 10^{10} cm^{-3} is the intrinsic carrier concentration in silicon and V_T = 0.026 V is the thermal voltage at 300 K. Consider the gate material to be n-type silicon, with an impurity concentration of 10^{20} cm^{-3}. At this level of doping, the gate material is degenerate and the fermi level can be assumed to be -0.56 eV. The work function difference between the gate and the substrate is,

$$\phi_{MS} = \phi_{F(gate)} - \phi_{F(substr)} \tag{F.2}$$

$$= -0.56 - 0.4 = -0.96 \text{ V}.$$

Consider also that the interface charge density at the oxide-semiconductor interface, Q_o = 0.1 fC/um^2. Let the oxide thickness for this technology be 12 nm. The gate-oxide capacitance, C_{OX}, is calculated as,

$$C_{OX} = \frac{\varepsilon_{ox}}{T_{OX}} \tag{F.3}$$

$$= \frac{3.9 \times 8.86 \times 10^{-14}}{12 \times 10^{-7}} = 287 \text{ nF/cm}^{-3}.$$

The flat-band voltage, V_{FB}, is calculated by,

$$V_{FB} = \phi_{MS} - \frac{Q_o}{C_{OX}} \tag{F.4}$$

$$= -0.96 - \frac{0.1}{2.87} = -1 \text{ V}.$$

The surface inversion potential is calculated by,

$$\phi_s = 2\phi_F = 0.8 \text{ V}. \tag{F.5}$$

The zero-bias body-effect coefficient, γ_1 is calculated by,

$$\gamma 1 = \frac{1}{C_{OX}}\sqrt{2q\varepsilon_{Si}N_A} \tag{F.6}$$

$$= \frac{1}{287 \times 10^{-9}}\sqrt{2 \times 1.6 \times 10^{-19} \times 11.6 \times 8.86 \times 10^{-14} \times 2 \times 10^{17}}$$

$$= 0.89 \sqrt{\text{V}}.$$

The high-bias body-effect coefficent, γ_2 is calculated by,

$$\gamma_2 = \frac{1}{C_{OX}}\sqrt{2q\varepsilon_{Si}N_B} \tag{F.7}$$

$$= \frac{1}{287 \times 10^{-9}} \sqrt{2 \times 1.6 \times 10^{-19} \times 11.6 \times 8.86 \times 10^{-14} \times 1.5 \times 10^{16}}$$

$$= 0.24 \sqrt{V}.$$

If the depletion charge-sharing coefficient, $K_S = 0.48$, the transition substrate voltage, V_{BST}, can be calculated as,

$$V_{BST} = \phi_s - \left[\frac{\gamma_1 - \gamma_2}{K_S} + \sqrt{\phi_s}\right] \tag{F.8}$$

$$= 0.8 - \left[\frac{0.89 - 0.24}{0.48} + \sqrt{0.8}\right]^2 = -5.1 \text{ V}.$$

The threshold voltage of the transistor can now be calculated. Since $V_{BS} < V_{BST}$, the threshold voltage is calculated as,

$$V_{th} = V_{FB} + \phi_s + \gamma_1(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s}) - \frac{K_S}{2}(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s})^2$$

$$+ \frac{K_{NZ}}{W} + \frac{K_{NB}V_{BS}}{W} - \left[\eta_Z + \frac{\eta_L}{L}\right]V_{DS} \tag{F.9}$$

$$= -1 + 0.8 + 0.89(\sqrt{2.8} - \sqrt{0.8}) - \frac{0.48}{2}(\sqrt{2.8} - \sqrt{0.8})^2$$

$$+ \frac{0.1}{5} - \frac{0.02 \times 2}{5} - \left[0.003 + \frac{0.001}{0.4}\right] \cdot 3.$$

$$= 0.34 \text{ V}.$$

Model parameter values $\eta_Z = 0.003$ and $\eta_L = 0.001$ um were assumed in this calculation. The saturation voltage is calculated by,

$$V_{DSAT} = \frac{V_{GS} - V_{th}}{a\sqrt{K}}, \tag{F.10}$$

where,

$$g = 1 - \frac{1}{1.744 + 0.8364\ (\phi_s - V_{BS})} \tag{F.11}$$

$$= 1 - \frac{1}{1.744 + 0.8364 \times 2.8} = 0.755,$$

$$a = 1 + \frac{g \cdot \gamma_1}{2\sqrt{\phi_s - V_{BS}}} \tag{F.12}$$

$$1 + \frac{0.755 \times 0.93}{2\sqrt{2.8}} = 1.21,$$

$$v_c = \frac{V_{GS} - V_{th}}{a \cdot E_{CRIT} \cdot L} \tag{F.13}$$

$$= \frac{1.5 - 0.34}{1.21 \times 3.6 \times 0.4} = 0.66,$$

and,

$$K = \frac{1 + v_c + \sqrt{1 + 2v_c}}{2} \tag{F.14}$$

$$= \frac{1 + 0.66 + \sqrt{1 + 2 \times 0.66}}{2} = 1.59.$$

From these calculations, the saturation voltage is,

$$V_{DSAT} = \frac{1.5 - 0.34}{1.21 \times \sqrt{1.59}} = 0.76\ V. \tag{F.15}$$

Since $V_{DS} > V_{DSAT}$, the transistor is operating in the saturation region. The

output conductance smoothing factor is calculated as,

$$F_{S,satn.} = 1 + H_0 \cdot \left[1 - e^{\frac{V_{DSAT} - V_{DS}}{H_1}}\right] \tag{F.16}$$

$$= 1 + 0.05\left[1 - e^{\frac{0.76 - 3}{1.8}}\right] = 1.036,$$

where the model parameters H_0 and H_1 are 0.05 and 1.8 V, respectively. The strong-inversion drain current is calculated as,

$$I_{DS,satn.} = \frac{\mu_0 C_{OX} \frac{W}{L} (V_{GS} - V_{th})^2 F_{S,satn.}}{\left[1 + \left[U_{GSZ} + \frac{U_{GSL}}{L}\right](V_{GS} - V_{th}) - U_{BS} V_{BS}\right] 2aK} \tag{F.17}$$

$$= \frac{580 \times 287 \times 10^{-9} \times \frac{5}{0.4}(1.5 - 0.34)^2 \times 1.036}{\left[1 + \left[0.3 + \frac{0.1}{0.4}\right](1.5 - 0.34) + 0.05 \times 2\right] 2 \times 1.21 \times 1.59}$$

$$= 433\ \mu A.$$

Since the transistor is operating in the strong-inversion region, the weak-inversion component of the drain current is clamped at I_0 which is of the order of several tens of nano-Amperes. Hence the total drain current which is calculated by adding the strong-inversion and weak-inversion components is 433 μA.

APPENDIX G

List of Publications

G.1 Journal Publications

[1] **S. M. Gowda**, B. J. Sheu, J. Choi, C.-G. Hwang, J. S. Cable, "Design and characterization of analog VLSI neural network modules," *to appear in IEEE Jour. of Solid-State Circuits*, Mar. 1993.

[2] **S. M. Gowda**, B. J. Sheu, "Explicit geometry dependence of MOS transistor parameters by the pseudo-boundary method," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 2, no. 2, pp. 105-115, Kluwer Academic Publishers: Boston, MA, Apr. 1992.

[3] W.-J. Hsu, B. J. Sheu, **S. M. Gowda**, C.-G. Hwang, "Advanced integrated-circuit reliability simulation including dynamic stress effects," *IEEE Jour. of Solid-State Circuits*, vol. 27, no. 3, pp. 247-257, Mar. 1992.

[4] W.-J. Hsu, B. J. Sheu, **S. M. Gowda**, "Integrated-circuit reliability simulation with emphasis on hot-carrier effects," *Jour. of Analog Integrated Circuits and Signal Processing*, vol. 1, no. 3, pp. 231-245, Kluwer Academic Publishers, Nov. 1991.

[5] W.-J. Hsu, B. J. Sheu, **S. M. Gowda**, "Design of reliable VLSI circuits using simulation techniques," *IEEE Jour. of Solid-State Circuits*, vol. 26, no. 3, pp. 452-457, Mar. 1991.

G.2 Conference Publications

[1] **S. M. Gowda**, B. J. Sheu, J. Choi, "Testing of programmable analog neural network processors," *Proc. of IEEE Custom Integrated Circuits Conf.*, pp. 17.1.1-4, Boston, MA, May 1992.

[2] W.-J. Hsu, B. J. Sheu, **S. M. Gowda**, "Testing of analog neural array-processor chips," *Proc. of IEEE Int'l. Conf. on Computer Design*, pp. 118-121, Cambridge, MA, Oct. 1991.

[3] **S. M. Gowda**, B. J. Sheu, J. S. Cable, "An accurate MOS transistor model for sub-micron VLSI circuits - BSIM_plus," *Proc. of IEEE Custom Integrated Circuits Conf.*, pp. 23.2.1-4, San Diego, CA, May 1991.

[4] W.-J. Hsu, **S. M. Gowda**, B. J. Sheu, C.-G. Hwang, "Integrated-circuit reliability simulation including dynamic stress effects," *Proc. of IEEE Custom Integrated Circuits Conf.*, pp. 4.2.1-4, San Diego, CA, May 1991.

[5] J. Choi, B. J. Sheu, **S. M. Gowda**, "Analog VLSI neural network implementations of hardware annealing and winner-take-all functions," *Proc. of 34th Midwest Symp. of Circuits and Systems*, pp. 344-347, Monterey, CA, May 1991.

[6] W.-J. Hsu, **S. M. Gowda**, B. J. Sheu, "VLSI circuit design with built-in reliability using simulation techniques," *Proc. of IEEE Custom Integrated Circuits Conf.*, pp. 19.3.1-19.3.4, Boston, MA, May 1990.

[7] **S. M. Gowda**, B. W. Lee, B. J. Sheu, "An improved neural network approach to the traveling salesman problem," *Proc. of IEEE Region 10 Int'l. Conf.*, pp. 552-555, Bombay, India, Nov. 1989.

[8] J.-C. Lee, **S. M. Gowda**, B. J. Sheu, "Fully automated layout generators for high-performance analog VLSI modules," *Proc. of IEEE Region 10 Int'l. Conf.*, pp. 893-896, Bombay, India, Nov. 1989.

G.3 Technical Reports

[1] Annual reports to TRW Electronic Systems Group, Redondo Beach, CA, *Deep-Submicron MOS Device Studies for Advanced Integrated-Circuit Design*, Mar. 1989 - Oct. 1992, (with Prof. B. J. Sheu).

[2] Quarterly reports to Samsung Electronics Co., Korea, *An Advanced Reliability Simulator and Device Models for Submicron CMOS Integrated Circuits*, Jan. 1990 - Dec. 1992, (with Prof. B. J. Sheu).

[3] Project report to Alameda Engineering Inc., Pasadena, CA, *Design of the 4-th Order Sigma-Delta Analog-to-Digital Converter with 16-bit Resolution*, Jan. 1990 - Aug. 1991, (with Prof. B. J. Sheu, J. Choi).