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A Deep Submicron Drain-Current and Charge Model for MOS Transistors

by

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Abstract

A unified short-channel Metal-oxide-semiconductor (S-CMOS) transistor model has been developed for design and simulation of deep-submicron mixed-signal very large-scale integration (VLSI) circuits for high-speed computing, high-frequency communication, and multimedia applications. Unified expressions for drain current, conductances, terminal charge, and capacitances are derived with the assistance of three smooth functions including hyperbola, exponential interpolation, and sigmoid functions, which provide excellent transitions between different regions of operation. A compact set of 35 parameters is used to characterize transistor behavior. Effects of non-uniform substrate doping, drain-induced-barrier-lowering, narrow-channel and reverse short-channel are included in the threshold voltage expression. Mobility reduction due to lateral and vertical electrical fields is modeled by including the second-order term to provide high accuracy for deep-submicron transistors. The charge/capacitance model uses an accurate formulation for back-gate degradation coefficient to model the channel charge density. The unified expressions of charge densities are derived which are valid for all operation regions including the accumulation region. Different channel-charge partitioning schemes, including 40/60, 0/100, and 50/50, are provided to have better usage of the model in various applications. Parameter extraction of S-CMOS model is based on physical meaning of each model parameter, and is implemented by using MATLAB program. Both the local determination and global optimization strategies are combined to increase the extraction accuracy and reduce computation time. The S-CMOS model is implemented in a modified version of the popular SPICE-3f3 circuit simulator from University of California, Berkeley. Simulation results of mixed-signal circuits including domino logic gate, folded-cascode operational amplifier, analog comparator, wide-range Gilbert multiplier, and DRAM circuit are presented. Comparison of simulated results and

measured data of transistors demonstrate the accuracy of the S-CMOS model and its strong capability in the deep-submicron technologies. In the appendix, research work on modeling MOS transistors for use up to 10 GHz is described with careful comparison of measured and simulation results.

Chapter 1

Introduction

Very large-scale integration (VLSI) circuits fabricated by metal-oxide-semiconductor (MOS) technologies are widely used in microelectronics industry to implement high-performance computing, signal processing, multimedia, and telecommunication systems [1]. The emergence of complementary MOS (CMOS) as the main-stream fabrication technology over the past decade has been accompanied by a reduction in feature size from longer than 2.0 μm to about 0.15 μm [2], an increase in chip area from 50 mm^2 to 300 mm^2, and an increase in the number of transistors from 100,000 to 1 billion for memories and from 50,000 to over 7 million in microprocessors [3], a drop in the on-chip gate delay from 1 neno-second to 5 pico-second, and an increase in the chip clock frequency from 10 MHz to over 1 GHz [2]. Figure 1.1 shows the trend of the advanced CMOS technologies.

In the competitive industrial and scientific environment, efficient design automation is invaluable in ensuring that high-quality products are developed within a short period of time. In such an environment, circuit and system designs can take place simultaneously with continuous technology improvement. This requires a closer relationship in the vertical direction from the device-level simulation through the circuit design to the system-level simulation. In recent years, concurrent engineering has been replacing traditional isolated design and manufacture philosophy.

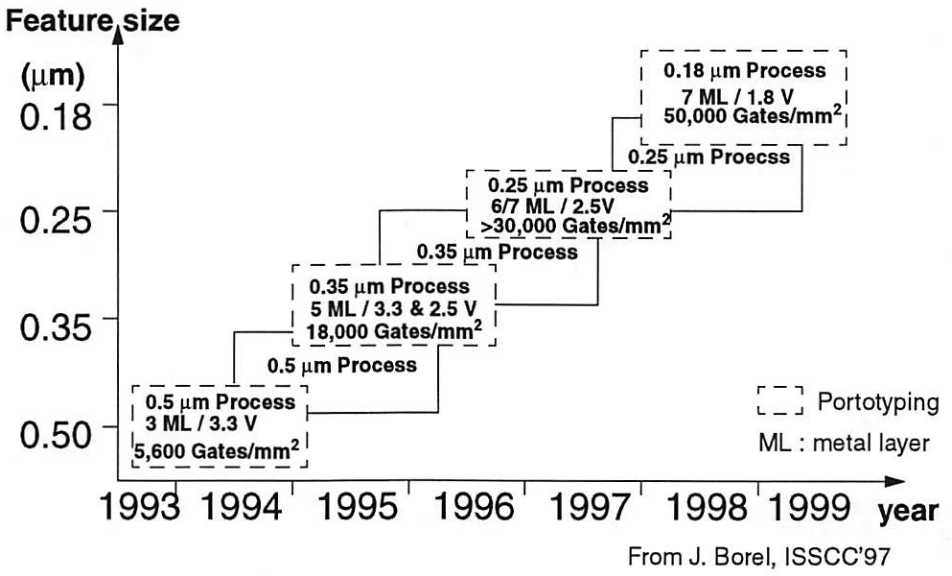
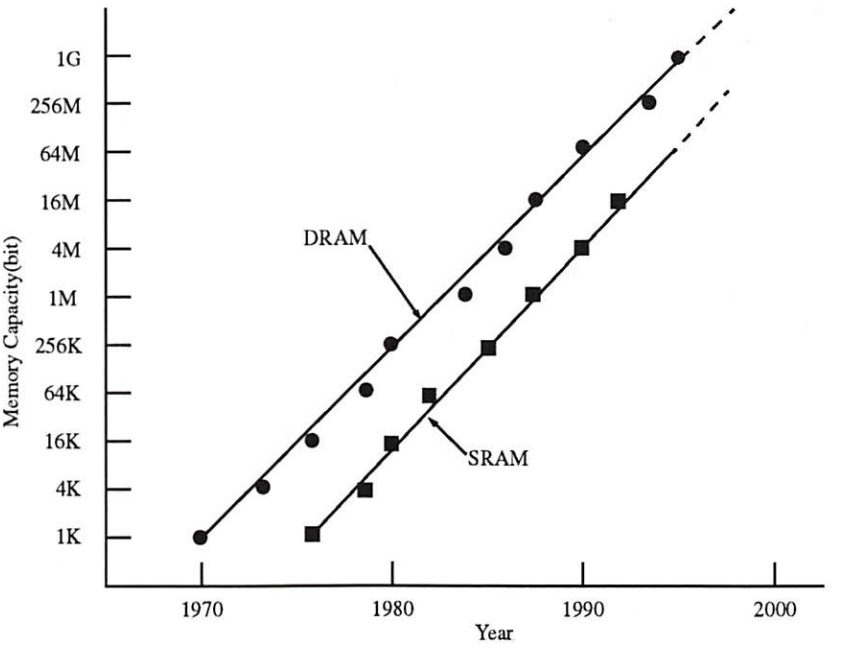


Figure 1.1: The advanced VLSI CMOS technologies trend [4].

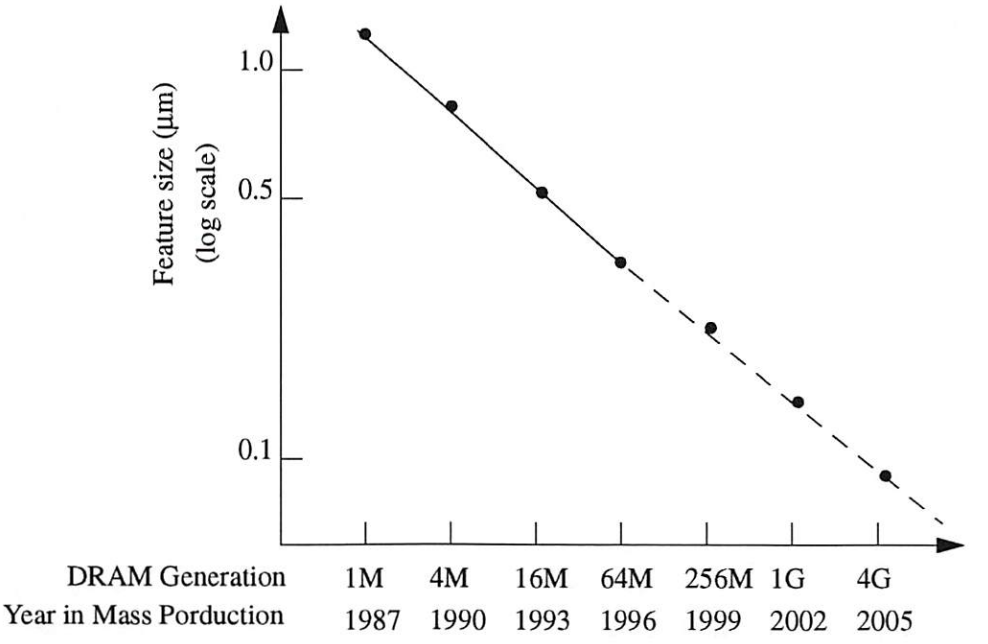
1.1 Deep-Submicron VLSI Technology

Fabrication technologies have progressed rapidly and the minimum feature sizes used in industrial processes have shrunk from 2 μm in the early 1980s to about 0.25 μm in 1998. The level of circuit integration on a single chip has been greatly increased by new lithography and etching techniques. The evolution of silicon integrated-circuit technologies used in the fabrication of semiconductor memories over the past decade and projected future direction are shown in Fig. 1.2 [5].

The increased use of deep-submicron technologies has created new challenges for researchers in mixed-signal VLSI hardware design, high-performance circuit simulation, and microelectronics system design. At the transistor level, detailed investigation of small-geometry effects on the behavior of transistors is required. Effects of coupling between interconnections and neighboring devices can be more significant due to compactness of the circuit [7]. The degradation of device behavior with time



(a)



(b)

Figure 1.2: Advances in fabrication technologies used for mass-production of CMOS memories.

of operation can be more significant due to higher electrical stresses in the channel region of MOS transistors. The signal coupling to the substrate of the device becomes more significant for deep-submicron transistors operating at high frequency [6]. At the circuit level, accurate modeling of transistors is urgently needed so that special features of advanced technologies can be exploited to the greatest extent. Desirable features of the analytical model include a compact set of parameters, continuity of the drain current and its derivatives across different regions of operation, and the ability to use a single parameter set over a large geometric design space. At the system level, new architectures are created in order to utilize advanced technologies effectively and extend boundaries of achievable performance. Advanced computer architectures are likely to use superpipelined configuration with distributed memories and multi-layer interconnections. Nowadays, the integrated media systems combine all the advanced audio/video, telecommunication, and memories technologies to support the high density personal multimedia communicators. Simultaneous efforts at the device, circuit and system levels are essential in order to achieve the demanded high-performance computing and communication [8].

1.2 Mixed-Signal VLSI Design Environment

A flowchart of mixed-signal VLSI circuit and system design is shown in Fig. 1.3. Application is the first and most important item to be determined, e.g. multimedia, telecommunication, microprocessor, network server, etc.. It provides overall guidance to major aspects of the VLSI design. Next, the design methodology and algorithm should be determined to optimize the design cost and expected performance. At the circuit implementation stage, simulation and verification are needed for each step to ensure the correctness of the functions and proper operation. In

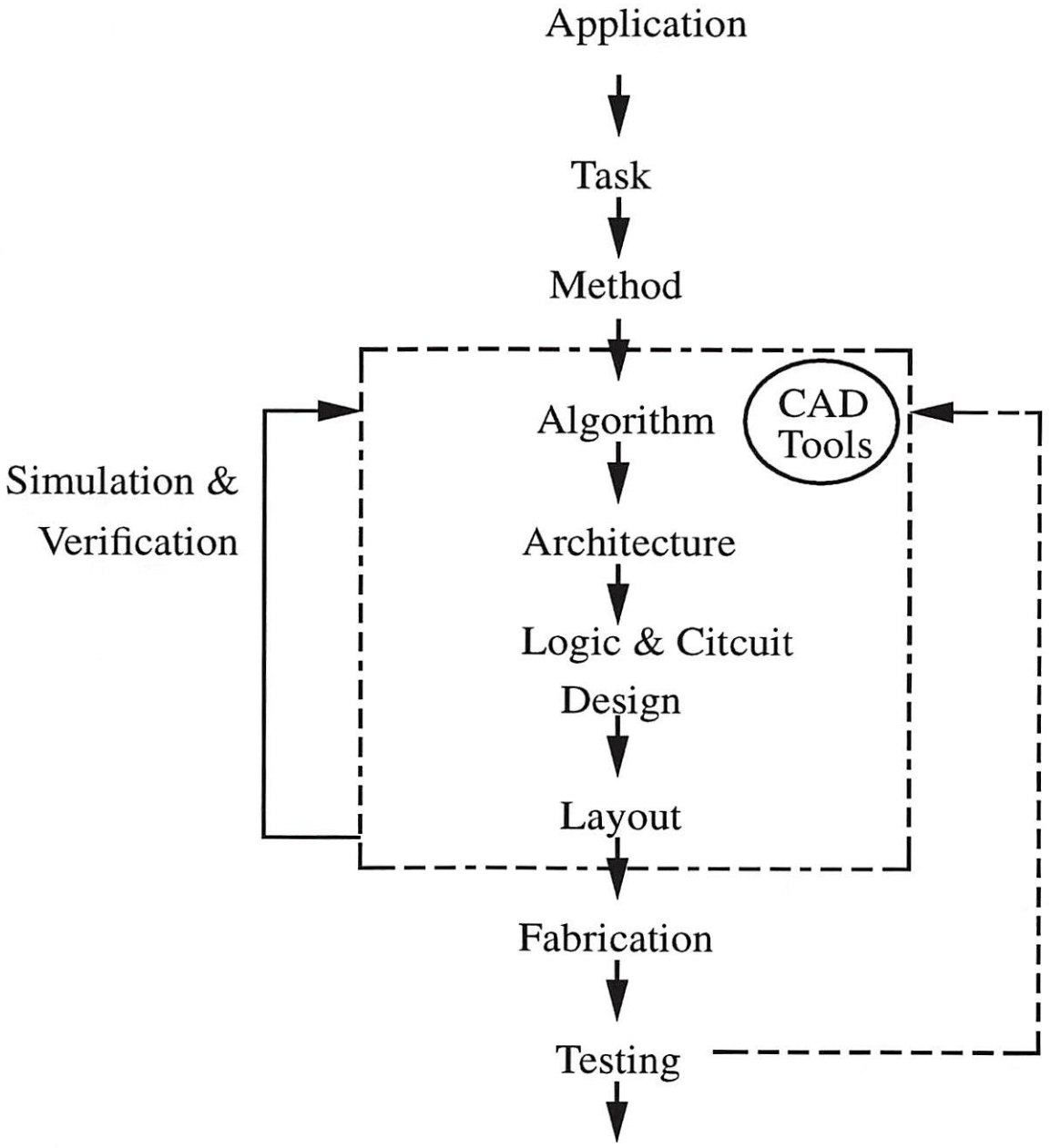


Figure 1.3: Flowchart of VLSI system-perspective design steps.

order to achieve new generation of VLSI design which involves a very complex design procedure, the advanced computer-aided design (CAD) tools are required. Fig. 1.4 shows key components of an advanced VLSI design environment. In the design and synthesis portion, the CAD tools for the digital domain are fairly well developed; however the design automation of the analog sections often remains a significant bottleneck. To increase the efficiency of the design process, and reduce the design time for the mixed-signal VLSI, the analog circuit CAD should be paid more attention. The core of circuit-level simulation environment contains circuit simulators such as SPICE from University of California, Berkeley [11], which use analytical models of discrete devices such as transistors to describe the detailed electrical behavior of analog and digital circuits. The model expressions describe the terminal voltage and current waveforms of devices based on the model parameters and biasing conditions. Several commercial circuit simulators are based upon the SPICE program including HSPICE from Avant! Corp. [12] and PSPICE from Microsim Corp. [13]. At the highest level of abstraction in the simulation environment, logic and timing simulators rely on behavioral models of the circuit to determine the functionality and speed performance of electronic sub-systems or systems. Behavioral models can be constructed from simulated data obtained by detailed circuit simulation. The circuit simulator at the core of the VLSI simulation environment and the individual device models that it contains are extremely important. Results from the circuit simulator affect crucial decisions that are made during architectural specification, and circuit design. Accurate and efficient MOS transistor models are key elements of such VLSI simulation environments.

The previous work on MOS transistor modeling is reviewed in Chapter 2. Existing publications in this area have been surveyed and significant results are described. Advanced deep-submicron modeling techniques that are used in the development of

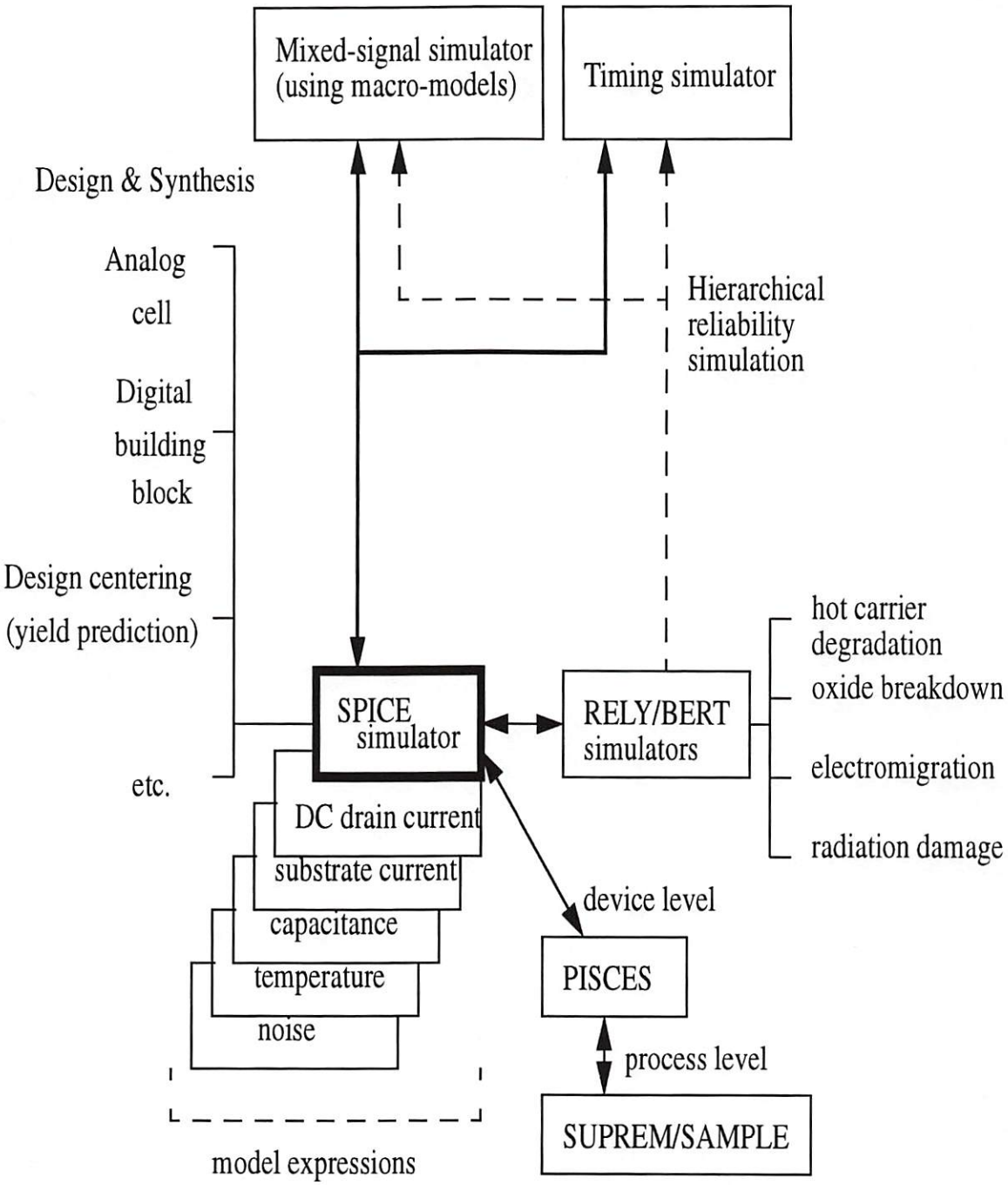


Figure 1.4: An advanced VLSI simulation environment.

the unified short-channel MOS transistor (S-CMOS) model are described in Chapter 3. A detailed description of S-CMOS model including the drain current expression and terminal charge expressions are presented in this chapter. Issues related to parameter extraction and a new approach to extract the S-CMOS model parameter values are described in Chapter 4. Implementation of the extraction program of S-CMOS model using MATLAB software is also described. In Chapter 5, the implementation of S-CMOS model in SPICE-3f3s circuit simulator is described. SPICE simulations of several selected digital and analog circuits using S-CMOS model are also included in this chapter. The contribution of this research to the scientific knowledge in the fields of mixed-signal VLSI circuit design is summarized in Chapter 6. A discussion of future directions is also included.

Reference List

[1] B. Sheu, M. Ismail, E. Sanchez-Sinencio, T. Wu, *Microsystems Technology for Multimedia Applications: An Introduction*, IEEE Press: Piscataway, NJ, 1995.

[2] J. Silberman, *et al.*, "A 1.0 GHz single-issue 64b PowerPC integer processor," *IEEE ISSCC 1998*, pp. 230-231, Feb. 1998.

[3] J. Schutz, R. Wallace, "A 450MHz IA32 P6 family microprocessor," *IEEE ISSCC 1998*, pp. 236-237, Feb. 1998.

[4] J. Borel, "Technologies for multimedia systems on a chip," *IEEE ISSCC 1997*, pp. 18-21, Feb. 1997.

[5] Y. Oshima, B. Sheu, S. Jen, Memory Architectures Technology for Multimedia Systems, Chapter 4 in *Multimedia Technology for Applications*, Editors: B. Sheu, M. Ismail, IEEE Press: New York, NY, 1998.

[6] W. Liu, *et al.* "R.F. MOSFET modeling accounting for distributed substrate and channel resistances with emphasis on the BSIM3v3 SPICE model," *IEEE IEDM Digest*, pp. 309-312, Dec. 1997.

[7] S.-Y. Oh, K.-J. Chang, K. Lee, "Interconnect modeling and design in high-speed VLSI/ULSI systems," *Proc. of IEEE Custom Integrated Circuits Conf.*, pp. 9.4.1-4, Boston, MA, May 1992.

[8] Committee on Physical, Mathematical and Engineering Sciences, "Grand challenges: high-performance computing and communications, The FY 1992 U.S. Research and Development Program," *National Science Foundation,* Washington, D.C., 1991.

[9] D. A. Antoniadis, S. E. Hansen, R. W. Dutton, *SUPREM-II: A Program for IC Process Modeling and Simulation,* Tech. Report, Stanford Electronics Lab., Stanford University, Oct. 1979.

[10] M. R. Pinto, C. Rafferty, R. W. Dutton, *PISCES-II: Poisson Continuity Equation Solver,* Tech. Report, Stanford Electronics Lab., Stanford University, 1984.

[11] B. Johnson, T. Quarles, A. R. Newton, D. O. Pederson, A. Sangiovanni-Vincentelli, *SPICE-3E1 User's Guide,* Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, Apr. 1991.

[12] *HSPICE User manual*, Avant! Corp., Fremont, CA, Mar. 1998.

[13] *PSPICE User's manual*, Microsim Corp., Irvine, CA, Jan. 1997.

[14] R. A. Saleh, A. R. Newton, *SPLICE User's Guide*, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA, 1986.

[15] R. Saleh, A. R. Newton, *Mixed-Mode Simulation*, Kluwer Academic Publishers: Boston, MA, 1990.

[16] J. White, A. Sangiovanni-Vincentelli, "RELAX2: A new waveform relaxation approach for the analysis of LSI MOS circuits," *Proc. of IEEE Int'l Symp. on Circuits and Systems*, pp. 756-759, Newport Beach, CA, May 1983.

[17] L. T. Pillage, R. A. Rohrer, "Asymtotic waveform evaluation for timing analysis," *IEEE Trans. on Computer-Aided Design,* vol. 9, no. 4, pp. 352-366, Apr. 1990.

[18] B. J. Sheu, W.-J. Hsu, B. W. Lee, "An integrated-circuit reliability circuit simulator - RELY," *IEEE J. of Solid-State Circuits,* vol. 24, no. 2, pp. 473-477, Apr. 1989.

[19] R. H. Tu, E. Rosenbaum, C. C. Li, W. Y. Chan, P. M. Lee, B.-K. Liew, J. D. Burnett, P. K. Ko, C. Hu, *BERT - Berkeley Reliability Tools*, University of California, Berkeley, CA, Feb. 1992.

Chapter 2

MOS Transistor Modeling for Circuit Simulation

Rapid advances in CMOS fabrication technologies have enabled the use of sub-half-micron devices to build high-speed VLSI circuits. The evolution of fabrication technologies has fueled the demand on research to further improve the MOS transistor models that are used by designers to simulate the circuits before fabrication. Three major criteria can be used to evaluate MOS transistor models for circuit simulation and circuit design:

- accuracy of simulation results,
- computational efficiency, and
- convenience of the model to circuit designers.

The accuracy of circuit simulation results depends upon the ability of the model and the associated parameter set to simulated transistor characteristics including drain current, conductances, terminal charges and internodal capacitances over useful ranges of terminal voltages and transistor geometries that are used in the circuits. There is usually a balance between the accuracy and computational efficiency of a model, and clever handling of such a balance is an important engineering challenge. The usefulness of a device model to circuit designers depends upon several factors

including the number of parameters, the different effects and features that are incorporated into the model, and how well the accuracy/efficiency balance is achieved.

Significant results were reported over the past two decades from research on MOS transistor modeling. The tremendous advance achieved in improving the performance of these devices demands corresponding amount of efforts and progress in modeling their behavior. Three main categories of MOS transistor modeling research include:

- type-1: investigation and modeling of specific important aspects of transistor behavior including threshold voltage, mobility, saturation velocity, and subthreshold conduction;

- type-2: development of highly accurate and computationally complex transistor drain current models that include many second-order and higher-order effects which are useful to device engineers; and

- type-3: development of accurate and computationally efficient transistor models with compact parameter sets that closely address the needs of VLSI circuit designers.

Study into detailed physical phenomena inside the semiconductor device contributes significantly to understanding of physics of the device and the ability to describe these phenomena. Such research has resulted in a large volume of knowledge about semiconductor devices that is very useful in understanding MOS transistor operation and in the design and development of new devices [1-4].

Several analytical models have been proposed in the literature to provide circuit designers with the capability to describe behavior of circuit building blocks over the entire design space [5-19]. For historical reasons, it is useful to classify the

existing SPICE MOSFET models into three evolutionary generations [20]. The first-generation models were based on the simple intention of physically-based analytical expressions, with all simple geometry dependence included in the model equations. These models concentrate on the description of the MOS transistor rather than the behavior of the model equations in a circuit simulator. This generation of models is comprised of Level-1, Level-2, and Level-3.

The second-generation models represented a major change from the philosophy for the first-generation ones. In this set of models, analytical equations are subject to extensive mathematical conditioning, with a clear focus on the circuit simulation usage. The parameter structure is twofold; there are individual device parameters, and there are also geometry-related (length and width) parameters. The model structure and its parameters take on considerable empirical character. This has the effect of shifting the challenge in the model to parameter extraction, which is imposed on a rather systematic formulation. This generation of models encompasses BSIM and BSIM2, along with HSPICE Level-28 which is based on BSIM.

More recently, third-generation models started to emerge. The fundamental intent is to return to a simple model structure, possibly with a reduced number of parameters. These parameters are strongly physically-based, rather than being very empirical. Mathematical conditioning is also important in these models. However, in contrast to the polynomial functions which are heavily used in the second-generation models, the third-generation models employ more specialized smoothing functions which are mathematically well behaved. With the use of smoothing functions, the analytical equations for drain current and terminal charge and their derivatives are continuous and smooth. A single equation can be used for all regions of transistor operation.

2.1 First-Generation MOS Transistor Models

The first-generation MOS transistor models were based on simple description of the device. The main focus is on the analytical description of the MOS transistor.

2.1.1 The Level-1 Model

The Level-1 MOS model is a first-order model that is useful for hand calculations when designing and analyzing new circuits. Simple expressions are used to describe the drain current characteristics. The Level-1 model applies well to large devices. The only geometry dependency is the inclusion of a simple λ-expression for channel length modulation. Also, there is no subthreshold conduction expression included.

2.1.2 The Level-2 Model

The Level-2 MOS model, reported by Vladimirescu and Liu [5], requires 18 parameters and includes many second-order effects suitable for in devices with channel length down to 1.2 μm. The threshold voltage expression in the Level-2 MOS model included the substrate-bias and narrow-channel effects. The body-effect coefficient due to the depletion charge at the drain and source terminals was modified by correction factors. A single parameter with inverse width dependence is used to model the drain-included barrier-lowering effect as well as the narrow-channel effect on the depletion charge-sharing coefficient. The channel length reduction was calculated from a complex expression that included the depletion layer width, the carrier mobility at the semiconductor surface, and the maximum carrier drift velocity at velocity saturation. The transition point between the weak and strong inversion regions was defined to be above the threshold voltage by a multiple of the thermal voltage value. A complex expression modeled the drain current in the weak-inversion region as an

exponential function of the gate terminal voltage and the transition voltage. Continuity of drain current expressions was achieved at the transition point between weak and strong inversion. However, continuity of the first-order derivative of the drain current expressions was not achieved at this transition point.

2.1.3 The Level-3 Model

The Level-3 MOS model, which was also reported by Vladimirescu and Liu [5], is a semi-empirical model and can be used for technologies with feature sizes down to 1.0 μm. The Level-3 model requires 18 parameters in the drain-current expressions that were mainly based on the curve fitting approach. The model took into account the two-dimensional nature of the potential distribution in the channel region. Geometrically dependent effects were included to a limited extent in order to increase the accuracy of the model for technologies below 1.5 μm.

The threshold voltage in the Level-3 MOS model was calculated from the flat-band voltage and the surface inversion potential, and included the drain-induced barrier-lowering effect and the non-uniform substrate-doping effect. The drain-induced barrier-lowering effect was modeled with an inverse dependency on the cubed channel length. The non-uniform substrate doping effect included correction terms for the short-channel and narrow-channel effects.

The surface carrier mobility was calculated from the intrinsic mobility in the channel region and an empirical fitting parameter. The effect of the vertical field on the intrinsic carrier mobility was modeled as a function of the gate voltage. The effective mobility also included the velocity saturation effect that was dependent upon the horizontal field in the channel and was calculated using the maximum carrier drift velocity parameter. The amount of channel-length reduction was calculated

from the lateral electric field at the channel pinch-off point. The coefficient of depletion layer width which was calculated from the substrate doping concentration, and an empirical fitting parameter, was also used to determine the amount of channel-length reduction. The drain-current expression included a Taylor series expansion coefficient of bulk charge and the transconductance coefficient. The saturation voltage was defined as the drain voltage at which the carrier velocity approached the value of the maximum carrier drift velocity parameter. If this parameter was not given, the saturation voltage was determined from the maximum of the drain-current equation. The weak-inversion drain current expression was similar to that used in the Level-2 MOS model.

The Level-3 MOS model used a compact set of parameters. This was convenient for circuit designers who used the model, and also eased the parameter extraction task in which device engineers characterized the technology in terms of the model parameters. Since many model parameters were empirical, integration of the circuit simulator with device-level simulators that solve Poisson equations is quite difficult. Such integration includes determining the transistor parameter values from electronic quantities that are predicted by the device-level simulators. Empirical parameters are usually extracted to fit a limited voltage range or geometric space, while circuit designers could require simulations over a large voltage range and extensive geometric design space. The use of a square-root dependence on $(V_{DS} - V_{DSAT})$ in the channel length modulation expression could cause discontinuity in derivatives of the drain-current expressions at the triode/saturation transition point. Such discontinuity could lead to non-convergence problems in the circuit simulation.

2.2 The Second-Generation MOS Transistor Models

In the second-generation models, the device geometry is excluded in the basic model equations. In addition, an entirely separate parameter group is used solely to describe the geometry dependence. Independent parameters are extracted for each device. Then the geometry parameters are extracted to fit initial set of independent parameters across the length and width. The goal is to provide an apparatus in which the original independent device parameters can be reconstituted for any particular choice of channel length and width.

2.2.1 The BSIM Model

The BSIM transistor model was the first of the second-generation models. It was a circuit-level MOS model with strong device physics emphasis which can accurately describe drain-current characteristics of transistors with channel lengths down to about 0.8 μm [7]. The model used a total of 62 parameters in the drain-current expression. There were 24 electrical parameters, of which 19 were calculated from nominal, inverse-length and inverse-width coefficients. The simple framework of geometry dependence was a salient feature of the BSIM model. The parameter values were calculated by,

$$P = P_0 + \frac{P_L}{L} + \frac{P_W}{W} \tag{2.1}$$

Where P_0, P_L, and P_W were the nominal value, length-dependence coefficient and width-dependence coefficient of the parameter P, respectively.

The threshold voltage expression in the BSIM model included the effect of non-uniform substrate doping on the depletion charge term. The effect of extra bulk charge at the edge of narrow transistor channels was not explicitly modeled in the

threshold voltage expression. The drain-induced barrier-lowering coefficient was calculated using zero-bias, substrate-voltage and drain-voltage dependence parameters, each of which has geometry dependency. The reduction of carrier mobility in the triode region due to vertical and horizontal electric fields was modeled by terms that were dependent upon the drain and gate voltages. The vertical field effect included only the gate voltage contribution explicitly. A second-order dependence upon the substrate voltage was included in the parameter that was used to model the vertical field effect. The parameter that describes the horizontal field effects was dependent upon the substrate and drain voltages. The drain-current expression in the saturation region included a body-effect coefficient term and a carrier saturation-velocity term. The drain current and its first-order derivatives were continuous at the transition between the triode and saturation regions.

The subthreshold conduction expression in the BSIM model was dominated by the diffusion current component. The diffusion component of the subthreshold current was modeled by using an exponential dependence on the gate and drain terminal voltages. The subthreshold current was limited in the strong-inversion region by clamping. The total drain current in all regions of transistor operations was expressed as the sum of weak-inversion and strong-inversion drain current components.

The simple geometric dependence framework included in the BSIM model was intended to increase accuracy of the model over a large geometric range. However, the number of parameters that are to be extracted is quite large. As a result, only a small geometric region can be accurately characterized. Simulation of transistors beyond this characterized region can result in abnormal simulation results. The technique used to model the non-uniform substrate doping effect can cause non-monotonic threshold voltage variation at high substrate voltages, resulting in simulation non-convergence problems. This happens because the terminal voltage

during intermediate circuit simulation iterations sometimes take very high values beyond the power supply rails of the circuit. The drain current and the first-order derivatives are continuous at the triode/saturation transition and this is critical for circuit simulation purpose. However, the second derivative of the drain current is not continuous, resulting in poor output conductance behavior at the triode/saturation transition and in the saturation region.

2.2.2 HSPICE Level-28 Model

HSPICE Level-28 model [21] is a proprietary model which has used HSPICE as a vehicle to gain rather widespread acceptance. The model structure is based on BSIM, but has been extensively enhanced. Through extensive mathematical conditioning, HSPICE Level-28 has been made suitable for analog design. It is thus commonly employed in the IC industry.

A unique feature of HSPICE Level-28 model is that the model structure is designed to accommodate model binning. Additional terms are introduced to provide the continuity of the model parameters at all four corners of a bin,

$$P = P_0 + P_L \cdot (\frac{1}{L} - \frac{1}{L_{ref}}) + P_W \cdot (\frac{1}{W} - \frac{1}{W_{ref}}) + P_P \cdot (\frac{1}{L} - \frac{1}{L_{ref}}) \cdot (\frac{1}{W} - \frac{1}{W_{ref}}) \quad (2.2)$$

In its structure, HSPICE Level-28 model conditions the quadratic expressions which appear in BSIM, so that they become less troublesome. The drain-current expression contains very extensive conditioning of the various transition points. This foreshadows the structure of the third-generation models, and has led to very successful results. The saturation voltage model defines a transition region in addition to the normal use of the linear region and the saturation region, which produces good results. A similar conditioning approach is used on the subthreshold model, where

several subregions are defined. In particular, the problems introduced in BSIM by the simple addition of the weak inversion current to the strong inversion current are eliminated.

HSPICE Level-28 model maintains the clear focus of the second-generation models on the circuit design purpose. However, the model parameter set is very empirical. In addition, due to its roots, HSPICE Level-28 model carried virtually the entire BSIM mathematical structure. It can thus be slow in the simulation of large circuits. Due to its suitability for analog circuit design, HSPICE Level-28 model is commonly employed in the industrial circuit design environment.

2.2.3 The BSIM2 Model

The BSIM2 model from U.C. Berkeley [8] was a significant modification of the BSIM model. Several additional empirical parameters were added to model second-order effects of transistor behavior. By increasing the number of parameters, the accuracy of the model in the submicron region was improved. However, additional problems of complexity in circuit simulation and parameter extraction were created due to the very large parameter set. The threshold voltage in BSIM2 was very similar to that used in BSIM. The drain-voltage dependence of the drain-induced barrier-lowering coefficient was removed in order to prevent the occurrence of negative output resistance at low current levels. The effect of the vertical field on the carrier mobility included a quadratic dependence upon the gate voltage in order to model the effect of large electric fields that occur in devices with thin gate oxides. The velocity saturation effect was modeled using the critical electric field parameter, which was calculated from a second-order dependence on the drain and saturation voltages. The effect of source/drain parasitic resistances were lumped with the mobility term

during parameter extraction. The horizontal and vertical field effects on the mobility were combined as a summation of terms rather than as a product. The subthreshold drain current was calculated using the charge-sheet approximation. The depletion-layer capacitance and the surface potential at the channel/oxide interface were calculated as functions of the gate voltage.

The ability to handle analog design requirements is a major feature of BSIM2. In addition, the drain current model is more accurate, and provides better convergence behavior during circuit simulation. The main problem with BSIM2 is its complexity as it contains a very large number of parameters.

2.3 The Third-Generation Models

The third-generation MOS transistor models have started to emerge. The original intent was simplification of the MOS transistor model formulation, a reduction of the number of model parameters, and the development of parameters which are physically-based rather than being empirical, as in the second-generation models. There is also extensive use of well-behaved mathematical smoothing functions, which allows for smooth and continuous expressions for model equations and their derivatives. The use of these smoothing functions usually leads to a combined equation which is valid for all regions of device operation.

2.3.1 The BSIM3 Model

The BSIM3 model form U.C. Berkeley [9], at present, has several different versions released. The original intent of BSIM3 was simplicity, with a simplified model structure and a small number of physically-based parameters. However, Versions 1 and 2 showed several shortcomings. An attempt to repair these problems is made in

Version 3, but this is done with large infusion of empirical equations and new model parameters. The model has evolved into an extremely complex form with a very large number of parameters. This seems to deviate from the original intent of the third-generation models. In addition, the complexity of the model and the large number of parameters suggest that parameter extraction task for BSIM3 could be complicated.

The BSIM3v3 has several new features as compared with BSIM3v2. A single I-V expression describes drain-current and output-conductance characteristics from the subthreshold to the strong inversion as well as from the triode to the saturation regions. Such formula garantees continuities of I_{DS}, g_{ds}, g_m and their derivatives throughout all V_{GS} and V_{DS} bias conditions. New width dependencies for bulk charge and source/drain resistance are included. This enhances the accuracy in modeling the narrow-width devices. The charge/capacitance model is still based on the BSIM1 structure including more high-order effects in modeling the saturation voltage and the active channel width and length. Non-quasi-static model expression is an option for charge/capacitances in BSIM3v3. It is based on the Elmore equivalent circuit to model the channel charge and channel time constant. However, the RC network and the time constant from gate to source and drain are not considered.

The BSIM3v3 was originally intended for one set of parameter values fitting the whole designing geometry space. It has about 110 parameters. However, the extraction procedure is very complicated. Many parameters are difficult to extract and obtain the proper values. Therefore, the 'binning" is still applied on BSIM3v3 and it results the number of parameters to be more than 300.

2.3.2 The MOS Model-9

The MOS Model-9 model was developed at Philips Laboratories [15, 16, 17]. Like BSIM3v3, numerical smoothing functions are added to the MOS Model-9 model to allow for the use of a single expression for device characteristics, e.g. the drain current, conductances, or terminal charges, over the entire operating range of a transistor. The geometry dependence is included with an HSPICE-Level-28-like approach. However, unlike the second-generation models, this method is applied selectively to only certain parameters, and is used in different ways for different parameters. This makes the model more amenable to "binning".

In the threshold-voltage modeling, besides the non-uniform doping effects, more efforts was spent on describing the drain-induced-barrier-lowering effect. The effect of static feedback on the threshold voltage is also considered. This effect is particularly important at large drain biases, when the drain depletion region is a major portion of the total device depletion region. The effective carrier mobility only includes the first-order terms from the vertical and lateral field effects. The terminal charge is derived with gradual channel approximation for different operation regions, and the smooth functions are used to unify the expressions. With less number of parameters, the unified current and terminal charge expressions have a simpler format than BSIM3v3. It is easier to perform the "binning" parameter extraction.

2.3.3 The EKV Model

The Enz-Krummenacher-Vittoz (EKV) model [18, 19] was developed in Swiss Federal Institute of Technology (EPFL). This model is oriented for low-power analog circuit design. Rather than using the source node as the voltage reference point, the substrate node serves this role. This allows the source and drain terminals to be

treated symmetrically, with separate voltages, which is particularly useful in circuits where the transistors are used bi-directionally. By developing a pinch-off voltage which applies independently to the source and drain terminals, the operation regions of weak-inversion, triode, and saturation regions can be determined.

2.4 Table Look-up Models

Table look-up models use data from devices of different geometries measured at different bias conditions. During circuit simulation, transistor voltage and current values for a specific point in the geometric-and-bias space are determined from the measurement data using various interpolation and extrapolation techniques. Various techniques are used to improve the accuracy of such models without greatly increasing the number of data points [22, 23, 24].

Shima, et al. [22] proposed a three-dimensional table look-up modeling technique. Interpolation was done by using curve-shape fitting techniques. The data were stored in a three-dimensional table which consisted of a main table and several sub-tables. The two-dimensional main table contained data at different drain and gate voltages at a substrate voltage of 0 V. In addition to the main table, the three-dimensional table contained sub-tables, each for a unique bulk bias. The variation of threshold voltage as a function of the substrate voltage was stored in a one-dimensional array. In order to calculated the DC current, the threshold voltage was first determined based upon the substrate bias using the stored data and second-order polynomial interpolation. Two sub-tables were selected, based upon the substrate voltage. A single point was found on each sub-table, corresponding to the drain current for the given drain and gate voltages. The drain current at the specified substrate

voltage was determined by interpolating between these points. Conductances were calculated from the differences in drain current and bias voltages in the table.

Shima, et al. also used the table look-up method to model the capacitances of MOS transistors. Measured gate-to-source and gate-to-drain capacitances and a calculated charge table were used to represent the MOS transistor capacitances. The bulk charge was formulated by an analytic expression and other charges were derived based on interpolation of measured capacitance data. Short-channel effects and subthreshold capacitance characteristics could be accurately simulated by using the experimental data in the table. The partitioning of the channel charge into the drain and source charges was done by using a partitioning factor.

Yoon, et al. [23] proposed an adjustable accuracy table look-up model in which the user could determine the tradeoff point between table size and model accuracy. This method could be used to emphasize the accuracy of the model in a certain region of operation such as the weak-inversion, triode, or saturation region. Special attention was given to the accurate calculation of small-signal quantities such as output conductance and transconductance.

2.5 Future Needs

As the CMOS technologies advance to the deep-submicron for low-voltage/low-power and high-speed/high-frequency applications, the accuracy and efficiency MOS transistor models have to be improved. In the past, most of the MOS transistor modeling work was focusing on the drain current and the terminal charge behavior at the MHz range. Representative comparison amount selective MOS transistor models from the 3 generations is listed in Table 2.1. Typically, model development was trying to improve the linkage between the technologies and the model behavior.

However, the parameter extraction was usually not carefully considered during the model development. This results in a large number of parameters which can not be easily extracted, and the extracted results are highly user- and program-dependent. On the other hand, the charge/capacitance model was derived associated with the DC model and also affected by DC model parameters. Once the DC model parameters are extracted, the charge characteristic is determined accordingly. This leaves little room to match the charge/capacitance behavior, and the results, typically, may not be as good as DC model. For the digital circuits, it does not cause significant trouble, once good DC model behavior is obtained. However in analog circuit design, the charge/capacitance characteristics are as important as the DC part. For the high-frequency behavior, it is even more important to achieve accurate charge/capacitance modeling. Especially, in the low-voltage design, a transistor can be biased near the transition between different operation regions. Although the DC may have very good accuracy, the improper model of the charge behavior may result in a significant error of the capacitance values in the transition region. Besides the intrinsic capacitance characteristics, as the channel length decreases to the deep-submicron range, the overlap capacitance and the space charge near the lightly-doped diffusion (LDD) portion become more important. The overlap capacitance also shows bias-dependent on the vertical field, as affected by the gate voltage and substrate voltage related to drain or source [25]. So far, only the BSIM3v3 model includes the gate-bias dependency on overlap capacitances.

On the other hand, almost all the available MOS transistor model, do not consider the high-speed and high-frequency operation effects. The quarter-micron CMOS application has been pushed to GHz operation frequency, e.g. Personal Communication Services (PCS) 1.9 GHz. Under that frequency range, the MOS transistor behavior is no longer dominated by the intrinsic behavior. The terminal resistance, especially

the gate resistance, and substrate coupling and loss effects play very important roles. The development of the advanced MOS transistor model has to be focusing not only on the unified intrinsic model for advance technologies, but also on the extrinsic components, including the bias-dependent overlap capacitances and the parasitics.

Table 2.1: Comparison between Level-2, BSIM, BSIM3v3 and S-CMOS models.

MOS Model	Level-2 (1st generation)	BSIM (2nd generation)	BSIM3v3 (3nd generation)	S-CMOS
Developers	Vladimirescu & Liu (1980)	Sheu, Scharfetter, Ko, & Jeng (1985)	Chen, Jeng, Ko, Hu (1996 - 1998)	This work (1996 - 1998)
Number of parameters	18	62	109	35
Model expression for different operation regions	different expressions	different expressions	unified expression	unified expression
Continuity of conductance	discontinuity at transitions between different operation regions	discontinuity at transitions between different operation regions	continuous and smooth through all operation regions	continuous and smooth though all operation regions
Accuracy of drain current and conductances prediction for advanced technology	moderate	moderate	good	good
Charge/capacitance model	separate equations for different operation regions	separate equations for different operation regions	unified terminal charge equations	unified terminal charge equations
Small-geometry effects	complex expressions (few additional parameters)	globally fixed format (triple number of parameters)	globally fixed format (quadruple number of parameters)	locally adapted format (some adapted parameters)
Suitability for circuit design hand-analysis	good	moderate	moderate	good
Applicable circuit type	Digital VLSI	Digital VLSI	Mixed-signal VLSI	Mixed-signal VLSI
Applicable technology	1.2 µm	0.8 µm	deep-submicron	deep-submicron

Reference List

[1] S. M. Sze, *Physics of Semiconductor Physics,* 2nd Edition, John Wiley and Sons: New York, NY, 1981.

[2] Y.P. Tsividis, *Operation and Modeling of the Transistor,* McGraw-Hill: New York, NY, 1987.

[3] K. Lee, M. Shur, T. A. Fjeldly, T. Ytterdal, *Semiconductor Device Modeling for VLSI*, Prentice Hall: Englewood Cliffs, NJ, 1993.

[4] R. S. Muller, T. I. Kamins, *Device Electronics for Integrated Circuits*, 2nd Edition, John Wiley: New York, NY, 1986.

[5] A. Vladimirescu, S. Liu, *The Simulation of MOS Integrated Circuits Using SPICE2*, Memo ERL-M80/7, Electronics Res. Lab., Univ. of California, Berkeley, Oct. 1980.

[6] T. Sakurai, A. R. Newton, "A simple MOSFET model for circuit analysis," *IEEE Trans. on Electron Devices*, vol. 38, no. 4, pp. 887-894, Apr. 1991.

[7] B. J. Sheu, D. L. Scharfetter, P. K. Ko, M.-C. Jeng, "BSIM: Berkeley short-channel IGFET model for MOS transistor," *IEEE J. Solid State Circuits*, vol. 22, no. 4, pp. 558-566, Aug. 1987.

[8] M.-C. Jeng, P. K. Ko, C. Hu, "A deep-submicrometer MOSFET model for analog/digital circuit simulations," *Tech. Digest of IEEE Int'l Electron Devices Meeting*, pp. 114-117, San Francisco, CA, Dec. 1988.

[9] J. H. Huang, Z. H. Liu, M. C. Jeng, P. K. Ko, C. Hu, "A robust physical and predictive model for deep-submicrometer MOS circuit simulation," *IEEE Custom Integrated Circuits Conf.*, San Diego, CA, May. 1993.

[10] S.-W. Lee, R. C. Rennick, "A compact IGFET model - ASIM," *IEEE Trans. on Computer-Aided Design*, vol. 7, no. 9, pp. 952-975, Sep. 1988.

[11] A. R. Boothroyd, S. W. Tarasewocz, C. Slaby, "MISNAN-A physically based continuous MOSFET model for CAD applications," *IEEE Trans. on Computer-Aided Design*, vol. 10, no. 12, pp. 1512-1529, Dec. 1991.

[12] S. M. Gowda, B. J. Sheu, "BSIM_plus: An advanced SPICE model for submicron MOS VLSI circuits," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 13, no. 9 , pp. 1166-1170, Sep. 1994.

[13] J. Huang, et al., *BSIM3 Version 2.0 Manual,* University of California, Berkeley, Electronics Research Laboratory, 1994.

[14] Y. Cheng, et al., *BSIM3 Version 3.0 Manual,* University of California, Berkeley, Electronics Research Laboratory, 1995.

[15] R. Velghe, D. Klaassen, F. Klaassen, "MOS Model 9," Unclassified Report NL-UR 003/94, Philips Electronics, N. V., Netherland, 1994.

[16] R. Velghe, D. Klaassen, F. Klaassen, "Compact MOS modeling for analog circuit simulation," *1993 IEDM Tech Dig.*, pp. 485-488, 1993.

[17] H. deGraaff, F. Klaassen, *Compact Transistor Modeling for Circuit Design,* Springer-Verlag, 1990.

[18] C. Enz, F. Krummenacher, E. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low voltage and low current applications," *Analog Integrated Circuits and Signal Processing,* vol. 8, pp. 83-114, 1995.

[19] M. Bucher, C. Lallement, C. Enz, F. Krummenacher, "Accurate MOS modeling for analog circuit simulation using the EKV model," *1996 IEEE Intl. Symposium on Circuits and Systems*, May, 1996.

[20] D. Foty, *MOSFET Modeling With SPICE - Principles and Practice*, Prentice Hall: Upper Saddle River, NJ, 1997.

[21] *Star-HSPICE User's Manual*, Avant! Corporation, Sunnyvale, CA, Feb. 1996.

[22] T. Shima, H. Yamada, R. L. M. Dang, "Table look-up MOSFET modeling system using a 2-D device simulator and monotonic piecewise cubic interpolation," *IEEE Trans. on CAD of Integrated Circuits and Systems*, vol. 2, no. 2, pp. 121-125, Apr. 1983.

[23] K. S. Yoon, P. E. Allen, "An adjustable accuracy model for VLSI analog circuits using lookup tables," *J. of Analog Integrated Circuits and Signal Processing,* Kluwer Academic Publishers, vol. 1, no. 1, pp. 45-64, Sep. 1991.

[24] T. Shima, "Table lookup MOSFET capacitance model for short-channel devices," *IEEE Trans. on Computer-Aided Design*, vol. 5, no. 4, Oct. 1986.

[25] P. Klein, "A compact-charge LDD-MOSFET model," *IEEE Trans. on Electron Devices*, vol. 44, no. 9, pp. 1483-1490, Sept. 1997.

Chapter 3

The Unified Short-Channel MOS (S-CMOS) Transistor Model

List of Symbols

μ_{eff}	effective carrier mobility
C_{OX}	gate-oxide capacitance per unit area
ϕ_n	electron quasi-Fermi potential
V_T	thermal voltage
Q_0	peak surface charge density at the source/drain ends
V_{ch}	potential level in the channel
α_x	back gate degradation coefficient

Design of high-performance very large-scale integration (VLSI) systems is made possible by rapid advances in fabrication technologies into the deep-submicron regime. Circuit designers using advanced CMOS technologies require an accurate MOS transistor model for proper circuit simulation over the geometric and biasing design spaces. An effective and efficient analytical model will enable VLSI designers to fully exploit advantages of aggressive technologies. The following features are required to make the transistor model very useful to circuit designers:

- a compact parameter set,
- model expressions based on knowledge from devices physics,
- accuracy of drain current, output conductance, and capacitances,
- continuity of drain current, terminal charge, and their derivatives across different regions of operation, and
- convenience to simulate transistors over the geometric design space for different circuit applications.

The unified short-channel MOS (S-CMOS) transistor model has been developed to address challenges posed by the rapid evolution of fabrication technologies and to enable accurate and efficient design of deep-submicron CMOS circuits for low-voltage mixed-signal high-speed VLSI. This model includes several advanced features:

- accurately modeling the threshold voltage down to 0.25 μm channel length, including, reverse short-channel, narrow-channel, non-uniform substrate doping, and drain-induced-barrier-lowering effects;
- second-order effects of vertical field on effective mobility reduction for deep-submicron devices;
- the vertical- and horizontal-filed effects on channel-length modulation for short-channel devices;
- accurately modeling on back-gate-degradation coefficient for charge densities; and
- unified drain current, conductances, terminal charge, capacitances expressions valid through all operation regions.

A compact set of parameters reduces the complexity of the parameter extraction task and enhances the ability to extract an accurate parameter set. The S-CMOS model uses 35 parameters for determination of the DC drain current from the terminal voltages, including 4 smooth function parameters to perform better transition between different operation regions. The model parameters and their default values are listed in Table 3.1. The small number of parameters also allows circuit designers to have better understanding of the relationship between the circuit performance and behavior of its constituent transistors.

3.1 Drain Current Formulation

Accuracy of the drain current expression is of primary importance in computer simulation of digital VLSI circuits. In addition, accurate output conductance and transconductance expressions are required in the design of analog LSI and VLSI circuits. The DC expression of the S-CMOS model has the capability to achieve good accuracy by including the higher-order effects and some modeling techniques.

In the saturation region, the function, f_L, describing the channel-length reduction effect of short-channel device is included to accurately describe the drain-current characteristics. This function, f_L, combined with two drain-induced-barrier-lowering effect parameters, η_Z, and η_L, in the threshold voltage expression can model the output conductance in the saturation region very well. In the transition between the triode and the saturation regions, a hyperbola function [6] is used to smooth out the abrupt transition. Therefore, the continuous drain current behavior in the strong-inversion region, including the triode and saturation regions, can be described by a unified analytical equation without any numerical iteration.

Table 3.1: Device parameters and their typical values of S-CMOS model for a 0.5 μm technology.

Name	Description	Value (NMOS)	Value (PMOS)	Unit
ϕ_s	surface inversion potential	1.05	0.93	V
V_{FB}	flat-band voltage	-0.4	-0.33	V
T_{ox}	gate oxide thickness	90	90	nm
γ_1	zero-bias body-effect coeff.	0.421	0.563	$V^{0.5}$
γ_{1L}	zero-bias short-channel body-effect coeff.	0.03	0.06	$V^{0.5}$-µm
γ_2	high-bias body-effect coeff.	0.328	0.309	$V^{0.5}$
K_S	depletion charge-sharing coeff.	2.7	3.4	-
K_{NZ}	narrow-width threshold voltage coeff.	0.244	0.217	V-µm
k_{NB}	narrow-width threshold voltage substrate coeff.	5.4e-4	-3.9e-4	µm
η_Z	drain-induced barrier lowering coeff.	0.002	-0.005	-
η_L	short-channel barrier lowering coeff.	0.001	0.038	µm
η_1	short-channel threshold voltage reduction coeff.	0	0	V-µm
η_2	characteristics length of reverse short-channel effect	0	0	V-µm
η_3	reverse short-channel coeff.	1	1	µm
μ_0	intrinsic surface mobility	450	130	cm^2/Vs
U_{GSZ}	gate-voltage mobility degradation coeff.	0.02	0.1	V^{-1}
U_{GSZ2}	gate-voltage mobility degradation 2nd-order coeff.	0.02	0.1	V^{-1}
U_{GSL}	short-channel adjustment of u_{gsz}	0.06	-0.1	V^{-1}µm
U_{GSL2}	second-order short-channel adjustment of u_{gsz}	0.06	-0.1	V^{-1}µm
U_{DS}	drain-voltage mobility degradation coeff.	0.08	0.01	V^{-1}
U_{BS}	substrate-voltage mobility degradation coeff.	0.005	0.02	V^{-1}
N	subthreshold drain current slope	1.5	1.5	-

Table 3.1 (continued)

Name	Description	Value (NMOS)	Value (PMOS)	Unit
k_{sub}	subthreshold current shifting coeff.	5	0.1	-
E_{crit}	critical electric field for velocity saturation	10	10	V/μm
λ_D	drain-voltage dependent CLME coeff.	0.001	1.15	V^{-1}
λ_G	gate-voltage dependent CLME coeff.	0.1	3.5	$V^{3/2}$
λ_B	substrate-voltage shifting CLME coeff.	2	2	-
λ_{BS}	substrate-voltage dependent CLME coeff.	1	1	V
ϕ_d	drain-voltage related CLME potential	0.5	0.1	V
K_{BSh}	bulk bias hyperbola function coeff.	1.01	1.01	-
K_{DSATh}	strong-inversion hyperbola function coeff.	1.03	1.05	-
K_{GSh}	gate-threshold hyperbola function coeff.	1.01	1.01	-
K_{sig}	sigmoid function coeff.	0.01	0.01	-
dL	channel length reduction	0	0	μm
dW	channel width reduction	0	0	μm

To properly handle the transition between weak- and strong-inversion regions, instead of the conventional direct-sum method, $I_{total} = I_{DSw} + I_{DSs}$, an alternative approach by using the interpolation [7] and sigmoid functions to combine the diffusion and drift components together is used in this research. Thus, the unified single-equation expression of DC MOS transistor model can accurately describe the drain current, output conductance, and transconductance characteristics.

In order to model the short-channel transistor behavior, the threshold voltage expression includes surface inversion potential, flat-band voltage, non-uniform substrate doping, drain-induced-barrier-lowering, and narrow-channel effects. Effective

mobility is modeled by using a reduction factor, M_r, to consider the contribution due to the transverse and lateral electrical fields. This reduction factor has flexibility to accommodate different effects in various operation regions. The velocity saturation effect in the strong-inversion region is also included in the reduction factor. Channel-length modulation effect described by the function, f_L, gracely reduces to zero in the triode and weak-inversion regions.

3.1.1 Threshold Voltage

The threshold voltage of an MOS transistor is the gate voltage separating the strong- and weak-inversion regions of operation. At the threshold voltage, the minority carrier concentration in the channel region is equal to the majority carrier concentration in the bulk semiconductor. In most devices, the threshold voltage decreases monotonically with decreasing channel length due to charge-sharing effect by the drain and source terminals with the gate terminal. This is called short-channel effects on threshold voltage. However, it has been observed that the threshold voltage in some devices increases with initial decreasing of the channel length. After it reaches a maximum value, it starts to decrease at even shorter channel lengths resulting in a "hump" in the threshold voltage versus channel length characteristics. This is the reverse short-channel effects [1, 2, 3, 4]. Modeling of the reverse short-channel effects on threshold voltage was originally proposed by N. Aroro and M. Sharma [4],

$$\delta V_{th} = -\frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - exp\left(-\frac{L}{\eta_3}\right)\right), \tag{3.1}$$

where

$$\eta_2 = \frac{2Q_0\eta_3}{C_{OX}}. \tag{3.2}$$

Here, the parameter, η_1 is the fitting parameter for short-channel effects, Q_0 is the peak surface charge density at the source/drain ends, and η_2 is the characteristic length over which this charge distribution is spread.

The threshold voltage in this research also includes the narrow-channel, non-uniform substrate doping and the drain-induced-barrier-lowering effects. The detailed expression is

$$\begin{aligned} V_{th} = \; & V_{FB} \; + \phi_s + (\gamma_1 - \frac{\gamma_{1L}}{L})(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi_s}) - \frac{K_S}{2}(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi_s})^2 \\ & + \; \gamma_2(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s - V_{BSh}}) + \frac{K_{NZ}}{W} + \frac{K_{NB}V_{BS}}{W} \\ & - \; (\eta_Z + \frac{\eta_L}{L})V_{DS} - \frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - exp\left(-\frac{L}{\eta_3}\right)\right) \end{aligned} \tag{3.3}$$

where

$$V_{BSh} = \frac{1}{2}\left(V_{BS} + K_{BSh} \cdot V_{BST} + \sqrt{(V_{BS} + K_{BSh}V_{BST})^2 - 4V_{BS}V_{BST}}\right) \tag{3.4}$$

and

$$V_{BST} = \phi_s - (\frac{\gamma_1 - \gamma_2}{K_S} + \sqrt{\phi_s})^2. \tag{3.5}$$

Here V_{FB} is the flat-band voltage, and $\phi_s = 2\phi_F$ is the surface inversion potential. The non-uniform substrate doping effect is included by using parameters $\gamma_1, \gamma_{1L}, \gamma_2$, and K_S. The drain-induced-barrier-lowering effect modeled by parameters η_L and η_Z is a function of channel length and drain voltage. The narrow-channel effect is also included by using parameters K_{NZ} and K_{NB}. Here, V_{BST} is the transition voltage at which the boundary of the depletion region reaches the bulk semiconductor with the impurity concentration of N_B. A hyperbola function, V_{BSh}, is used to combine the nonuniform substrate doping effects for $|V_{BS}| \leq |V_{BST}|$ and $|V_{BS}| > |V_{BST}|$ [5]

together in order to realize a continuous curve for the derivative of threshold voltage expression at the transition point, $V_{BS} = V_{BST}$.

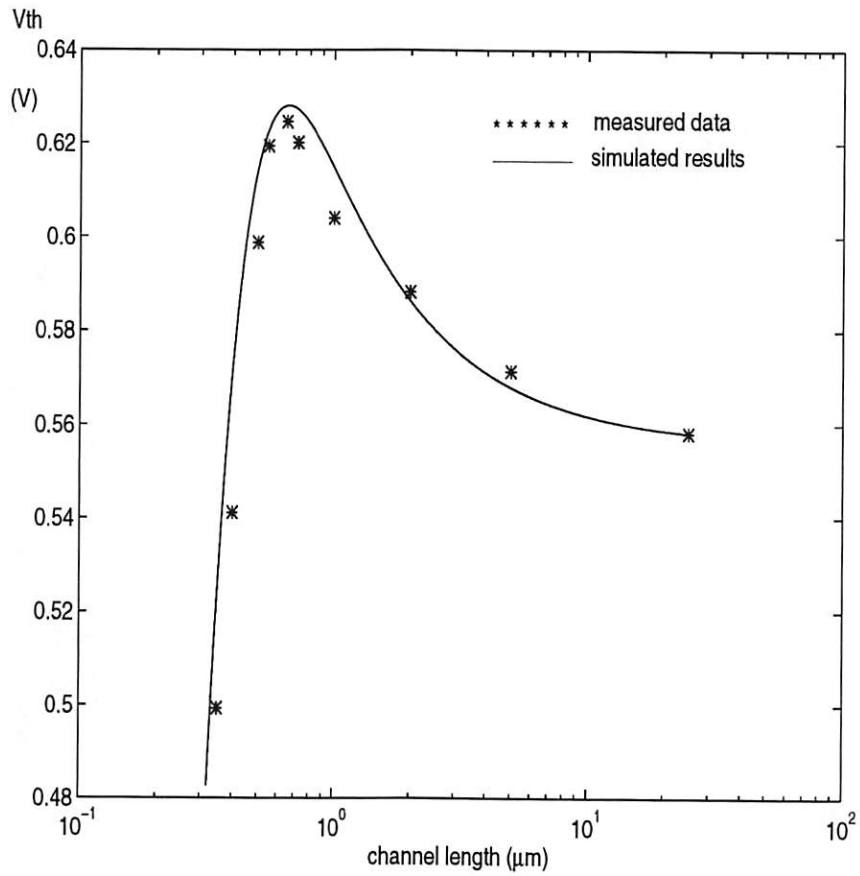


Figure 3.1: Plot of the measured and modeled threshold voltage versus channel length.

As shown in Fig. 3.1, the threshold voltage increases as the channel length decreases and reaches the maximum value around 0.6 μm. It then decreases for shorter channel-length transistors. This model provide good description on this behavior. Figure 3.2 shows a plot of threshold voltage versus V_{BS} with different channel lengths. Notice that the threshold voltage decreases as decreasing V_{BS}. The body effects on threshold voltage is also affected by the channel length. For short channel devices,

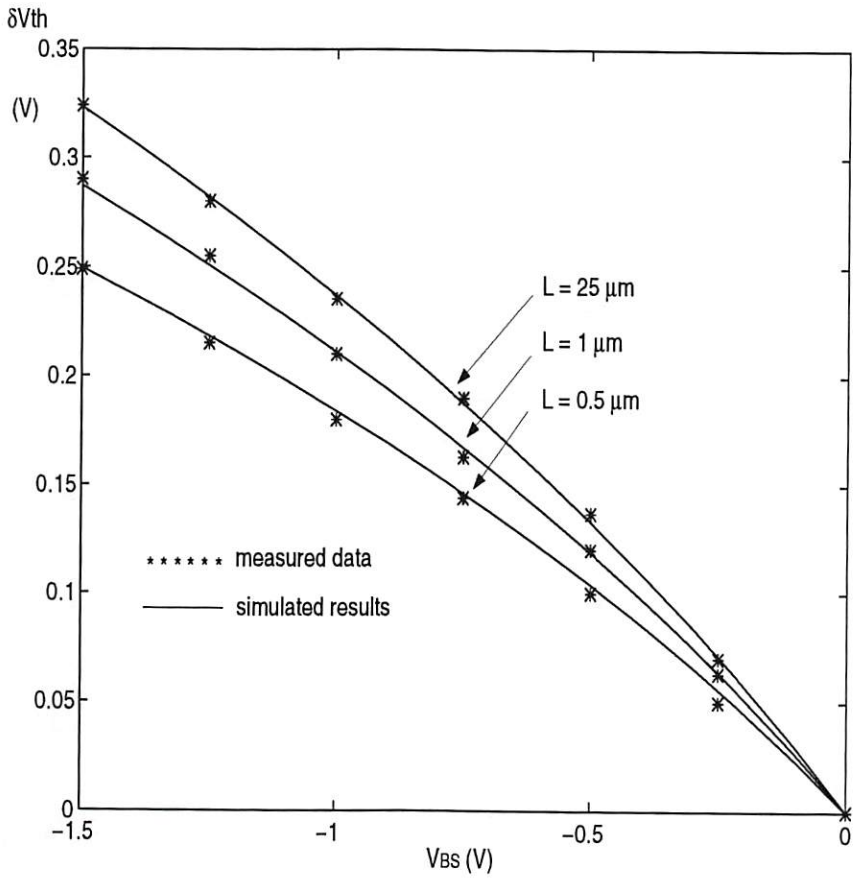


Figure 3.2: Plots of measured and modeled threshold voltage values due to the body effect versus V_{BS} with different channel lengths.

the amount of δV_{th} becomes smaller. In this model, this channel length dependency effect is modeled by the parameter, γ_{1L}.

3.1.2 Effective Mobility

The intrinsic carrier mobility at the surface of the silicon, μ_0, can be viewed as a technology-dependent model parameter. During device operation, the mobility of carriers is reduced due to the transverse and lateral electrical fields. The effective

mobility is a function of $(V_{GS} - V_{th})$, V_{BS}, and V_{DS}. In this model a reduction factor, $M_r(V_{GS} - V_{th}, V_{BSh}, V_{DS}) = \mu_0/\mu_{eff}$, is used to describe the effective mobility [5, 6]:

$$\begin{aligned} M_r = \quad & [\quad 1 + (U_{GSZ} + \frac{U_{GSL}}{L})(V_{GSh} - V_{th}) + (U_{GSZ2} + \frac{U_{GSL2}}{L})(V_{GSh} - V_{th})^2 \\ & - \quad U_{BS}(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi_s}) + U_{DS}V_{DS}] \cdot [1 + \frac{V_{DS}(1 - f_s)}{E_{crit}L}] \end{aligned} \tag{3.6}$$

where

$$V_{GSh} = \frac{1}{2}\left(V_{GS} + K_{GSh} \cdot V_{th} + \sqrt{(V_{GS} + K_{GSh}V_{th})^2 - 4V_{GS}V_{th}}\right). \tag{3.7}$$

Here, parameters $U_{GSZ}, U_{GSL}, U_{GSZ2}, U_{GSL2}$, and U_{BS} are used to model the reduction of mobility due to carrier scattering by the transverse electric field. The gate-voltage contribution to transverse field is combined with parameters U_{GSZ} and U_{GSZ2}, while the parameter U_{GSL} and U_{GSL2} are short-channel correction parameters [5]. The parameter U_{DS} is used to model the effect from the drain voltage. The continuous velocity saturation effect due to the influence of the lateral field in the channel on the carrier mobility is also included by the term $V_{DS}(1 - f_s)/(E_{crit}L)$. Here, E_{crit} is the critical-field parameter for velocity saturation. The sigmoid function, f_s, and the expression for V_{GSh} make the reduction factor valid in both strong- and weak-inversion region. As shown in Fig. 3.3, $(V_{GSh} - V_{th})$ is equal to zero in the weak-inversion region. The sigmoid function is described in detail in section 3.1.6.

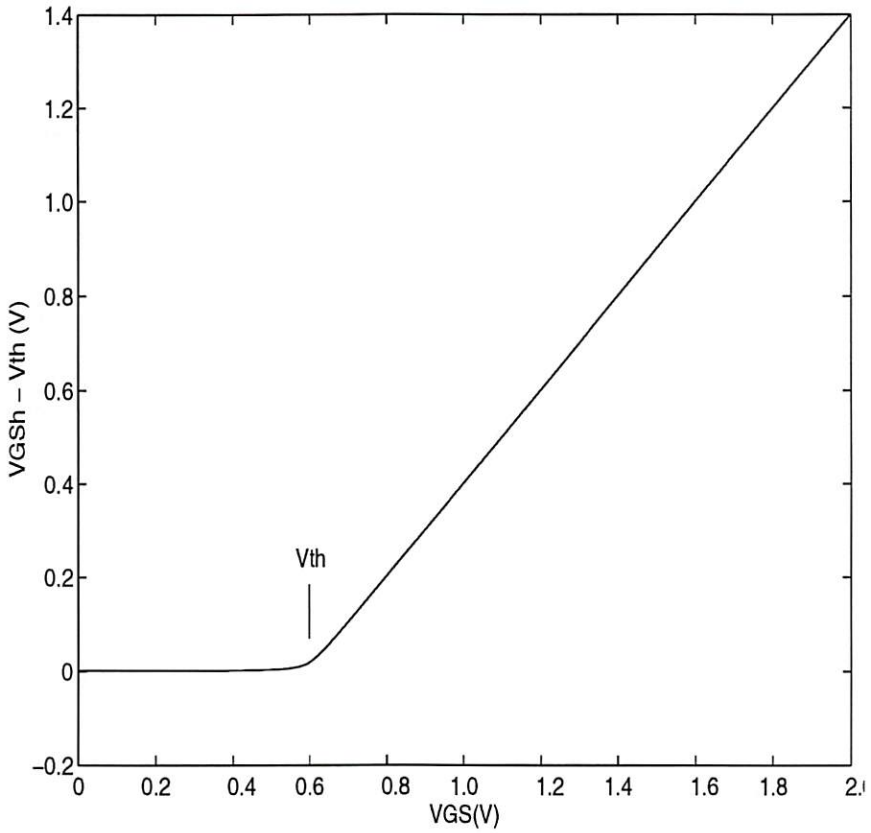


Figure 3.3: Graphical illustration of the function $(V_{GSh} - V_{th})$ which reduces to zero in weak-inversion region.

3.1.3 Strong-Inversion Current

The transistor operates in the strong-inversion region if the gate-to-source voltage is greater than the threshold voltage. The strong-inversion current can be determined by integrating the channel charge density, q_c, which can be expressed as [15]:

$$q_c = -C_{OX}[(V_{GS} - \phi_s - V_{FB} - \phi_n) - \gamma_1\sqrt{\phi_s + \phi_n - V_{BS}}], \tag{3.8}$$

where ϕ_n is the quasi-Fermi potential in the channel region. Thus, the strong-inversion current can be described by the following expression,

$$I_{DSs} = \mu_{eff} C_{OX} \frac{W}{L} [(V_{GS} - V_{th}) V_{DS} - \frac{a}{2} V_{DS}^2] \tag{3.9}$$

where the term "a" is defined as [5, 15]:

$$a = 1 + \frac{g\gamma_1}{2\sqrt{\phi_s - V_{BS}}} \tag{3.10}$$

and

$$g = 1 - \frac{1}{1.744 + 0.8364(\phi_s - V_{BS})}. \tag{3.11}$$

The saturation region is bounded by the onset of velocity saturation at $\phi_n = V_{DSAT}$. Due to the change of the channel charge density, the saturation voltage, V_{DSAT}, can be determined by [5]:

$$V_{DSAT} = \frac{V_{GS} - V_{th}}{a\sqrt{K}} \tag{3.12}$$

where

$$K = \frac{1 + V_c + \sqrt{1 + 2V_c}}{2} \tag{3.13}$$

and

$$V_c = \frac{V_{GSh} - V_{th}}{aE_{crit}L}. \tag{3.14}$$

The value of V_{DSAT} determines the separation between the triode and saturation regions. Here, use of V_{GSh} in V_c helps to make $K = 1$ in the weak-inversion region.

Thus, V_{DSAT} can also be used in the unified single-equation expression which will be described in section 3.1.6.

In order to describe the drain current behavior in the saturation region, a hyperbola interpolation function, V_{DSATh}, which was proposed by A. Chatterjee, et al. [6], is used to smooth out the abrupt transition from the triode to the saturation regions. The expression, V_{DSATh}, is given by,

$$V_{DSATh} = \frac{1}{2}\left(V_{DS} + K_{DSATh}V_{DSAT} - \sqrt{(V_{DS} + K_{DSATh}V_{DSAT})^2 - 4V_{DS}V_{DSAT}}\right) \quad (3.15)$$

where K_{DSATh} is a model parameter.

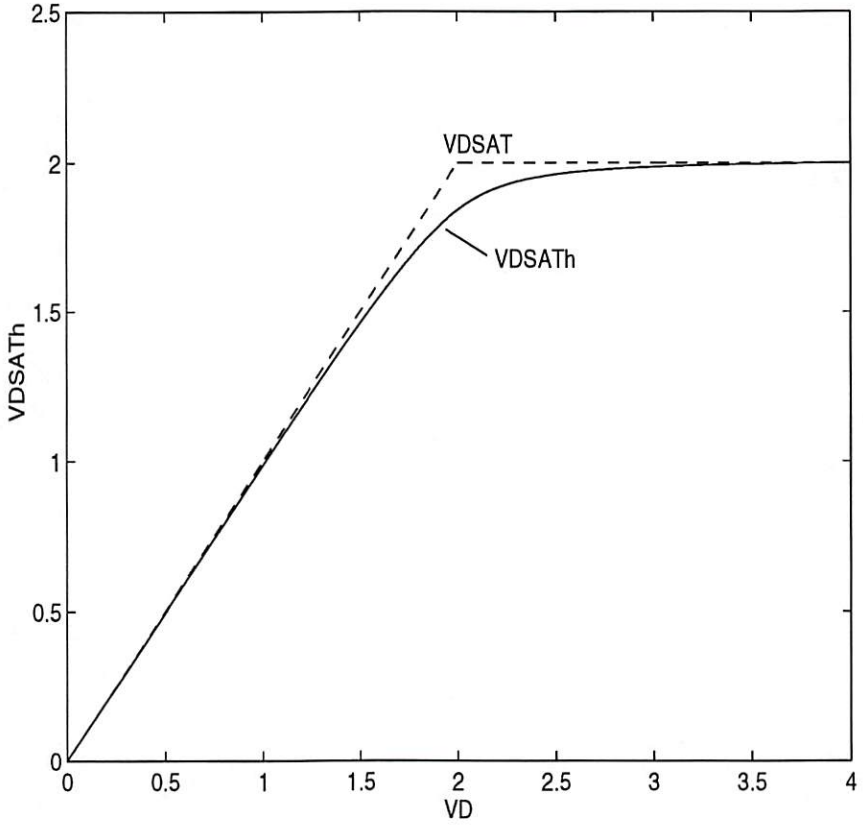


Figure 3.4: Graphical illustration of the hyperbola function for smoothing the transition between triode and saturation regions.

As shown in Fig. 3.4, V_{DSATh} closely tracks V_{DS} when the transistor operates in the triode region. It saturates at the value of V_{DSAT} in the saturation region. This formula ensures that $V_{DSATh} = 0$ when $V_{DS} = 0$, which is very important for not creating artificial offset. The V_{DSATh} is used to replace all the V_{DS} terms in (3.6) and (3.9). Therefore the reduction factor of effective mobility and drain current expression can be rewritten as:

$$M_r = [\ 1 + (U_{GSZ} + \frac{U_{GSL}}{L})(V_{GSh} - V_{th}) + (U_{GSZ2} + \frac{U_{GSL2}}{L})(V_{GSh} - V_{th})^2 - U_{BS}(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi_s}) + U_{DS}V_{DSATh}] \cdot [1 + \frac{V_{DSATh}(1 - f_s)}{E_{crit}L}], \quad (3.16)$$

and

$$I_{DSs} = \mu_{eff}C_{OX}\frac{W}{L}[(V_{GS} - V_{th})V_{DSATh} - \frac{a}{2}V_{DSATh}^2]. \quad (3.17)$$

Thus the drain current saturation behavior can be described by the same current equation even for $V_{DS} > V_{DSAT}$. The parameter, K_{DSATh}, controls the curvature of the hyperbola and is an important model parameter to accurately describe the output conductance characteristics.

3.1.4 Channel-Length Modulation Effect

In the saturation region, the effective channel length, $L_{eff} = L - dL$, determined from the channel-length modulation effect is further reduced as the drain voltage increases. Therefore, the drain current is increased by a factor, L/L_{eff}. For a long-channel device, the channel-length reduction, dL, can be simply modeled by a function of V_{DS} [14]. However, for deep-submicron devices, the channel-length reduction effect should include the original channel length [6]. The fraction of dL and L should be taken into account in order to properly model the channel-length

modulation effect. By applying the Taylor-series expansion, $1 + dL/L$ can be used to describe L/L_{eff} term. From experimental results, the term, dL/L, is a function of $(V_{GS} - V_{th}), (V_{DS} - V_{DSAT})$, and, V_{BS} [6, 14, 16]. In this research, the expression for the channel-length modulation effect is described as [6, 14],

$$f_L = \frac{dL}{L} = \frac{\lambda_D[\sqrt{\phi_D + V_{DS} - V_{DSATh}} - \sqrt{\phi_D}]}{L((V_{GSh} - V_{th})^{3/2} + \lambda_G)(\frac{\lambda_B}{1-\frac{V_{BS}}{\lambda_{BS}}})}. \tag{3.18}$$

Here, λ_G, λ_B, and λ_{BS} were fist described in [14]. The effects modeled by λ_D and ϕ_D were mentioned in [14]. The term, V_{DSATh}, is used to replace V_{DSAT} in order to set f_L equal to zero in the triode region. Thus, this expression can be used in both the triode and saturation regions.

3.1.5 Weak-Inversion Region

The MOS transistor operates in the weak-inversion region when $V_{GS} < V_{th}$. Design of low-power circuits using MOS transistors biased in the subthreshold region requires an accurate subthreshold drain-current expression. Continuity of the drain-current expression and its derivatives across the weak-inversion and strong-inversion regions is also highly desirable especially for transistors biased to achieve large dynamic range. The drain current in the weak-inversion region is mainly dominated by the diffusion component which can be expressed as [15]:

$$I_{DSw} = C_{OX} \cdot \mu_{eff} \cdot \frac{W}{L} \cdot n \cdot V_T^2 e^{\frac{V_{GS}-V_{th}}{nV_T}}[1 - e^{-\frac{V_{DS}}{V_T}}]. \tag{3.19}$$

This component increases exponentially with the gate voltage. The parameter, n, is used to model the subthreshold slope of the diffusion drain-current component.

3.1.6 Unified Drain Current Expression

Notice that the drain current behavior is modeled by (3.17) in strong-inversion region and (3.19) in weak-inversion region. To achieve smooth transition between the weak- and strong-inversion regions, several existing models [6, 15] use the direct sum approach, $I_{total} = I_{DSw} + I_{DSs}$, to add the diffusion and drift components together. Because I_{DSs} is defined to be 0 in weak-inversion region, this approach can realize continuous drain-current behavior. However the derivative of the transconductance is not smooth at the point $V_{GS} = V_{th}$ with this approach. Since the diffusion component of the drain current in the strong-inversion region is much smaller than the drift component and can be neglected, (3.17) and (3.19) can be combined by using a suitable interpolation function [7, 8, 9],

$$f_i(x) = ln(1 + exp(x)). \tag{3.20}$$

Thus, the complete unified single-equation current expression can be described as,

$$I_{DS} = \alpha \cdot \beta \cdot F \tag{3.21}$$

where

$$\alpha = [1 - f_s e^{-\frac{V_{DS}}{V_T}}] \cdot [1 + (1 - f_s) f_L + f_s \cdot K_{sub}] \tag{3.22}$$

$$\beta = C_{OX} \cdot \mu_{eff} \cdot \frac{W}{L} \tag{3.23}$$

$$F = V_{GSth} \cdot V_{DSATh} - \frac{a}{2} V_{DSATh}^2 \tag{3.24}$$

and

$$V_{GSth} = 2 \cdot n \cdot V_T \cdot ln\left(1 + exp\left(\frac{V_{GS} - V_{th}}{2 \cdot n \cdot V_T}\right)\right) \tag{3.25}$$

In a typical situation, K_{sub} is very close to the value of $(a/2n - 1)$. In this proposed model, both n and K_{sub} are model parameters.

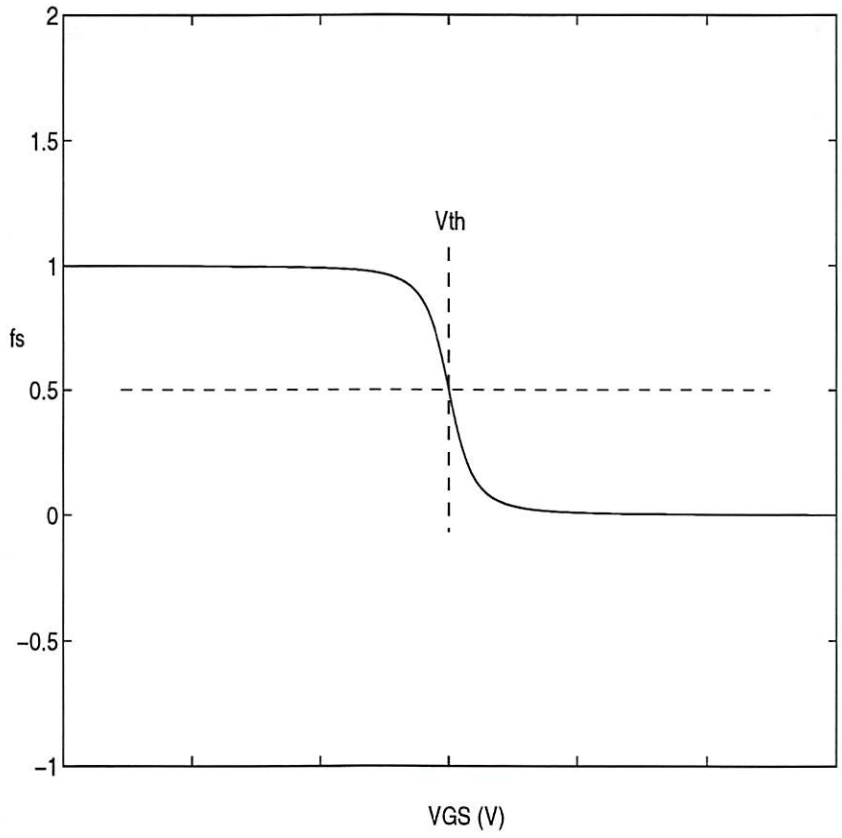


Figure 3.5: The sigmoid function, f_s, used for smoothing the drain current equation from weak- to strong-inversion regions.

f_s is a sigmoid function, as shown in Fig. 3.5, which is used to ensure smooth transition from weak-inversion to strong-inversion regions. This function is defined as,

$$f_s = \frac{1}{2}\left(1 - \frac{V_{GS} - V_{th}}{\sqrt{(V_{GS} - V_{th})^2 + K_{sig}}}\right). \tag{3.26}$$

Here, f_s facilitates a continuous characteristic of the derivative of transconductance at the transition point between the weak- and strong-inversion regions, and can be used in two different formats of smooth function as a linear product, or an exponential product,

$$f1 = e^{f_s K_{p1}} \tag{3.27}$$

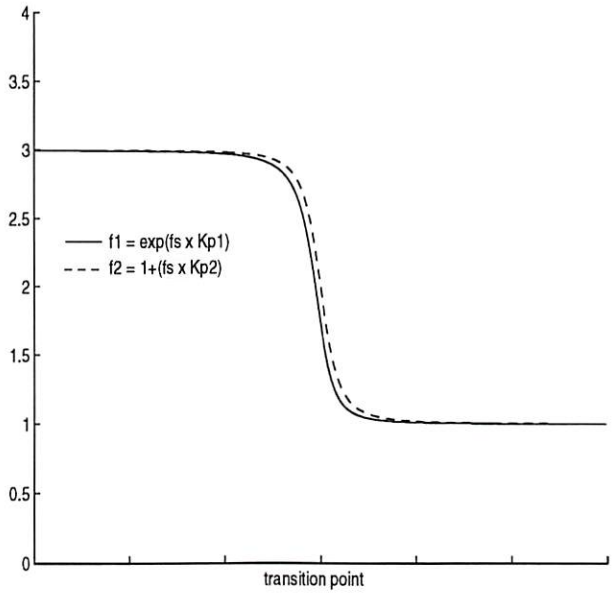
and

$$f2 = 1 + f_s \cdot K_{p2}. \tag{3.28}$$

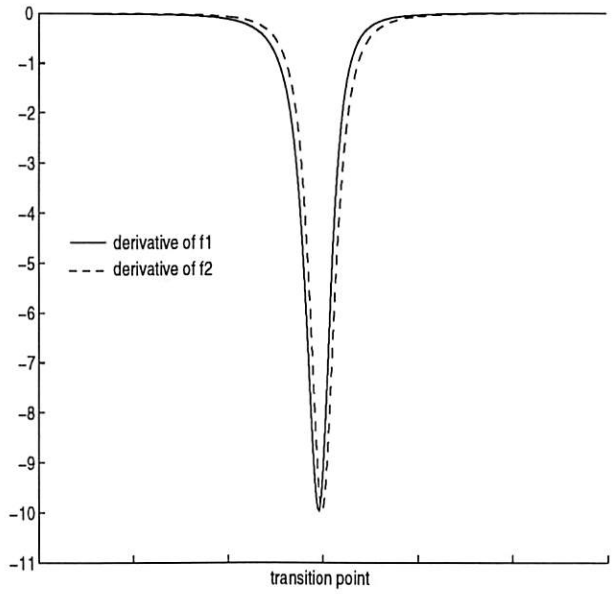
K_{p1} and K_{p2} can be constants or functions. As shown in Fig. 3.6(a), both $f1$ and $f2$ have satisfactory transition characteristics between two operation regions. Their derivatives are also continuous, as shown in Fig. 3.6(b). However, minor difference does exist. By applying these smooth functions into the unified drain current expression, both channel-length modulation and velocity saturation effects are reduced to zero in the weak-inversion region, and the terms K_{sub} and e^{-V_{DS}/V_T} only have effects in the weak-inversion region.

3.2 Experimental Results of DC Model

Comparison of the measured and simulated $I - V$ results is shown in Fig. 3.7. Good agreement has been achieved in both the triode and saturation regions. In addition, the modeled results also provide an excellent transition from the triode to saturation regions for both the drain current and output conductance. Figure 3.8



(a)



(b)

Figure 3.6: Graphical illustration of two smoothing functions, $f1$ and $f2$, with parameters $K_{p1} = 1.1$ and $K_{p2} = 2$. (a) Functions, $f1$ and $f2$. (b) Derivatives of $f1$ and $f2$.

shows the measured and modeled results of output conductance. Notice that this model achieves better transition than BSIM model [15] and accurately handles the channel length modulation effect with the assistance of the f_L function. The same equation can also describe the current characteristics in both weak- and strong-inversion regions with respect to the changing of V_{GS} and V_{BS}. Figure 3.9 shows the plot of drain current curves at different substrate bias voltages. A test for the smooth characteristics of transconductance has been conducted by plotting g_m values on both linear and logarithmic scales. As shown in Fig. 3.10, the BSIM model [15] which uses the $I_{total} = I_{DSw} + I_{DSs}$ for the transition between weak- and strong-inversion regions does produce a continuous transconductance behavior. However, the transition at the threshold voltage is very sharp. The S-CMOS model uses the interpolation and sigmoid functions to combine I_{DSw} and I_{DSs} into a unified expression. Thus, all the terms in this unified expression are continuously differentiable throughout the whole V_{GS} and V_{DS} ranges. It achieves smooth transition for the transconductance which can be verified by the continuity of the second-order derivative of the drain current equation, as shown in Fig. 3.11. The S-CMOS DC model also performs good description of characteristics of PMOS transistors. Figure. 3.13 shows the I_{DS} versus V_{DS} behavior of a long-channel PMOS transistor, while the short-channel characteristics are shown in Fig. 3.14 and Fig. 3.15. Another important benchmark test suggested by Tsividis and Suyama [10] is the plot of g_m/I_{DS} versus $log(I_{DS})$. Figure 3.12 shows the results of the proposed model and those from Level-2 [17] and BSIM model [15].

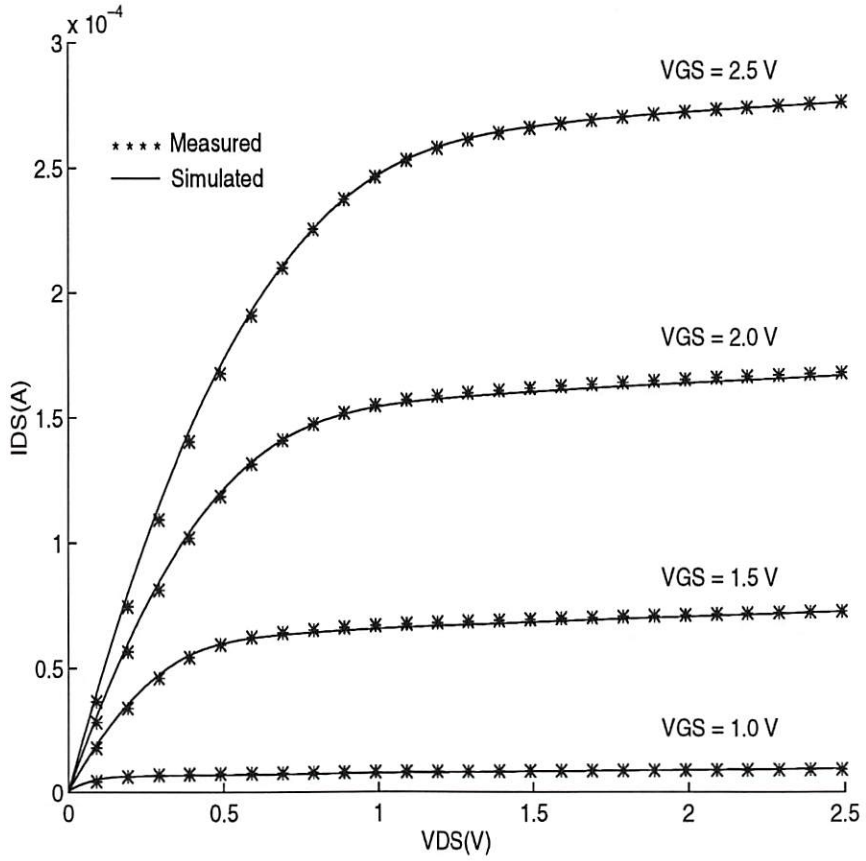


Figure 3.7: Measured versus simulated drain current results for an NMOS transistor with $W/L = 0.75\ \mu m/0.3\ \mu m$ at $V_{BS} = 0$.

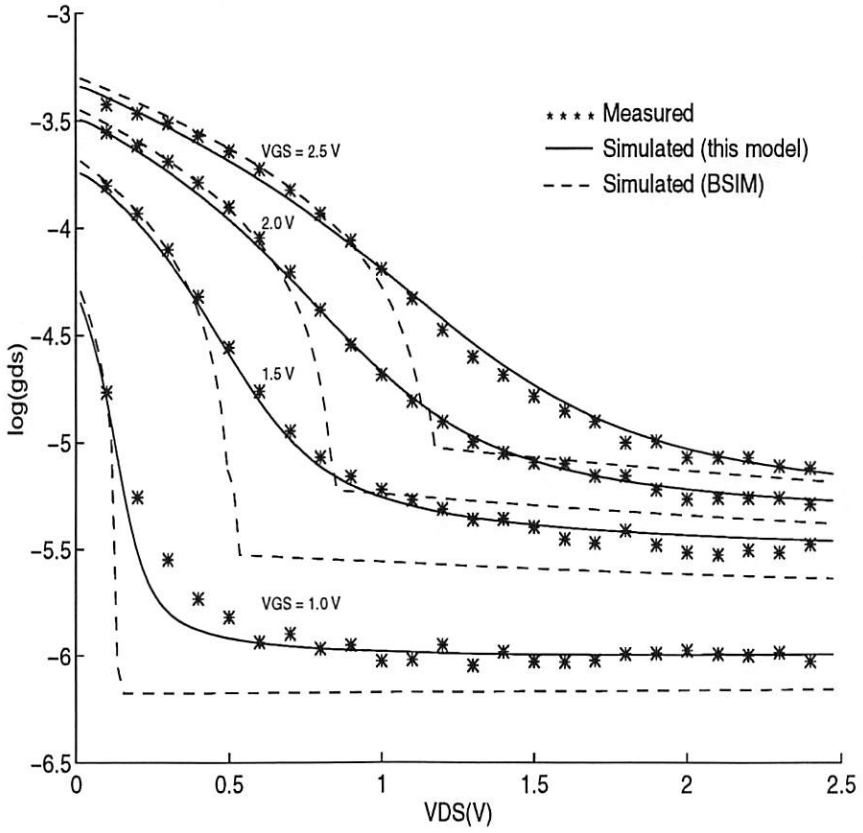
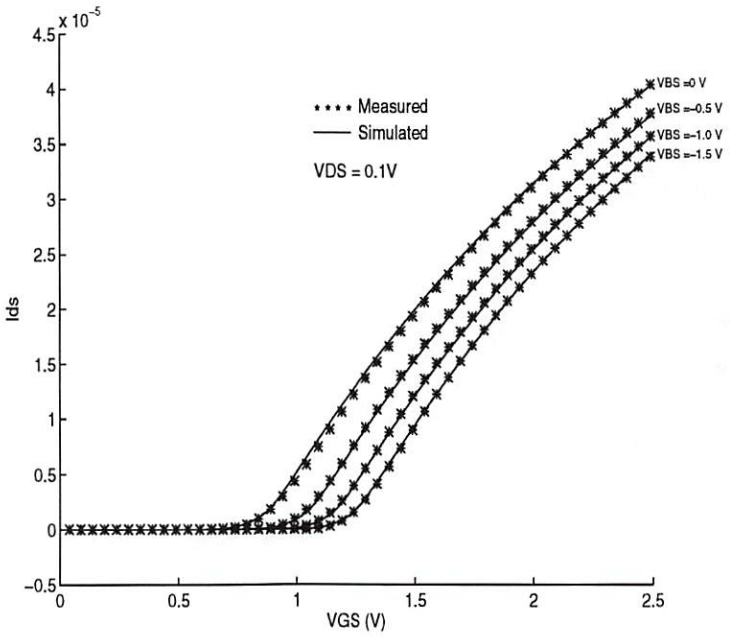
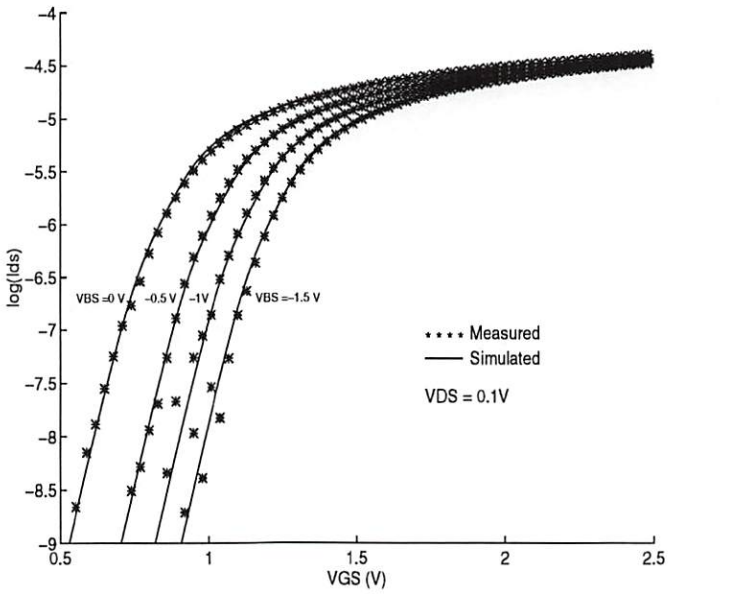


Figure 3.8: Comparison of the measured versus simulated output conductance values of a short-channel ($L = 0.3\ \mu m$) NMOS transistor. The proposed model accurately simulates the output conductance characteristics in the triode, and saturation regions.

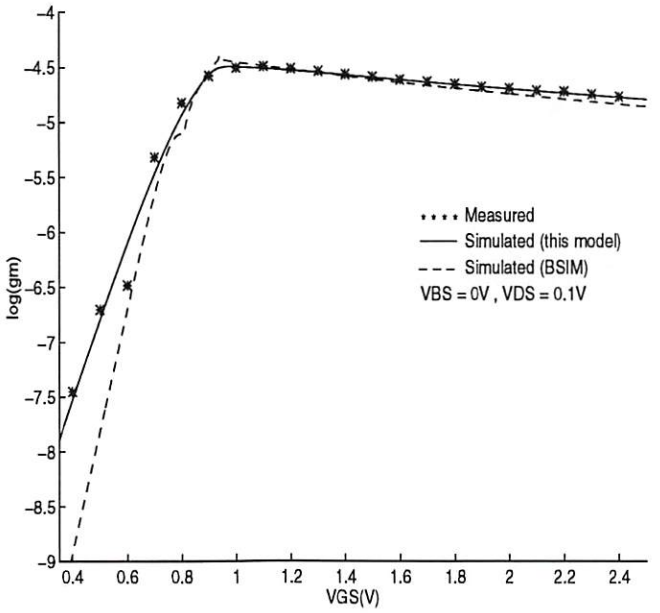


(a)

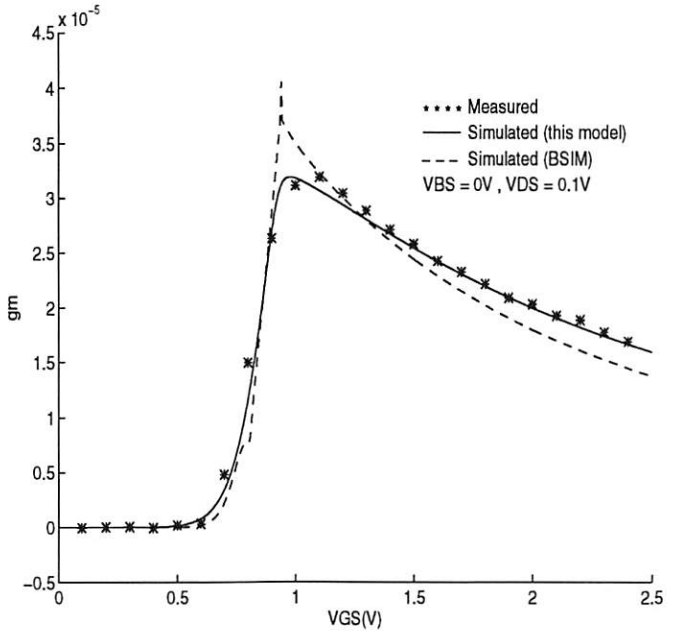


(b)

Figure 3.9: I_{DS} versus V_{GS} characteristics for a short-channel NMOS transistor with a small drain bias voltage. (a) On a linear scale for drain current. (b) On a logarithmic scale for drain current.



(a)



(b)

Figure 3.10: Comparison of predicted g_m for both the BSIM and the proposed model. (a) On a logarithmic scale. (b) On a linear scale.

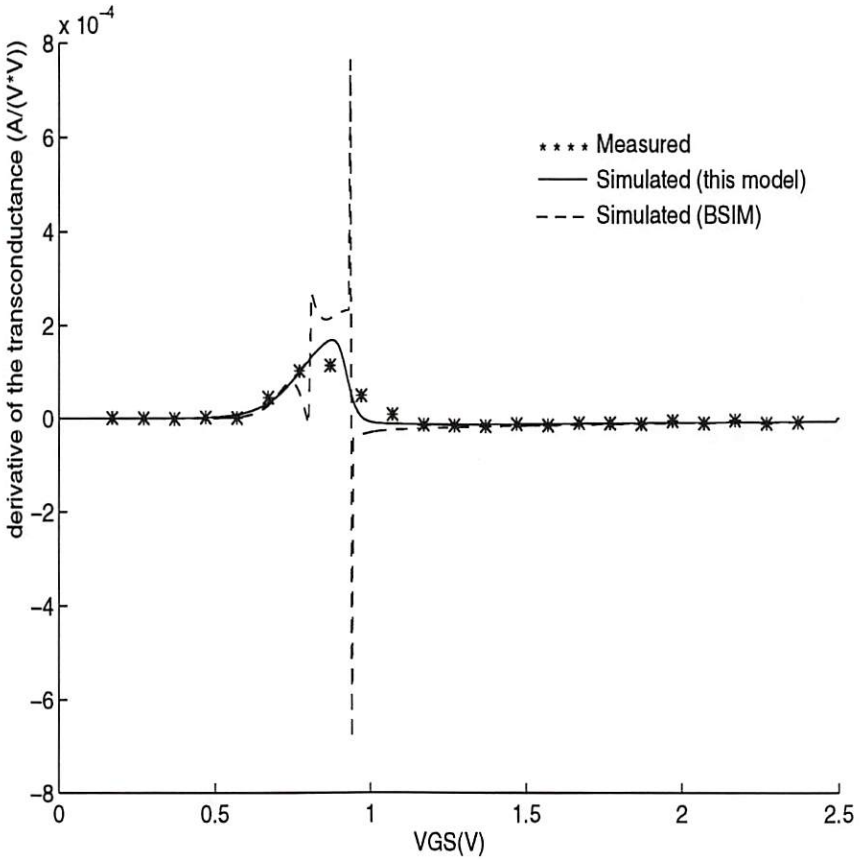


Figure 3.11: Comparison of the derivative of transconductances with respect to V_{GS} for both the BSIM and the proposed S-CMOS model.

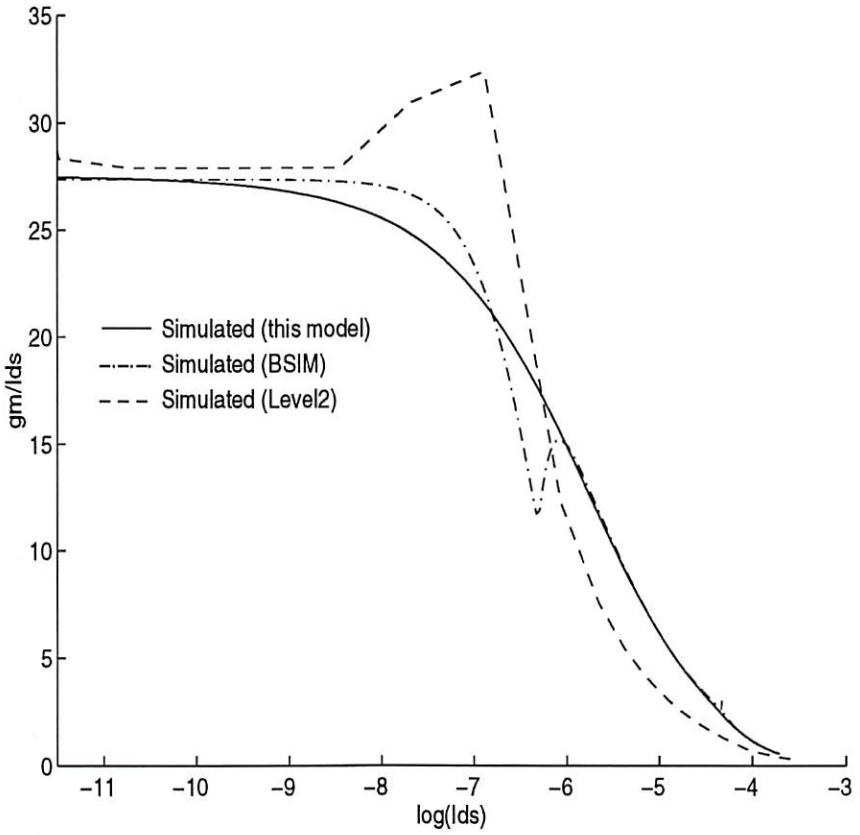


Figure 3.12: g_m/I_{DS} versus I_{DS} plot for the benchmark test suggested by Tsividis and Suyama [1]. The result of the proposed model shows smooth behavior for the curve from weak- to strong-inversion regions.

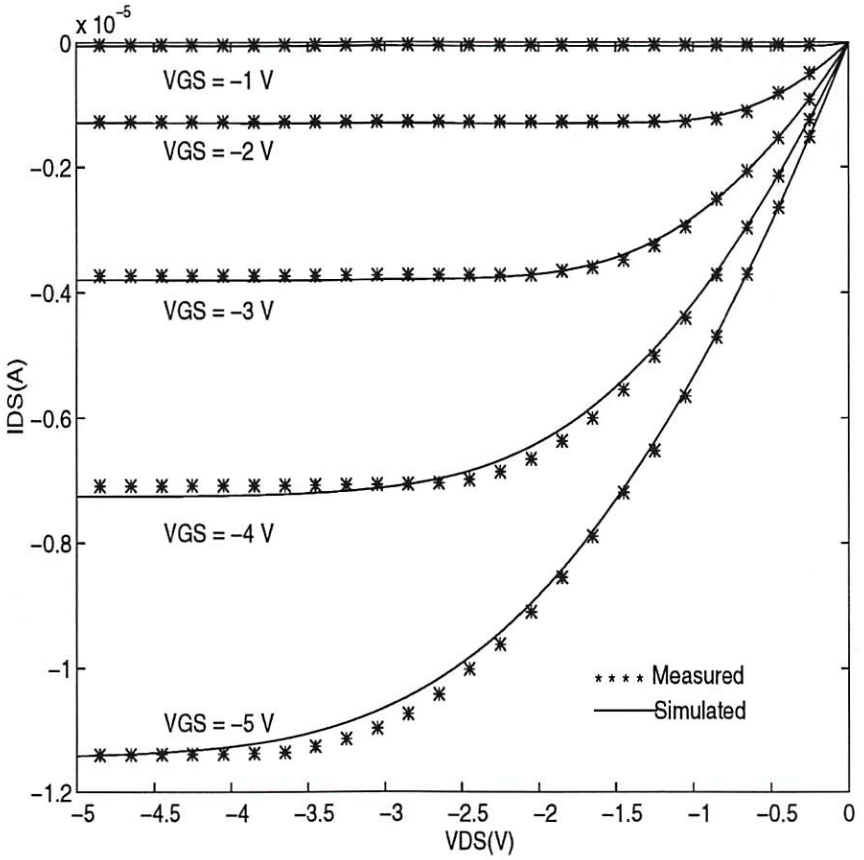
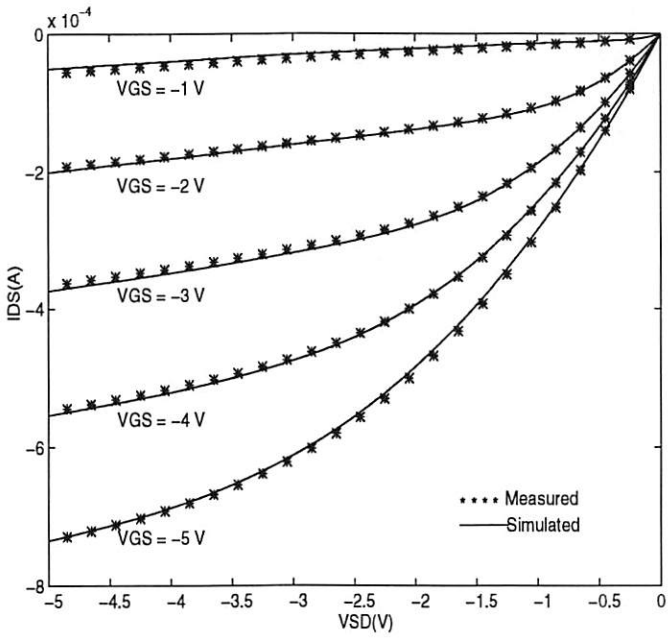
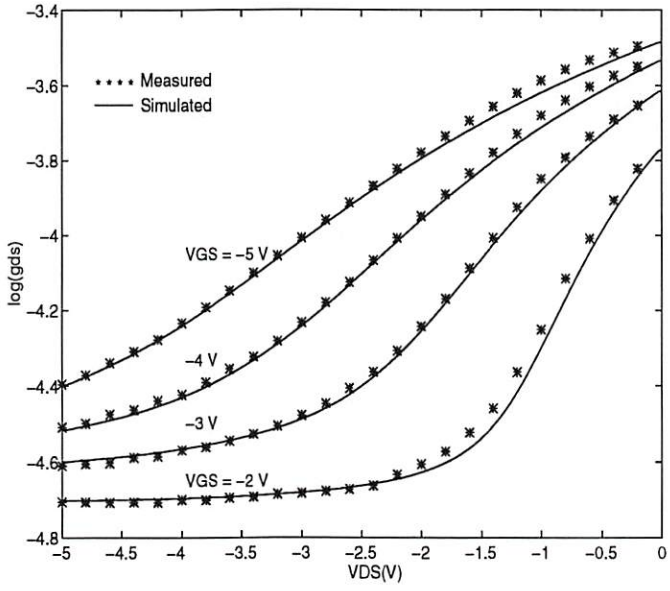


Figure 3.13: Plots of I_{DS} versus V_{DS} characteristics of a long-channel PMOS transistor with $W = 1.75\ \mu m$ and $L = 25\ \mu m$.

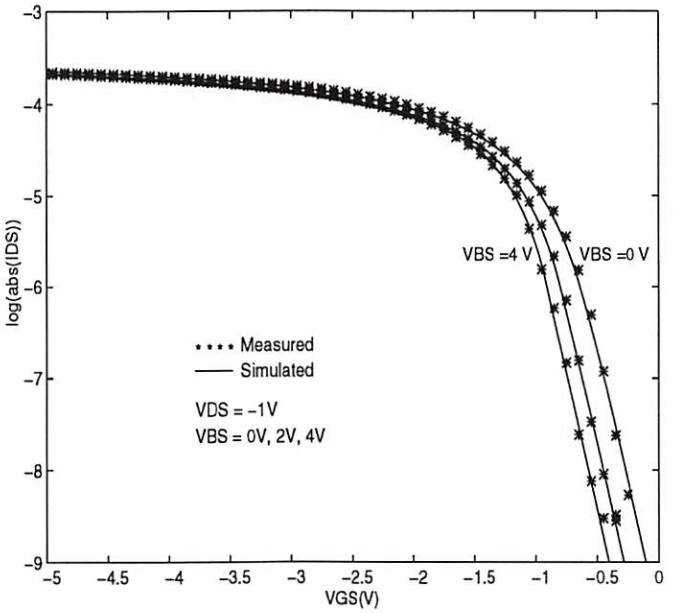


(a)

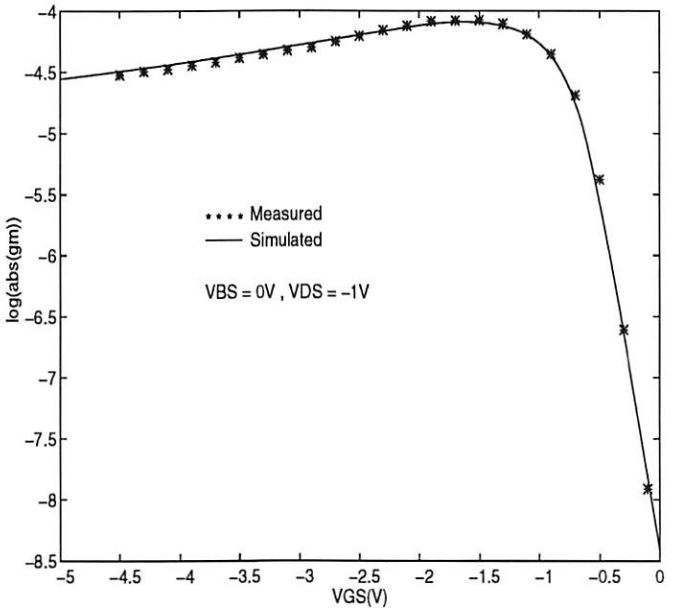


(b)

Figure 3.14: Plots of DC characteristics of a short-channel PMOS transistor with $W = 1\ \mu m$ and $L = 0.24\ \mu m$. (a) I_{DS} versus V_{DS}. (b) g_{ds} versus V_{DS}.



(a)



(b)

Figure 3.15: Plots of DC characteristics of a short-channel PMOS transistor with $W = 1\ \mu m$ and $L = 0.24\ \mu m$. (a) I_{DS} versus V_{GS}. (b) g_m versus V_{GS}.

3.3 Unified Charge/Capacitance Model

Derivation of MOS charge model is based on the quasi-static approximation [14, 19], which is suitable for many applications. The cross section of an NMOS transistor is shown in Fig. 3.16. Here, expressions for the intrinsic channel area of an MOS transistor are presented. Expressions for the extrinsic portions, including the source/drain junction capacitances, can be directly added.

3.3.1 The Charge Model

The region of operation of an MOS transistor is mainly determined by the voltage drop from the gate to the source terminals and from the drain to the source terminals. As the gate-to-source bias voltage increases and becomes higher than the threshold voltage, the transistor enters the strong-inversion region where the drain current is dominated by drift current component as contributed by the electric field. In the strong-inversion region, the drain current and channel inversion charge exhibit approximately linear behavior with respect to drain-to-source bias voltage until the channel reaches the saturation condition. The separation point between the triode and saturation regions is defined as saturation voltage, V_{DSAT}. As shown in Fig. 3.17, the saturation voltage is a function of V_{GS} which can be represented as [14, 20]

$$V_{DSAT} = \frac{V_{GS} - V_{th}}{\alpha_x}. \tag{3.29}$$

By identifying the maximum current value of strong-inversion expression, e.g. (4.4.17) in Tsividis's book [14], the saturation voltage can be obtained,

$$V_{DSAT} = V_{GS} - \phi_S - V_{FB} + \frac{\gamma_1^2}{2} - \gamma_1\sqrt{V_{GS} - V_{FB} - V_{BS} + \frac{\gamma_1^2}{4}}. \tag{3.30}$$

In this work, the differential version of α_x is used in order to slightly reduce the complexity of the expression. Therefore, α_x can be modified to be

$$\begin{aligned} \alpha_x &= \left(\frac{\partial V_{DSAT}}{\partial V_{GS}}\right)^{-1} \\ &= \left(1 - \frac{\gamma_1}{2\sqrt{V_{GS} - V_{FB} - V_{BS} + \frac{\gamma_1^2}{4}}}\right)^{-1}, \end{aligned} \tag{3.31}$$

where γ_1 is the body effect coefficient.

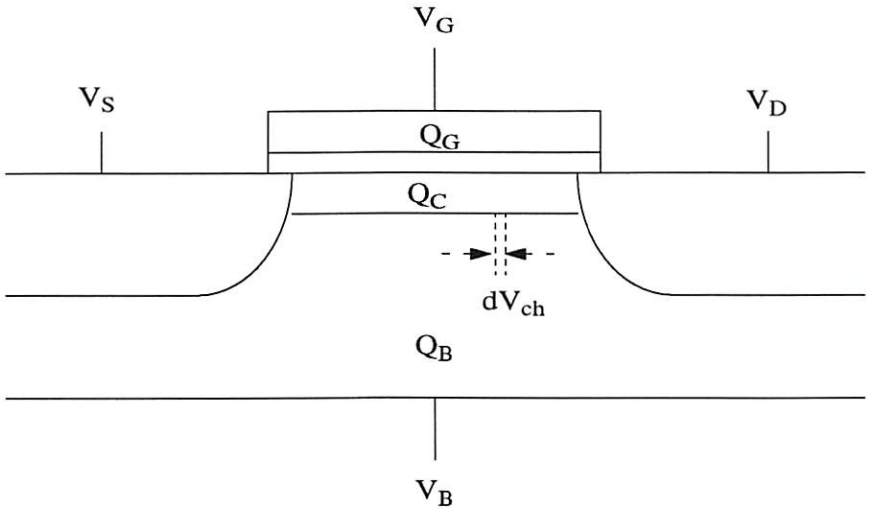


Figure 3.16: The cross section of an NMOS transistor to illustrate the space charge.

The charge of an MOS transistor is made up of three fundamental components: the charge residing on the gate electrode, q_g, the fixed charge residing in the bulk depletion layer, q_b, and the mobile channel charge residing in the channel region, q_c. By using gradual-channel approximation and depletion approximation, the charge densities in strong-inversion region can be expressed as [20],

$$q_g = C_{OX}(V_{GS} - V_{FB} - \phi_S - V_{ch}) \tag{3.32}$$

$$q_c = -C_{OX}(V_{GS} - V_{th} - \alpha_x V_{ch}) \tag{3.33}$$

and

$$q_b = -C_{OX}[V_{th} - V_{FB} - \phi_S - (1 - \alpha_x)V_{ch}]. \tag{3.34}$$

Here V_{FB} is the flat-band voltage, and ϕ_S is the surface inversion potential. Notice that the accuracy of channel and bulk charge densities is highly dependent on the accuracy of α_x.

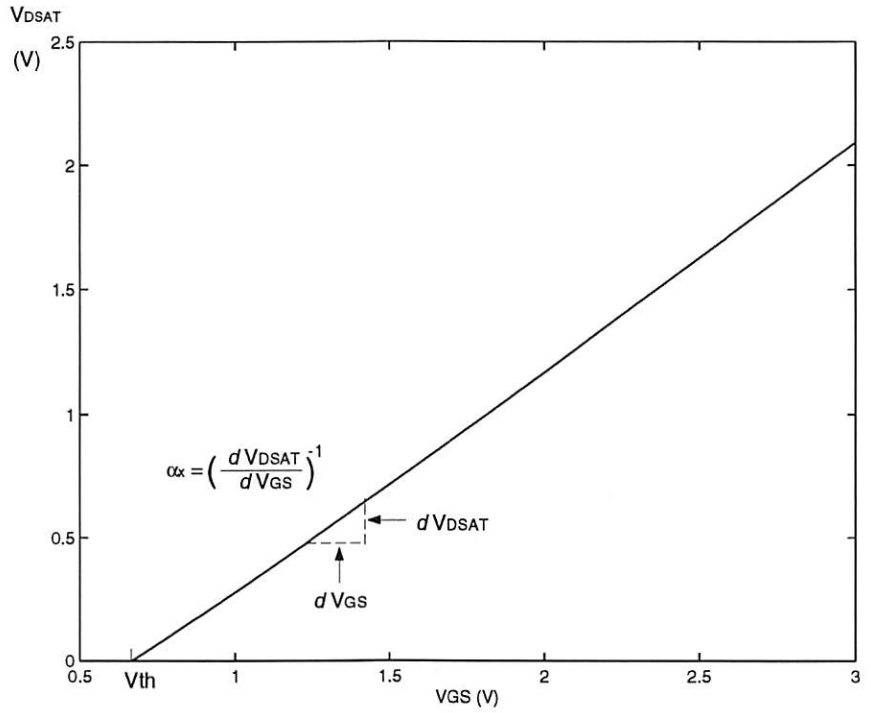


Figure 3.17: The characteristics of the saturation voltage, V_{DSAT}, with respect to the gate voltage, V_{GS}.

When the gate voltage drops below the threshold voltage, the transistor enters the weak-inversion region, and further enters the accumulation region if the gate voltage is decreased below the flat-band voltage. The gate charge density expression

becomes [14, 20]

(i) weak-inversion region

$$q_g = C_{OX}\frac{\gamma_1^2}{2}\left(-1+\sqrt{1+\frac{4(V_{GS}-V_{FB}-V_{BS})}{\gamma_1^2}}\right), \tag{3.35}$$

(ii) accumulation region

$$q_g = C_{OX}(V_{GS}-V_{FB}-V_{BS}). \tag{3.36}$$

In order to ensure the continuity of the terminal charge expressions and high accuracy of modeling the transitions between different operation regions, instead of separate charge expressions for various operation regions, the unified charge density expressions are obtained by applying the hyperbola and sigmoid techniques,

$$\begin{aligned} q_g &= C_{OX}\left[(V_{GSth}+(1-f_s)(V_{th}-V_{FB}-\phi_S)-(1-f_s)\cdot V_{ch}\right. \\ &+ \left.\frac{\gamma_1^2}{2}\left(-1+\sqrt{1+\frac{4(V_{GFh}-V_{GSth}-V_{FS})}{\gamma_1^2}}\right)+(V_{GS}-V_{GFh})\right] \end{aligned} \tag{3.37}$$

$$q_c = -C_{OX}(V_{GSth}-\alpha_x\cdot(1-f_s)\cdot V_{ch}) \tag{3.38}$$

$$q_b = -(q_g+q_c) \tag{3.39}$$

where

$$V_{GFh} = \frac{1}{2}\left(V_{GS}+K_{GFh}V_{FS}+\sqrt{(V_{GS}+K_{GFh}V_{FS})^2-4V_{GS}V_{FS}}\right) \tag{3.40}$$

and

$$V_{FS} = V_{FB}+V_{BS}. \tag{3.41}$$

Here, V_{FS} is defined as flat-band voltage referring to source terminal potential. The value of α_x is saturated when V_{GS} is smaller than V_{th}, and expression of α_x is further modified to be

$$\alpha_x = \left(1 - \frac{\gamma_1^2}{2\sqrt{V_{GSth} + V_{th} - V_{FS} + \frac{\gamma_1^2}{4}}}\right)^{-1}. \tag{3.42}$$

To unify the $(V_{GS} - V_{th})$ effects for both strong- and weak-inversion regions, a very popular interpolation function [21, 7, 22], V_{GSth}, which performs the same linear behavior as $(V_{GS} - V_{th})$ in the strong-inversion region, and reduces to the exponential decay in the weak-inversion region, is used. This function has been described in section 3.1.6.

The total charge stored in each of the gate, channel, and bulk regions is obtained by integrating the distributed charge densities, q_g, q_c, and q_b, over the channel area,

$$Q_G = W \int_0^L q_g(y) \cdot dy, \tag{3.43}$$

$$Q_B = W \int_0^L q_b(y) \cdot dy, \tag{3.44}$$

and

$$Q_C = W \int_0^L q_c(y) \cdot dy. \tag{3.45}$$

By substituting the expressions for the charge densities and performing the integration, the following expressions for the total charge can be obtained,

$$\begin{aligned} Q_G &= W_{eff} L_{eff} C_{OX} \left[\left(V_{GSth} + f_c(V_{th} - V_{FB} - \phi_S) - f_c \cdot V_{DSATh} \frac{4T_C - 1}{6T_C} \right) \right. \\ &+ \left. \frac{\gamma_1^2}{2} \left(-1 + \sqrt{1 + \frac{4(V_{GFh} - V_{GSth} - V_{FS})}{\gamma_1^2}} \right) + (V_{GS} - V_{GFh}) \right], \end{aligned} \tag{3.46}$$

$$Q_C = -W_{eff}L_{eff}C_{OX}\left(V_{GSth} - \alpha_x \cdot f_c \cdot V_{DSATh}\frac{4T_C - 1}{6T_C}\right), \tag{3.47}$$

$$Q_B = -(Q_G + Q_C), \tag{3.48}$$

where

$$f_c = 1 - f_s \ , \tag{3.49}$$

$$T_C = 1 - \frac{\alpha_x}{2}\frac{V_{DSATh}}{V_{GSth}}, \tag{3.50}$$

$$V_{DSATh} = \frac{1}{2}\left(V_{DS} + K_{DSATh}V_{DSAT} - \sqrt{(V_{DS} + K_{DSATh}V_{DSAT})^2 - 4V_{DS}V_{DSAT}}\right) \tag{3.51}$$

The saturation voltage, $V_{DSAT} = V_{GSth}/\alpha_x$, is valid for both the weak- and strong-inversion regions. The hyperbola function, V_{DSATh}, is used to describe the saturation behavior of the charge expression when the transistor operates in the saturation regions [6].

3.3.2 Channel-Charge Partitioning Methods: 40/60, 0/100, 50/50

To complete the charge model, expressions for the drain and source terminal charges should also be included. This can be done by channel-charge partitioning. Three channel-charge partitioning schemes are used for the S-CMOS model.

(A) 40/60 channel-charge partitioning

A physically meaningful 40/60 partitioning scheme as for the drain and source terminal charges, developed by Ward [23], is defined by

$$Q_D = W \int_0^L \frac{y}{L} \cdot q_c \cdot dy,$$
$$Q_S = W \int_0^L \left(1 - \frac{y}{L}\right) \cdot q_c \cdot dy. \tag{3.52}$$

By carrying out the integration, the charges associated with the drain and source terminals are obtained,

$$Q_D = -W_{eff} L_{eff} C_{OX} V_{GSth} \left(\frac{-1}{2} + T_C + \frac{(1 - T_C)(1 + 3 \cdot T_C + 6 \cdot T_C^2)}{30 \cdot T_C^2}\right), \tag{3.53}$$

$$Q_S = -W_{eff} L_{eff} C_{OX} V_{GSth} \left(\frac{1}{2} + \frac{(1 - T_C)^2}{3 \cdot T_C} - \frac{(1 - T_C)(1 + 3 \cdot T_C + 6 \cdot T_C^2)}{30 \cdot T_C^2}\right) \tag{3.54}$$

(B) 0/100 channel-charge partitioning

The 0/100 channel-charge partitioning method can be derived using the following boundary conditions,

- Charges Q_S and Q_D are equal and capacitances C_{sg} and C_{dg} are equal when V_{DS} is zero.
- In the saturation region, all the channel mobile charge is only associated with the source, and Q_D is zero [24].
- For the simplicity of model equations, partition is done using the existing terms in the Q_C expression. No additional terms are introduced.

Therefore, expressions for the drain and source terminal charges are derived,

$$Q_D = -W_{eff} L_{eff} C_{OX} V_{GSth} \left(-1 + \frac{3T_C}{2} + \frac{(1 - T_C)^2}{2T_C}\right), \tag{3.55}$$

$$Q_S = -W_{eff}L_{eff}C_{OX}V_{GSth}\left(1 - \frac{T_C}{2} - \frac{(1-T_C)^2}{6\cdot T_C}\right). \tag{3.56}$$

(C) 50/50 channel-charge partitioning

The 50/50 channel-charge partitioning scheme is simply dividing the channel charge to equally,

$$Q_D = -\frac{1}{2}W_{eff}L_{eff}C_{OX}\left(V_{GSth} - \alpha_x \cdot f_c \cdot V_{DSATh}\frac{4T_C - 1}{6T_C}\right), \tag{3.57}$$

$$Q_S = -\frac{1}{2}W_{eff}L_{eff}C_{OX}\left(V_{GSth} - \alpha_x \cdot f_c \cdot V_{DSATh}\frac{4T_C - 1}{6T_C}\right). \tag{3.58}$$

3.3.3 The Capacitance Model

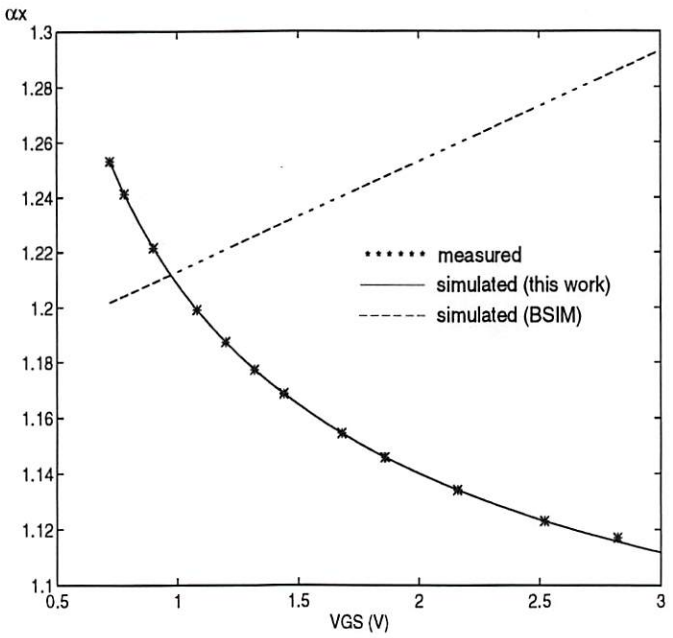
The inter-nodal capacitances are represented as derivatives of the terminal charges, Q_G, Q_B, Q_D, and Q_S, with respect to the terminal voltages, i.e.,

$$C_{ij} = x_{ij}\frac{\partial Q_i}{\partial V_j} \quad , \tag{3.59}$$

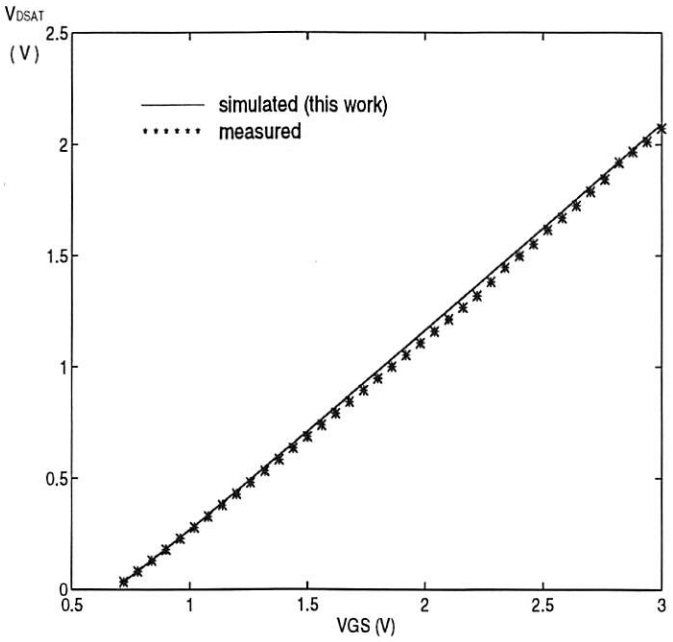
where the indices i and j represent any of the four terminals, gate, bulk, drain, or source. $x_{ij} = -1$ for $i \neq j$, and $x_{ij} = 1$ for $i = j$. The differentiation of these charge expressions is also unified through all operation regions.

3.4 Experimental Results of Charge/Capacitance Model

The unified MOS transistor charge/capacitance model has been developed to accurately model the behavior of back gate degradation coefficient. As shown in Fig. 3.18(a), the value of α_x decreases with the increase of the gate voltage. The



(a)



(b)

Figure 3.18: Plots of the back gate degradation coefficient, α_x, and saturation voltage, V_{DSAT}. (A) α_x vs. V_{GS}. (B) V_{DSAT} vs. V_{GS}.

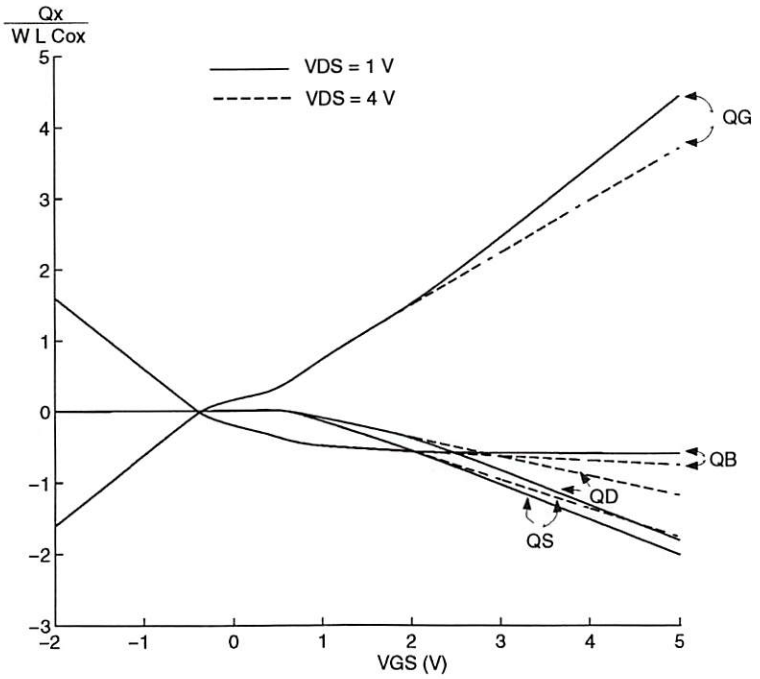


Figure 3.19: Normalized terminal charges versus gate bias for two drain voltages with $V_{BS} = 0V$.

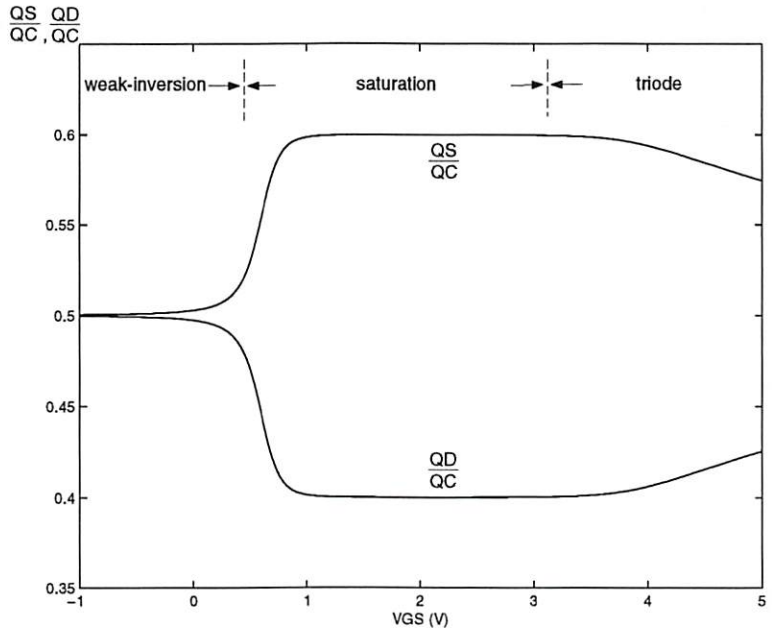


Figure 3.20: Plots of drain and source charges in different operation regions. The ratio of drain charge to source charges is 40/60 in the saturation region.

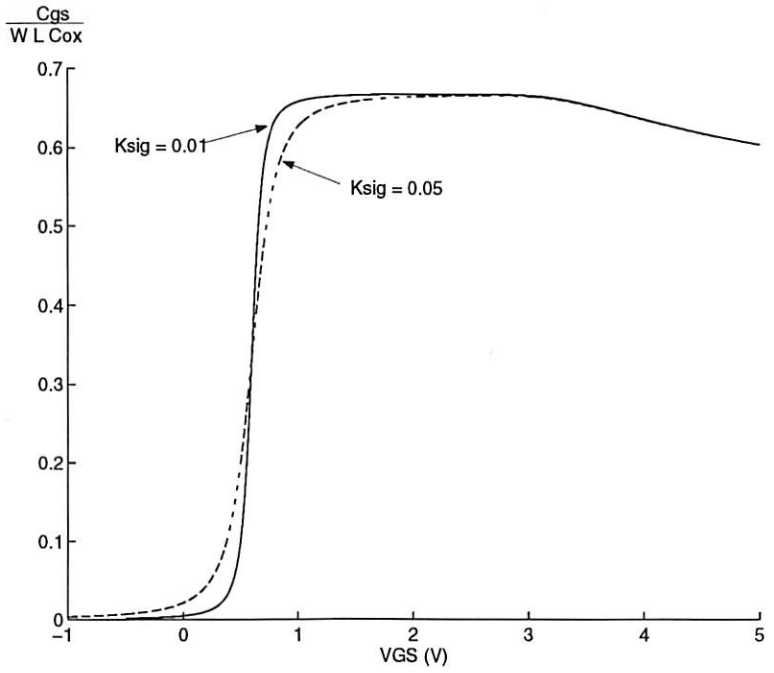


Figure 3.21: Plots of normalized C_{gs} versus V_{GS} for two K_{sig} values.

original BSIM1 model [20] did not handle the α_x behavior properly. Figure 3.18(b) shows the comparison of simulated results and measured data of V_{DSAT} for different gate voltages.

Figure 3.19 shows the normalized plots of the four terminal charges of a short-channel MOS transistor with the 40/60 channel-charge partitioning method. The normalization factor is $(W_{eff}L_{eff}C_{OX})$. Notice that the unified charge expressions are continuous over all operation regions. Figure 3.20 shows the plots of source and drain charges in different operation regions with $V_{DS} = 2.5\ V$. The ratio of the drain charge to the source charge is 40/60 in the saturation region and smoothly changes to 50/50 as the gate voltage becomes much larger than the drain voltage. The sigmoid function, f_s, facilitates the smooth transition between the weak- and strong-inversion regions. Here, fitting parameter, K_{sig}, helps to model the curvature of capacitances at the transition portion, as shown in Fig. 3.21. The plots of gate

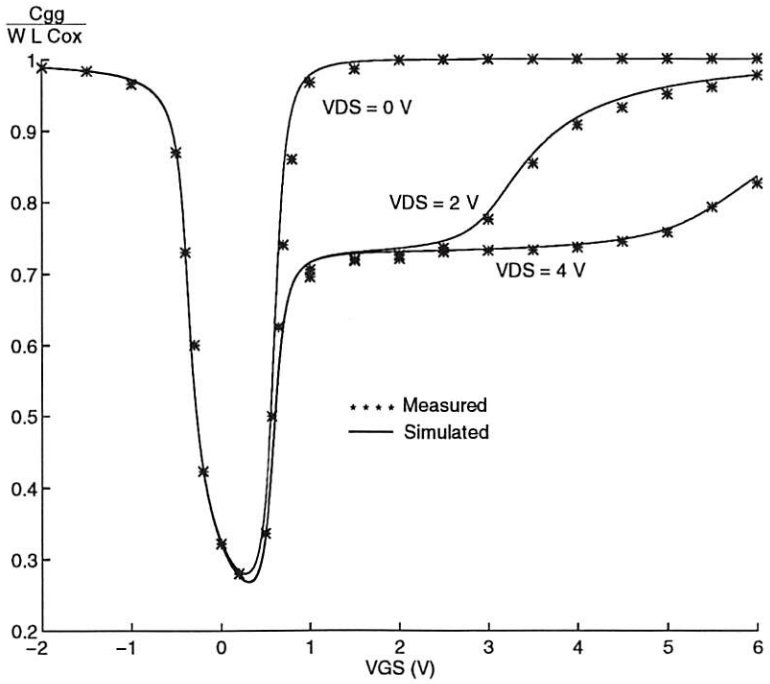
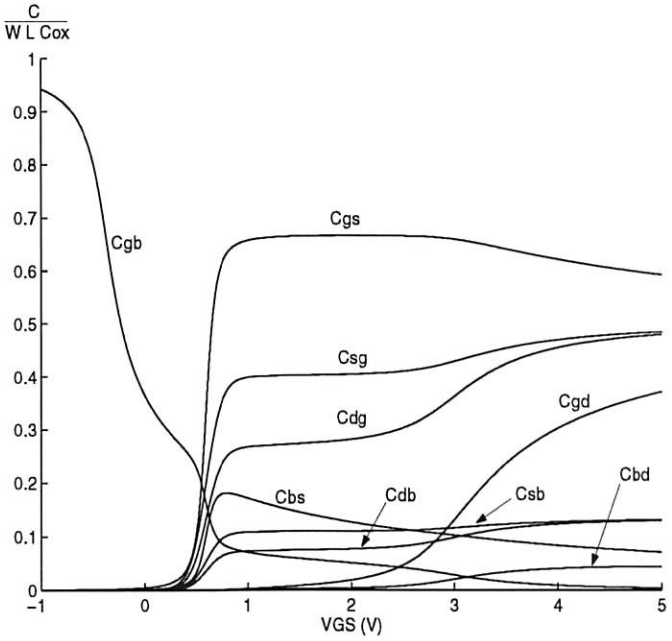


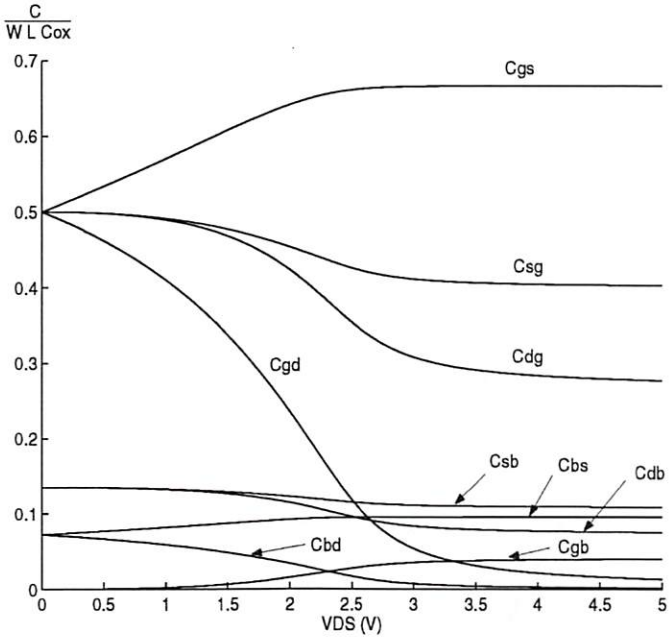
Figure 3.22: Normalized gate capacitance, C_{gg}, versus gate bias from accumulation to strong-inversion regions with $V_{BS} = 0V$ for an MOS transistor of W/L = 100 $\mu m/0.8$ μm.

capacitances are shown in Fig. 3.22. The calculated results agree well with the experimental data for different drain voltages.

In the time-domain large-signal analysis and frequency-domain small-signal analysis for the charge-based approach, 16 charge derivatives are needed in the assembly of the nodal admittance matrix. These derivatives may be regarded as inter-nodal capacitances. To form the matrix, nine of the 16 capacitances are independent [23]. Figure 3.23(a) and (b) show the normalized plots of nine capacitances against the gate voltage and drain voltage, respectively. Notice that the capacitance curves are smooth throughout all operation regions. The non-reciprocal capacitance property is also clearly shown. Comparison of measured and calculated results of the capacitances associated with gate and bulk terminals for an $L_{eff} = 0.35$ μm transistor is



(a)



(b)

Figure 3.23: Plots of nine normalized capacitances. (A) Capacitances versus V_{GS} with $V_{DS} = 2\ V$ and $V_{BS} = 0\ V$. (B) Capacitances versus V_{DS} with $V_{GS} = 3.5\ V$ and $V_{BS} = 0\ V$.

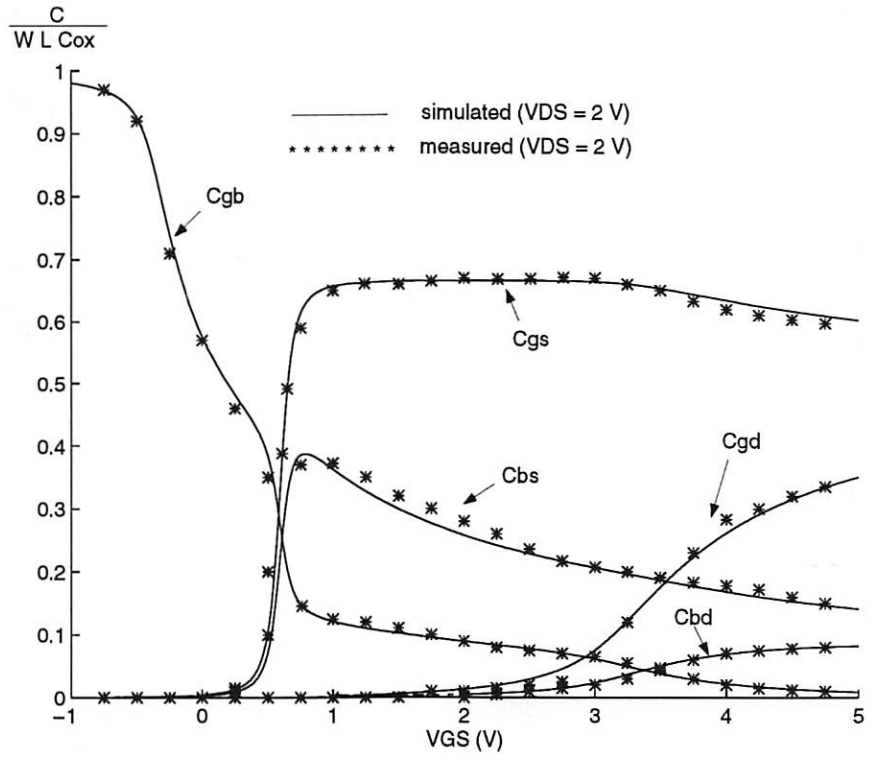


Figure 3.24: Plots of normalized capacitances versus V_{GS} of an NMOS transistor of W/L = 25 μm/0.35 μm for two V_{DS} values.

shown in Fig. 3.24. Good agreement between measured data and calculated results has been obtained.

Reference List

[1] M. Nishida, H. Onodera, "An anomalous increase of threshold voltages with shortening the channel lengths for deeply boron-implanted n-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-28, pp. 1101-1103, 1981.

[2] M. Orlowski, C. Mazure, F. Lau, "Submicron short channel effects due to gate reoxidation induced lateral interstitial diffusion," *IEDM Tech. Dig.*, pp. 632-635, 1987.

[3] C. Y. Lu, J. M. Shung, "Reverse short-channel effects on threshold voltage in submicrometer salicide devices," *IEEE Electron Device Letters*, vol. 10, pp. 446-448, 1989.

[4] N. Arora, M. Sharma, "Modeling the anomalous threshold voltage behavior of submicrometer MOSFET's," *IEEE Electron Device Letters*, vol. 13, no. 2, pp. 92-94, Feb. 1992.

[5] S. M. Gowda, B. J. Sheu, "BSIM_plus: An advanced SPICE model for submicron MOS VLSI circuits," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 13, no. 9 , pp. 1166-1170, Sep. 1994.

[6] A. Chatterjee, C. F. Machala, P. Yang, "A submicron DC MOSFET model for simulation of analog circuits," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 14, no. 10, pp. 1193-1207, Oct. 1995.

[7] C. C. Enz, F. Krummnacher, E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *J. Analog Integrated Circuits and Signal Processing*, Kluwer Academic Publishers, vol. 8, no. 1, pp. 83-114, Jul. 1995.

[8] H. Oguey, S. Cserveny, "MOS modelling at low current density," summer Course on "Process and Device Modelling," ESAT Leuven-Heverlee, Belgium, June 1983.

[9] H. Oguey, S. Cserveny, "Modele du transistor MOS valable dans un grand domaine de vourants," *Bull. SEV/ VSE*, Feb. 1982.

[10] Y. P. Tsividis, K. Suyama, "MOSFET modeling for analog circuit CAD: problems and prospects," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 210-216, Mar. 1994.

[11] A. R. Boothroyd, S. W. Tarasewocz, C. Slaby, "MISNAN-A physically based continuous MOSFET model for CAD applications," *IEEE Tran. on Computer-Aided Design*, vol. 10, no. 12, pp. 1512-1529, Dec. 1991.

[12] A. I. A. Cunha, S. M. Acosta, M. C. Schneider, C. Galup-Montoro, "An explicit MOSFET model for analog circuit simulation," *IEEE ISCAS 1995*, vol. 3, pp. 1592-1595, Apr. 1995.

[13] G. A. Machado, C. C. Enz, M. Bucher, "Estimating key parameters in the EKV MOST model for analogue design and simulation," *IEEE ISCAS 1995*, vol. 3, pp. 1588-1591, Apr. 1995.

[14] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw-Hill: New York, NY, 1987.

[15] B. J. Sheu, D. L. Scharfetter, P. Ko, "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE J. Solid-State Circuits*, vol. sc-22, no. 4, pp.558-566, Aug. 1987.

[16] T. Poorter, and J. H. Satter, "A DC model for an MOS transistor in the saturation region," *Solid-State Electron.*, vol. 23, no. 7 , pp. 765-772, 1980.

[17] A. Vladimirescu, S. Liu, *The Simulation of MOS Integrated Circuits Using SPICE2*, Memo ERL-M80/7, Electronics Res. Lab., Univ. of California, Berkeley, Oct. 1980.

[18] H. J. Park, P. K. Ko, C. Hu, "A charge sheet capacitance model of short channel MOSFET's for SPICE," *IEEE Trans. on Computer-Aided Design*, vol. 10, no. 3, pp. 376-389, Mar. 1991.

[19] M. Shur, *Physics of Semiconductor Devices*, Prentice-Hall: Englewood Cliffs, NJ, 1990.

[20] B. J. Sheu, W.-J. Hsu, P. K. Ko, "A MOS transistor charge model for VLSI design," *IEEE Trans. on Computer-Aided Design*, vol. 7, no. 4, pp. 520-527, Apr. 1988.

[21] R. Velghe, D. Klaassen, F. Klaassen, "MOS Model 9", *Unclassified Report NL-UR 003/94*, Philips Electronics, N.V., Netherland, 1994.

[22] *BSIM3v3 Manual*, Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley, 1995-1997.

[23] D. E. Ward, "Charge-based modeling of capacitance in MOS transistor," Ph.D. dissertation, Tech. Rep. G 201-11, Integrated Circuit Laboratory, Stanford University, June 1981.

[24] P. Yang, B. Epler, P. Chatterjee, "An investigation of the charge conservation problem for MOSFET circuit simulation," *IEEE Jour. of Solid State Circuits*, vol. SC-18, no. 1, pp. 128-138, Feb. 1983.

Chapter 4

Parameter Extraction

Performance of the MOS transistor model during circuit simulation depends on the parameter set that is used with the model. Parameter extraction for the MOS transistor model is a complicated task due to the large number of parameters that need to be optimized over a wide range of bias conditions and transistor geometries for the design space. The appropriate extraction methodology depends on the model and is sometimes influenced by particular applications. The important issues that must be resolved in the parameter extraction procedure include:

- clear understanding of physical meaning of each parameter,
- number of transistors and the transistor geometries for which measured data are required,
- terminal voltage biases for which data are required, and
- choice of transistor characteristics to be optimized.

4.1 Properties of Parameters of The S-CMOS Model

The MOS transistor model described in this research includes several important effects of submicron technology from different operation regions. It is equipped with 35 model parameters, as listed in Table 4.1. The parameters can be summarized into three subgroups as the primary physical parameters, secondary physical parameters for fitting, and smooth function parameters.

4.1.1 Primary Physical Parameters

The primary physical parameters strongly represent the key device behavior. Most of the parameters in this category can be determined directly from local extraction of measured data without global optimization. As listed in Table 4.1, this subgroup includes $t_{ox}, \phi_s, V_{FB}, \gamma_1$, and μ_0. This group of parameters can be used to determine characteristics of transistors with large channel length and width.

The gate-oxide thickness, t_{ox}, can be directly determined from the devices measured data. The flat-band voltage, V_{FB}, and the surface inversion potential, ϕ_s, are the main contribution to the zero-bulk-bias threshold voltage, V_{tho}, which can be extracted by calculating the threshold voltage from the low drain-bias measurement. The intrinsic surface mobility, μ_0, can be extracted from the drain current behavior with respect to the gate voltage between the measured data and modeled results under the zero-bulk-bias and low-drain-bias conditions.

4.1.2 The Fitting Parameters

The fitting parameters are used to model the device effects including short-channel/reverse short-channel effects, narrow-channel effects, body-effect, velocity

Table 4.1: S-CMOS model parameters for a 0.5 μm technology. (a) Primary physical parameters. (b) Secondary physical parameters. (c) Smooth function parameters.

(a) Primary physical parameters.

Name	Description (primary physical parameters)	Value (NMOS)	Value (PMOS)	Unit
ϕ_s	surface inversion potential	1.05	0.93	V
V_{FB}	flat-band voltage	-0.4	-0.33	V
T_{ox}	gate oxide thickness	90	90	nm
μ_0	intrinsic surface mobility	450	130	cm^2/Vs
dL	channel length reduction	0	0	µm
dW	channel width reduction	0	0	µm
γ_1	zero-bias body-effect coeff.	0.421	0.563	$V^{0.5}$

saturation effects, mobility reduction due to the transverse and lateral electric fields, and channel-length modulation effects. The optimization steps are usually used to extract the fitting parameter values. We have to pay attention to three key issues for this type of extraction: optimization algorithm, bias conditions of measured data and modeled results, and the number of transistors and the transistor sizes chosen for optimization. Twenty-four secondary physical parameters are used to properly model deep-submicron MOS transistors. In the S-CMOS model, the goal is to enhance the model accuracy for deep-submicron applications. Therefore, accurate extraction of the secondary physical parameters is very important to ensure the model applicability for advanced technologies.

Table 4.1 (continued): (b) Secondary physical parameters.

Name	Description (secondary physical parameters)	Value (NMOS)	Value (PMOS)	Unit
γ_{1L}	zero-bias short-channel body-effect coeff.	0.03	0.06	$V^{0.5}$-µm
γ_2	high-bias body-effect coeff.	0.328	0.309	$V^{0.5}$
K_S	depletion charge-sharing coeff.	2.7	3.4	-
K_{NZ}	narrow-width threshold voltage coeff.	0.244	0.217	V-µm
k_{NB}	narrow-width threshold voltage substrate coeff.	5.4e-4	-3.9e-4	µm
η_Z	drain-induced barrier lowering coeff.	0.002	-0.005	-
η_L	short-channel barrier lowering coeff.	0.001	0.038	µm
η_1	short-channel threshold voltage reduction coeff.	0	0	V-µm
η_2	characteristics length of reverse short-channel effect	0	0	V-µm
η_3	reverse short-channel coeff.	1	1	µm
U_{GSZ}	gate-voltage mobility degradation coeff.	0.02	0.1	V^{-1}
U_{GSZ2}	gate-voltage mobility degradation 2nd-order coeff.	0.02	0.1	V^{-1}
U_{GSL}	short-channel adjustment of u_{gsz}	0.06	-0.1	V^{-1}µm
U_{GSL2}	second-order short-channel adjustment of u_{gsz}	0.06	-0.1	V^{-1}µm
U_{DS}	drain-voltage mobility degradation coeff.	0.08	0.01	V^{-1}
U_{BS}	substrate-voltage mobility degradation coeff.	0.005	0.02	V^{-1}
N	subthreshold drain current slope	1.5	1.5	-
k_{sub}	subthreshold current shifting coeff.	5	0.1	-
E_{crit}	critical electric field for velocity saturation	10	10	V/µm
λ_D	drain-voltage dependent CLME coeff.	0.001	1.15	V^{-1}
λ_G	gate-voltage dependent CLME coeff.	0.1	3.5	$V^{3/2}$
λ_B	substrate-voltage shifting CLME coeff.	2	2	-
λ_{BS}	substrate-voltage dependent CLME coeff.	1	1	V
ϕ_d	drain-voltage related CLME potential	0.5	0.1	V

Table 4.1 (continued): (c) Smooth function parameters.

Name	Description (smooth function parameters)	Value (NMOS)	Value (PMOS)	Unit
K_{BSh}	bulk bias hyperbola function coeff.	1.01	1.01	-
K_{DSATh}	strong-inversion hyperbola function coeff.	1.03	1.05	-
K_{GSh}	gate-threshold hyperbola function coeff.	1.01	1.01	-
K_{sig}	sigmoid function coeff.	0.01	0.01	-

4.1.3 The Smooth-Function Parameters

In order to unify the model expressions to be valid for all operation regions, several smooth functions are applied to achieve better transitions between different regions. In S-CMOS model, there are three types of smooth functions: sigmoid function, hyperbola function, and exponential interpolation function. The exponential interpolation function is widely used to model $V_{GS}-V_{th}$ from the weak-inversion region to the strong-inversion region, which performs the exponential behavior in the subthreshold and approaches square term in strong-inversion region. There is no parameter required in this function. The sigmoid function, f_s, is also used to smooth out the transition between the weak- and strong-inversion regions for high-order effects, and is equipped with one parameter. The hyperbola function is used to achieve better transition between the triode and saturation regions, and is equipped with another parameter. In this model, all the smooth function parameters are first set to the default values while extracting other model parameters, which are $K_{sig} = (V_t/4\phi_s)$ and $K_{GSh} = K_{DSATh} = K_{BSh} = (1 + V_t/4\phi_s)$. The extraction of those 4 parameters is done at the latter step by optimizing the transitions between different operation regions. The effect of this step is to achieve better fitting at those transitions.

4.2 Extraction Strategy

Parameter extraction is a very critical part for VLSI circuits development. There are several issues that affect the accuracy of the extraction results, including the optimization strategy, device sizes selected to be optimized, and the number of parameters to be optimized.

4.2.1 Optimization Method

There are two different optimization strategies: local determination and global optimization. Global optimization relies on the explicit use of computer software to find one set of model parameters which will best fit the experimental data. This methodology may produce the minimum average error between measured and simulated data points. But it also treats each parameter as an empirical parameter without strong consideration of their physical meaning. In the local determination approach, many parameters are extracted independently. Parameters are extracted from unique bias conditions which correspond to the dominant physical mechanisms. To properly execute the local determination, the bias condition has to be carefully selected for each extraction step. A combination of the local determination and global optimization will be most suitable.

4.2.2 Geometric Space

Some strategies available for extraction parameters: the single device extraction strategy and group device extraction strategy; the extraction for global parameter values and "binning" extraction strategy. In single device extraction strategy, experimental data from a single transistor are used to extract a complete set of model parameters. This strategy will fit on one device very well, but it does not

fit other devices with other sizes. Furthermore, single device extraction strategy can not guarantee that the extracted parameters have strong physical meaning. On the other hand, for the short-channel or narrow-channel effects, if we just use the "corner" devices in the extraction, the results might not be properly for the devices with the intermediate geometries. The group device extraction usually requires a device with large channel length and width, one set of devices with different channel length, and one set of devices with different channel width. However, the results might not be the best "fitting" for each individual device. Furthermore, this type of extraction consumes more computer time for the optimization. The number of devices and their sizes in each set have to be properly determined in order to achieve a good accuracy with reduced extraction time.

Most of the MOS models were developed to cover all the device geometries of the design space with one set of parameter values. However, the extraction accuracy is usually not suitable for various applications. The key reasons are improper inclusion of higher-order effects in the model expressions and selection of parameters. A very common solution used in the microelectronics industry is "binning", which breaks the whole geometry space into sub-regions. The extraction is done within each sub-region. Partitioning of the sub-regions depends on the specific application and the given fabrication technology. This approach provides higher accuracy but requires more extraction time. In order to accommodate the binning for better results, there is an explicit formula for parameters which is introduced by HSPICE Level-28 model [2] as an extension to the original BSIM1 model [1],

$$Z = Z_0 + Z_L \cdot (\frac{1}{L} - \frac{1}{L_{ref}}) + Z_W \cdot (\frac{1}{W} - \frac{1}{W_{ref}}) + Z_P \cdot (\frac{1}{L} - \frac{1}{L_{ref}}) \cdot (\frac{1}{W} - \frac{1}{W_{ref}}) \quad (4.1)$$

The reference geometries which are the right-upper corner devices of the sub-regions are introduced to enhance the accuracy. By doing so, the number of parameters becomes quadrupled [2, 3]. In fact, it is not necessary to apply this structure to all the parameters.

4.3 The Efficient DC Parameter Extraction for S-CMOS

The S-CMOS model uses a selective way to include the geometry dependence only in certain parameters, e.g. γ_{1L}, K_{NZ}, etc. With this development technique, the model parameter set can be minimized while includes most of the small-geometry effects. The efficient DC parameter extraction is designed based on the properties of the S-CMOS model by considering the physical behavior of each parameter in the model equations. Due to the availability of the optimization software program, the extraction program has been developed by the m-code for MATLAB software [4], which can be run on most of the computer platform, including MS windows, Mcintosh, and Unix system.

4.3.1 The Parameter Extraction Procedure

The proposed extraction procedure is developed based on the basic property of each parameter. In order to simplify the initial extraction condition, the extraction should be started from a large device to exclude the short-channel and narrow-channel effects. The threshold voltage is the first step to be focused. The parameters, γ_1, and V_{FB} can be extracted by optimizing the expression of α_x with the measured data. The zero-bulk biased threshold voltage, $V_{tho} = V_{FB} + \phi_s$, is extracted from the I_{DS} vs. V_{GS} measurement. The short-channel and narrow-channel effects on the

threshold voltage are extracted by optimizing the expression with the measured data of the threshold voltages on different transistors with different channel lengths, and channel widths, respectively. The reverse short-channel effect modeled by η_1, η_2, and η_3 is extracted from the threshold voltages with different channel lengths. The extraction of non-uniform substrate doping effect parameters, γ_2, K_S, is done by curve fitting. In order to extract the intrinsic mobility and vertical field-effect parameter values, the measured data have to be done with a small V_{DS} value to reduce the saturation-region effects. The subthreshold parameters, K_{sub} and n, are extracted by optimizing the I_{DS} characteristics in the weak-inversion region. The critical field parameter, E_{crit}, affects the saturation voltage and velocity saturation effect. It can be extracted by optimizing the I_{DS} vs. V_{DS} characteristics. The channel-length modulation effect parameters are used to model the output conductance characteristics in the saturation region especially for short-channel devices. Therefore the extraction should be done by fitting drain current and output conductance curves in the saturation regions. All the smooth function parameters are extracted at the last step to fine-tune the behavior at the transitions between different operation regions.

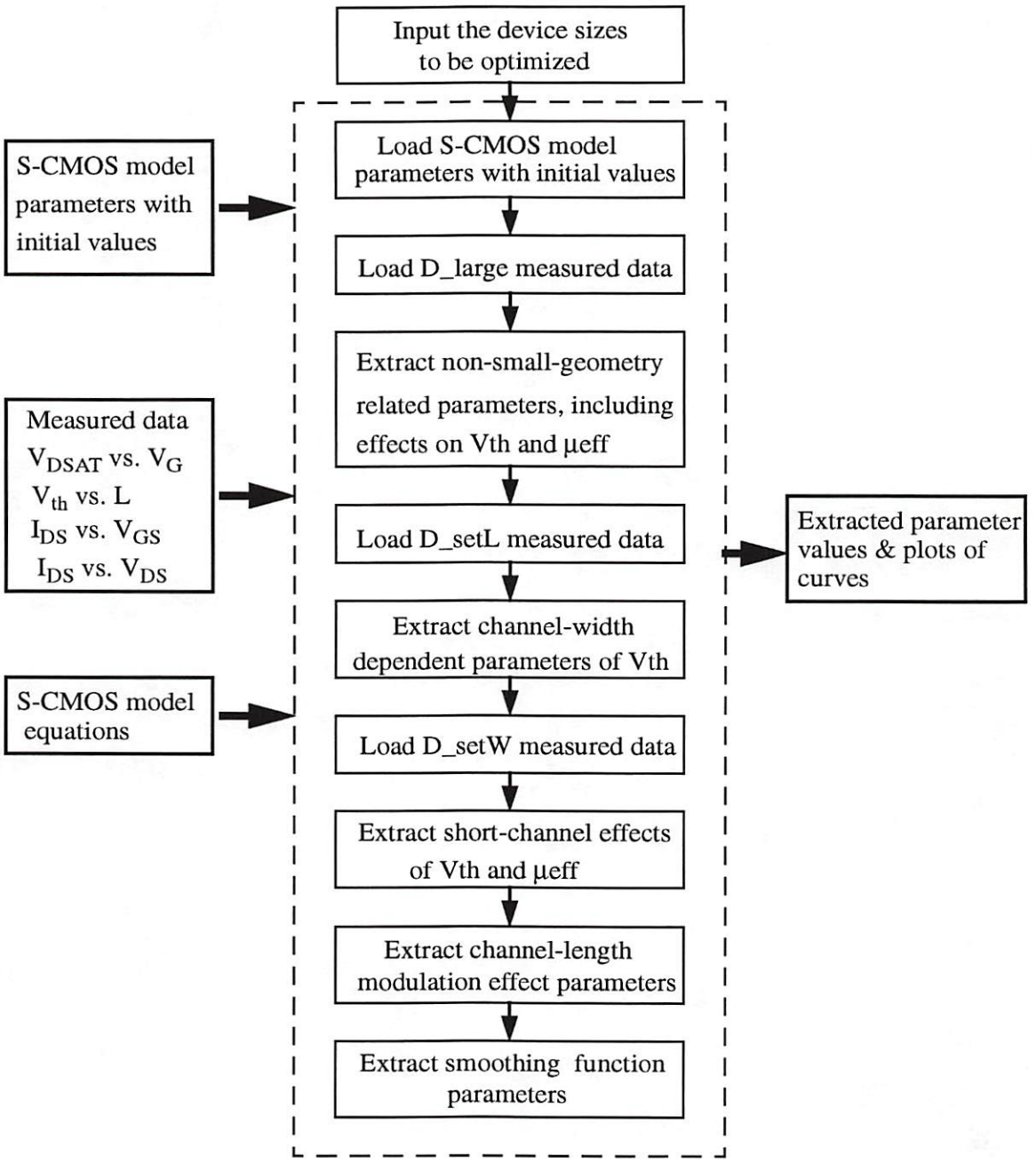
4.3.2 S-CMOS Model Extractor in MATLAB

In most of model extractions, either the specific extraction software or the interface between the optimization program and SPICE simulator are required in order to extract the parameters of a specific model. Usually, the extraction program is implemented by the user instead of the model developer. This may result in user-dependent parameter values and accuracy due to the understanding of model characteristics. MATLAB [4] is a popular mathematical software which can run in most of the computer platforms, and has almost the best availability to the users. Parameter extraction of the S-CMOS model is implemented in MATLAB m-code.

The core of the extraction program is controlled by a main routine following the flowchart as show in Fig. 4.1. All the measured data are stored in the data bank. The S-CMOS model equations, parameter set, and all the optimization steps are implemented in the separate m-code functions. The minimum set of transistors for the complete extraction includes a large transistor, a short-channel transistor, and a narrow-channel transistor. All of those transistors should include the measured data of V_{DSAT} versus V_G, I_{DS} versus V_{GS} with different $V'_{BS}s$, and I_{DS} versus V_{DS} with different $V'_{GS}s$. For extracting the reverse short-channel effect and accurately modeling the threshold voltage, additional measurement of threshold voltage for different channel lengths has to be performed.

The extraction starts from the zero-bias threshold voltage, V_{tho}, which can be obtained from V_{DSAT} versus V_G measurement, i.e., $V_{tho} = V_G \mid_{V_{DSAT}=0}$. As shown in Fig. 4.2, parameters, η_1, η_2, and η_3, can be extracted by fitting the threshold voltage behavior with $V_{BS} = 0\ V$ and V_{DS} being close to $0\ V$. The flat-band voltage, V_{FB}, and body-effect coefficient, γ_1, are the major parameters affecting the saturation voltage behavior, V_{DSAT}. Therefore, they can be extracted from a large transistor, as shown in Fig. 4.3. The non-uniform substrate doping effect causes the change of threshold voltage with different V_{BS} biases. This effect is modeled by parameters, γ_1, γ_2, and K_S to include the second-order term. Figure 4.4 shows the extraction of γ_2 and K_S values from V_{th} versus V_{BS} with a small V_{DS} to exclude the drain-induced barrier lowering effect.

Once the threshold voltage characteristics of a large device are determined, the drain current characteristics can be used to extract the effective mobility. In S-CMOS, the effective mobility is described by a reduction factor to include the vertical- and horizontal-field effects. With a large device, the effects of the mobility reduction are observed. To extract the vertical-field effect, the I_{DS} versus V_{GS}



D_large : A large device with long channel length and wide channel width

D_setL : A set of devices with long channel length and different channel widths

D_setW : A set of devices different channel lengths and wide channel width

Figure 4.1: The flowchart of the S-CMOS model parameter extraction.

characteristics with different V_{BS} biases are used to determine the intrinsic mobility, μ_0, and parameters, U_{GSZ}, U_{GSZ2} and U_{BS}. Notice that, in this step, the horizontal-field effect has to be excluded by setting $V_{DS} = 0.05\ V$. The results of this step are shown in Fig. 4.5. The horizontal-field effect on effective mobility modeling by parameter, U_{DS}, as well as the drain-induced-barrier-lowering effect by parameter η_Z, therefore, can be seen and extracted from the I_{DS} versus V_{DS} characteristics. In the weak-inversion operation, the drain current is contributed by the diffusion current, which is modeled, in logarithmic domain, by a slope factor, n, and an offset factor, K_{sub}. Thus, those two parameters are extracted by optimizing the weak-inversion current characteristics.

In the short-channel and narrow-width transistors, the body effect is affected by the channel width and length. Those effects are modeled by parameters, K_{NZ}, K_{NB}, and γ_{1L}, and can be extracted from the behavior of V_{th} versus V_{BS}, as shown in Fig. 4.8 and Fig. 4.9. To analyze the short-channel effect on effective mobility and velocity saturation, the I_{DS} versus V_{GS} and the I_{DS} versus V_{DS} characteristics of a short-channel transistor have to be used. The vertical-field effects on the effective mobility for short-channel transistors are modeled by parameters, U_{GSL} and U_{GSL2}, and the velocity saturation effect is modeled by the critical field, E_{crit}. The results of those effects are shown in Fig. 4.10 and Fig. 4.11. The channel-length modulation effect is more significant for the short-channel transistors, and is to be extracted from the I_{DS} versus V_{DS} in the saturation region. All the smooth function parameters are fine-tuned in the last step by optimizing the transition portion between different operation regions.

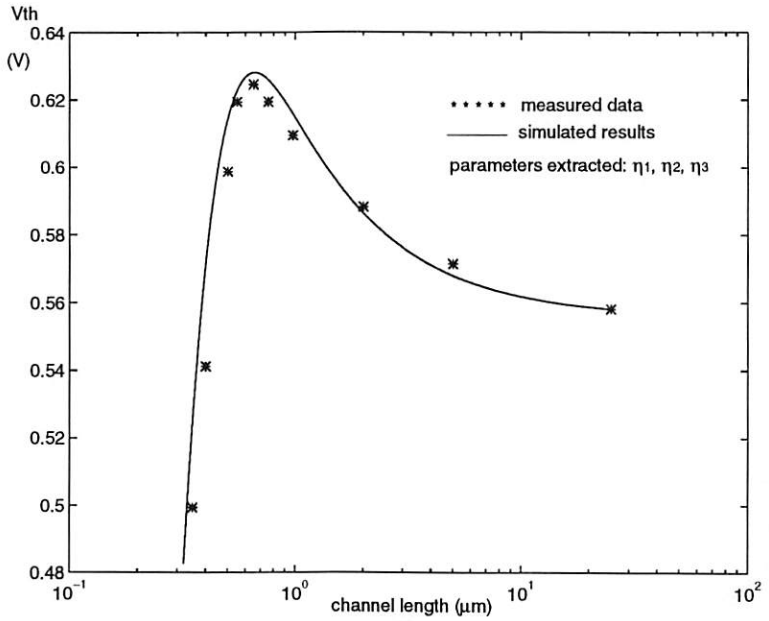


Figure 4.2: Plot of reverse short-channel effect for extracting the parameter, η_1, η_2, and η_3.

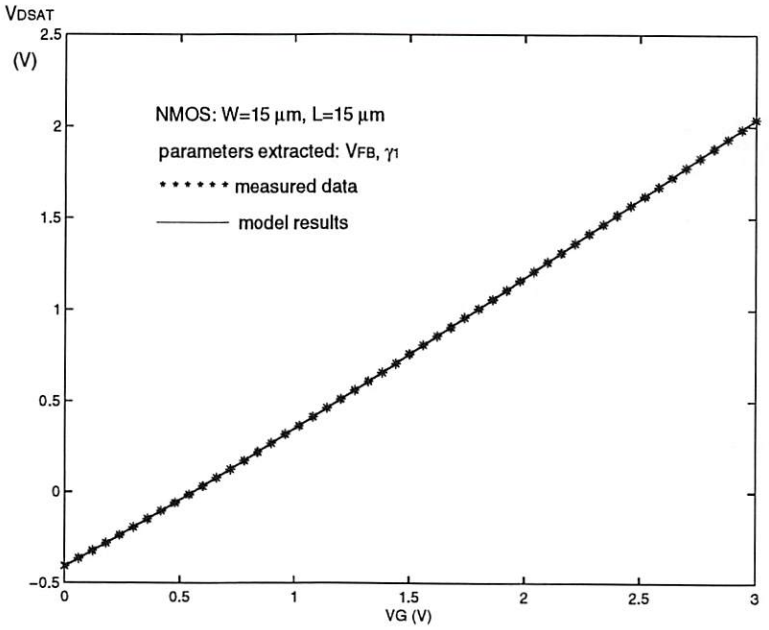


Figure 4.3: Plot of V_{DSAT} versus V_G to optimize α_x and V_{DSAT} for extracting V_{FB}, γ_1, and $\phi_s = V_{T0} - V_{FB}$ with a long- and wide-channel transistor to exclude the short- and narrow-channel effects.

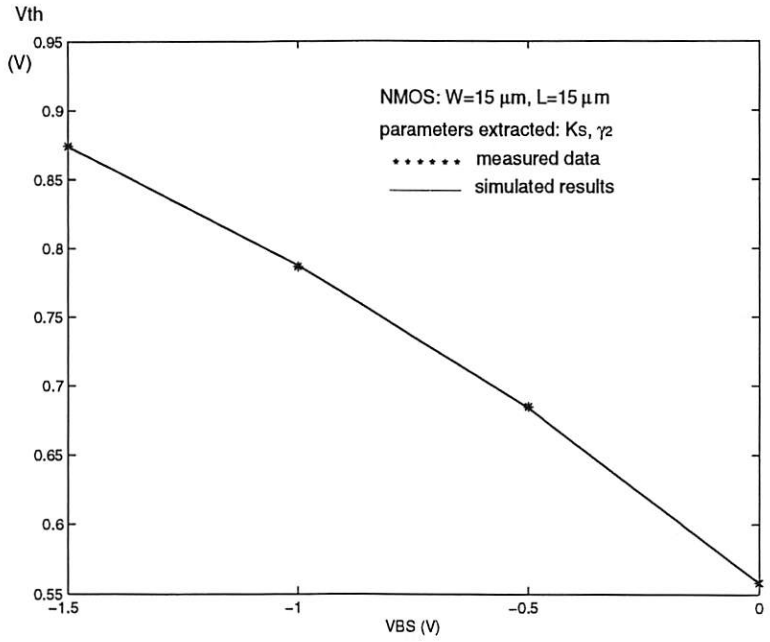


Figure 4.4: Plot of V_{th} versus V_{BS} of a large transistor to extract the higher-order body effect parameters, K_S and γ_2.

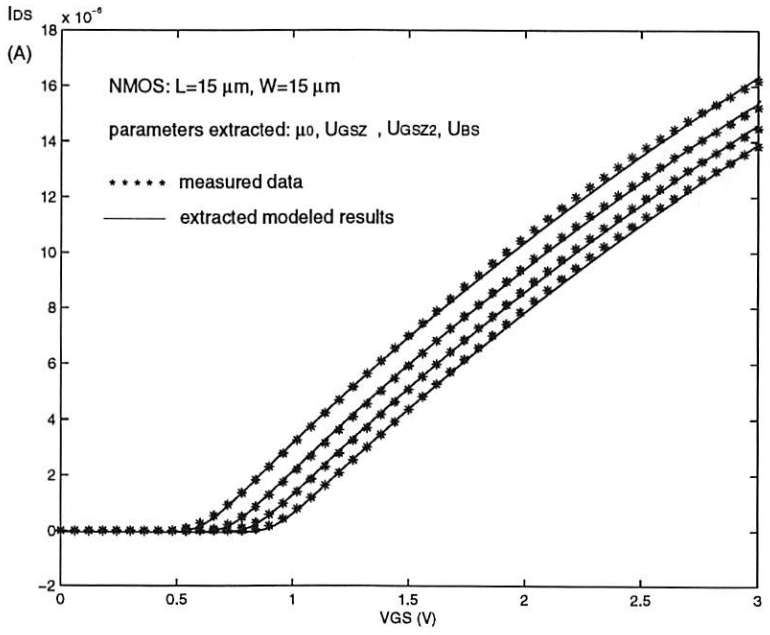


Figure 4.5: Plots of I_{DS} versus V_{GS} of a large transistor at $V_{DS} = 0.05\ V$ and $V_{BS} = 0, -0.5, -1, -1.5\ V$ to exclude the small-geometry effects and V_{DS} effects for extracting μ_0, U_{GSZ}, and U_{BS}.

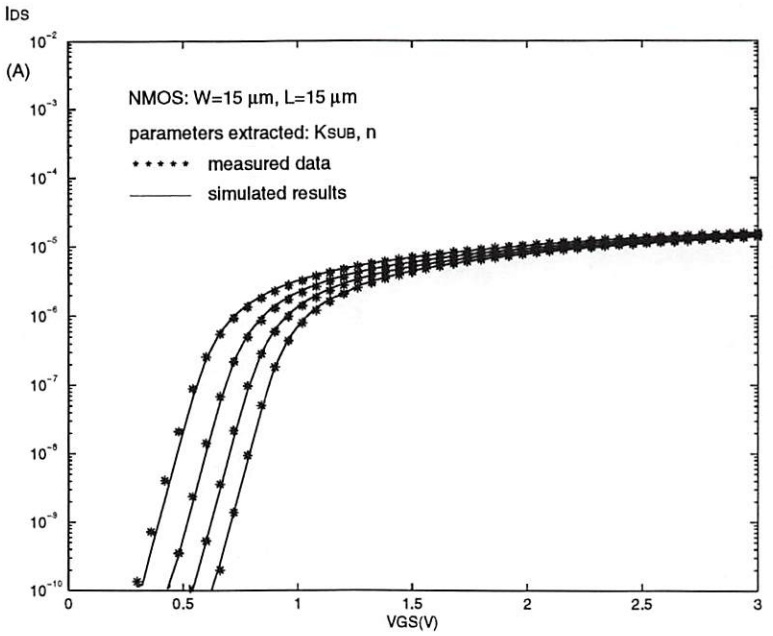


Figure 4.6: Plots of I_{DS} versus V_{GS} in the logarithmic scale for extracting the weak-inversion region parameters, K_{sub} and n.

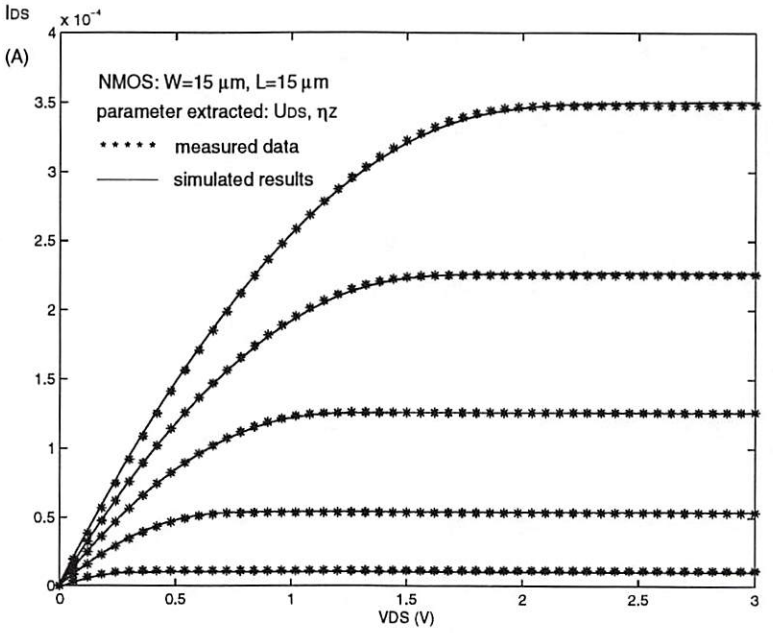


Figure 4.7: Plots of I_{DS} versus V_{DS} at $V_{GS} = 1, 1.5, 2, 2.5, 3\ V$ of a large transistor for extracting U_{DS} and η_Z.

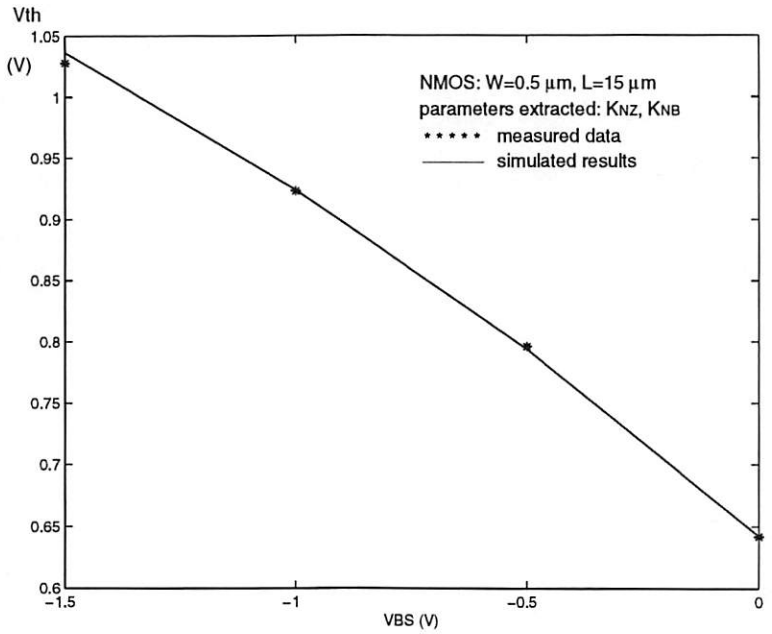


Figure 4.8: Plot of V_{th} versus V_{BS} of a narrow-channel transistor for extracting K_{NZ} and K_{NB}.

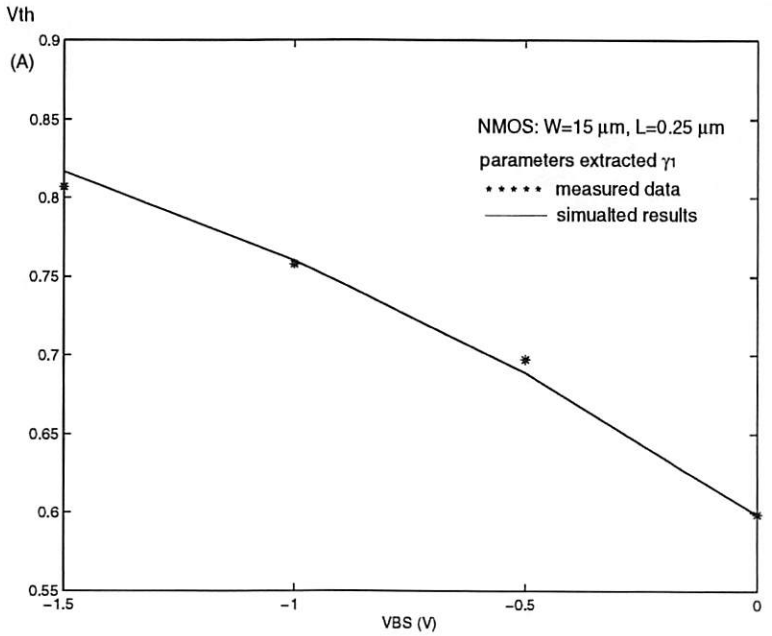


Figure 4.9: Plot of V_{th} versus V_{BS} of a short-channel transistor for extracting γ_{1L}.

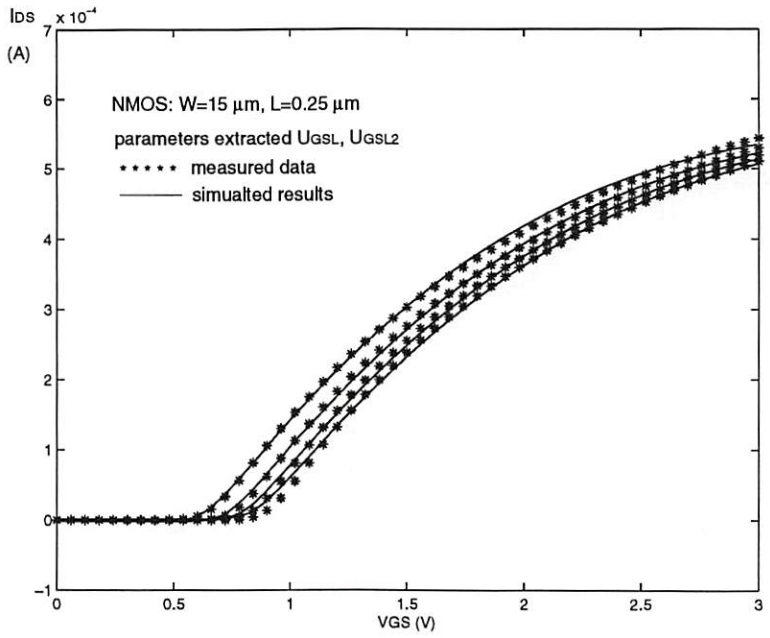


Figure 4.10: Plots of I_{DS} versus V_{GS} of a short-channel transistor at $V_{DS} = 0.05\ V$ and $V_{BS} = 0, -0.5, -1, -1.5\ V$ to exclude V_{DS} effects for extracting U_{GSL} and U_{GSL2}.

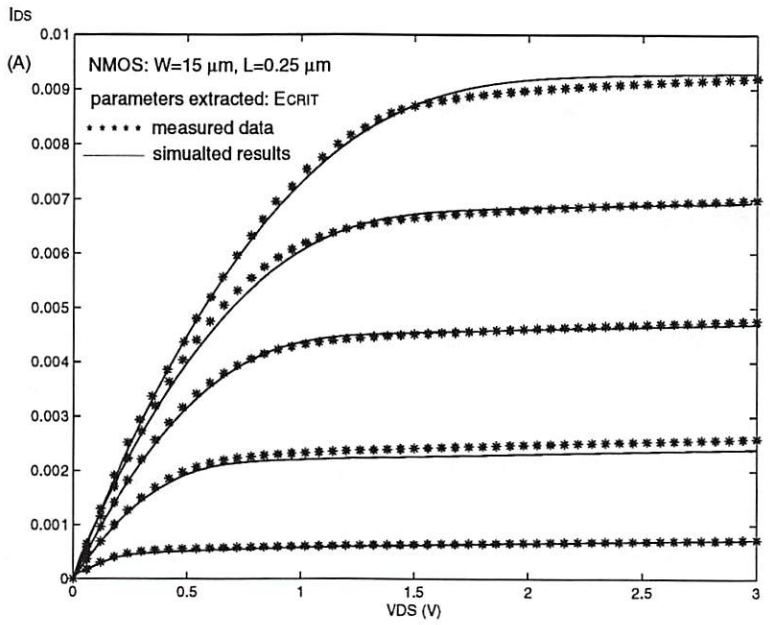


Figure 4.11: Plots of I_{DS} versus V_{DS} at $V_{GS} = 1, 1.5, 2, 2.5, 3\ V$ of a short-channel transistor for extracting E_{crit}.

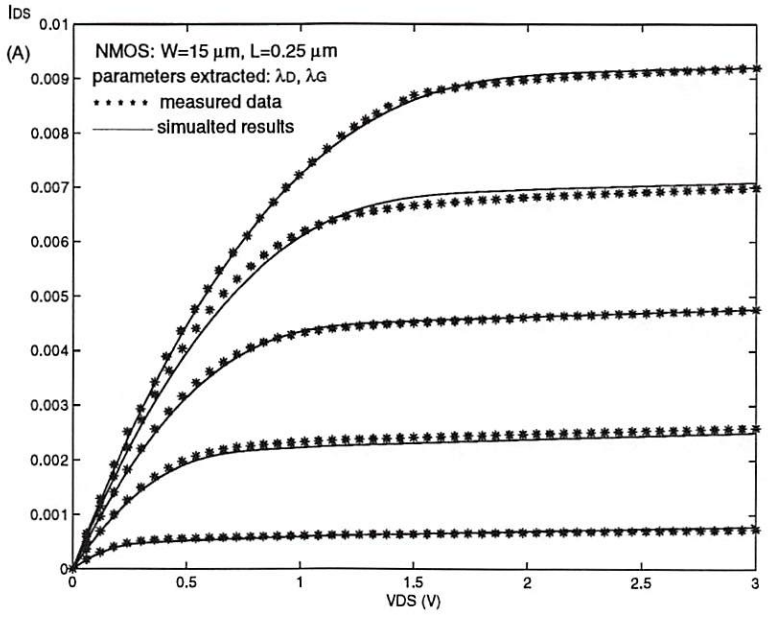


Figure 4.12: Plots of I_{DS} versus V_{DS} at $V_{GS} = 1, 1.5, 2, 2.5, 3\ V$ of a short-channel transistor for extracting λ_D, λ_G, and ϕ_D.

Reference List

[1] B. J. Sheu, W.-J. Hsu, P. K. Ko "A MOS transistor charge model for VLSI design," *IEEE Trans. on Computer-Aided Design*, vol. 7, no. 4, pp. 520-527, Apr. 1988.

[2] *Star-HSPICE User's Manual*, Avant! Corporation, Sunnyvale, CA, Feb. 1996.

[3] *BSIM3v3 Manual*, Dept. of Electrical Engineering and Computer Sciences University of California, Berkeley, 1995-1997.

[4] *Matlab User's Guide*, The MathWorks Inc., Natick, MA, 1996.

Chapter 5

Implementation in SPICE-3f3 Circuit Simulator

The SPICE program is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analyses [1]. An early version of the SPICE program was described by Nagel and Pederson [2]. In 1980s, the SPICE-2g6 program was used widely in the academic community and was the basis of many commercial circuit simulation programs. The SPICE-3f3 program [1] is the more recent version of the SPICE program, which was written in C-language. Several new techniques are used to solve convergence problems and improve the performance of the simulator [3].

5.1 SPICE-3f3s implementation of S-CMOS model

The S-CMOS model was developed to enhance the capability of circuit simulation for high-performance VLSI design in deep-submicron technologies. In order to enable circuit designers to use the model, it was necessary to implement it into a popular circuit simulator. The SPICE-3f3 simulation program was selected for the implementation of S-CMOS model and the modified version with the S-CMOS model is

called SPICE-3f3s. The structure of the SPICE-3f3s program for the new model implementation is shown in Fig. 5.1. A brief description of the primary functions served by the files contained in these directories and the S-CMOS model implementation procedure are given following.

The implementation of a new device model into the SPICE-3f3 program requires three types of changes:

- new routines written specifically to support the device,
- modifications of existing routine to include knowledge required for parsing, and
- changes to integrate the new device model into the main loops of the simulation algorithm.

The C-language files that were created to support the S-CMOS model were placed in the src/lib/dev/scmos directory. The main files and a brief description of the routines contained in them are listed below:

- *scmosdef.h*: This file contains two data structures, one for the device model and one for a specific instance of model.
- *scmositf.h*: This file contains pointers to routines that are used to interface with the device model, as well as a number of tables and constants.
- *scmosext.h*: This file declares the different routines associated with the S-CMOS model.
- *sc.c*: This file contains two parameter descriptor arrays that list the parameters along with the type of values that can be assigned to the parameters, as well as integers that can be used to refer to the parameters in other routines.

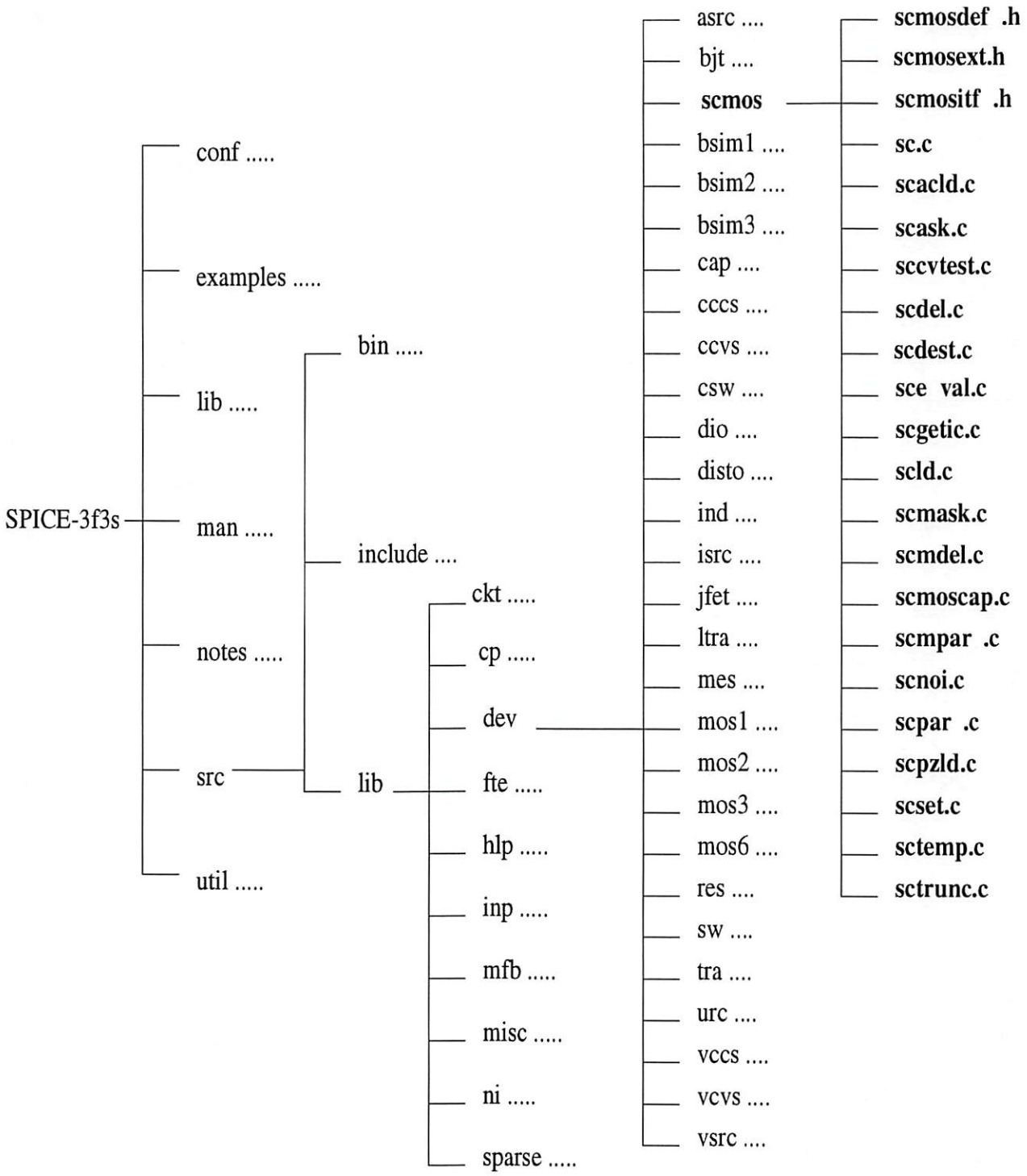


Figure 5.1: The structure of implementation of S-CMOS model in SPICE-3f3.

- *scacld.c*: This routine is used to load the sparse matrix during A.C. analysis where complex quantities may need to be loaded.

- *scask.c*: This routine allows users to access internal values of S-CMOS devices instances. Certain parameters of instances can be passed to it in order to compute and return the values of such parameters.

- *sccvtest.c*: This routine performs the convergence test for each device.

- *scdel.c*: This routine deletes a single instance of the S-CMOS model from the data structures, leaving everything else alone.

- *scdest.c*: This routine is used to dismantle the data structure and free all space used by S-CMOS model and instances.

- *sceval.c*: This routine contains the S-CMOS model expressions. The drain current, terminal charges, their derivatives with respect to drain, gate, source, bulk voltages are evaluated in this routine.

- *scgetic.c*: This routine gets the initial conditions of S-CMOS devices from the node initial conditions.

- *scld.c*: This routine is used in the D.C. and transient analyses to load the sparse matrix.

- *scmask.c*: This routine allows users to access internal values of S-CMOS model parameters.

- *scmdel.c*: This routine is used to dismantle data structures and free space occupied by a specific S-CMOS model and all instances of that model.

- *scmoscap.c*: This routine calculates and assigns values of equivalent conductances and total terminal charge.

- *scmpar.c*: This routine assigns a value to a specific S-CMOS model parameter.

- *scnoi.c*: This routine calculates the thermal noise due to the source/drain and channel conductances, as well as the flicker noise.

- *scpar.c*: This routine assigns a value to a specific parameter field of a device instance.

- *scpzld.c*: This routine is used for evaluating and loading the matrix during pole-zero analysis.

- *scset.c*: This routine is called once during parameter preprocessing, and all the one-time operations such as allocating sparse matrix entries and getting pointers to them are done here.

- *sctemp.c* This routine is used to preprocess the S-CMOS model parameters.

- *sctrunc.c*: Calculation of truncation errors on energy storage elements or components of elements is done here.

In order to enable the SPICE program to identify the S-CMOS model, there are several files have to be modified. The *config/defaults* file contains several variables that are used during the compilation of the program which need to be set according to the environment in which the program is being compiled. These variables include the command to run the C-language compiler, the paths to the libraries that are required during compilation, the directories containing the source files, intermediate files and output files, the default editor when using SPICE interactively, the analyses that the program is to perform, and the device models that the program is to be

capable of simulating. The *defaults* file has been modified to include the S-CMOS model as part of the DEVICES variable.

The *inp* directory contains the routine necessary to parse the input format and produce the subroutine calls that are required by the front-end to simulator interface. These include routines that parse the model definitions and descriptions of various active and passive elements in the input decks. The files, *src/lib/inp/inp2m.c*, *src/lib/inp/inpdomod.c*, and *src/lib/inp/inpfindl.c*, were modified to enable the SPICE-3f3s program to identify the S-CMOS model in the input deck.

5.2 Simulation Results of Selected Circuits Using S-CMOS Model

The S-CMOS model has been implemented in the SPICE-3f3s version of the circuit simulation program to give VLSI designers the ability to use the model for design of low-power high-performance circuit in advanced deep-submicron technologies. Several conventional and advanced CMOS circuit blocks were simulated by using SPICE-3f3s to demonstrate the capability of S-CMOS model in different types of circuit simulation.

5.2.1 Charge Conservation Property

A single MOS transistor was simulated using the S-CMOS and the Level-3 [4] models in order to compare the charge conservation property between these models based on methods reported in [5]. The transistor was connected to the voltage sources, a capacitor and a resistor as shown in Fig. 5.2(a). The voltages to the drain, bulk and gate of the transistor were pulsed between 0 V and V_{DD}. The pulse waveforms of the voltage sources are given as in Fig. 5.2(b). Comparison of the simulated voltages

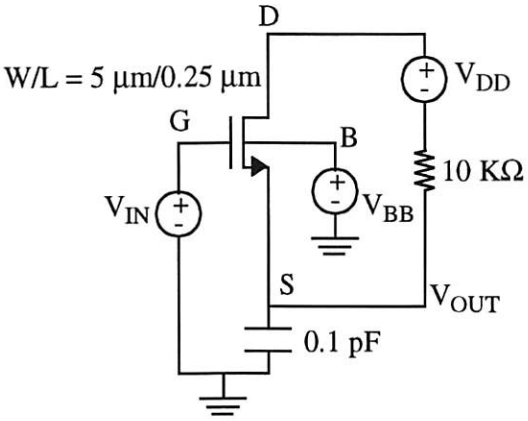
across the capacitor using the S-CMOS and Level-3 models is shown in Fig. 5.2(c). Here, the 40/60 channel charge partitioning scheme is used for both models. The voltage across the capacitor that was obtained using the Level-3 model did not return to zero after several pulse. This is due to the charge which is generated by the numerical non-conservation effect in the simulated results accumulated on the capacitor. The simulation results in Fig. 5.2(c) confirm that charge conservation is achieved by the S-CMOS model.

5.2.2 Domino Logic Gate

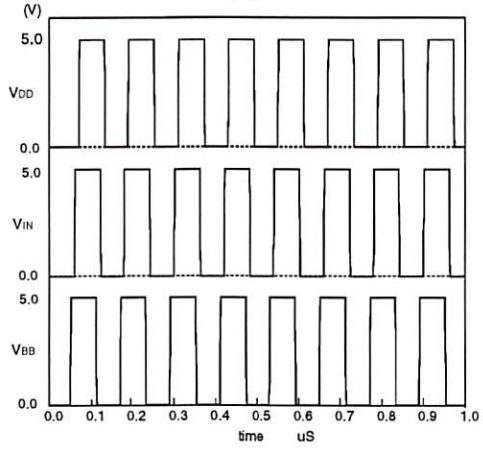
The domino logic allows a single clock to precharge and evaluate a set of dynamic logic blocks. This involves incorporating a static CMOS inverter into each logic blocks. Figure 5.3(a) shows the circuit scheme of a logic function gate which performs $A(B+CD)$. The PMOS transistors, M1, M2, and M3, are used to precharge during the clock $CLK = 0$. When the clock $CLK = 1$, the logic gate is evaluated by the n-logic circuitry. In the time-domain transient analysis, this type of circuits can be used to test the convergence property of the model. The simulated result using the S-CMOS model is shown in Fig. 5.3(b). It shows the correct result. Notice that the same circuit simulation performed by using one set of Level-2 model parameter values in SPICE-3f3 results in the non-convergence problem with the time-step error.

5.2.3 Folded-Cascode Operational Amplifier

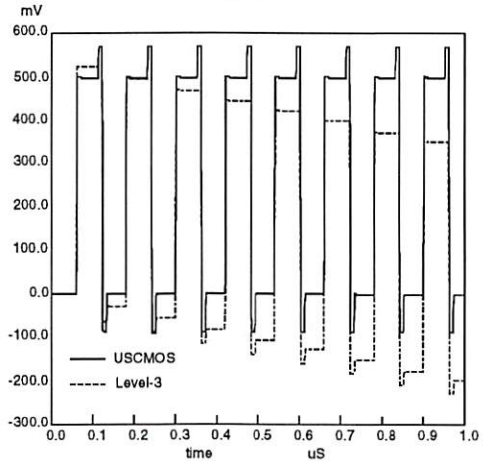
A fully-differential folded-cascode operational amplifier was designed in a 0.35 μm technology. The circuit schematic diagram of the amplifier is shown in Fig. 5.4(a) [6]. The amplifier was designed to realize a wide and stable closed-loop bandwidth and the minimized settling time for a large capacitive load. Two additional differential



(a)

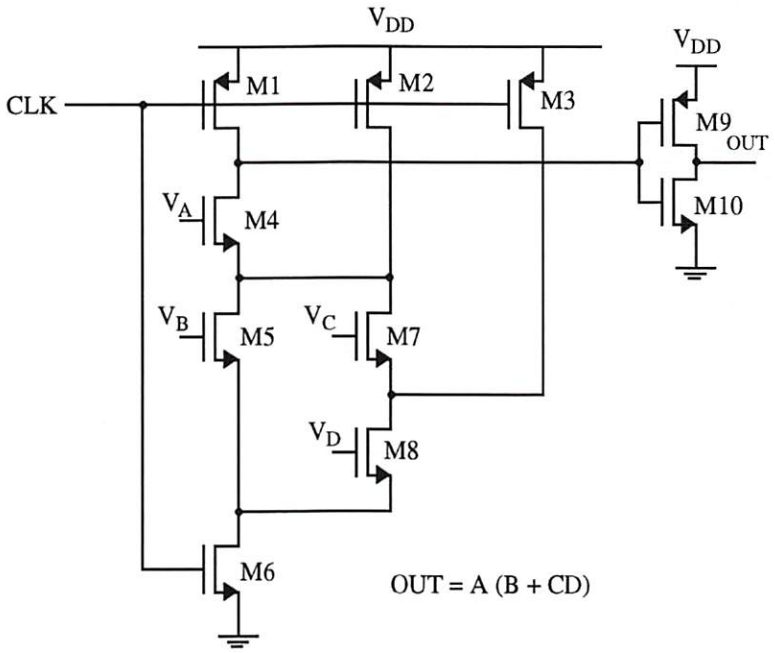


(b)

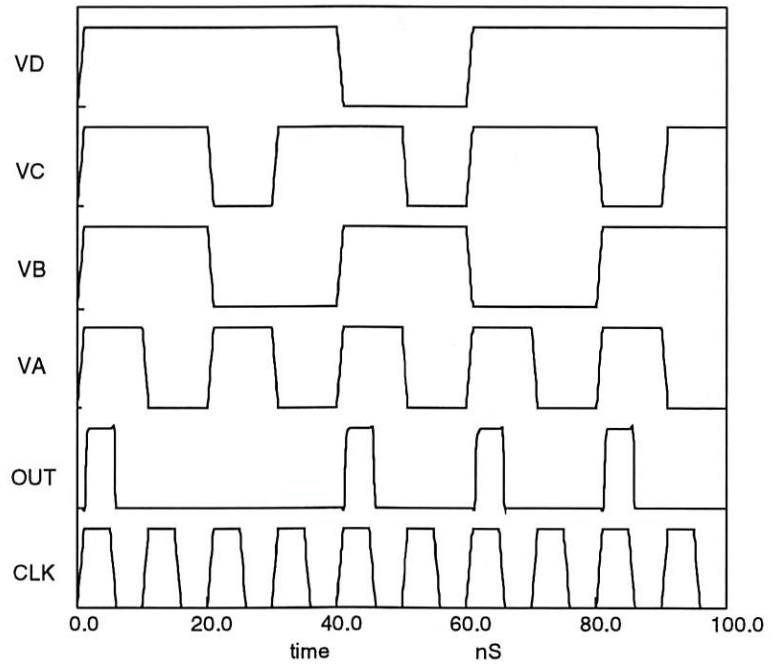


(c)

Figure 5.2: Charge conservation test of S-CMOS model. (a) Test circuit. (b) Input waveforms. (c) Output waveforms.



(a)



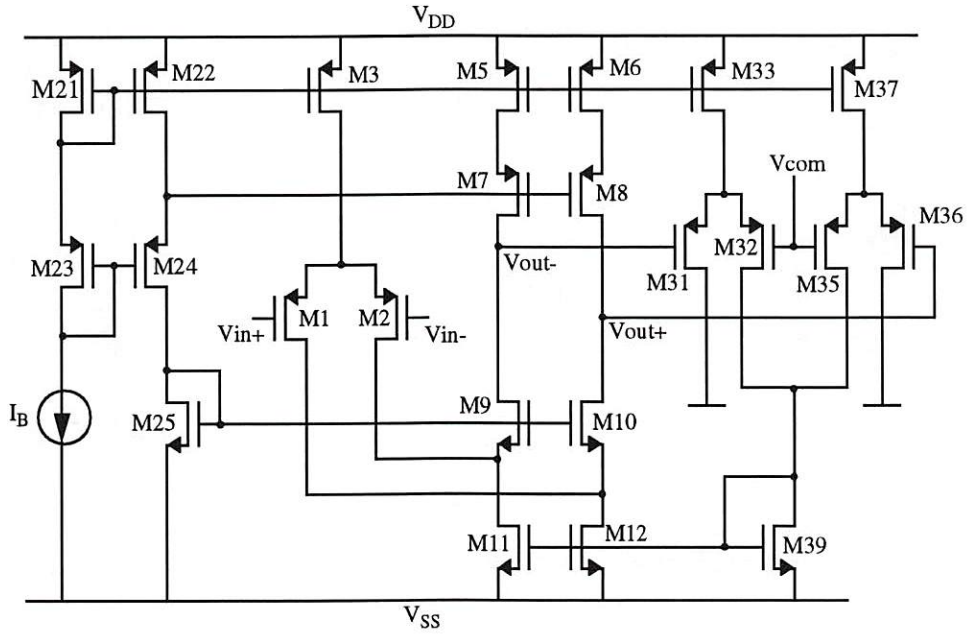
(b)

Figure 5.3: Domino circuit with dynamic precharge scheme and $V_{DD} = 4\ V$. (a) Circuit diagram of function $A(B + CD)$. (b) Output waveforms.

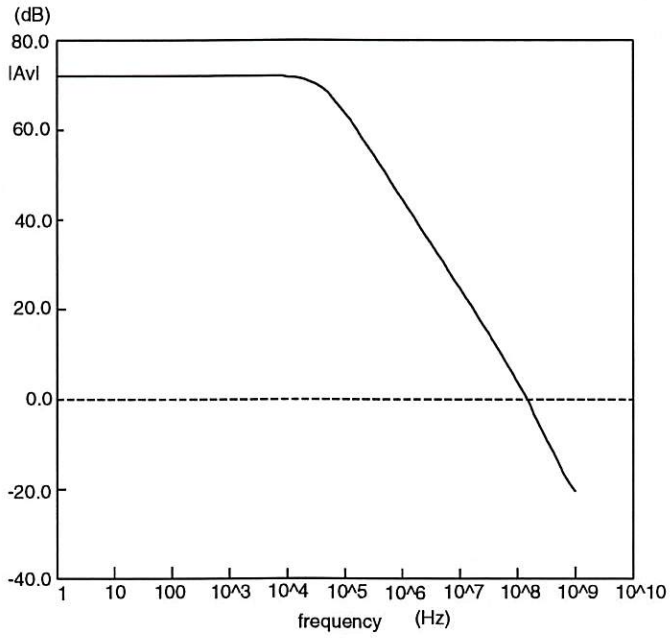
pairs are used to balance the common-mode output levels instead of using the linear-region-biased MOS transistors in the serially-connected output branches [7]. The amplifier was designed to operate with a power supply voltage of 2.5 V. A bias current of 40 μA was used in the simulation. To determine D.C. voltage gain and unity-gain frequency, the amplifier was simulated in the open-loop configuration. The output range was also determined with the amplifier in the open-loop configuration. The slew rate and settling time were determined by simulating the amplifier in a unity-gain configuration and applying a step voltage to the input. Figure 5.4(b) shows the voltage gain characteristics of the amplifier. Basically, this is a single-stage amplifier. It contains one dominant pole only. In order to increase the accuracy of the output gain of the circuit, the folded-cascode technique is used. However, with this scheme, a second pole is introduced in the circuit, which is contributed by C_{gs}/g_m of transistor $M9$. This is defined as the transit frequency, f_T, of a transistor. Therefore, to make sure the circuit having a better stability with larger phase margin, biasing of transistor $M9$ is very important. Usually a larger biasing current in saturation region can maintain a higher f_T. The common-mode rejection ratio was determined from the differential-mode and common-mode gains. The common-mode gain was determined by connecting the inverting and non-inverting inputs of the amplifier together and simulating the amplifier using an A.C. analysis. The simulated results that were obtained by S-CMOS model are listed in Table 5.1.

5.2.4 Analog Comparator

A latch-type analog comparator with fully-differential capability was designed in a 0.25 μm CMOS technology. The circuit schematic of the comparator is shown in Fig. 5.5(a), and the output waveforms are shown in Fig. 5.5(b). The comparator operates at the 250 MHz frequency. In order to achieve the high-speed performance,



(a)



(b)

Figure 5.4: A folded-cascode operational amplifier. (a) Circuit schematic diagram. (b) Voltage-gain frequency response.

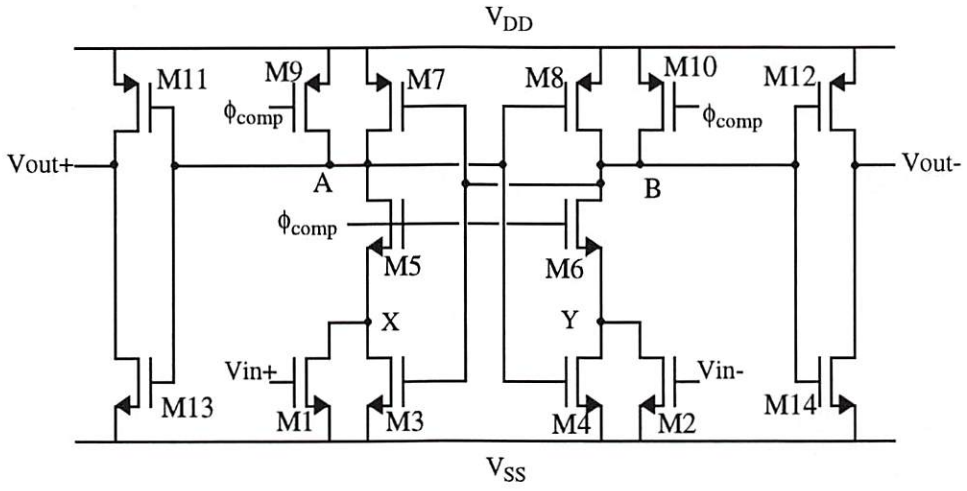
Table 5.1: Performance of the folded-cascode operational amplifier.

Performance characteristics	Simulated results
bias current	40 μA
supply voltage	2.5 V
DC gain	72.3 dB
unit-gain frequency	175 MHz
phase margin	69.0 degree
settling time (0.1%)	69 ns
CMRR @ 1KHz	68 dB

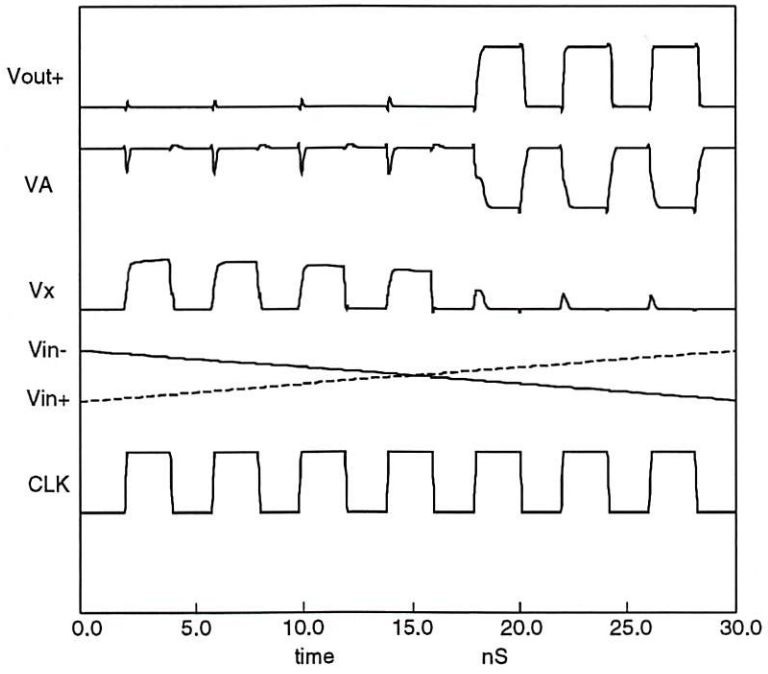
the comparator is precharged to V_{DD} when ϕ_{comp} is low. When the comparator enters the evaluation mode, ϕ_{comp} is high in order to maintain the same current flowing into node X (or Y). The voltage V_X increases for the lower V_{in+} value, or V_X decreases for the higher V_{in+} value. Therefore, the output of the comparator can be determined vary fast.

5.2.5 Wide-Range Gilbert Multiplier

A wide-range Gilbert multiplier was designed using 0.25 μm technology, as shown in Fig. 5.6(a). Transistors, $M1$, $M2$, $M6$, $M7$, $M9$, and $M10$, form the basic Gilbert multiplier structure [9]. Different from the basic Gilbert multiplier, this circuit uses two PMOS transistor pairs for the inputs V_3 and V_4 to realize large operation range of input voltages from very close to V_{DD} to very close to ground. In order to have a more precise current mirror between two output stages in both sides of the circuit, M_{18} - M_{21} are used as a cascode structure. The simulated result of the output current over a wide range of V_1 for several fixed values of differential input $V_3 - V_4$



(a)



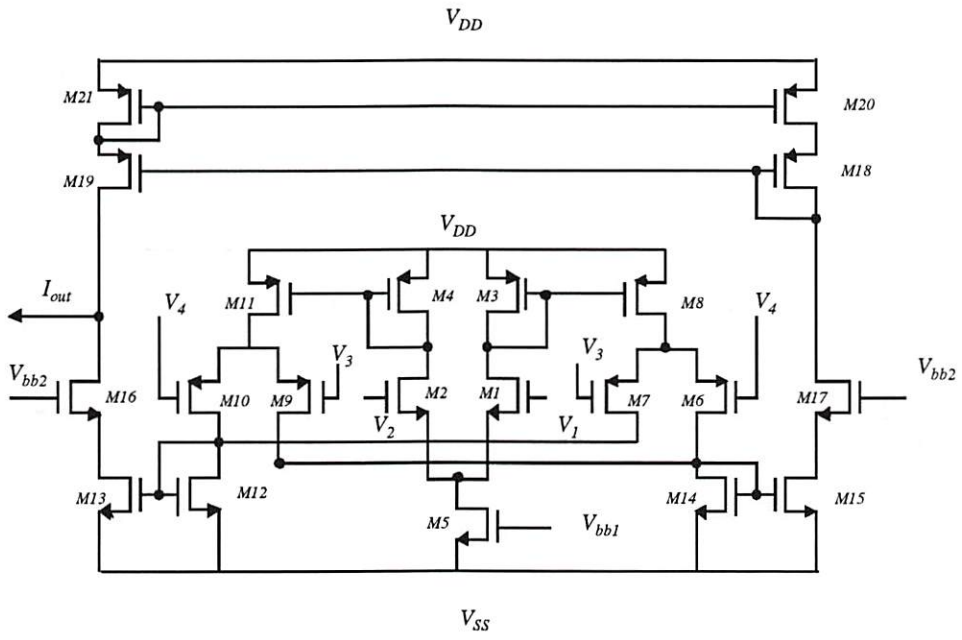
(b)

Figure 5.5: An analog comparator. (a) Circuit schematic diagram. (b) Output waveforms of S-CMOS simulation results.

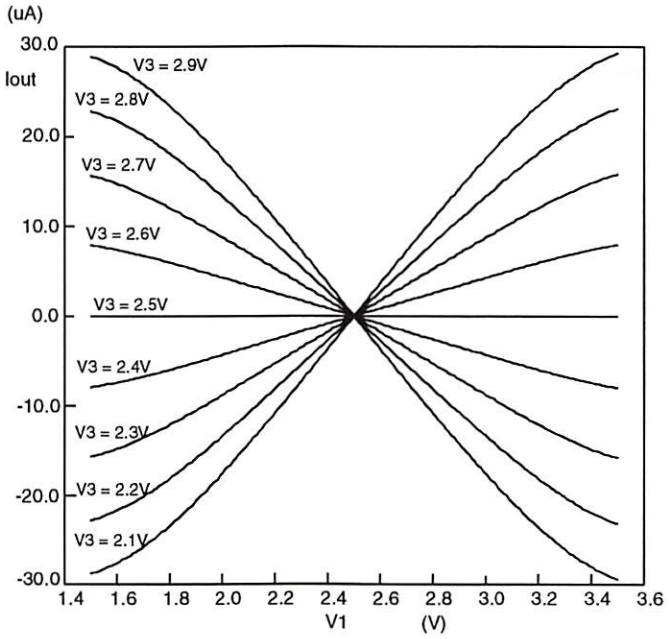
by using S-CMOS model is shown in Fig. 5.6(b). It demonstrates that the output current is proportional to $(V_1 - V_2) \cdot (V_3 - V_4)$.

5.2.6 DRAM Memory Circuit

The basic circuit schematic of a dynamic memory (DRAM) is shown in Fig. 5.7, which includes storage capacitors, precharge circuit, and sense amplifier. A sense amplifier is as important as the memory cell because its performance affects the whole memory chip considerably [8]. Thus, accuracy of the MOS transistor modeling becomes very important for simulation of DRAM circuits to obtain the correct behavior of sense amplifier. A complete 16-word x 1-bit dynamic memory circuit was designed in a 0.25 μm CMOS technology and simulated using the S-CMOS model. The schematic of the memory circuit including the writing circuitry, precharge circuitry, memory cell, sense amplifier and read circuitry is shown in Fig. 5.8(a). The simulated waveforms of control and data signals are shown in Fig. 5.8(b). Simulation was done for a single cycle containing Write-0, Read-0, Write-1, and Read-1 operations. The bit-line and dummy cell were first precharged using the PRECHARGE and PRECHARGE(DUM) signal lines. The bit-line was precharged to 2.5 V while the dummy cell was precharged to 1.8 V. The precharging was then disabled and the WRITE signal was used to enable entry of data onto the bit line to a specific memory cell. The data in the memory cell can be refreshed to V_{DD} by using the RESTORE signal. During the read operation, the word line was enabled and the data flow was from the memory cell onto the bit line. The sense amplifier, which consists of a cross-coupled common-source transistor pair, drove the signal to V_{DD} or ground.



(a)



(b)

Figure 5.6: A modified Gilbert multiplier for a wide operation range at $V_{DD} = 5\ V$. (a) Circuit schematic diagram. (b) Output waveforms of S-CMOS simulation results.

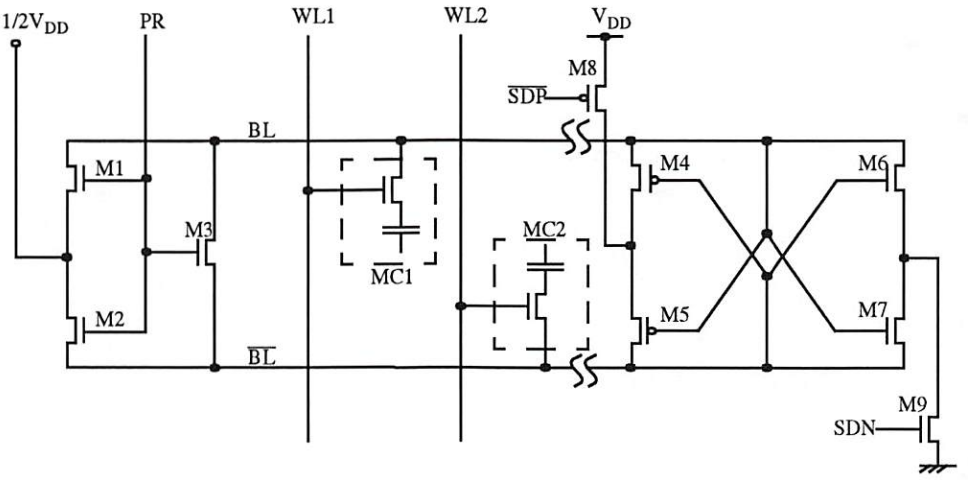
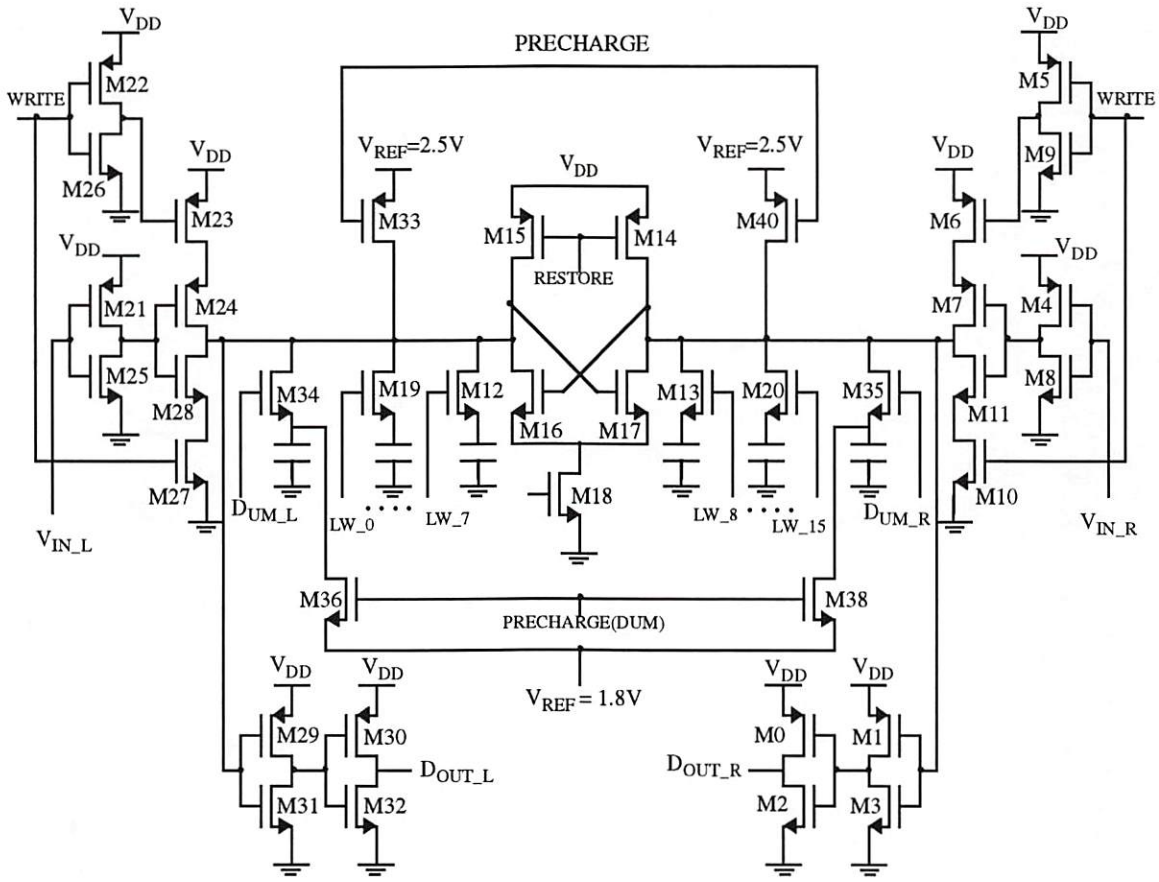
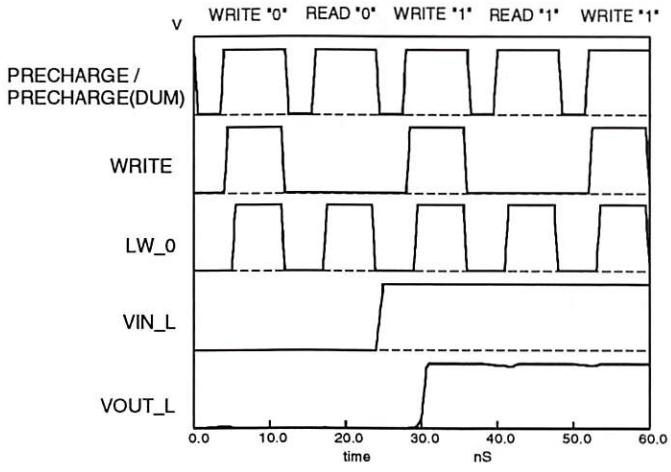


Figure 5.7: A conventional sensing scheme in a DRAM circuit.



(a)



(b)

Figure 5.8: A 16-word x 1-bit dynamic memory circuit. (a) Circuit schematic diagram. (b) Output waveforms of S-CMOS simulation results.

Reference List

[1] T. Quarles, A. Newton, D. Pederson, A. Sangiovanni-Vincentelli, *SPICE3 version 3f3 User's Manual*, University of California, Berkeley, CA, May 1993.

[2] L. Nagel, D. Pederson, "Simulation program with integrated circuit emphasis," *IEEE Proc. of 16-th Midwest Symposium on Circuit Theory*, Waterloo, Canada, 1973.

[3] T. Quarles, *Analysis of performance and Convergence Issues*, Memo ERL-M89/42, Electronics Research Lab., University of California, Berkeley, Apr. 1989.

[4] A. Vladimirescu, S. Liu, *The Simulation of MOS Integrated Circuit Using SPICE2*, Memo ERL-M80/7, Electronics Research Lab., University of California, Berkeley, Oct. 1980.

[5] P. Yang, B. Epler, P. Chatterjee, "An investigation of the charge conservation problem for MOSFET circuit simulation," *IEEE Jour. of Solid-State Circuits*, vol. 18, no. 1, pp. 128-138, Feb. 1983.

[6] J. Choi, B. Sheu, B. Lee, "A 16-bit sigma-delta A/D converter with high-performance operation amplifiers," *Journal of Analog Integrated Circuits and Signal Processing*, Kluwer Academic Publishers, vol. 6, no. 2, pp. 105-119, Sept. 1994.

[7] R. Gregorian, G. Temes, *Analog MOS Integrated Circuits for Signal Processing*, A Wiley-Interscience Publication: New York, NY, 1986.

[8] Y. Oshima, B. Sheu, S. Jen, Memory Architectures Technology for Multimedia Systems, Chapter 4 in *Multimedia Technology for Applications*, Editors: B. Sheu, M. Ismail, IEEE Press: New York, NY, 1998.

[9] C. Mead, *Analog VLSI and Neural Systems*, Addison-Wesley Publishing Company: New York, NY, 1989.

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Chapter 6

Discussion and Conclusion

The unified short-channel MOS transistor model (S-CMOS) was developed to provide VLSI designers with a critically needed tool to simulate low-voltage/low-power, high-speed mixed-signal circuits in deep-submicron CMOS technologies. The key features of the model that make it very valuable include:

- unified drain current and terminal charge expressions in all regions of operation, which provides a highly continuous behavior for the conductances and capacitances,
- accurate modeling of charge densities by a better expression of conductance degradation coefficient;
- better threshold voltage and mobility expressions for deep-submicron behavior,
- accurate modeling the output conductance behavior in saturation region including the vertical and horizontal field effects;
- accurate modeling the transition between the weak- and strong-inversion regions;
- a compact set of physically-based parameters; and

- efficient parameter extraction strategy.

The use of three smoothing functions, hyperbola, exponential interpolation, and sigmoid functions, for the drain current and terminal charge provides excellent transitions between different operation regions in the unified expressions. The threshold voltage expression in the S-CMOS model includes effects of flat-band voltage, surface-inversion potential, non-uniform substrate doping, reverse short-channel, narrow-channel, and drain-induced-barrier-lowering effects. The effective mobility expression includes the effects of lateral and vertical electric fields in the channel. The contribution of the vertical electric field is modeled as a function of the gate and substrate voltages which includes the second-order term to provide a higher accuracy for deep-submicron transistors, while the contribution of the lateral electric field is modeled by the critical electric field for velocity saturation. The hyperbola and exponential interpolation functions provides the effective mobility expression valid for both weak- and strong-inversion regions. The sigmoid and exponential interpolation functions are used to combine the drift and diffusion currents into unified current expression. The charge model uses the better formulation of conductance degradation coefficient to model the channel charge density. The unified expressions of charge densities are valid for all operation regions, including the accumulation region. Different channel charge partitioning schemes, including 40/60, 0/100, and 50/50, are provided to support good usage of the model in different applications. All the terminal charge and inter-nodal capacitances are unified and have good prediction at the transition between different operation regions. This is especially important for the capacitance model. The features of the S-CMOS model are summarized in Table 6.1.

The use of a compact set of 35 parameters, including 31 physics-based parameters and 4 smoothing function parameters, for the drain-current expression greatly

Table 6.1: The advanced features of the S-CMOS model.

MOS Model	BSIM3v3	S-CMOS
Developers	Chen, Jeng, Ko, Hu (1996-1998)	This work (1996-1998)
Organization	University of California, Berkeley	University of Southern California
Number of parameters	109	35
Model expression for different operation regions	unified expression	unified expression
Continuity of conductance	continuous and smooth through all operation regions	continuous and smooth though all operation regions
Accuracy of drain current and conductances prediction for advanced technology	good	good
Charge/capacitance model	unified terminal charge expressions	unified terminal charge expressions
Small-geometry effects	globally fixed format (quadruple number of parameters)	locally adapted format (certain number of adapted parameters)
Suitability for circuit design hand-analysis	moderate	good
Applicable circuit type	Mixed-signal VLSI	Mixed-signal VLSI & radio-frequency circuits
Applicable technology	deep-submicron	deep-submicron

reduces the complexity of the parameter extraction procedure. Instead of the globally fixed format of small-geometry effects for "binning", the locally adapted format is applied in certain selected parameters to include the small-geometry effects and minimize the number of parameters. The parameter extraction is based on the physical characteristics of each parameter in the model to extract the value. Both the local determination and global optimization strategies are combined to increase the extraction accuracy and reduce the extraction computation time. The extraction procedure of the S-CMOS model was implemented in MATLAB software. Parameter sets were extracted from different industrial deep-submicron technologies from

TRW Inc. and Rockwell International Corp. Comparison of measured data and simulated results demonstrated the accuracy of the S-CMOS model on drain current, conductances, terminal charge, and capacitances.

As fabrication technologies evolve, so must the tools available to circuit designers in order to exploit advanced features of new technologies. On the other hand, the design technologies has been pushed to low-voltage/low-power, high-speed/high-frequency applications. Research on circuit simulation and modeling can not only focus on following the evolution of fabrication technologies, but also on the demand from the application sides. While trying to address the challenges of transistor modeling in 1998, we also strive to provide researchers with a platform upon which to continue to address the new problem of upcoming generations of microelectronic circuits and fabrication technologies.

Appendix A

List of Model Equations

A.1 DC Model

(A) Threshold Voltage

$$V_{BST} = \phi_s - (\frac{\gamma_1 - \gamma_2}{K_S} + \sqrt{\phi_s})^2 \quad ,$$

$$V_{BSh} = \frac{1}{2}\left(V_{BS} + K_{BSh} \cdot V_{BST} + \sqrt{(V_{BS} + K_{BSh}V_{BST})^2 - 4V_{BS}V_{BST}}\right) \quad ,$$

$$V_{tho} = V_{FB} + \phi_s + \frac{K_{NZ}}{W} + \frac{K_{NB}V_{BS}}{W} - (\eta_Z + \frac{\eta_L}{L})V_{DS} - \frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - exp\left(-\frac{L}{\eta_3}\right)\right) \quad ,$$

$$\begin{aligned} V_{th} &= V_{tho} + (\gamma_1 - \frac{\gamma_{1L}}{L})(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi_s}) - \frac{K_S}{2}(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi_s})^2 \\ &+ \gamma_2(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s - V_{BSh}}) \quad . \end{aligned}$$

(B) Effective VGS - Vth & Saturation Voltage

$$V_{GSth} = 2 \cdot n \cdot V_t \cdot ln\left(1 + exp\left(\frac{V_{GS} - V_{th}}{2 \cdot n \cdot V_t}\right)\right) \quad ,$$

$$g = 1 - \frac{1}{1.744 + 0.8364(\phi_s - V_{BS})} \quad ,$$

$$a = 1 + \frac{g\gamma_1}{2\sqrt{\phi_s - V_{BS}}} \quad ,$$

$$V_c = \frac{V_{GSth}}{aE_{crit}L} \quad ,$$

$$K = \frac{1 + V_c + \sqrt{1 + 2V_c}}{2} \quad ,$$

$$V_{DSAT} = \frac{V_{GSth}}{a\sqrt{K}} \quad ,$$

$$V_{DSATh} = \frac{1}{2}\left(V_{DS} + K_{DSATh}V_{DSAT} - \sqrt{(V_{DS} + K_{DSATh}V_{DSAT})^2 - 4V_{DS}V_{DSAT}}\right) \quad .$$

(C) Sigmoid Function

$$f_s = \frac{1}{2}\left(1 - \frac{V_{GS} - V_{th}}{\sqrt{(V_{GS} - V_{th})^2 + K_{sig}}}\right) \quad ,$$

$$f_c = 1 - f_s \quad .$$

(D) Effective Mobility

$$\begin{aligned} M_r = \quad & [\quad 1 + (U_{GSZ} + \frac{U_{GSL}}{L})V_{GSth} + (U_{GSZ2} + \frac{U_{GSL2}}{L})V_{GSth}^2 \\ & - \quad U_{BS}(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi_s}) + U_{DS}V_{DSATh}] \cdot [1 + \frac{f_c V_{DSATh}}{E_{crit}L}] \quad , \end{aligned}$$

$$\mu_{eff} = \frac{\mu_0}{M_r} \quad .$$

(E) Channel-Length Modulation Effect

$$f_L = \frac{\lambda_D[\sqrt{\phi_D + V_{DS} - V_{DSATh}} - \sqrt{\phi_D}]}{L \cdot ((V_{GSth})^{3/2} + \lambda_G)(\frac{\lambda_B}{1 - \frac{V_{BS}}{\lambda_{BS}}})} \quad .$$

(F) Unified Drain Current

$$\alpha = [1 - f_s e^{-\frac{V_{DS}}{V_T}}] \cdot [1 + f_c \cdot f_L + f_s \cdot K_{sub}] \quad ,$$

$$\beta = C_{OX} \cdot \mu_{eff} \cdot \frac{W}{L} \quad ,$$

$$F = V_{GSth} \cdot V_{DSATh} - \frac{a}{2} V_{DSATh}^2 \quad ,$$

$$I_{DS} = \alpha \cdot \beta \cdot F \quad .$$

A.2 Conductances

$$\frac{\partial V_{th}}{\partial V_{GS}} = 0 \quad ,$$

$$\frac{\partial V_{th}}{\partial V_{DS}} = -(\eta_Z + \frac{\eta_L}{L}) \quad ,$$

$$\frac{\partial V_{th}}{\partial V_{BS}} = \frac{K_{NB}}{W} - \frac{\gamma_1}{2\sqrt{\phi_s - V_{BSh}}} + \frac{K_S(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi_s})}{2\sqrt{\phi_s - V_{BSh}}} \quad .$$

$$\frac{\partial V_{GSth}}{\partial V_{GS}} = \frac{(1 - \frac{\partial V_{th}}{\partial V_{GS}}) \cdot exp\left(\frac{V_{GS} - V_{th}}{2nV_t}\right)}{1 + exp\left(\frac{V_{GS} - V_{th}}{2nV_t}\right)} \quad ,$$

$$\frac{\partial V_{GSth}}{\partial V_{DS}} = \frac{-\frac{\partial V_{th}}{\partial V_{DS}} \cdot exp\left(\frac{V_{GS} - V_{th}}{2nV_t}\right)}{1 + exp\left(\frac{V_{GS} - V_{th}}{2nV_t}\right)} \quad ,$$

$$\frac{\partial V_{GSth}}{\partial V_{BS}} = \frac{-\frac{\partial V_{th}}{\partial V_{BS}} \cdot exp\left(\frac{V_{GS} - V_{th}}{2nV_t}\right)}{1 + exp\left(\frac{V_{GS} - V_{th}}{2nV_t}\right)} \quad .$$

$$\frac{\partial V_c}{\partial V_{GS}} = \frac{1}{aE_{crit}L} \cdot \frac{\partial V_{GSth}}{\partial V_{GS}} \quad ,$$

$$\frac{\partial V_c}{\partial V_{DS}} = \frac{1}{aE_{crit}L} \cdot \frac{\partial V_{GSth}}{\partial V_{DS}} \quad ,$$

$$\frac{\partial V_c}{\partial V_{BS}} = \frac{1}{aE_{crit}L} \cdot \frac{\partial V_{GSth}}{\partial V_{BS}} \quad .$$

$$\frac{\partial K}{\partial V_{GS}} = \frac{1}{2}\left(1 + \frac{1}{\sqrt{1+2V_c}}\right)\frac{\partial V_c}{\partial V_{GS}} \quad ,$$

$$\frac{\partial K}{\partial V_{DS}} = \frac{1}{2}\left(1 + \frac{1}{\sqrt{1+2V_c}}\right)\frac{\partial V_c}{\partial V_{DS}} \quad ,$$

$$\frac{\partial K}{\partial V_{BS}} = \frac{1}{2}\left(1 + \frac{1}{\sqrt{1+2V_c}}\right)\frac{\partial V_c}{\partial V_{BS}} \quad .$$

$$\frac{\partial V_{DSAT}}{\partial V_{GS}} = \frac{\frac{\partial V_{GSth}}{\partial V_{GS}}}{a\sqrt{K}} - \frac{V_{GSth}}{2aK^{1.5}}\frac{\partial K}{\partial V_{GS}} \quad ,$$

$$\frac{\partial V_{DSAT}}{\partial V_{DS}} = \frac{\frac{\partial V_{GSth}}{\partial V_{DS}}}{a\sqrt{K}} - \frac{V_{GSth}}{2aK^{1.5}}\frac{\partial K}{\partial V_{DS}} \quad ,$$

$$\frac{\partial V_{DSAT}}{\partial V_{BS}} = \frac{\frac{\partial V_{GSth}}{\partial V_{BS}}}{a\sqrt{K}} - \frac{V_{GSth}}{2aK^{1.5}}\frac{\partial K}{\partial V_{BS}} \quad .$$

$$\frac{\partial V_{DSATh}}{\partial V_{GS}} = \left(\frac{K_{DSATh}}{2} - \frac{K_{DSATh}(V_{DS} + K_{DSATh}V_{DSAT}) - 2V_{DS}}{2\sqrt{(V_{DS} + K_{DSATh}V_{DSATh})^2 - 4V_{DS}V_{DSAT}}}\right)\frac{\partial V_{DSAT}}{\partial V_{GS}} \quad ,$$

$$\begin{aligned}\frac{\partial V_{DSATh}}{\partial V_{DS}} &= \frac{1}{2} + \frac{K_{DSATh}}{2}\frac{\partial V_{DSAT}}{\partial V_{DS}} \\ &- \frac{(1 + K_{DSATh}\frac{\partial V_{DSAT}}{\partial V_{DS}})(V_{DS} + K_{DSATh}V_{DSAT}) - 2(V_{DSAT} + V_{DS}\frac{\partial V_{DSAT}}{\partial V_{DS}})}{2\sqrt{(V_{DS} + K_{DSATh}V_{DSATh})^2 - 4V_{DS}V_{DSAT}}} \quad ,\end{aligned}$$

$$\frac{\partial V_{DSATh}}{\partial V_{BS}} = \left(\frac{K_{DSATh}}{2} - \frac{K_{DSATh}(V_{DS} + K_{DSATh}V_{DSAT}) - 2V_{DS}}{2\sqrt{(V_{DS} + K_{DSATh}V_{DSATh})^2 - 4V_{DS}V_{DSAT}}}\right)\frac{\partial V_{DSAT}}{\partial V_{BS}} \quad .$$

$$\begin{aligned}\frac{\partial M_r}{\partial V_{GS}} &= \left(1 + \frac{f_c V_{DSATh}}{E_{crit}L}\right)\left(((U_{GSZ2} + \frac{U_{GSL2}}{L}) + 2(U_{GSZ} + \frac{U_{GSL}}{L})V_{GSth})\frac{\partial V_{GSth}}{\partial V_{GS}}\right. \\ &+ \left. U_{DS}\frac{\partial V_{DSATh}}{\partial V_{GS}}\right) + \frac{M_r f_c}{E_{crit}L + f_c V_{DSATh}}\frac{\partial V_{DSATh}}{\partial V_{GS}} \quad ,\end{aligned}$$

$$\frac{\partial M_r}{\partial V_{DS}} = \left(1+\frac{f_c V_{DSATh}}{E_{crit}L}\right)\left(((U_{GSZ2}+\frac{U_{GSL2}}{L})+2(U_{GSZ}+\frac{U_{GSL}}{L})V_{GSth})\frac{\partial V_{GSth}}{\partial V_{GD}} + U_{DS}\frac{\partial V_{DSATh}}{\partial V_{DS}}\right)+\frac{M_r f_c}{E_{crit}L+f_c V_{DSATh}}\frac{\partial V_{DSATh}}{\partial V_{DS}} \quad ,$$

$$\frac{\partial M_r}{\partial V_{DS}} = \left(1+\frac{f_c V_{DSATh}}{E_{crit}L}\right)\left(((U_{GSZ2}+\frac{U_{GSL2}}{L})+2(U_{GSZ}+\frac{U_{GSL}}{L})V_{GSth})\frac{\partial V_{GSth}}{\partial V_{GD}} + \frac{U_{BS}}{2\sqrt{\phi_s-V_{BS}}}+U_{DS}\frac{\partial V_{DSATh}}{\partial V_{DS}}\right)+\frac{M_r f_c}{E_{crit}L+f_c V_{DSATh}}\frac{\partial V_{DSATh}}{\partial V_{BS}} \quad .$$

$$\frac{\partial \mu_{eff}}{\partial V_{GS}} = \frac{-\mu_0}{M_r^2}\frac{\partial M_r}{\partial V_{GS}} \quad ,$$

$$\frac{\partial \mu_{eff}}{\partial V_{DS}} = \frac{-\mu_0}{M_r^2}\frac{\partial M_r}{\partial V_{DS}} \quad ,$$

$$\frac{\partial \mu_{eff}}{\partial V_{BS}} = \frac{-\mu_0}{M_r^2}\frac{\partial M_r}{\partial V_{BS}} \quad .$$

$$\frac{\partial f_L}{\partial V_{GS}} = f_L\left(\frac{-\frac{\partial V_{DSATh}}{\partial V_{GS}}}{\sqrt{\phi_D+V_{DS}-V_{DSATh}}-\sqrt{\phi_D}}-\frac{3\sqrt{V_{GSth}}\frac{\partial V_{GSth}}{\partial V_{GS}}}{2(V_{GSth}^{3/2}+\lambda_G)}\right) \quad ,$$

$$\frac{\partial f_L}{\partial V_{GS}} = f_L\left(\frac{-\frac{\partial V_{DSATh}}{\partial V_{GS}}}{\sqrt{\phi_D+V_{DS}-V_{DSATh}}-\sqrt{\phi_D}}-\frac{3\sqrt{V_{GSth}}\frac{\partial V_{GSth}}{\partial V_{GS}}}{2(V_{GSth}^{3/2}+\lambda_G)}\right) \quad ,$$

$$\frac{\partial f_L}{\partial V_{BS}} = f_L\left(\frac{1-\frac{\partial V_{DSATh}}{\partial V_{BS}}}{\sqrt{\phi_D+V_{DS}-V_{DSATh}}-\sqrt{\phi_D}}-\frac{3\sqrt{V_{GSth}}\frac{\partial V_{GSth}}{\partial V_{BS}}}{2(V_{GSth}^{3/2}+\lambda_G)}\right) \quad .$$

$$\frac{\partial \alpha}{\partial V_{GS}} = [1-f_s e^{-\frac{V_{DS}}{V_t}}]f_c\frac{\partial f_L}{\partial V_{GS}} \quad ,$$

$$\frac{\partial \alpha}{\partial V_{DS}} = [1-f_s e^{-\frac{V_{DS}}{V_t}}]f_c\frac{\partial f_L}{\partial V_{DS}}+\frac{f_s}{V_t}e^{-\frac{V_{DS}}{V_t}}[1+f_c f_L+f_s K_{sub}] \quad ,$$

$$\frac{\partial \alpha}{\partial V_{BS}} = [1 - f_s e^{-\frac{V_{DS}}{V_t}}] f_c \frac{\partial f_L}{\partial V_{BS}} \quad .$$

$$\frac{\partial \beta}{\partial V_{GS}} = C_{OX} \frac{W}{L} \frac{\partial \mu_{eff}}{\partial V_{GS}} \quad ,$$

$$\frac{\partial \beta}{\partial V_{DS}} = C_{OX} \frac{W}{L} \frac{\partial \mu_{eff}}{\partial V_{DS}} \quad ,$$

$$\frac{\partial \beta}{\partial V_{BS}} = C_{OX} \frac{W}{L} \frac{\partial \mu_{eff}}{\partial V_{BS}} \quad .$$

$$\frac{\partial F}{\partial V_{GS}} = V_{GSth} \frac{\partial V_{DSATh}}{\partial V_{GS}} + \frac{\partial V_{GSth}}{\partial V_{GS}} V_{DSATh} + a V_{DSATh} \frac{\partial V_{DSATh}}{\partial V_{GS}} \quad ,$$

$$\frac{\partial F}{\partial V_{DS}} = V_{GSth} \frac{\partial V_{DSATh}}{\partial V_{DS}} + \frac{\partial V_{GSth}}{\partial V_{DS}} V_{DSATh} + a V_{DSATh} \frac{\partial V_{DSATh}}{\partial V_{DS}} \quad ,$$

$$\frac{\partial F}{\partial V_{BS}} = V_{GSth} \frac{\partial V_{DSATh}}{\partial V_{BS}} + \frac{\partial V_{GSth}}{\partial V_{BS}} V_{DSATh} + a V_{DSATh} \frac{\partial V_{DSATh}}{\partial V_{BS}} \quad .$$

$$g_m = \frac{\partial \alpha}{\partial V_{GS}} \cdot \beta \cdot F + \alpha \cdot \frac{\partial \beta}{\partial V_{GS}} \cdot F + \alpha \cdot \beta \cdot \frac{\partial F}{\partial V_{GS}} \quad ,$$

$$g_{ds} = \frac{\partial \alpha}{\partial V_{DS}} \cdot \beta \cdot F + \alpha \cdot \frac{\partial \beta}{\partial V_{DS}} \cdot F + \alpha \cdot \beta \cdot \frac{\partial F}{\partial V_{DS}} \quad ,$$

$$g_{mbs} = \frac{\partial \alpha}{\partial V_{BS}} \cdot \beta \cdot F + \alpha \cdot \frac{\partial \beta}{\partial V_{BS}} \cdot F + \alpha \cdot \beta \cdot \frac{\partial F}{\partial V_{BS}} \quad .$$

A.3 Charge/Capacitance Model

(A) Terminal Charge

$$V_{FS} = V_{FB} + V_{BS} \quad ,$$

$$V_{GFh} = \frac{1}{2}\left(V_{GS} + K_{GFh}V_{FS} + \sqrt{(V_{GS} + K_{GFh}V_{FS})^2 - 4V_{GS}V_{FS}}\right) \quad ,$$

$$\alpha_x = \left(1 - \frac{\gamma_1^2}{2\sqrt{V_{GSth} + V_{th} - V_{FS} + \frac{\gamma_1^2}{4}}}\right)^{-1} \quad ,$$

$$V_{DSAT} = \frac{V_{GSth}}{\alpha_x} \quad .$$

$$V_{DSATh} = \frac{1}{2}\left(V_{DS} + K_{DSATh}V_{DSAT} - \sqrt{(V_{DS} + K_{DSATh}V_{DSAT})^2 - 4V_{DS}V_{DSAT}}\right) \quad ,$$

$$T_C = 1 - \frac{\alpha_x}{2}\frac{V_{DSATh}}{V_{GSth}} \quad .$$

$$\begin{aligned} Q_G &= WLC_{OX}\left[\left(V_{GSth} + (1-f_s)(V_{th} - V_{FB} - \phi_S) - (1-f_s)\cdot V_{DSATh}\frac{4T_C - 1}{6T_C}\right)\right. \\ &+ \left.\frac{\gamma_1^2}{2}\left(-1 + \sqrt{1 + \frac{4(V_{GFh} - V_{GSth} - V_{FS})}{\gamma_1^2}}\right) + (V_{GS} - V_{GFh})\right] \quad , \end{aligned}$$

$$Q_C = -WLC_{OX}\left(V_{GSth} - \alpha_x \cdot (1-f_s)\cdot V_{DSATh}\frac{4T_C - 1}{6T_C}\right) \quad ,$$

$$Q_B = -(Q_G + Q_C) \quad .$$

(B) 40/60 Channel-Charge Partitioning

$$Q_D = -WLC_{OX}V_{GSth}\left(\frac{-1}{2} + T_C + \frac{(1-T_C)(1+3\cdot T_C + 6\cdot T_C^2)}{30\cdot T_C^2}\right) \quad ,$$

$$Q_S = -WLC_{OX}V_{GSth}\left(\frac{1}{2} + \frac{(1-T_C)^2}{3\cdot T_C} - \frac{(1-T_C)(1+3\cdot T_C + 6\cdot T_C^2)}{30\cdot T_C^2}\right) \quad .$$

(C) 0/100 Channel-Charge Partitioning

$$Q_D = -W_{eff}L_{eff}C_{OX}V_{GSth}\left(-1+\frac{3T_C}{2}+\frac{(1-T_C)^2}{2T_C}\right) \quad ,$$

$$Q_S = -W_{eff}L_{eff}C_{OX}V_{GSth}\left(1-\frac{T_C}{2}-\frac{(1-T_C)^2}{6\cdot T_C}\right) \quad .$$

(D) 50/50 Channel-Charge Partitioning

$$Q_D = -\frac{1}{2}W_{eff}L_{eff}C_{OX}\left(V_{GSth}-\alpha_x\cdot(1-f_s)\cdot V_{DSATh}\frac{4T_C-1}{6T_C}\right) \quad ,$$

$$Q_S = -\frac{1}{2}W_{eff}L_{eff}C_{OX}\left(V_{GSth}-\alpha_x\cdot(1-f_s)\cdot V_{DSATh}\frac{4T_C-1}{6T_C}\right) \quad .$$

(E) Five Major Capacitances for Small Signal Analysis

$$C_{GB} = WLC_{OX}\cdot\left(\frac{f_s}{\sqrt{1+\frac{4(V_{GFh}-V_{FS})}{\gamma_1^2}}}+\frac{f_c(\alpha_x-1)}{3\alpha_x}\cdot\frac{(1-T_C)^2}{T_C^2}\right) \quad ,$$

$$C_{GD} = WLC_{OX}\cdot\left(\frac{2f_c}{3}\cdot\frac{4\cdot T_C^2-1}{4\cdot T_C^2}\right) \quad ,$$

$$C_{GS} = WLC_{OX}\cdot\left(\frac{2f_c}{3}\cdot\frac{4\cdot T_C-1}{4\cdot T_C^2}\right) \quad ,$$

$$C_{BD} = WLC_{OX}\cdot\left(\frac{2f_c(\alpha_x-1)}{3}\cdot\frac{4\cdot T_C^2-1}{4\cdot T_C^2}\right) \quad ,$$

$$C_{BS} = WLC_{OX}\cdot\left(\frac{2f_c(\alpha_x-1)}{3}\cdot\frac{4\cdot T_C-1}{4\cdot T_C^2}\right) \quad .$$

Appendix B

RF MOS Transistor Modeling and Parameter Extraction Valid up to 10-GHz

List of Symbols

d_i	intrinsic drain reference node
g_i	intrinsic gate reference node
s_i	intrinsic source reference node
b_i	intrinsic substrate reference node
f_T	transit frequency
C_{gdo}	gate-to-drain overlap capacitance
C_{gso}	gate-to-source overlap capacitance
τ	transadmittance time constant
N_F	number of fingers for multiple-finger MOS transistor
N_S	number of sources for multiple-finger MOS transistor
W_G	gate width per finger
L_G	gate length
L_{sb}	distance between source and substrate contacts
H_{DIF}	length of the heavily doped diffusion from contact to lightly doped area
R_{pds}	substrate resistance under the channel area

R_{psb} substrate resistance between source and substrate contact

L_{ov} length of the overlap area between gate and drain/source

C_{jdb} junction capacitance between drain and substrate

C_{jsb} junction capacitance between source and substrate

As the wireless communication markets continue to expand, advances in wireless transceivers demand higher levels of integration and low cost technologies. A popular solution is CMOS, where low-power performance advantage in the baseband are well established and significant work has been aggressively targeting a CMOS radio-frequency (RF) front end that can be integrated into a single chip [1, 2]. A critical issue for production design is the availability of RF CMOS circuit model to accurately describe MOS transistor behaviors at very high frequencies. This is a critical determinant to the first-time design success and the meeting of market windows with CMOS RF products. In [1-4], fundamental analysis on high-frequency FET behavior was described. The distributed substrate effects were described in [8]. Due to the complexity of the equivalent circuit, a time-consuming optimization approach was used to extract the parameter values [8]. In this appendix, a physically-based small signal equivalent circuit of the MOS transistor for RF, and an accurate direct parameter extraction approach by Y-parameter analysis from measured S-parameters to determine the parameter values are described.

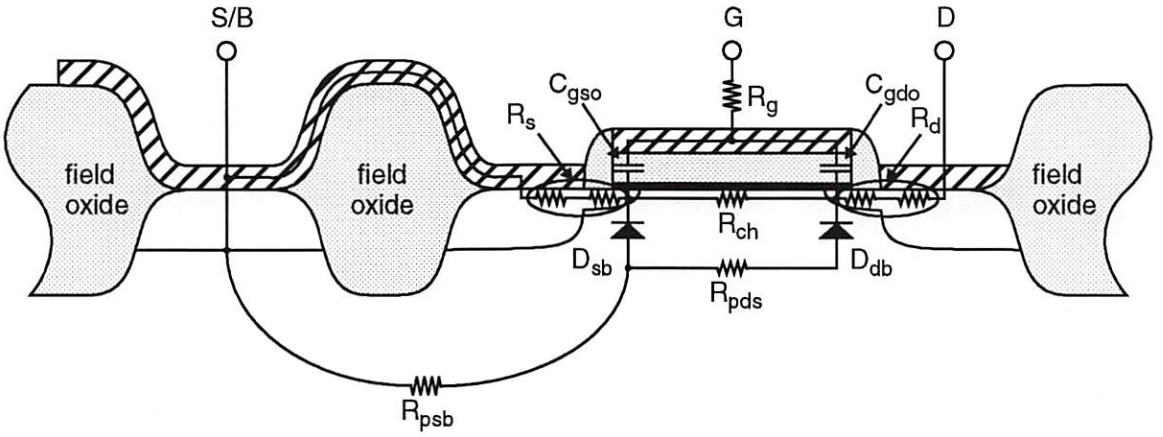
Most of the commercially available MOS transistor models [9, 10] were originally developed for digital and low-frequency analog circuit design, which focus on the DC drain current, conductances and intrinsic charge/capacitance behavior around the MHz range. However, as the operation frequency increases to the GHz range, the

importance of extrinsic components rivals that of the intrinsic counterparts. For efficient circuit design, simplicity of the MOS transistor model is to be maintained. The quasi-static intrinsic channel-region model, which is suitable for submicron CMOS high-frequency applications, is used. The gate series resistance, R_G, which is not included in most CMOS circuit models but significantly affects the input behavior at RF, needs to be carefully considered. In addition, the substrate coupling effects through the substrate resistances which plays an important role for the output admittance is also very critical. All the components of the equivalent circuit are extracted by Y-parameter analysis. Information when the MOS transistor is biased in the triode region is used to reliably extract the extrinsic component values, including the gate, source, and drain series resistances. These are used to de-embed the extrinsic equivalent circuit components from the intrinsic ones. This methodology provides critical information about the relative magnitude of parasitics components

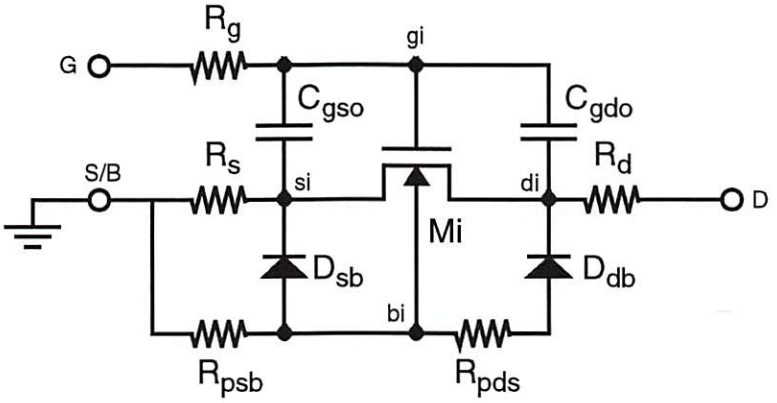
B.1 Small-Signal Equivalent Circuit of MOS Transistors at RF

Analysis of the MOS transistor at RF can be based on the quasi-static approximation in order to minimize mathematical complexity. In [11], it is shown that the quasi-static and non-quasi-static models have similar accuracy of operation for frequencies up to the transit frequency, f_T. With aggressive submicron CMOS technologies, e.g. 0.5 μm technology, f_T can reach several GHz range for the low-voltage/low-power applications. For a quarter-micron technology, f_T is as high as 20 GHz, which is suitable for future RF CMOS applications.

The cross section of an NMOS transistor is shown in Fig. B.1 (a). There are finite resistances in the drain, source, and gate terminal and substrate layer. In the



(a)



Mi : intrinsic part of the MOST

(b)

Figure B.1: A complete diagram of an NMOS transistor including the extrinsic effects. (a) The cross section of an NMOS transistor. (b) The equivalent extrinsic effects.

low-frequency operation, the substrate is treated as being ideal without any loss and coupling. However, as the operation frequency increases, the equivalent impedance of the junction capacitances reduces. The signal coupling through the substrate resistances from the drain to the source and from the source to the substrate contact has to be carefully considered. This nonideal coupling effect especially affects the transadmittance, Y_{12}, and output admittance, Y_{22}, which are always treated as the important indices for RF design. On the other hand, the terminal series resistances also play very important role at RF, especially affecting the input impedance.

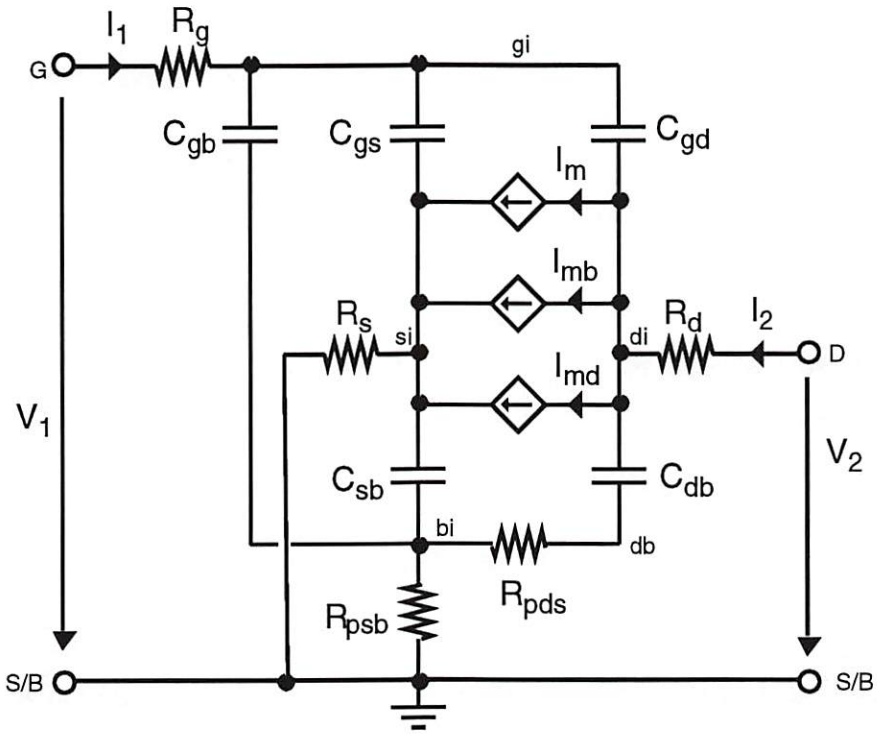
As shown in Fig. B.1 (b), the equivalent behavior of an MOS transistor at high frequency includes the intrinsic transistor behavior, terminal resistances, substrate resistance, and junction diodes. Determination of the terminal reference nodes for intrinsic behavior is very important, especially for high frequency analysis. In this model, the intrinsic source, drain, and gate reference nodes are determined by the interface points of the source/drain to channel and the gate to thin oxide. Notice that the distributed effect in substrate through the channel area has to be considered for determining the intrinsic substrate. However, this results in the intrinsic substrate being located in the middle of R_{pds}. By doing so, the R_{pds} has to be separated to become two resistors, and one extra node is created in the equivalent circuit. From the experimental results for short-channel devices, the value of R_{pds} is small and there are no significant differences for the transistor modeling behavior by choosing either end or the middle point of R_{pds} as the intrinsic substrate. Therefore, to save one node and one component count in the equivalent circuit, the source-related side of R_{pds} is used as the intrinsic substrate reference node, as shown in Fig. B.1 (b). On the other hand, the overlap capacitances, C_{gdo} and C_{gso}, are also playing an important role for the short-channel devices, especially in the saturation region

where the intrinsic $C_{gdi} \cong 0$ and the total gate to drain capacitance is dominated by C_{gdo}.

The small-signal equivalent circuit of an MOS transistor for high frequency is shown in Fig. B.2. The complete quasi-static model is performed on the intrinsic behavior, including the transcapacitances in the channel [13]. Here, in order to simplify the circuit representation, overlap capacitances and junction capacitances are merged into the correspondent intrinsic capacitances. Therefore, the components in the circuit are described by

$$
\begin{aligned}
I_m &= Y_m \cdot V_{gsi} = (g_m - j\omega C_m) \cdot V_{gsi} = g_m \cdot (1 - j\omega\tau) \cdot V_{gsi}, && \text{(B.1)}\\
I_{mb} &= Y_{mb} \cdot V_{bsi} = (g_{mb} - j\omega C_{mb}) \cdot V_{bsi} = g_{mb} \cdot (1 - j\omega\tau) \cdot V_{bsi}, && \text{(B.2)}\\
I_{md} &= Y_{md} \cdot V_{dsi} = (g_{ds} + j\omega C_{sd}) \cdot V_{dsi} = g_{ds} \cdot (1 - j\omega\tau) \cdot V_{dsi}, && \text{(B.3)}\\
\tau &= \frac{C_m}{g_m} = \frac{C_{mb}}{g_{mb}} = \frac{-C_{sd}}{g_{ds}} = L_G^2 \cdot \tau', && \text{(B.4)}
\end{aligned}
$$

$$
\begin{aligned}
C_{gs} &= C_{gsi} + C_{gso}\\
&= N_F \cdot W_G \cdot (L_G \cdot c'_{gsi} + L_{ov} \cdot c'_{gso}), && \text{(B.5)}\\
C_{gd} &= C_{gdi} + C_{gdo}\\
&= N_F \cdot W_G \cdot (L_G \cdot c'_{gdi} + L_{ov} \cdot c'_{gdo}), && \text{(B.6)}\\
C_{gb} &= C_{gbi} + C_{gbo}\\
&= N_F \cdot W_G \cdot L_G \cdot c'_{gsi} + N_F \cdot L_G \cdot W_{ov} \cdot c'_{gbo}, && \text{(B.7)}\\
C_{sb} &= C_{bsi} + C_{jsb}\\
&= N_F \cdot W_G \cdot L_G \cdot c'_{bsi} + N_S \cdot W_G \cdot 2H_{DIF} \cdot c'_{jsb}, && \text{(B.8)}\\
C_{db} &= C_{bdi} + C_{jdb}\\
&= N_F \cdot W_G \cdot L_G \cdot c'_{bdi} + (N_F + 1 - N_S) \cdot W_G \cdot 2H_{DIF} \cdot c'_{jsb}, && \text{(B.9)}
\end{aligned}
$$



$$I_m = Y_m \cdot (V(gi) - V(si))$$
$$I_{mb} = Y_{mb} \cdot (V(bi) - V(si))$$
$$I_{md} = Y_{md} \cdot (V(di) - V(si))$$

$$Y_m = g_m - j\omega \cdot C_m = g_m \cdot (1 - j\omega \cdot \tau)$$
$$Y_{mb} = g_{mb} - j\omega \cdot C_{mb} = g_{mb} \cdot (1 - j\omega \cdot \tau)$$
$$Y_{md} = g_{ds} + j\omega \cdot C_{sd} = g_{ds} \cdot (1 - j\omega \cdot \tau)$$
$$\tau = \frac{C_m}{g_m} = \frac{C_{mb}}{g_{mb}} = \frac{-C_{sd}}{g_{ds}}$$

Figure B.2: The complete small-signal equivalent circuit of an MOS transistor for all operation regions.

and

$$R_g = \frac{W_G}{N_F \cdot L_G} \cdot r'_g, \tag{B.10}$$

$$R_d = \frac{H_{DIF}}{N_F \cdot W_G} \cdot r'_d, \tag{B.11}$$

$$R_s = \frac{H_{DIF}}{N_F \cdot W_G} \cdot r'_s, \tag{B.12}$$

$$R_{pds} = \frac{2H_{DIF} + L_G}{N_F \cdot W_G} \cdot r'_{pds}, \tag{B.13}$$

$$R_{psb} = \frac{L_{sb}}{N_S \cdot W_G} \cdot r'_{psb}. \tag{B.14}$$

Here, all the c' and r' are defined as the capacitances and resistances per unit length and unit width. The transcapacitances, C_m and C_{mb}, are derived from the inter-nodal capacitances to represent the non-reciprocal capacitance effects,

$$C_m = C_{dg} - C_{gd}, \tag{B.15}$$

$$C_{mb} = C_{db} - C_{bd}. \tag{B.16}$$

The capacitve effect can be calculated from $j\omega \cdot C_{ij} = -dI_i/dV_j$. Thus, the small signal current and voltage relationship, $-dI_g/dV_d = j\omega \cdot C_{gd}$ and $-dI_d/dV_g = j\omega \cdot (C_{gd} + C_m)$ can be obtained. The capacitive coupling of drain to gate is represented by C_{gd}, and $C_{gd} + C_m = C_{dg}$ represents the capacitive coupling of gate to drain. Similar descriptions hold for C_{mb}. Notice that, to complete the transadmittance behavior, there is another transcapacitance, $C_{mx} = C_{bg} - C_{gb}$, in parallel with C_{sb}. However, this transcapacitance always takes zero value in all operation regions [13]. Thus, it can be neglected from the small-signal equivalent circuit.

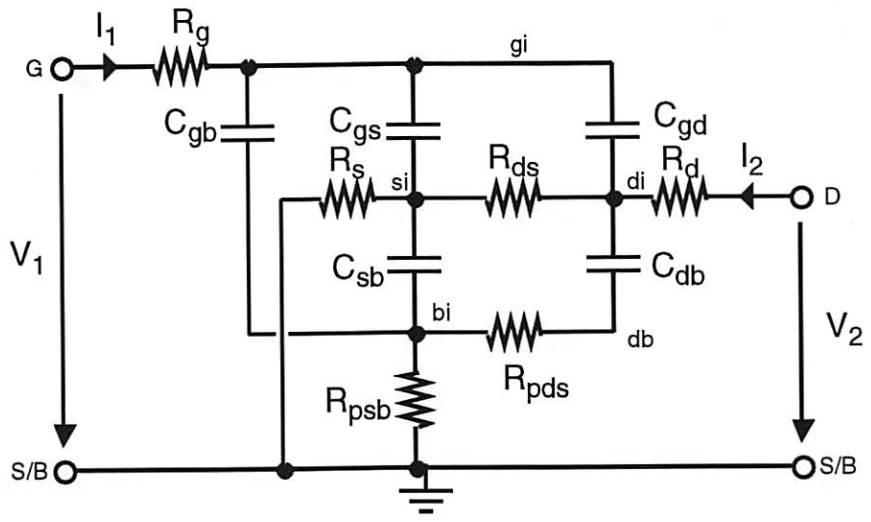


Figure B.3: The small-signal equivalent circuit for the triode region with $V_{DS} = 0\ V$.

B.2 Y-Parameter Analysis of The Two-Port MOS Transistor in Triode Region

Analysis of the small-signal equivalent circuit for high-frequency operation is done by Y-parameter analysis. In Fig. B.2, there are totally 13 components in the two-port network, which make the analysis and extraction to be very complicated. In order to more clearly analyze the effects of each component, the physical meaning and behavior of all the components are emphasized.

In order to extract the effects of extrinsic components, the transistor can be biased in specific region of operation to reduce the intrinsic effects. By biasing the transistor in the triode region with the drain-to-source voltage, V_{DS}, set to zero, the intrinsic behavior of the transistor becomes symmetric in terms of the gate to the drain/source. Therefore, the effects of transconductances and transcapacitances become very small, $g_m \cong 0$, $g_{mb} \cong 0$, $c_m \cong 0$, and $C_{mb} \cong 0$, and the small-signal equivalent circuit can be simplified, as shown in Fig. B.3. This simplified two-port network has only the capacitances and resistances to includes the substrate coupling,

terminal resistive, and intrinsic capacitive effects. By considering the RC time constant effects of the network, further simplification can be made to the equivalent circuit by the following assumptions:

- Assumption I: R_g, R_s, and R_d are dominated by the resistive poly-silicon and diffusion layers and treated as bias- and frequency-independent;

- Assumption II: the equivalent impedance from intrinsic source/drain to the outer source/drain are dominated by the terminal resistances, R_s and R_d,

$$| j\omega C_{sb} R_s | = \omega \cdot (\frac{N_S}{N_F} \cdot 2H_{DIF} \cdot c'_{jsb} + L_G \cdot c'_{bsi}) \cdot H_{DIF} \cdot r'_s \ll 1, \quad \text{(B.17)}$$

$$| \frac{1}{j\omega C_{sb}} | \gg R_s, \quad \text{(B.18)}$$

and

$$| \frac{1}{j\omega C_{db}} | \gg R_d; \quad \text{(B.19)}$$

- Assumption III: in the triode region with $V_{DS} = 0\ V$, the intrinsic gate to bulk capacitance, C_{gbi}, is close to zero, and the total C_{gb} is dominated by C_{gbo} which is much smaller than C_{gs} and C_{gd};

- Assumption IV: the operation frequency is up to around 10 GHz, which results,

$$\begin{aligned} (\omega C_{gd} R_d)^2 &= (\omega \cdot (L_G \cdot c'_{gdi} + L_{ov} \cdot c'_{gdo}) \cdot H_{DIF} \cdot r'_d)^2 \ll 1, \\ (\omega C_{gs} R_s)^2 &\ll 1, \end{aligned} \quad \text{(B.20)}$$

$$\omega^2 C_{gs} C_{gd} (R_d + R_d) R_g \ll 1, \quad \text{(B.21)}$$

and

$$\frac{1}{1+j\omega C_{gg}R_g} \cong 1 - j\omega C_{gg}R_g, \tag{B.22}$$

where C_{gg} is defined as the total gate capacitance;

- Assumption V: with proper V_{GS} bias, the channel resistance is much larger than terminal series resistance, $R_{ds} \gg R_d, R_s$.

All those assumptions are valid for large RF MOS transistors and can be experimentally verified.

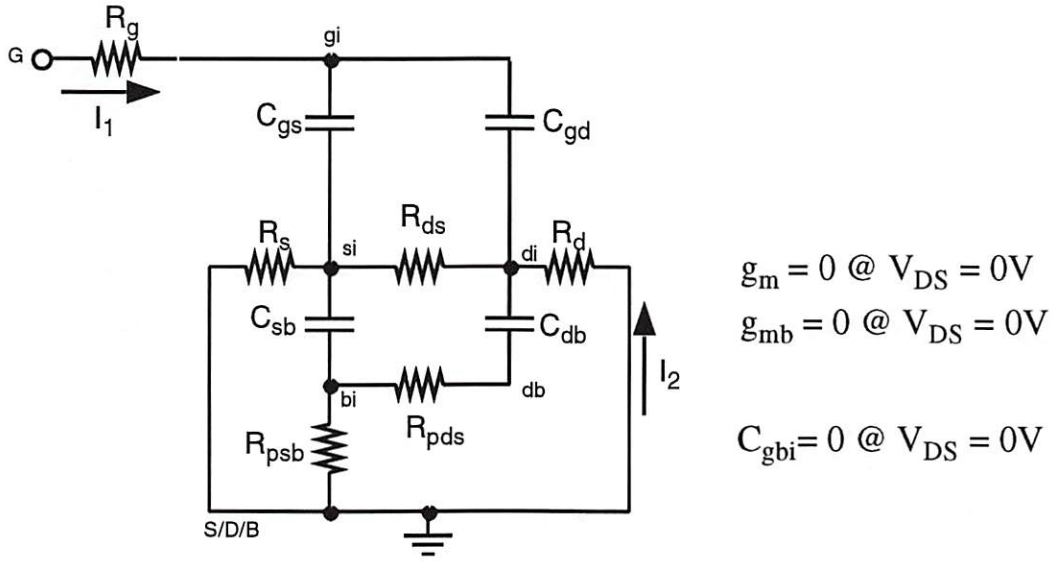


Figure B.4: The small-signal equivalent circuit for Y_{11} analysis in the triode region at $V_{DS} = 0\ V$.

As shown in Fig. B.4, the equivalent circuit for the Y_{11} analysis is obtained by shorting the output port to the ground. Since the transistor operates in the triode region with $V_{DS} = 0\ V$, C_{gs} is approximately equal to C_{gd}. The structure and the equivalent effects of the circuit is fully symmetric, which makes the effect of R_{ds} very small and can be neglected. By using Assumption II, the substrate effects from C_{sb},

C_{db}, R_{pds}, and R_{psb} can be neglected as compared to the effects of R_d and R_s. Thus, the input admittance Y_{11} can be expressed as

$$Y_{11} = \left(R_g + \left(\frac{1}{R_s + \frac{1}{j\omega C_{gs}}} + \frac{1}{R_d + \frac{1}{1+j\omega C_{gd}}} \right)^{-1} \right)^{-1}. \quad \text{(B.23)}$$

If it is expanded, (B.23) has many higher order terms. By using Assumption IV, some of the higher-order terms have negligible effect, and (B.23) can be simplified to

$$Y_{11} \cong j\omega C_{gg} + \omega^2 (C_{gg}^2 R_g + C_{gs}^2 R_s + C_{gd}^2 R_d). \quad \text{(B.24)}$$

Here, C_{gg} is defined as the total gate capacitance from the gate to the ground. The above expression reveals that Y_{11} is mainly affected by the total gate capacitance and the RC effects in the terminals.

To determine Y_{12} expression, the gate terminal of the equivalent circuit in Fig. B.3 has to be shorted to the ground. However, the circuit, even at $V_{DS} = 0\ V$, still has a very complicated signal path from R_g to the output, i.e., the drain terminal. In order to reduce the complexity of the equivalent circuit, a voltage-controlled voltage-source is added in parallel with R_s to represent the equivalent effect of output voltage on R_{ds}, as shown in Fig. B.5. Since the impedance of R_d is much smaller than the equivalent impedance from V_{di} to the ground, the voltage drop on R_d is small and can be neglected. Therefore, by assuming $V_d \cong V_{di}$, Y_{12} can be expressed as,

$$\begin{aligned} Y_{12} &= \frac{I_1}{V_{di}} \cdot \frac{V_{di}}{V_d} \\ &\cong \frac{I_1}{V_{di}} \\ &= -(R_g + \frac{1 + \frac{j\omega C_{gs} R_g}{1+j\omega C_{gs} Z_x}}{j\omega C_{gd}})^{-1} \end{aligned}$$

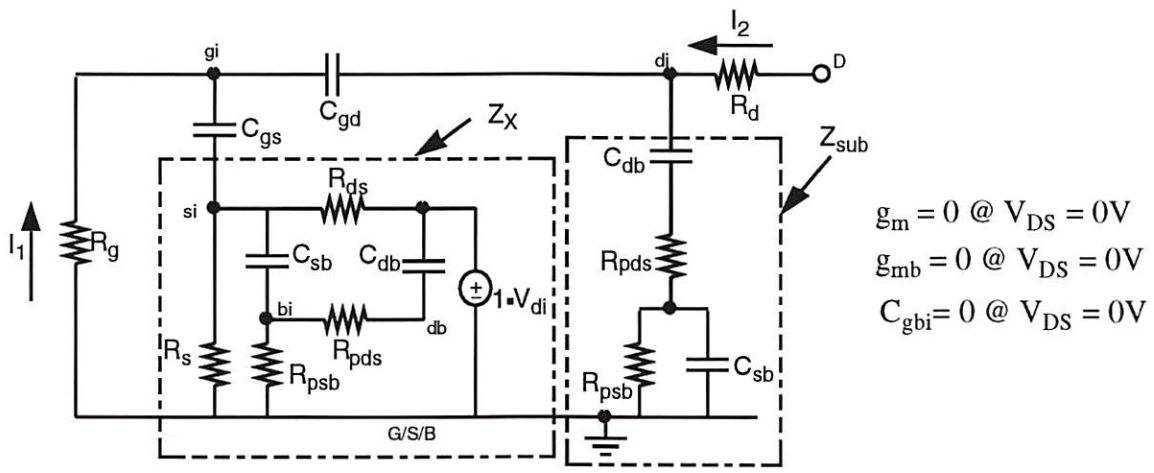


Figure B.5: The small-signal equivalent circuit for Y_{12} analysis in the triode region at $V_{DS} = 0\ V$.

$$\cong \quad -j\omega C_{gd} - \omega^2 C_{gd} C_{gg} R_g. \tag{B.25}$$

Here, Assumption IV is used in the above expression to simplify the higher-order terms.

For the analysis of Y_{21}, the same circuit employed for Y_{11} in Fig. B.4 can be used. By taking the transadmittance from the output to the input, the Y_{21} is expressed as,

$$\begin{aligned} Y_{21} &= \frac{-j\omega C_{gd}}{1 + j\omega(C_{gd} R_d + C_{gg} R_g)} \\ &\cong -j\omega C_{gd} - \omega^2 (C_{gd}^2 R_d + C_{gd} C_{gg} R_g). \end{aligned} \tag{B.26}$$

The above expressions for Y_{11}, Y_{12}, and Y_{21} contain all the information required for extraction of the series resistances and intrinsic capacitances. By taking the related Y-parameters, the extracted values for capacitances and resistances are determined,

$$C_{gg} = \left| \frac{Imag(Y_{11})}{\omega} \right| , \tag{B.27}$$

$$C_{gd} = |\frac{Imag(Y_{12})}{\omega}| \ , \tag{B.28}$$

$$C_{gs} = C_{gd} \ , \tag{B.29}$$

$$C_{gb} = C_{gg} - C_{gd} - C_{gs} \ , \tag{B.30}$$

$$R_g = |\frac{Real(Y_{12})}{Imag(Y_{12}) \cdot Imag(Y_{11})}| \ , \tag{B.31}$$

$$R_d = |\frac{Real(Y_{21}) - Real(Y_{12})}{Imag(Y_{12})^2}| \ , \tag{B.32}$$

$$R_s = |\frac{Real(Y_{11})}{Imag(Y_{11})^2} - R_g - \frac{C_{gd}^2}{C_{gg}^2} R_d | \cdot \frac{C_{gg}^2}{C_{gs}^2} \ . \tag{B.33}$$

Figure B.6 and Figure B.7 show the extracted series resistances and capacitances as a function of frequency with the transistor biased in the triode region. These components are frequency-independent. The extracted gate resistance is about 4.27 Ω per square area. The total gate capacitance, including the overlap capacitances, of a 20-finger transistor is about 417 fF. Notice that the gate to bulk capacitance, C_{gb}, at $V_{DS} = 0\ V$ is dominated by the overlap capacitance, which is around 25 fF and accounts for about 6% of the total gate capacitance. Since R_g, R_d, and R_s are bias-independent, the extracted values from the triode region can also be used to evaluate the transistor characteristics in the saturation region.

B.3 Y-Parameter Analysis of The Two-Port MOS Transistor in Saturation Region

In most of MOS circuit applications at RF, the transistor is biased in the saturation region in order to achieve high voltage gain and large dynamic range. The purpose of the analysis in the previous section at $V_{DS} = 0\ V$ is to extract the series resistances with the simplified equivalent circuit, and to extract the related capacitances. Since

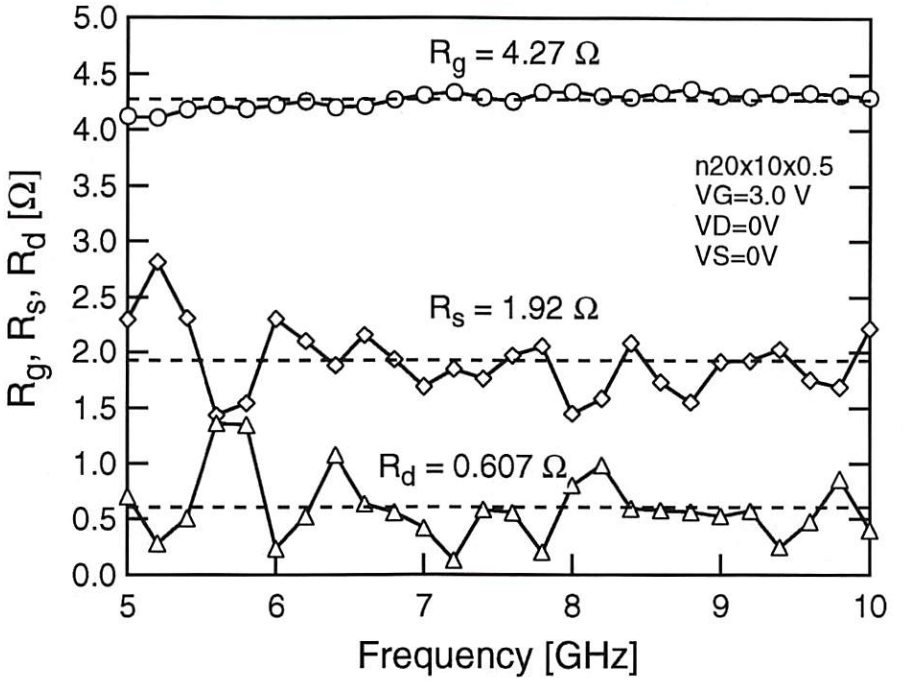


Figure B.6: The extracted terminal resistances of an NMOS transistor at $V_{DS} = 0\ V$ and $V_{GS} = 3\ V$.

only the imaginary parts are needed to determine the intrinsic capacitances, this extraction method for C_{gg} and C_{gd} can also be applied to the saturation region.

In the saturation region, the depletion charge is not changed by perturbing the drain terminal voltage. Therefore, the capacitance $C_{bdi} \cong 0$ can be separated from the substrate effects and C_{bd} in the equivalent circuit is dominated by junction capacitance, C_{jdb}. To extract the equivalent admittance of substrate effects, the series resistance, R_g and R_d, from the input and output ports are de-embedded first to simplify the equivalent circuit, as shown in Fig. B.8. Thus,

$$Z'_{11} = Z_{11} - R_g,$$

$$Z'_{12} = Z_{12},$$

$$Z'_{21} = Z_{21},$$

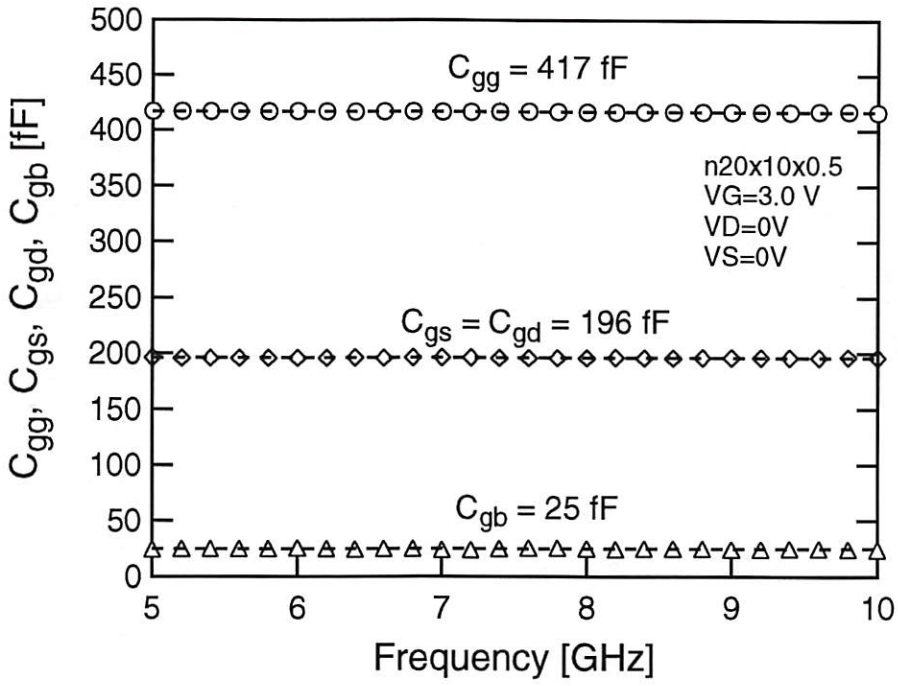


Figure B.7: The extracted intrinsic capacitances of an NMOS transistor at $V_{DS} = 0\ V$ and $V_{GS} = 3\ V$.

$$Z'_{22} = Z_{22} - R_d, \tag{B.34}$$

where Z is the Z-parameter of Fig. B.2 and Z' is the Z-parameter of Fig. B.8. In order to extract the substrate effects, the Y'_{22} analysis has to be performed by shorting the gate to the ground. In the saturation region, the channel capacitance, C_{sd}, is close to zero [13], and the resistor $R_{ds} = 1/g_{ds}$, which is dominated by the channel-length modulation effect, has a high resistance value. Thus, I_{md} can be reduced to R_{ds}. On the other hand, as the gate is shorted to the ground, the intrinsic gate to source voltage, V_{gsi}, is controlled by the voltage drop in R_s. In saturation region, R_s is much smaller than R_{ds}. Therefore, $V_{gsi} \cong \frac{R_s}{R_{ds}+R_s} \cdot V_{dsi} \cong 0$ and $I_m \cong 0$. The equivalent

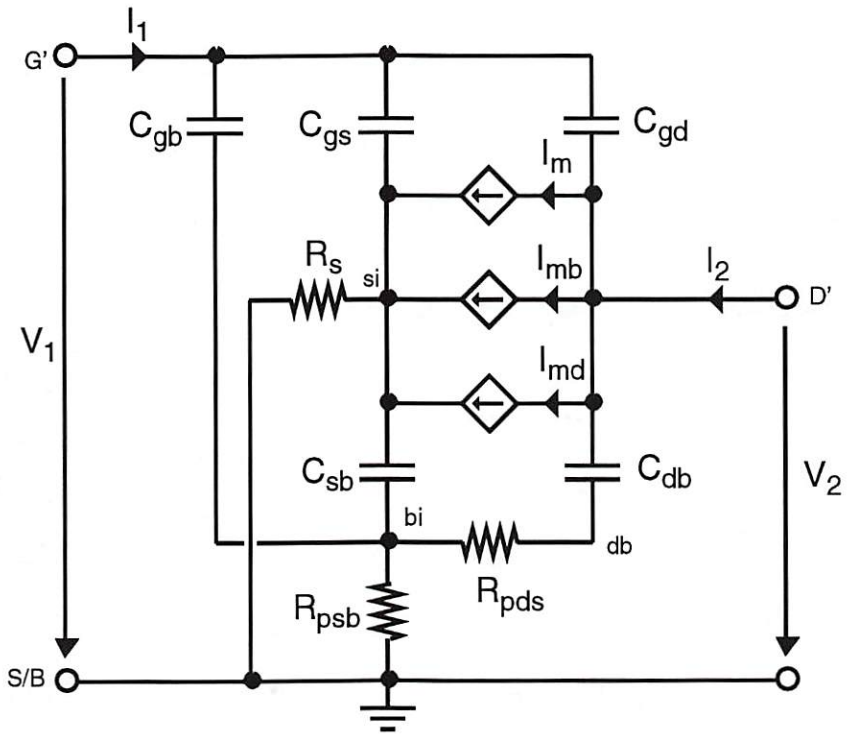
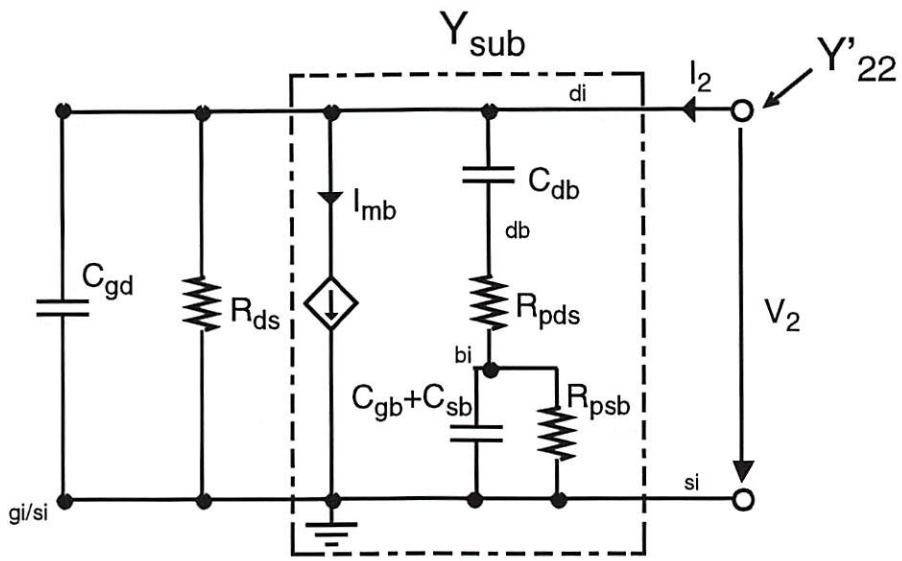


Figure B.8: An equivalent circuit for the Y-parameter analysis in the saturation region by de-embedding R_D and R_G.

circuit for Y'_{22} can be further simplified to Fig. B.9. By carrying out the Y'_{22} analysis, the equivalent substrate admittance, Y_{sub}, is derived,

$$Y_{sub} = Y'_{22} - j\omega C_{gd} - g_{ds}. \tag{B.35}$$

Here g_{ds} is extracted from the value of $(\frac{1}{Real(Y'_{22})} - R_s)^{-1}$ at low frequency ($< 1GHz$), and C_{gd} is obtained from $|\ \frac{Imag(Y_{12})}{\omega}\ |$. Thus, Y_{sub} is extracted from (B.35). The voltage-controlled current, I_{mb}, is controlled by the intrinsic substrate voltage, V_{bsi}, which is an internal node of the substrate network and can not be separated at this step. Therefore the extracted Y_{sub} includes the effect from I_{mb}. This substrate network is mainly contributed by two capacitances, two substrate resistances, and I_{mb}. Since in the test structure, the source and the substrate are always tied together,



$$I_{mb} = Y_{mb} \cdot (V(bi) - V(si))$$

Figure B.9: The simplified equivalent circuit by neglecting R_S in the saturation region.

g_{mb} can not be directly extracted. In this work, the g_{mb} is calculated from g_m by the relationship between g_m and g_{mb}, where g_m is obtained from $Real(Y'_{21})$ at low frequency.

In order to extract all the components in Y_{sub}, local optimization is performed on the equivalent circuit of Y_{sub} to fit the measured data. As shown in Fig. B.10, the extracted Y_{sub} from the measured data of a 20-finger NMOS transistor with $W_G = 10\ \mu m$ and $L_G = 0.5\ \mu m$ has the significant values in both real and imaginary parts as compared to the intrinsic behavior. The extracted C_{db} is about 116 fF which is contributed by the dynamic behavior of the junction diode, C_{jdb}. Notice that $C_{bdi} \cong 0$ in the saturation region. The other capacitive term from the intrinsic substrate to the ground has the value of about 382 fF. This term includes all the effects from the junction capacitance, C_{jsb}, intrinsic C_{bsi}, and the gate to substrate capacitance, C_{gb}. Figure B.10 also shows the excellent accuracy of this substrate

network model. Both the solid and dash lines are the SPICE simulated results by the equivalent circuit of Y_{sub} in Fig. B.9. Notice that good agreement has been achieved up to 10 GHz.

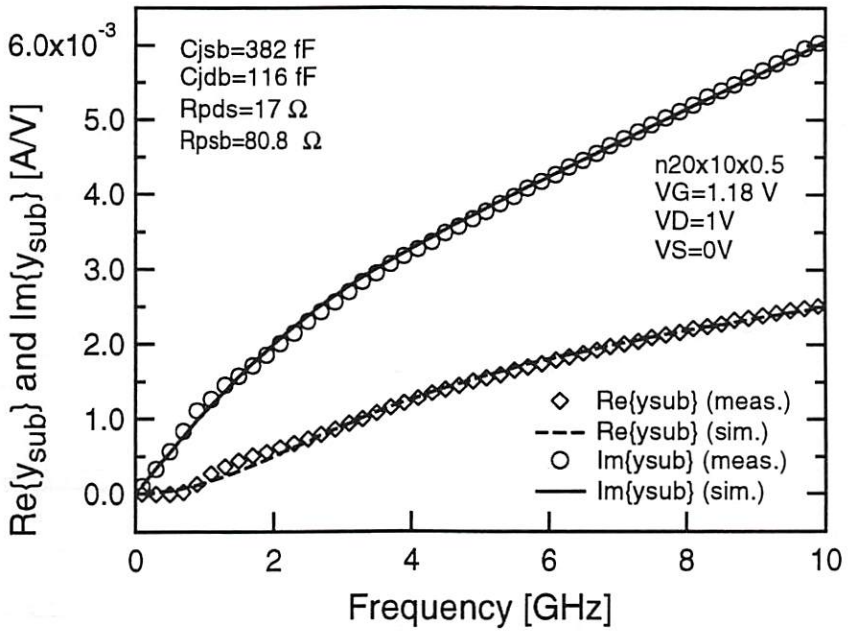


Figure B.10: The de-embedded measured data and simulated results of Y_{sub}.

B.4 Experimental Results and Discussion

The flowchart of direct extraction strategy is shown in Fig. B.11. Before starting the extraction process, effective capacitances of input/output pads, and the resistances and inductances of connection lines have to be completely de-embedded from the measured data. The extraction is very sensitive to the input/output pads de-embedding. If de-embedding is not complete, the correct characteristics of the equivalent circuit components from direct extraction results may not be obtained. In this work, a complete 2-step pad de-embedding procedure is used [14].

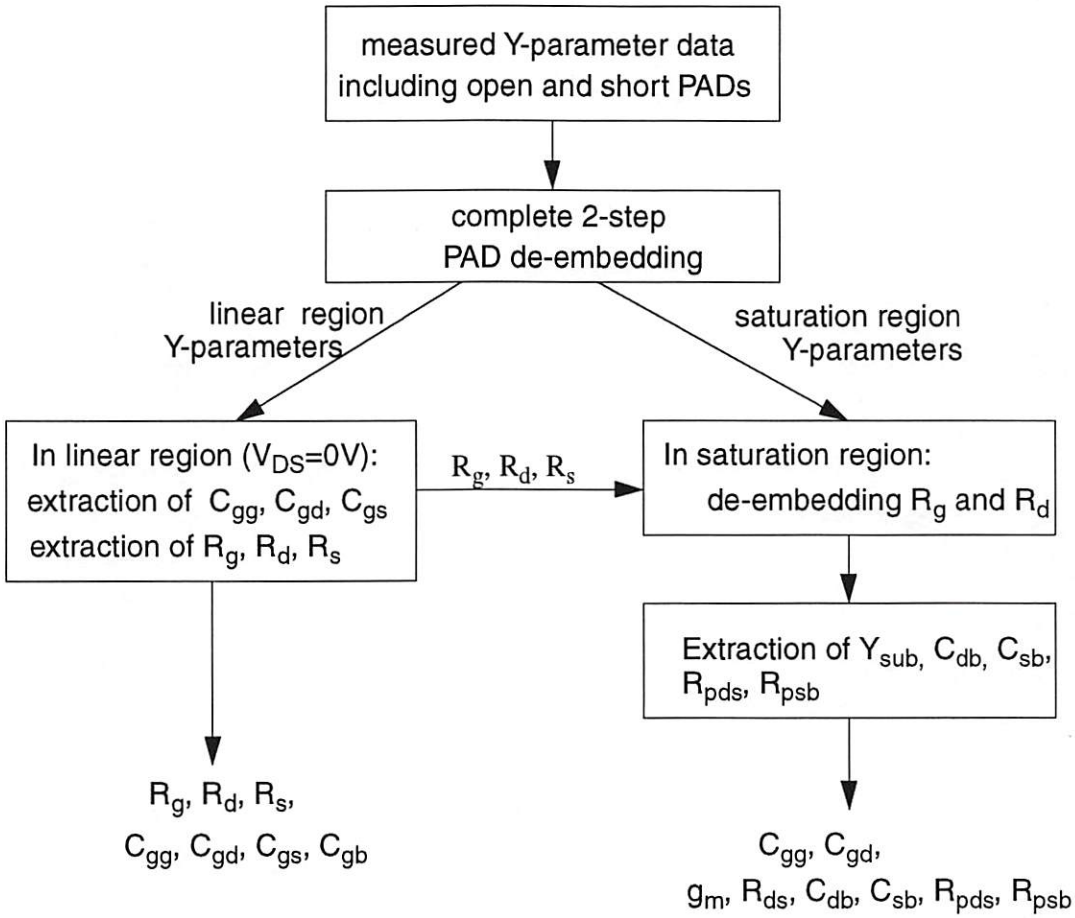


Figure B.11: The flowchart of the physics-based direct extraction strategy.

Extracted results of intrinsic capacitances in the saturation region with different bias conditions are shown in Fig. B.12. The frequency-independent and bias-dependent characteristics of the capacitances are clearly shown. On the other hand, by using a spot frequency measurement, the capacitances in different operation regions can be obtained. Figure B.13 shows the extracted intrinsic capacitances in all operation regions by using (B.27) and (B.28). The data are measured at 0.9 GHz. The total gate capacitances in the strong-inversion region and accumulation region do not match with the values at $V_{DS} = 0$. This is due to the bias-dependent overlap capacitance effects [15]. This method provides another efficient way to extract the intrinsic capacitances without C-V measurement. The value of total gate

capacitance C_{gg} is about 417 fF which is very close to the calculated result from $N_F \cdot W_G \cdot L_G \cdot C_{OX} + C_{ov}$. The plots of imaginary part of Y_{sub} with four different V_{GS} bias voltages are shown in Fig. B.14. All four lines meet together and are bias-insensitive to V_{GS}. As shown in Fig. B.15, SPICE simulation results by using the small-signal equivalent circuit in Fig. B.2 with extracted values are compared with the measured data in the saturation region. Notice that the simplified quasi-static model without including transcapacitances generates a significant error on Y_{21} at high frequency. This is due to the under-estimate of the transadmittance on I_2 from V_1. By comparing Fig. B.10 and Fig. B.15(d), it is clear that the substrate effect accounts for about 50 % of total output admittance, Y_{22}, especially in the high-frequency range. The values of the substrate junction capacitances and substrate resistances are comparable to the intrinsic capacitances and conductances, which make this network become very important in RF MOS transistor modeling. The SPICE simulation results from the complete RF MOS transistor model by including the extrinsic substrate and terminal resistance model, and the intrinsic S-CMOS model are shown in Fig. B.16. Good agreement between measured data and simulated results is obtained that supports the usefulness of the S-CMOS model as an important contributor to the overall RF circuit modeling.

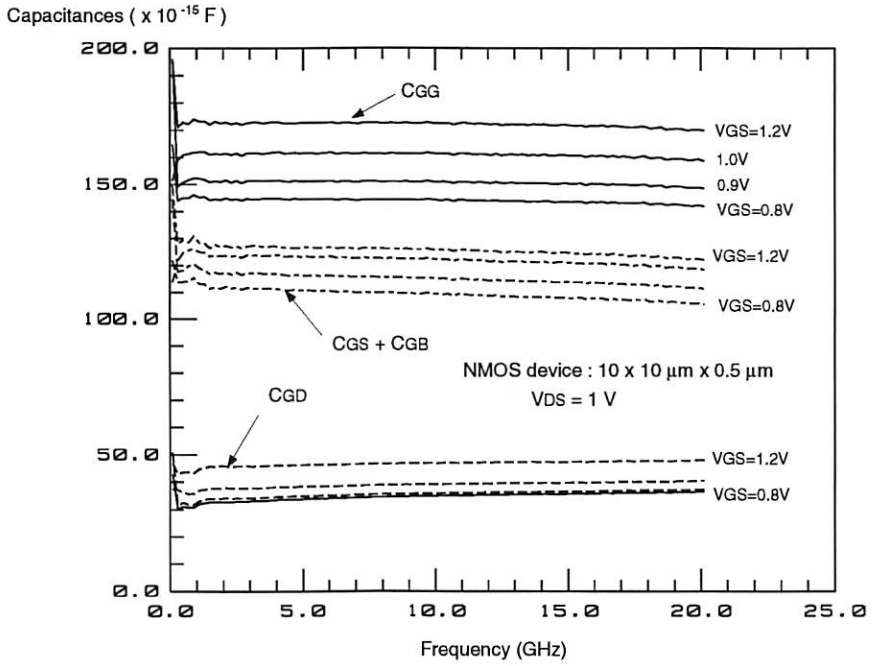


Figure B.12: Extracted results of the intrinsic capacitances in the saturation region.

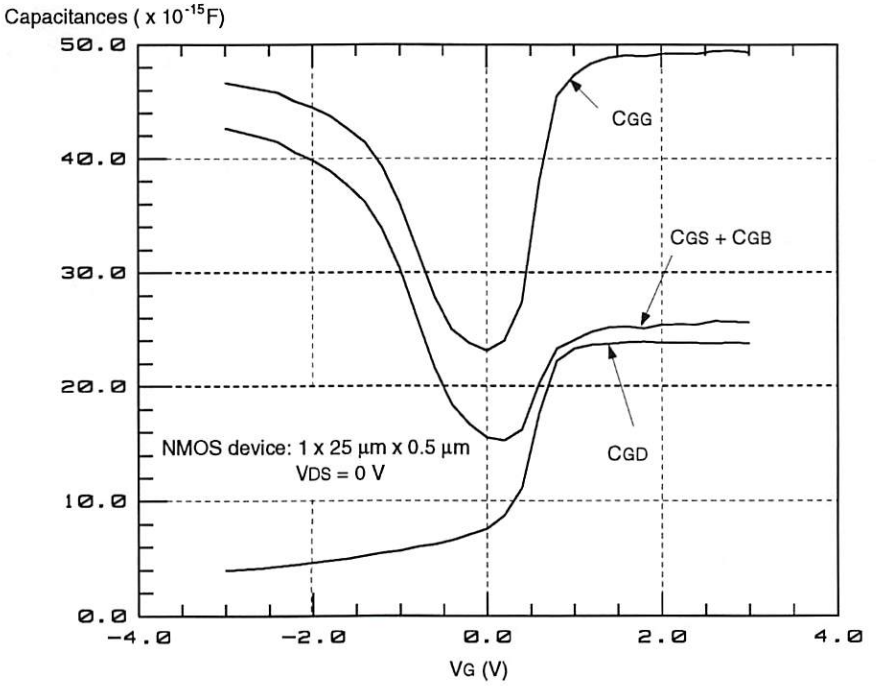


Figure B.13: Extracted results of the intrinsic capacitances at 0.9 GHZ in all operation regions at $V_{DS} = 0\ V$.

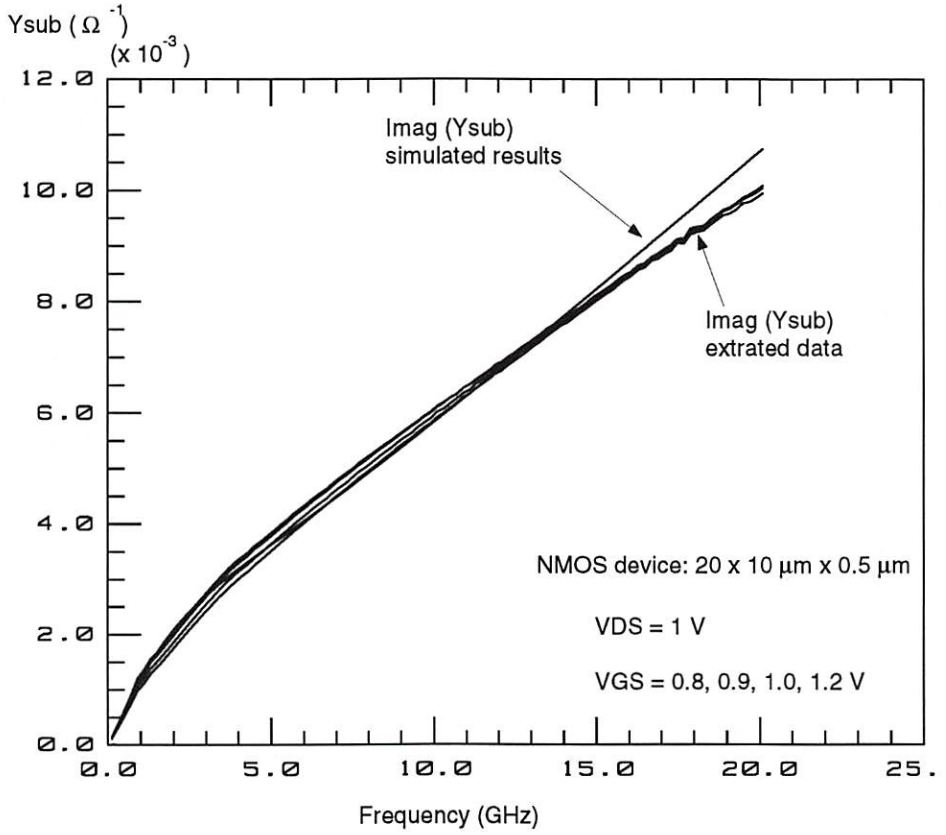
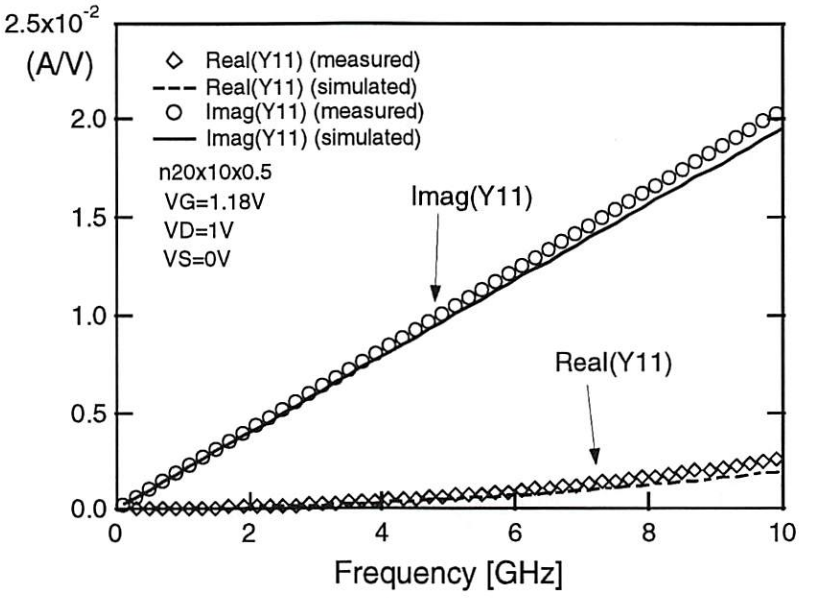
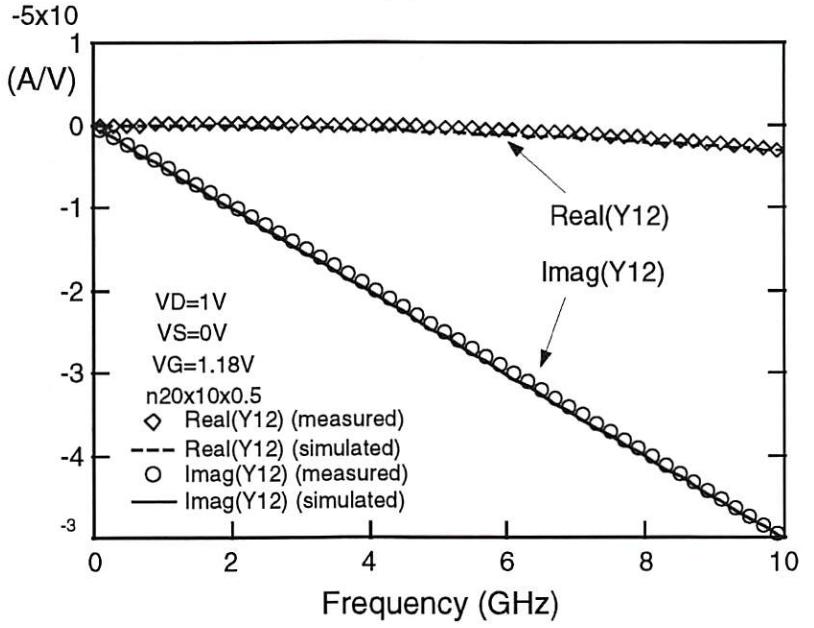


Figure B.14: De-embedded measured data and simulated results of imaginary part of Y_{sub} at $V_{DS} = 1\ V$ and $V_{GS} = 0.8\ V, 0.9\ V, 1.0\ V, 1.2\ V$.

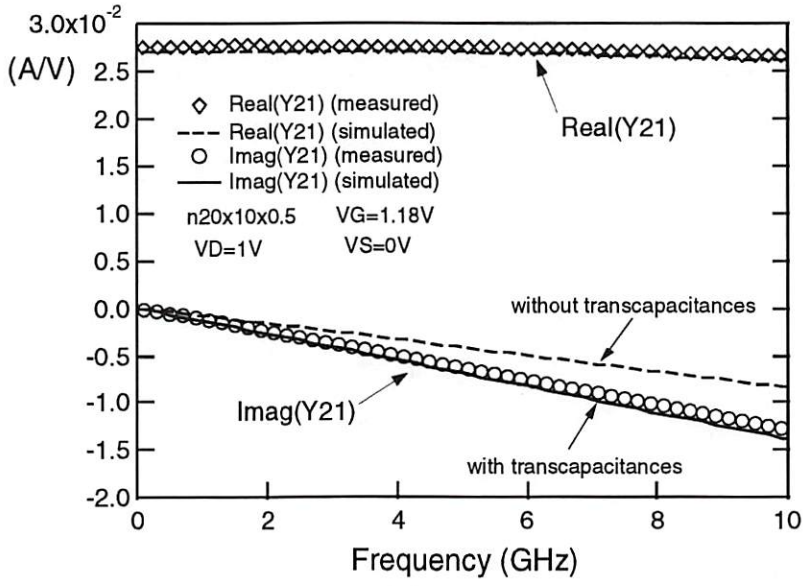


(a)

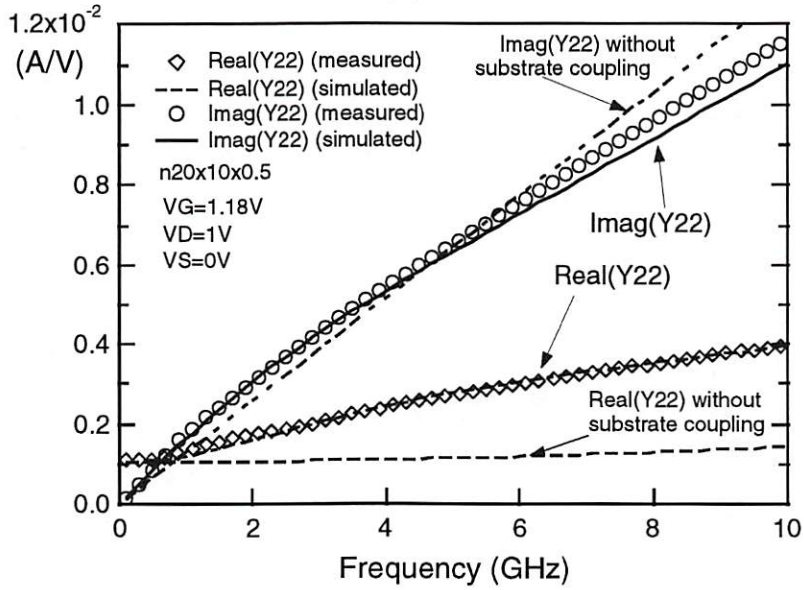


(b)

Figure B.15: Plots of Y-parameters of a 20-finger NMOS transistor with $W_g = 10\ \mu m, L_g = 0.5\ \mu m$ per finger at $V_{DS} = 1\ V$ and $V_{GS} = 0.8, 1.2\ V$. (a) Y_{11}. (b) Y_{12}. (c) Y_{21}. (d) Y_{22}. SPICE simulation results are obtained with the small-signal equivalent circuit.

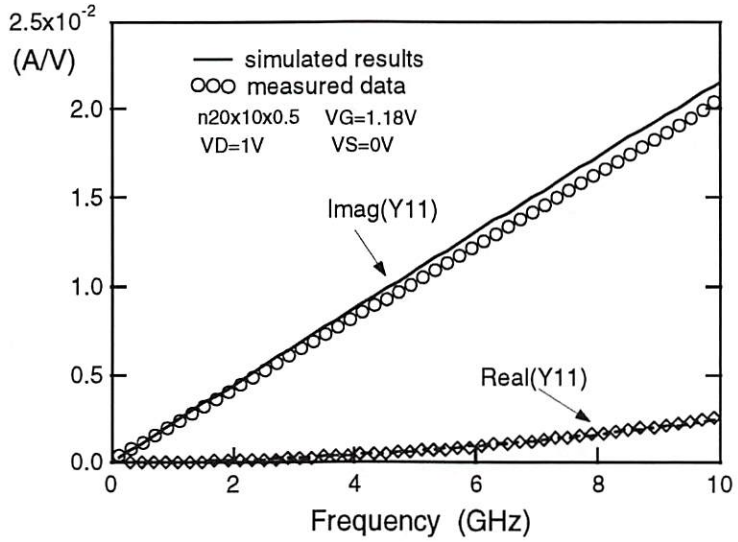


(c)

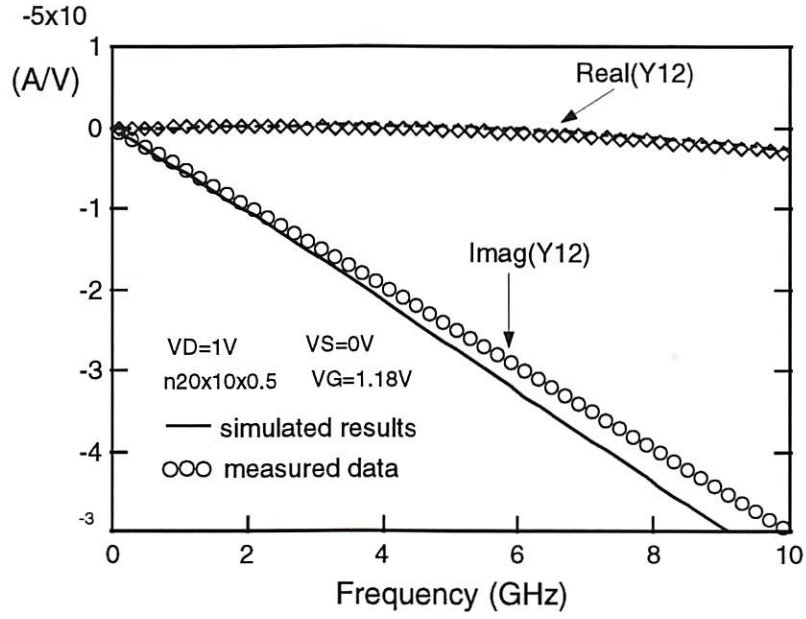


(d)

Figure B.15 (continued)

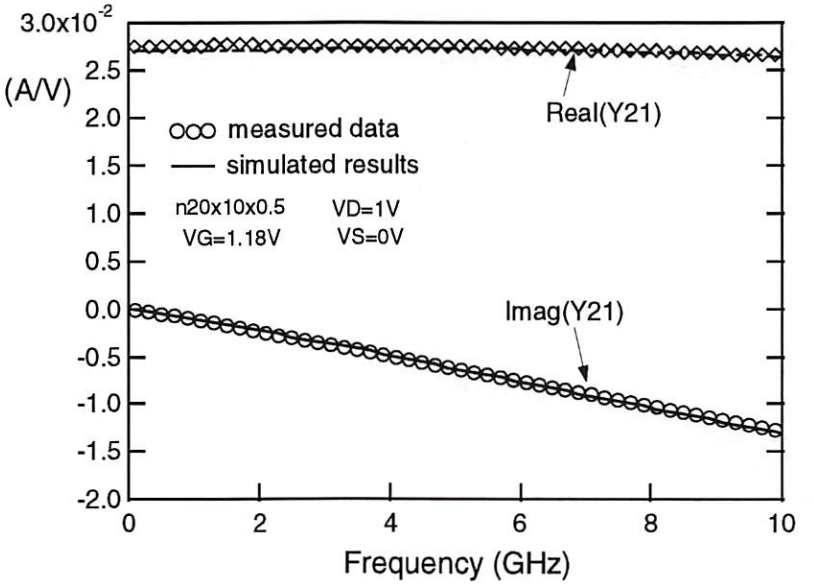


(a)

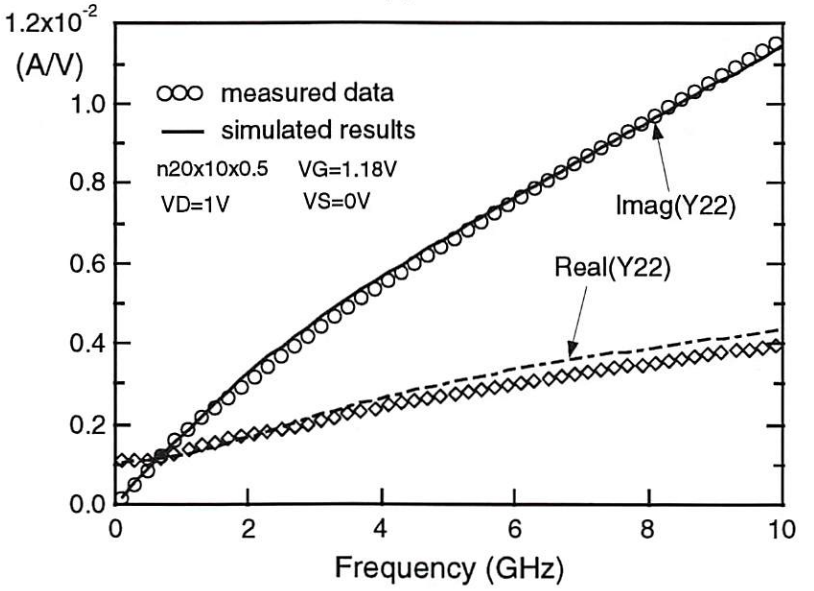


(b)

Figure B.16: Plots of Y-parameters of a 20-finger NMOS transistor with $W_g = 10\ \mu m, L_g = 0.5\ \mu m$ per finger at $V_{DS} = 1\ V$ and $V_{GS} = 0.8, 1.2\ V$. (a) Y_{11}. (b) Y_{12}. (c) Y_{21}. (d) Y_{22}. SPICE simulation results are obtained with S-CMOS intrinsic model.



(c)



(d)

Figure B.16 (continued)

Reference List

[1] A. Abidi, A. Rofougaran, G. Chang, J. Rael, "The future of CMOS wireless transceivers," *IEEE ISSCC Digest*, pp. 118-119, Feb. 1997.

[2] J. Rudell, J. Ou, T. Cho, G. Chien, F. Brianti, J. Weldon, P. Gray, "A 1.9 GHz wide-band IF double conversion CMOS integrated receiver for cordless telephone applications," *IEEE ISSCC Digest*, pp. 304-305, Feb. 1997.

[3] R. Vanoppen, J. Geelen, D. Klaassen, "The high-frequency analogue performance of MOSFETs," *IEEE IEDM 1994*, pp. 173-176, 1994.

[4] G. Dambrine, A. Cappy, F. Heliodore, E. Playez, "A new method for determining the Fet small-signal equivalent circuit," *IEEE Trans. on Microwave Theory and Techniques*, vol. 36, no. 7, pp. 1151-1159, July 1988.

[5] M. Berroth, R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit," *IEEE Trans. on Microwave Theory and Techniques*, vol. 38, no. 7, pp. 891-895, July 1990.

[6] D. Lovelace, J. Costa, N. Camilleri, "Extracting small-signal model parameters of silicon MOSFET transistors," *IEEE MTT-S Digest*, pp. 865-868, Apr. 1994.

[7] S. Lee, H. Yu, C. Kim, J. Koo, K. Nam, "A novel approach to extracting small-signal model parameters of silicon MOSFET's," *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 3, pp. 75-77, Mar. 1997.

[8] W. Liu, R. Gharpurey, M. C. Chang, U. Erdogan, R. Aggarwal, J. P. Mattia, "R.F. MOSFET modeling accounting for distributed substrate and channel resistances with emphasis on the BSIM3v3 SPICE model," *IEEE IEDM Digest*, pp. 309-312, Dec. 1997.

[9] *BSIM3v3 Manual*, Dept. of Electrical Engineering and Computer Sciences University of California, Berkeley, 1995-1997.

[10] *Star-HSPICE User's Manual*, Avant! Corporation, Sunnyvale, CA, Feb. 1996.

[11] M. Bagheri, Y. Tsividis, "A small signal dc-to-high-frequency nonquasistatic model for the four-terminal MOSFET valid in all regions of operation," *IEEE Trans. Electron Devices*, vol. ED-32, no. 11, pp. 2383-2391, Nov. 1985.

[12] *Eldo Device Equations Manual*, Mentor Graphics Corporation, Wilsonville, Oregon, June 1997.

[13] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw-Hill: New York, NY, 1987.

[14] M. Koolen, J. Geelen, M. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," *IEEE Bipolar Circuits and Technology Meeting*, pp. 188-191, 1991.

[15] P. Klein, "A compact-charge LDD-MOSFET model," *IEEE Trans. on Electron Devices*, vol. 44, no. 9, pp. 1483-1490, Sept. 1997.

Appendix C

High-Frequency MOS Transistor S-Parameter Measurement and PAD De-embedding

In order to characterize the AC small-signal behavior of transistors at high frequency, usually a set of two-port S-parameter is measured using a scalar network analyzer. The possibility of on-wafer measurement up to 50 GHz is supported by HP-8510 network analyzer.

When performing high-frequency measurement on wafers, two correction procedures have to be applied. First, the measurement system has to be calibrated by defining a reference plane for the S-parameter measurement at the probe tips using a standard calibration technique [1]. Secondly the on-wafer parasitics have to be characterized so that the actual transistor two-port parameters can be obtained.

C.1 Test Equipment and Testing Structure

Measurement of high-frequency characteristics of MOS transistors requires a shielded probe station for the testing fixture to shield out the light, a pair of high-frequency two-port measurement probe tips (standard GSG probes are used in this work), HP-4145B (or HP-4142 for larger current compliance) for DC biasing, and HP-8510 network analyzer for S-parameter measurement.

The layout of the device test patterns are shown in Fig. C.1. Here, besides the pattern for device under test (DUT), the additional patterns for "open" and "short" are measured in order to collect enough information for pads and interconnection lines de-embedding.

C.2 Testing Procedure

The whole measurement can be controlled by a computer using HP-ICCAP [2] software though the GP-IB interface. The measurement configuration of HP-8510 network analyzer has to be carefully selected. Table. C.1 lists an example of the input controlling parameters of the network analyzer for MOS transistor at radio frequency. Before starting the measurement, the system has to be calibrated. A standard complete two-port S-parameter measurement calibration procedure including open, short, through, and 50 Ω load are performed to set up the reference plane from the probe tips to the network analyzer. Notice that accurately performing the calibration is very important for high-frequency measurement. The noise level of S-parameters from the calibration result should be within 0.01 dB.

The testing procedure includes measurement of the DUT, and measurement of the open and short test patterns under the same operation frequencies as the DUT measurement. Different from the DC measurement, the high-frequency S-parameter measurement is very sensitive in the measurement environment. There several things have to be carefully controlled:

- During the calibration steps and measurement steps, the "power flatness" has to be turned on in order to have the network analyzer self-calibrate the power level at the interconnection of the cables and network analyzer.

- The contact between probe tips and the pads has to be maintained in the same strength level for calibration of network analyzer, measuring open and short patterns, and measuring the DUTs.
- Probe cables of the network analyzer should not be touched once the test fixture has been set up.

C.3 Complete Two-Step PAD De-embedding

A suitable equivalent circuit of a transistor with the testing pattern is shown in Fig. C.2. It shows the actual DUT as a two-port transistor embedded in parasitics of the interconnection lines and bonding pads. Here, the "π" network with Y_1, Y_2, and Y_3 is contributed by the bonding pads. Y_1 and Y_2 are the equivalent RC network from the pads to substrate, whereas Y_3 is the substrate coupling between input and putout pads. The "T" network with Z_1, Z_2, and Z_3 is the equivalent RL effects of the interconnection lines. In the measurement of "open" pattern as shown in Fig. C.1(b), the equivalent effects of Y_1, Y_2, and Y_3 are measured. In the measurement of the "short" pattern, the equivalent effects of Z_1, Z_2, and Z_3 are obtained. Thus,

$$Y_{open} = \begin{pmatrix} Y_1 + Y_3 & Y_3 \\ Y_3 & (Y_2 + Y_3) \end{pmatrix} , \tag{C.1}$$

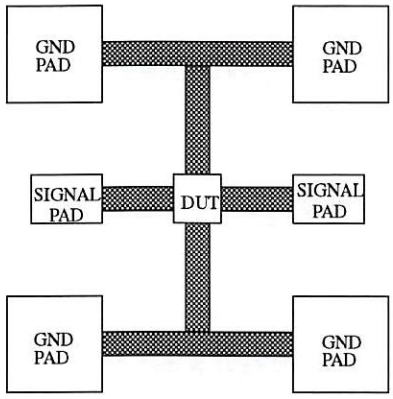
$$\begin{aligned} Z_{short} &= \begin{pmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & (Z_2 + Z_3) \end{pmatrix} \\ &= ZtoY(Y_{short} - Y_{open}) \ . \end{aligned} \tag{C.2}$$

The Y-parameters of DUT can be obtained from,

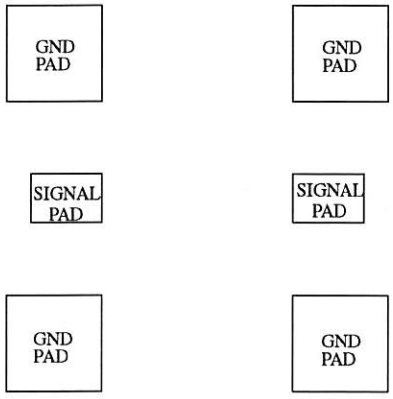
$$Y_{DUT} = ZtoY(YtoZ(Y_{meas} - Y_{open}) - Z_{short}), \tag{C.3}$$

where Y_{meas} is the measured Y-parameter matrix of the transistor together with parasitics and Y_{DUT} is the actual transistor Y-parameter matrix. The function $ZtoY$ performs the transform from Z-parameter to Y-parameter, and $YtoZ$ performs the transform from Y-parameter to Z-parameter.

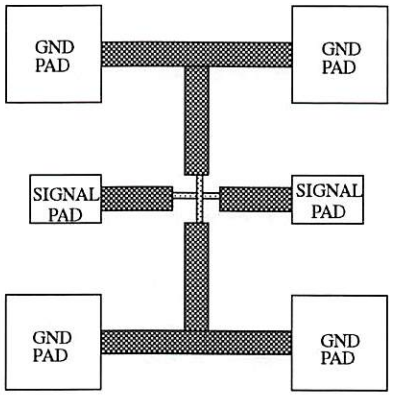
The de-embedding results of an NMOS transistor test pattern are shown in Fig. C.3. The measured Y-parameters from the test pattern have inductive and capacitive parasitics which are easily shown from the high-frequency characteristics of Y_{meas}. The dash lines are the Y_{DUT} after completing 2-step de-embedding of the measured data. The parasitic RC effect of the I/O pad are de-embedded, especially for Y_{11} and Y_{22}. In addition, the RL effects which have significant effects on Y_{12} and Y_{21} are de-embedded.



(a)



(b)

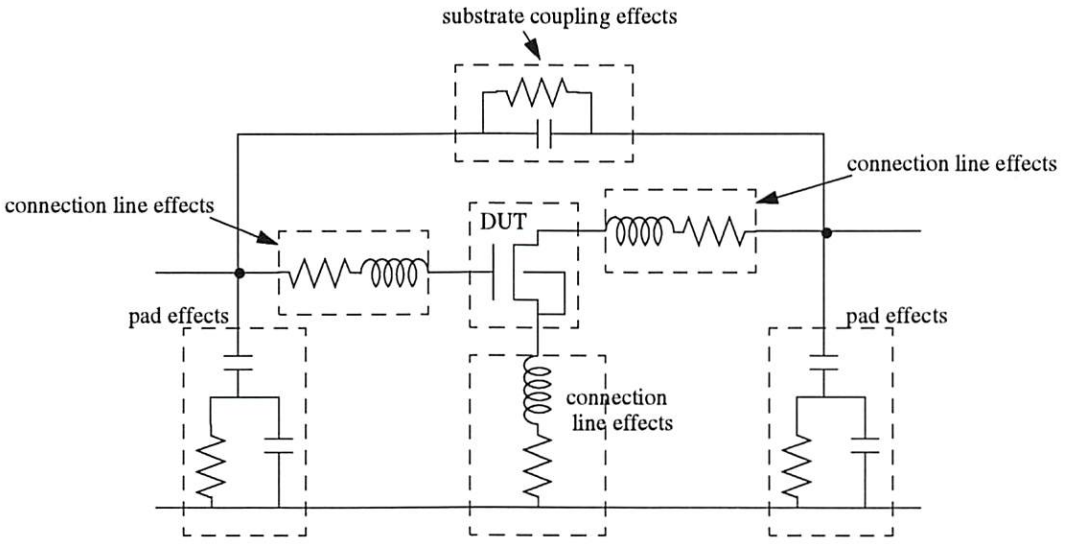


(c)

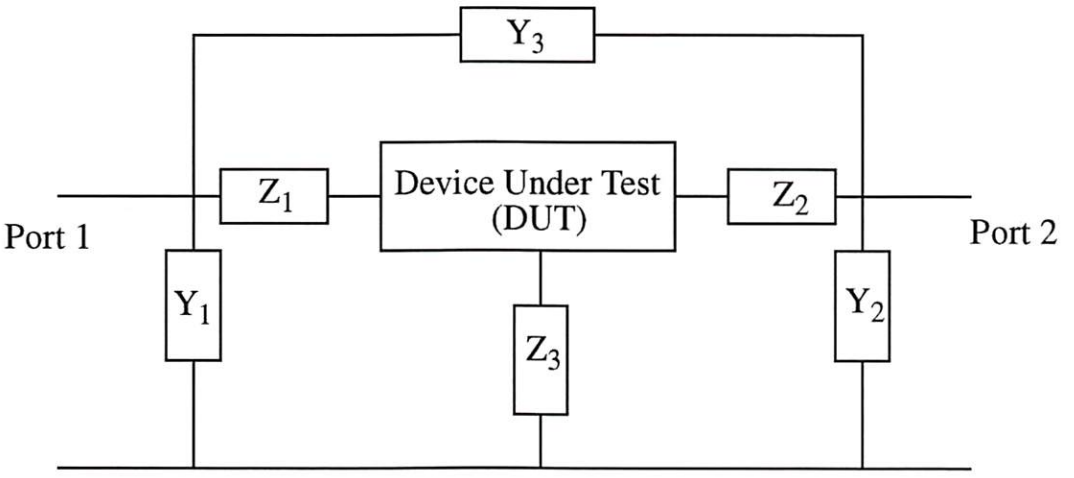
Figure C.1: Test patterns of the MOS transistor at radio-frequency and the parasitic calibration. (a) Test pattern of the device. (b) Test pattern of open pad. (c) Test pattern of short pad.

Table C.1: An example of the input controlling variables of HP-8510 network analyzer for MOS transistor S-parameter measurement.

HP8510 instrument options	controlling variable
Use User Sweep	No (Yes for spot frequency)
Hold Time	0
Delay Time	100m
Port1 Atten	20 dBm
Port2 Atten	20 dBm
Source Power	-10 dBm
Power Slope	0.1
Fast Sweep (RAMP)	No
Sweep Time [0.05-100]	166m
Use Fast CW	Yes (No for spot frequency)
Trim Sweep	0
Avg Factor [1-4096]	100
Cal Type [SHN]	H
Cal Set No. [1..8]	1
Soft Cal Sequency	LOST
Delay for Timeouts	0
Use Linear List	No
Pulse Mode	No
Trigger Delay	300n
Init Command	

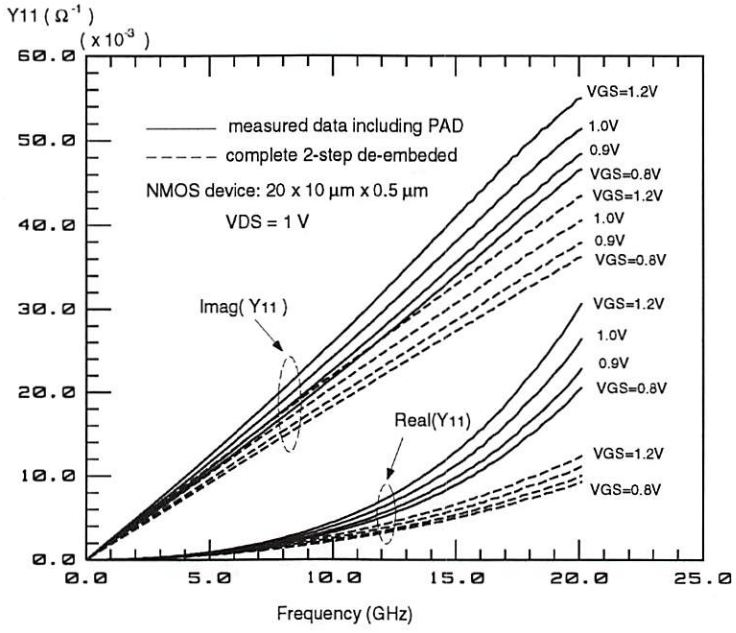


(a)

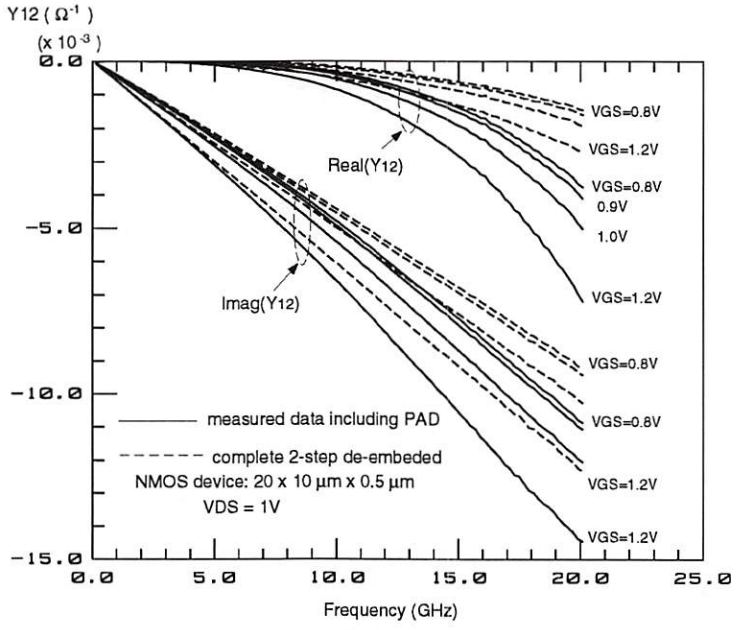


(b)

Figure C.2: An equivalent circuit of an MOS transistor at radio-frequency. (a) The detailed equivalent effects. (b) The equivalent circuit of the T and π networks.

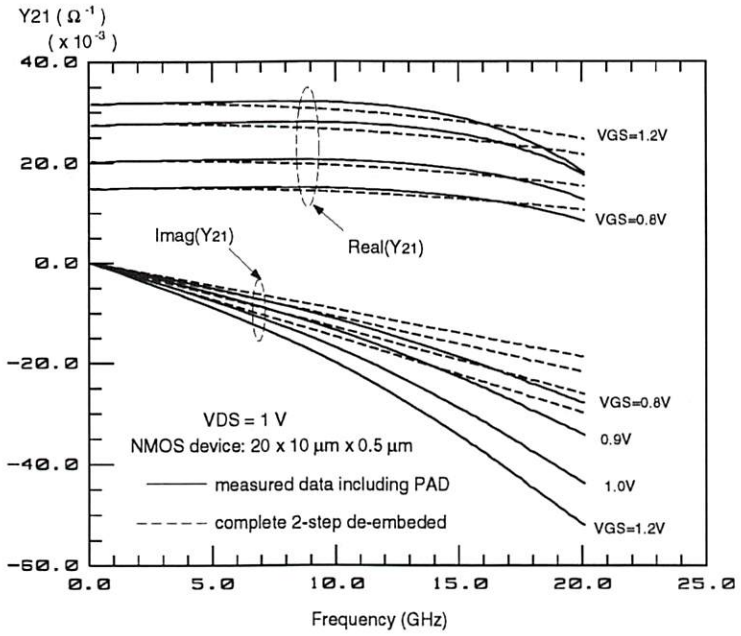


(a)

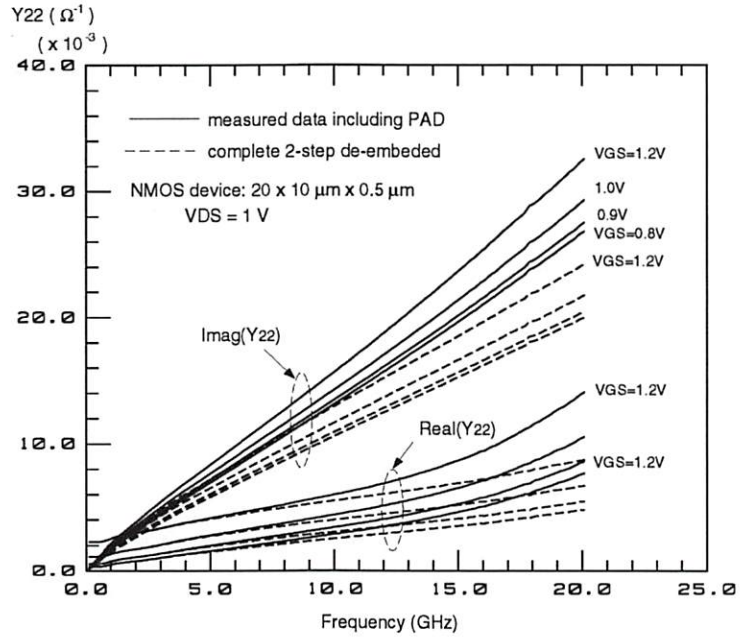


(b)

Figure C.3: Plots of Y-parameters of a 20-finger NMOS transistor with $W_g = 10\ \mu m, L_g = 0.5\ \mu m$ per finger at $V_{DS} = 1\ V$ and $V_{GS} = 0.8, 0.9, 1.0, 1.2\ V$ for both the measured data and de-embedded data. (a) Y_{11}. (b) Y_{12}. (c) Y_{21}. (d) Y_{22}.



(c)



(d)

Figure C.3 (continued).

Reference List

[1] *HP-8510 Network Analyzer User's Manual*, Hewlett Packard Company, Santa Clara, CA.

[2] *IC-CAP User's Manual*, Hewlett Packard Company, Santa Clara, CA, 1996.

Appendix D

S-CMOS Model Parameter Extraction Programs

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        Copyright  Steve H. Jen, Bing J. Sheu, 1998
%        Assisted by Alex Y. Park
%        file name: ext_dc
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
            clear all;
            clear global;
%%% define global parameters %%%
            glo_par;
            Wwid = 25e-6;
            Wnrw = 9e-7;
            Llng = 25e-6;
            Lsht = 5e-7;
%%% define matlab path %%%
            matlab_path=path;
            path('c:\user\steve\project\model\meas\c05\dcmos\n25x25',path);
%%% load VDSAT-VG data for large device: extract VFB, GAMMA1, PHIS %%%
            vp_vg;
            param;
            par_rult;
            W = 25e-6;
            L = 25e-6;
            VD = VD_m;
            VG = VG_m;
            VS = VS_m;
            VB = VB_m;
            init_vp;            % initial plot for VDSAT vs. VG %
                   param_dc=[VFB GAMMA1];
                   param_dc(1)=-0.4;
                   param_dc(2)=0.8;
            disp('initial values');
            fprintf('VFB = %6.5e, GAMMA1 = %6.5e\n\n',param_dc(1), param_dc(2));
            param_dc = fmins('err_vsat',param_dc);  % extraction VFB and GAMMA1
```

```
                VFB=param_dc(1);
                GAMMA1=param_dc(2);
                PHIS = vto -VFB;
          disp('final values');
          fprintf('VFB=%6.5e, GAMMA1=%6.5e, PHIS=%6.5e, ERROR=%6.5e\n\n',
                    param_dc(1), param_dc(2), PHIS, ERROR);
%%% extract substrate-bias effects on Vth:  KS GAMMA1 GAMMA2 %%%
          cleariv;
          clear param_dc;
%%% load the data of IDS-VGS %%%
          id_vg_gm;
          VD=VD_m;
          VG=VG_m;
          VS=VS_m;
          VB=VB_m;
          IDS_M=ID_m;
          gm_M=gm_m;
%%% set number of substrate bias points %%%
     % 4 different VBS bias conditions
          indexbs=4;
%%% calculate the delta_Vth and Vth from measured data %%%
          delta_vth=cal_dvt(VG,IDS_M,indexbs);
          Vth_M = vto + delta_vth;
          k=size(VB) ;
          m=k(1)/indexbs;
          for i=1:indexbs
               cal_VBS(i)=VB(2 + (i-1)*m);
          end
%%% extracting KS GAMMA1 %%%
          init_vt1;
                param_dc=[KS GAMMA1];
                param_dc(1)=0.9;
                param_dc(2)=0.8;
          disp('initial values');
          fprintf('KS = %6.5e\n\n',param_dc(1));
          param_dc = fmins('err_dvt',param_dc); % extraction VFB and GAMMA1
                KS=param_dc(1);
          disp('final values');
          fprintf('KS=%6.5e, GAMMA1=%6.5e, ERROR=%6.5e\n\n',param_dc(1),
                    param_dc(2),ERROR);
%%% extracing mu0, UGSZ, UBS from IDS - VGS %%%
          IDS_M = ID_m;
          init_dc1;
          clear param_dc;
                    param_dc = [mu0 UGSZ UBS];
                    param_dc(1) = 600e-4;
                    param_dc(2) = 0.25;
```

```
                    param_dc(3) = 0.02;
            disp('initial values');
    fprintf('mu0=%6.5e, UGSZ=%6.5e, UBS=%6.5e\n\n',param_dc(1), param_dc(2),
                    param_dc(3));
            param_dc = fmins('err_id1',param_dc);
            disp('final values');
    fprintf('mu0=%6.5e, UGSZ=%6.5e, UBS=%6.5e, ERROR=%6.5e\n\n',param_dc(1),
                    param_dc(2), param_dc(3),ERROR);
                    mu0=param_dc(1);
                    UGSZ=param_dc(2);
                    UBS=param_dc(3);
%%% extract subthreshold current parameters: N, KSUB %%%%
            init_dc2;
            clear param_dc;
                    param_dc = [KSUB N];
                    param_dc(1) = 1;
                    param_dc(2) = 1;
            disp('initial values');
    fprintf('KSUB=%6.5e, N=%6.5e\n\n',param_dc(1), param_dc(2));
            param_dc = fmins('err_id2',param_dc);
            disp('final values');
    fprintf('KSUB=%6.5e, N=%6.5e, ERROR=%6.5e\n\n',param_dc(1), param_dc(2),
                    ERROR);
            KSUB=param_dc(1);
            N=param_dc(2);
%%%  extracting KDSAh ECRIT UDS
            cleariv;
            clear param_dc;
            id_vd_gd;
            VD = VD_m;
            VG = VG_m;
            VS = VS_m;
            VB = VB_m;
            IDS_M = ID_m;
            gds_M = gd_m;
            W = 25e-6;
            L = 25e-6;
            init_dcp;
                    param_dc = [ECRIT UDS];
                    param_dc(1) = 10 * 10^6;
                    param_dc(2) = 0.035;
            disp('initial values');
            fprintf('ECRIT=%6.5e, UDS=%6.5e\n\n',param_dc(1), param_dc(2));
            param_dc = fmins('err_id',param_dc);
            disp('final values');
            fprintf('ECRIT=%6.5e, UDS=%6.5e, ERROR=%6.5e\n\n',param_dc(1),
                    param_dc(2), ERROR);
```

```
            ECRIT=param_dc(1);
            UDS=param_dc(2);
%%% extract narrow channel effects %%%
             %%% define matlab path %%%
            matlab_path=path;
            path('c:\user\steve\project\model\meas\c05\dcmos\n0p9x15',path);
            W = 9e-7;
            L = 15e-6;
            cleariv;
            clear param_dc;
            vp_vg;
            vto=cal_vto(VG_m,VS_m);
                 %mode=2;
                        cal_VDS = cal_VBS;
%%% load the data of IDS-VGS %%%
            id_vg_gm;
            VD=VD_m;
            VG=VG_m;
            VS=VS_m;
            VB=VB_m;
            IDS_M=ID_m;
            gm_M=gm_m;
%%% get number of substrate bias points %%%
            indexbs=4;          % 4 different VBS bias conditions
%%% calculate the delta_Vth and Vth from measured data %%%
            delta_vth=cal_dvt(VG_m,IDS_M,indexbs);
            Vth_M = vto + delta_vth;
%%% extracting GAMMA1L KNZ KNB %%%
            init_vt2;
                        param_dc=[KNB];
                        param_dc(1)=0;
            disp('initial values');
            fprintf('KNZ=%6.5e, KNB=%6.5e\n\n',KNZ,param_dc(1));
            param_dc = fmins('err_vtw',param_dc);   % extraction KNZ, KNB
                        KNB=param_dc(1);
            disp('final values');
            fprintf('KNZ=%6.5e, KNB=%6.5e, ERROR=%6.5e\n\n', KNZ,param_dc(1),
                        ERROR);
%%% extract short channel effects for Vth%%%%%%%%%%%%%%%%%%
            %%% define matlab path %%%
            matlab_path=path;
            path('c:\user\steve\project\model\meas\c05\dcmos\n25x0p5',path);
            W = 25e-6;
            L = 5e-7;
            cleariv;
            clear param_dc;
            vp_vg;
```

```
            vto=cal_vto(VG_m,VS_m);
                        %mode=3;
                        cal_VDS = cal_VBS;
%%% load the data of IDS-VGS %%%
            id_vg_gm;
            VD=VD_m;
            VG=VG_m;
            VS=VS_m;
            VB=VB_m;
            IDS_M=ID_m;
            gm_M=gm_m;
%%% set number of substrate bias points %%%
            indexbs=4;          % 4 different VBS bias conditions
%%% calculate the delta_Vth and Vth from measured data %%%
            delta_vth=cal_dvt(VG_m,IDS_M,indexbs);
            Vth_M = vto + delta_vth;
%%% extracting GAMMA1L KNZ KNB %%%
            init_vt3;
                        param_dc=[GAMMA1L];
                        param_dc(1)=0;
            disp('initial values');
            fprintf('ETA1=%6.5e, GAMMA1L=%6.5e\n\n',ETA1,param_dc(1));
            param_dc = fmins('err_vtl',param_dc); % extraction ETA1, GAMMA1L
                        GAMMA1L=param_dc(1);
            disp('final values');
            fprintf('ETA1=%6.5e, GAMMA1L=%6.5e, ERROR=%6.5e\n\n', ETA1,
                        param_dc(1),ERROR);
%%% extracting UGSL, UGSL2: using short-channel IDS-VGS %%%%
            init_dc3;
            clear param_dc;
                        param_dc = [UGSL UGSL2];
                        param_dc(1) = 1.5e-7;
                        param_dc(2) = 1e-8;
            disp('initial values');
            fprintf('UGSL=%6.5e,UGSL2=%6.5e\n\n',param_dc(1), param_dc(2));
            param_dc = fmins('err_id3',param_dc);
            disp('final values');
            fprintf('UGSL=%6.5e, UGSL2=%6.5e, ERROR=%6.5e\n\n',param_dc(1),
                        param_dc(2),ERROR);
            UGSL=param_dc(1);
            UGSL2=param_dc(2);
%%%  extracting ETAZ ECRIT
            cleariv;
            clear param_dc;
            id_vd_gd;
            VD = VD_m;
            VG = VG_m;
```

```
            VS = VS_m;
            VB = VB_m;
            IDS_M = ID_m;
            gds_M = gd_m;
            init_dc4;
                        param_dc = [ECRIT ETAZ];
                        param_dc(1) = 10e6;
                        param_dc(2) = 2e-8;
            disp('initial values');
            fprintf('ECRIT=%6.5e, ETAZ=%6.5e\n\n',param_dc(1), param_dc(2));
            param_dc = fmins('err_id4',param_dc);
            disp('final values');
            fprintf('ECRIT=%6.5e, ETAZ=%6.5e, ERROR=%6.5e\n\n',param_dc(1),
                        param_dc(2),ERROR);
            ECRIT=param_dc(1);
            ETAZ=param_dc(2);
%%%% extracting LAMBDAD, LAMBDAG
            clear param_dc;
            init_dc5;
                        param_dc = [LAMBDAD LAMBDAG ECRIT];
                        param_dc(1) = 1e-7;
                        param_dc(2) = 1;
                        param_dc(3) = ECRIT;
            disp('initial values');
            fprintf('LAMBDAD=%6.5e, LAMBDAG=%6.5e, ECRIT=%6.5e\n\n',param_dc(1),
                        param_dc(2),param_dc(3));
            param_dc = fmins('err_id5',param_dc);
            disp('final values');
            fprintf('LAMBDAD=%6.5e, LAMBDAG=%6.5e, ECRIT=%6.5e, ERROR=%6.5e\n\n',
                        param_dc(1), param_dc(2),param_dc(3),ERROR);
            LAMBDAD=param_dc(1);
            LAMBDAG=param_dc(2);
            ECRIT = param_dc(3);


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        file name: glo_par.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% global parameters
            %model parameters
global Tox VFB PHIS mu0 GAMMA1 GAMMA2 KS ETA1 ETA2 ETA3 ETAZ KNZ KNB
global UGSL UDS UBS PHID LAMBDAG LAMBDAB LAMBDABS LAMBDAD KSIG
global KBSh KDSATh KGFh ECRIT DL DW N KSUB Vt Cox UGSZ
            %controlling & expression parameters
global Weff Leff W L Llng Lsht Wwid Wnrw GAMMA1L UGSL2 UBS2 UDSL
global VDS VGS VBS VD VG VS VB IDS_S gds_S gm_S IDS_M gds_M gm_M
global VFS VGFh VBST VBSh Vth Vto VGSth ALPHAX VDSAT VDSATh
```

```
global Mr mueff fL fs fc ALPHA BETA F vto
            %global VD_m VG_m VS_m VB_m
global plotHandle1 plotHandle2 plotHandle3 plotHandle4 plotHandle5
global plotHandle6 plotHandle7 plotHandle8 plotHandle9 ERROR
global indexbs delta_vth cal_VBS cal_VDS mode Vth_S Vth_M


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: cleariv.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% clear all the setting of I, V
            clear VDS VGS VBS;
            global VDS VGS VBS;
            clear VD VG VS VB;
            global VD VG VS VB;
            clear VD_m VG_m VS_m VB_m;
            global VD_m VG_m VS_m VB_m;
            clear ID_m gd_m gm_m;
            global ID_m gd_m gm_m;
            clear IDS_M IDS_S gds_M gds_S;
            global IDS_M IDS_S gds_M gds_S;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: param.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% parameter set
Tox=9e-9;       %gate oxide thickness (m)
VFB=-0.4;        %flat-band voltage (volt)
PHIS=0.85;         %surface inversion potential (volt)
mu0=450e-4;       %intrinsic surface mobility (m^2/volt/sec)
GAMMA1= 0.8;      %zero-bias boly-effect coefficient (volt^0.5)
GAMMA1L=0;
GAMMA2= 0.328;       %high-bias body-effect coefficient (volt^0.5)
KS=2.7e-4;      %depletion charge-sharing coefficient
ETA1= 0;         %short-channel effect coefficient (m*volt)
ETA2= 0;       %reverse short-channel effect coefficient (m*volt)
ETA3= 1e-6;      %exponential reverse short-channel effect coefficient (m)
ETAZ= 0;        %drain-induced barrier lowering coefficient
KNZ=0.244e-6;     %narrow-width threshold voltage coefficient (m*volt)
KNB=5.4e-9;      %narrow-width threshold voltgae substrate coefficient (m)
UGSZ= 0.25;       %gate-voltage mobility degradation coefficient (volt^-1)
UGSL= 0.06e-6;      %short-channel adjustment of UGSZ (m/volt)
UGSL2= 0;
UDS=0.035;       %drain voltage mobility degradation coefficient (volt^-1)
UDSL= 0;
UBS=0.02; %substrate-voltage mobility degradation coefficient (volt^-0.5)
```

```
PHID=0.05; %drain-voltage related channel-length modulation effect potential (volt)
LAMBDAG= 0.5;   %gate-voltgae dependent CLME coefficient (volt^1.5)
LAMBDAB= 2;       %substrate-voltage shifting CLME coefficient
LAMBDABS= 1;      %substrate-voltage dependent CLME coefficient (volt)
LAMBDAD= 0;        %drain-voltage dependent CLME coefficient (volt)
KSIG=0.02;      %sigmoid function coefficient (volt^2)
KBSh=1.01;         %substrate-bias hyperbola function coefficient
KDSATh=1.01;       %strong-inversion hyperbola function coefficient
KGFh= 1.01;       %gate to flat-band hyperbola function coefficient
ECRIT=20e6;         %critical electric field for velocity saturation (volt/m)
DL=0;          %channel-length reduction (m)
DW=0;         %channel-width reduction (m)
N=1.5;         %subthreshold drain current slope
KSUB=0.1;          %subthreshold current shifting coefficient


Vt =0.026;            %thermal voltage (volt)
Cox=3.5e-11 / Tox;          %gate oxide capacitance (farad/m^2)


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: cal_vto.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function calc_vto=calc_vto(VG_m,VS_m)
            glo_par;
            k=size(VG_m);
            for i=1:(k-1)
                      if (VS_m(i)*VS_m(i+1)) <= 0
                            index=i;
                      end
            end
            calc_vto = VG_m(index+1) - (VG_m(index+1) - VG_m(index))
                     * VS_m(index+1) / (VS_m(index+1) - VS_m(index));
return;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: cal_dvt.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function cal_dvt=cal_dvt(VG, IDS_M, indexbs)
            glo_par;
            VG = VG;
            IDS_M = IDS_M;
            k=size(VG);
            indexbs = indexbs;
            m=k(1)/indexbs;
            for ind1=1:indexbs
```

```
                index1=0;
                index2=0;
                for ind2=1:(m-1)
                      jj = ind2+(ind1-1)*m;
                      if index1==0;
                           if ((VG(jj)) >= (vto+0.3+(ind1-1)*0.1))
                                 index1=ind2;
                           end
                      end
                      if index2==0;
                           if (VG(jj) >= (vto+0.7+(ind1-1)*0.1))
                                  index2=ind2;
                           end
                      end
                   end
             cal_dvt_vth(ind1)=VG(index2+(ind1-1)*m) - (VG(index2+(ind1-1)*m)
                    - VG(index1+(ind1-1)*m)) * IDS_M(index2+(ind1-1)*m)
                    / (IDS_M(index2+(ind1-1)*m) - IDS_M(index1+(ind1-1)*m));
             end
             for i=1:(indexbs)
                         cal_dvt(i)=cal_dvt_vth(i) - cal_dvt_vth(1);
             end
return;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: cal_vth.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
        Weff = W - DW;
        Leff = L - DL;
%%%%%%%% mode = 1 : calculate substrate bias effects %%%%%
        if mode==1
                    Vto = vto;
        end
%%%%%% mode = 2: calculate short-channel narrow-channel effects
        if mode == 2
          KNZ = (vto - VFB - PHIS) / ( 1 / Weff - 1/Wwid);
          Vto = VFB + PHIS + KNZ*(1 / Weff - 1/Wwid) + KNB* (1/ Weff - 1/Wwid)
              * cal_VBS - ETAZ * cal_VDS - ETA1*(1 / Leff - 1/Llng) + ETA2
              *(1/ Leff - 1/Llng)* (1 - exp(- Leff / ETA3));
         end
%%%%%% mode = 3: calculate short-channel effects
        if mode == 3
           ETA1 = - (vto - VFB - PHIS) / ( 1 / Leff - 1/Llng);
           Vto = VFB + PHIS + KNZ*(1 / Weff - 1/Wwid) + KNB* (1/ Weff - 1/Wwid)
                 * cal_VBS - ETAZ * cal_VDS - ETA1*(1 / Leff - 1/Llng)
                 + ETA2 *(1/ Leff - 1/Llng) * (1 - exp(- Leff / ETA3));
```

```
        end
cvth = Vto + (GAMMA1-GAMMA1L*(1/Leff-1/ Llng))*(sqrt(PHIS-cal_VBS)-sqrt(PHIS))
      + KS * (sqrt(PHIS - cal_VBS) - sqrt(PHIS)).^2 + GAMMA2
      * (sqrt(PHIS - cal_VBS) - sqrt(PHIS - cal_VBS));


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: jen_equ.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Weff=W - DW;
Leff=L - DL;
VDS = VD - VS;
VGS = VG - VS;
VBS = VB - VS;
VFS = VFB + VBS;
T_GFh = VGS + KGFh * VFS;
VGFh = 0.5 * (T_GFh + sqrt(T_GFh.^2 - 4 * VGS .* VFS));
VBST = PHIS - ((GAMMA1 - GAMMA2)/KS + sqrt(PHIS))^2;
T_BSh = VBS + KBSh * VBST;
VBSh = 0.5 * ( T_BSh + sqrt(T_BSh.^2 - 4 * VBS .* VBST));
Vto = VFB + PHIS + KNZ *(1 / Weff - 1/ Wwid) + KNB* (1/ Weff - 1/Wwid)* VBS
     - ETAZ * VDS * (1/Leff - 1/Llng) - ETA1 *(1/ Leff - 1/ Llng)+ ETA2
     * (1/ Leff - 1/Llng)*(1 - exp(- Leff / ETA3));
Vth = Vto+(GAMMA1-GAMMA1L*(1/Leff-1/Llng))*(sqrt(PHIS-VBSh)-sqrt(PHIS))
     + KS*(sqrt(PHIS-VBSh)-sqrt(PHIS)).^2+GAMMA2*(sqrt(PHIS-VBS)-sqrt(PHIS-VBSh));
VGSth = 2 * N * Vt * log(1 + exp((VGS - Vth) / (2 * N * Vt)));
ALPHAX = (1 - GAMMA1 / 2 * (sqrt(VGSth + Vth - VFS + GAMMA1^2 / 4)).^(-1)).^(-1);
g=1-1/(1.744+0.8364*(PHIS-VBS));
a=1+g*GAMMA1/2*(sqrt(PHIS-VBS)).^(-1);
Vc=VGSth.* a.^(-1)/ECRIT *(1/Leff - 1/Llng);
K=(1+Vc+sqrt(1+2*Vc))/2;
VDSAT=(VGSth).* ALPHAX.^(-1);
KDSATh1 = KDSATh * (1 + 1e-8 / (Leff));
T_DSATh = VDS + KDSATh1 * VDSAT;
VDSATh = 0.5 * (T_DSATh - sqrt(T_DSATh.^2 - 4 * VDS.*VDSAT));
fc = 0.5 * (1 + (VGS - Vth) .* (sqrt((VGS - Vth).^2 + KSIG)).^(-1));
fs = 1 - fc;
Mr=(1+(UGSZ+UGSL*(1/Leff-1/Llng) )*VGSth+UGSL2*(1/Leff-1/Llng)*(VGSth.^2)
    -UBS*(sqrt(PHIS-VBSh)-sqrt(PHIS))+(UDS-UDSL*(1/Leff-1/Llng))*VDSATh)
    .*(1 +VDSATh/ECRIT*(1/Leff-1/Llng));
mueff=mu0*Mr.^(-1);
fL=LAMBDAD*(1/Leff)*(sqrt(PHID+VDS-VDSATh)-sqrt(PHID)).*(1-VBS/LAMBDABS)
    .*((VGSth).^(3/2) +LAMBDAG).^(-1)/LAMBDAB;
BETA = Weff / Leff * Cox * mueff;
ALPHA = ( 1 - fs.* exp(- VDS ./ Vt)).*(1 + fc.*fL + fs .* KSUB);
F = VGSth.*VDSATh - ALPHAX / 2 .* VDSATh.^2;
IDS_S = ALPHA.*BETA.*F;
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: init_vp.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%% initial plot%%%%
        VDSAT = VS;
        figure;
        plotHandle1=plot(VG,VDSAT, 'b*', VG, VDSAT, 'r--', 'EraseMode', 'Xor');
        %grid on;
        %axis([0,4,-Inf,Inf]);
        xlabel('VG (V)');
        ylabel('VDSAT (V)');
        title('extracting VFB GAMMA1 .....');
        drawnow;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: err_vsat.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function err_vsat=err_vsat(param_dc)
       glo_par;
       VFB = param_dc(1);
       GAMMA1 = param_dc(2);
       alphax=(1 - (GAMMA1 / 2)  ./ sqrt(VG - VFB - VB + GAMMA1^2 / 4) ).^(-1);
       vto=cal_vto(VG,VS);
       VDSAT_s=(VG - vto) ./ alphax;
       err_vsat=sum((VS - VDSAT_s).^2);
       ERROR=err_vsat;
       set(plotHandle1(2), 'Ydata', VDSAT_s);
       drawnow;
return;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: init_vt1.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%% initial plot %%%%
       figure;
       plotHandle3=plot(cal_VBS,Vth_M,'b',cal_VBS,Vth_M,'r','EraseMode','Xor');
       xlabel('VBS (V)');
       ylabel('Vth (V)');
       title('extracting KS and GAMMA2......');
       drawnow;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: err_dvt.m
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function err=err_dvt(param_dc)
        glo_par;
        KS = param_dc(1);
        GAMMA1 = param_dc(2);
        mode=1;
        cal_vth;
        Vth_S = cvth;
        err=sum((Vth_M - Vth_S).^2);
        k=size(Vth_M);
        ERROR=sqrt(sum((Vth_M - Vth_S).^2 ./ Vth_M.^2) / k(1));
        set(plotHandle3(2), 'Ydata', Vth_S);
        drawnow;
return;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: init_dc1.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% initial plot
        VDS = VD - VS;
        VGS = VG - VS;
        VBS = VB - VS;
        figure;
        plotHandle4=plot(VGS, IDS_M, 'b*', VGS, IDS_M, 'r+', 'EraseMode', 'Xor');
        xlabel('VGS (V)');
        ylabel('IDS (A)');
        title('extracting mu0, UGSZ, UBS .....');
        drawnow;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: err_id1.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function err=err_id1(param_dc)
        glo_par;
        mu0 = param_dc(1);
        UGSZ = param_dc(2);
        UBS=param_dc(3);
        jen_equ;
        err=sum((IDS_M - IDS_S).^2);
        k=size(IDS_M);
        ERROR=sqrt(sum((IDS_M - IDS_S).^2 ./ IDS_M.^2) / k(1));
        set(plotHandle4(2), 'Ydata', IDS_S);
        drawnow;
return;
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: init_dc2.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% initial plot
        VDS = VD - VS;
        VGS = VG - VS;
        VBS = VB - VS;
        figure;
        axis([0 3 10^(-10) 10^(-2)]);
        xlabel('VGS(V)');
        ylabel('IDS (A)');
        title(' extracting KSUB and N .....')
        drawnow;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: err_id2.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function err=err_id2(param_dc)
        glo_par;
        KSUB = param_dc(1);
        N = param_dc(2);
        jen_equ;
        k=size(VG);
        m=k(1)/indexbs;
        index=0;
        for i=1:m
           if index==0
                if VG(i) >= (vto + 0.1)
                   index = i;
                end
           end
        end
        ii=1;
        for i=1:indexbs
            for j=1:index
                IDS_Ms(ii) = IDS_M(j+(i-1)*m);
                IDS_Ss(ii) = IDS_S(j+(i-1)*m);
                ii = ii + 1;
            end
        end
        err=sum((IDS_Ms - IDS_Ss).^2);
        k = size(IDS_Ms);
        ERROR=sqrt(sum((IDS_Ms - IDS_Ss).^2 ./ IDS_Ms.^2) / k(1));
        set(plotHandle5(2), 'Ydata', IDS_S);
        drawnow;
return;
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: init_dcp.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% initial plot
        VDS = VD - VS;
        VGS = VG - VS;
        VBS = VB - VS;
        figure;
        plotHandle2=plot(VDS,IDS_M,'b*',VDS,IDS_M,'r+','EraseMode','Xor');
        xlabel('VDS (V)');
        ylabel('IDS (A)');
        title(' extracting UDS ........');
        drawnow;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: err_id.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function err=err_id(param_dc)
        glo_par;
        if param_dc(1) >= 20e6
            param_(1) = 20e6
        end
        ECRIT = param_dc(1);
        UDS = param_dc(2);
        jen_equ;
        err=sum((IDS_M - IDS_S).^2);
        k=size(IDS_M);
        ERROR=sqrt(sum((IDS_M - IDS_S).^2 ./ IDS_M.^2) / k(1));
        set(plotHandle2(2), 'Ydata', IDS_S);
        drawnow;
return;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: init_vt2.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% initial plot
     figure;
     plotHandle6=plot(cal_VBS,Vth_M,'b',cal_VBS,Vth_M,'r','EraseMode','Xor');
     xlabel('VBS (V)');
     ylabel('Vth (V)');
     title('extracting KNZ, KNB ......');
     drawnow;
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: err_vtw.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function err=err_vtw(param_dc)
        glo_par;
        KNB = param_dc(1);
        mode=2;
        cal_vth;
        Vth_S = cvth;
        err=sum((Vth_M - Vth_S).^2);
        ERROR=err;
        set(plotHandle6(2), 'Ydata', Vth_S);
        drawnow;
return;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        Copyright Steve H. Jen, Bing J. Sheu,  1998
%        function: init_vt3.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% initial plot
     figure;
     plotHandle7=plot(cal_VBS,Vth_M,'b',cal_VBS,Vth_M,'r','EraseMode','Xor');
     xlabel('VBS (V)');
     ylabel('Vth (V)');
     title('extracting GAMMA1L, ETAZ ......');
     drawnow;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: err_vtl.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function err=err_vtl(param_dc)
        glo_par;
        GAMMA1L = param_dc(1);
        mode=3;
        cal_vth;
        Vth_S = cvth;
        err=sum((Vth_M - Vth_S).^2);
        ERROR=err;
        set(plotHandle7(2), 'Ydata', Vth_S);
        drawnow;
return;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
%        function: init_dc3.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% initial plot
        VDS = VD - VS;
        VGS = VG - VS;
        VBS = VB - VS;
        figure;
        plotHandle8=plot(VGS,IDS_M,'b*',VGS,IDS_M,'r+','EraseMode','Xor');
        xlabel('VGS (V)');
        ylabel('IDS (A)');
        title('extracting UGSL, UGSL2 .....');
        drawnow;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: err_id3.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function err=err_id3(param_dc)
        glo_par;
        UGSL = param_dc(1);
        UGSL2 = param_dc(2);
        jen_equ;
        err=sum((IDS_M - IDS_S).^2 * 10^8);
        k = size(IDS_M);
        ERROR=sum((IDS_M - IDS_S).^2);
        set(plotHandle8(2), 'Ydata', IDS_S);
        drawnow;
return;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: init_dc4.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% initial plot
        VDS = VD - VS;
        VGS = VG - VS;
        VBS = VB - VS;
        figure;
        plotHandle9=plot(VDS,IDS_M,'b*',VDS,IDS_M,'r+','EraseMode','Xor');
        xlabel('VDS (V)');
        ylabel('IDS (A)');
        title(' extracting ECRIT, ETAZ ........');
        drawnow;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: err_id4.m
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function err=err_id4(param_dc)
        glo_par;
        ECRIT = param_dc(1);
        ETAZ = param_dc(2);
        jen_equ;
        k=size(VG);
        ind = 1;
        for i=1:k(1)
            if (VD(i) <=2)
                IDS_Ms(ind) = IDS_M(i);
                IDS_Ss(ind) = IDS_S(i);
                VGset(ind)=VG(i);
                ind = ind + 1;
            end
        end
        err=sum((IDS_Ms - IDS_Ss).^2 );
        ERROR=err;
        set(plotHandle9(2), 'Ydata', IDS_S);
        drawnow;
return;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: init_dc5.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% initial plot
        VDS = VD - VS;
        VGS = VG - VS;
        VBS = VB - VS;
        figure;
        plotHandle9=plot(VDS, IDS_M, 'b*', VDS, IDS_M, 'r+', 'EraseMode', 'Xor');
        xlabel('VDS (V)');
        ylabel('IDS (A)');
        title(' extracting LAMBDAD, LAMBDAG ........');
        drawnow;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        function: err_id5.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function err=err_id5(param_dc)
        glo_par;
        LAMBDAD = param_dc(1);
        LAMBDAG = param_dc(2);
        ECRIT = param_dc(3);
        jen_equ;
```

```
        k=size(VG);
        ind = 1;
        for i=1:k(1)
            if (VD(i) > 1.5)
                IDS_Ms(ind) = IDS_M(i);
                IDS_Ss(ind) = IDS_S(i);
                VGset(ind)=VG(i);
                ind = ind + 1;
            end
        end
        err=sum((IDS_M - IDS_S).^2 );
        ERROR=err;
        set(plotHandle9(2), 'Ydata', IDS_S);
        drawnow;
return;
```

endverbatim

Appendix E

SPICE Input Files of The Select Circuits

(A) Charge Conservation Property

```
***** charge conservation test *****
M1 1 2 3 4 CMOSN W=5u L=0.25u

Vin 2 0 DC 0 PULSE(0 5 60ns 2ns 2ns 60ns 120ns)
VBB 0 4 DC 0 PULSE(0 5 50ns 2ns 2ns 60ns 120ns)
VDD 1 5 DC 0 PULSE(0 5 70ns 2ns 2ns 60ns 120ns)

RD 5 3 100k
CS 3 0 0.1p

.tran 1ns 1us
.include modelcard.uscmos
.end
```

(B) Domino Logic Gate

```
**** Domino Logic : out=a(b+cd) *****

M1 7 2 1 1    CMOSP W=10u L=1u
M2 9 2 1 1    CMOSP W=10u L=1u
M3 10 2 1 1   CMOSP W=10u L=1u
M4 7 3 9 9    CMOSN W=5u  L=1u
M5 9 4 11 11  CMOSN W=5u  L=1u
M6 11 2 0 0   CMOSN W=5u  L=1u
M7 9 5 10 10  CMOSN W=5u  L=1u
M8 10 6 11 11 CMOSN W=5u  L=1u
```

```
* inverter *
M9 8 7 1 1    CMOSP W=20u L=1u
M10 8 7 0 0   CMOSN W=10u L=1u

Vdd 1 0 DC 4V
Vck 2 0 DC 0V PULSE(0 4 0n 1n 1n 4ns 10ns)
Va 3 0 DC 0V PULSE(0 4 0n 1n 1n 9ns 20ns)
Vb 4 0 DC 0V PULSE(0 4 0n 1n 1n 19ns 40ns)
Vc 5 0 DC 0V PULSE(0 4 0n 1n 1n 19ns 30ns)
Vd 6 0 DC 0V PULSE(0 4 0n 1n 1n 39ns 60ns)

.tran 1n 0.1u
.include modelcard.uscmos
.end
```

(C) Folded-Cascode Operational Amplifier

```
*** Fully Differential Folded-Cascode Operational Amplifier
*
* 1=in+ 2=in- 8=out+ 7=out- 50=vdd 60=vss
*
m1  9  1  4  50 cmosp w=200u l=0.35u ad=100p pd=200u as=100p ps=200u
m2  10 2  4  50 cmosp w=200u l=0.35u ad=100p pd=200u as=100p ps=200u
m3  4  21 50 50 cmosp w=600u l=0.7u  ad=300p pd=600u as=300p ps=600u
*
m5  5  21 50 50 cmosp w=180u l=0.7u  ad=90p pd=180u  as=90p ps=180u
m6  6  21 50 50 cmosp w=180u l=0.7u  ad=90p pd=180u  as=90p ps=180u
m7  7  22 5  50 cmosp w=160u l=0.35u ad=80p pd=160u  as=80p ps=160u
m8  8  22 6  50 cmosp w=160u l=0.35u ad=80p pd=160u  as=80p ps=160u
m9  7  24 9  9  cmosn w=30u  l=0.35u ad=15p pd=30u   as=15p ps=30u
m10 8  24 10 10 cmosn w=30u  l=0.35u ad=15p pd=30u   as=15p ps=30u
m11 9  35 60 60 cmosn w=100u l=0.7u  ad=50p pd=100u  as=50p ps=100u
m12 10 35 60 60 cmosn w=100u l=0.7u  ad=50p pd=100u  as=50p ps=100u
*
m21 21 21 50 50 cmosp w=20u  l=0.7u  ad=10p  pd=20u  as=10p  ps=20u
m22 22 21 50 50 cmosp w=10u  l=0.7u  ad=5p   pd=10u  as=5p   ps=10u
m23 23 23 21 50 cmosp w=4.2u l=0.7u  ad=2.2p pd=4.4u as=2.2p ps=4.4u
m24 24 23 22 50 cmosp w=16u  l=0.7u  ad=8p   pd=16u  as=8p   ps=16u
m25 24 24 60 60 cmosn w=0.7u l=0.7u  ad=0.4p pd=0.8u as=0.4p ps=0.8u
*
m31 60 7  31 50 cmosp w=0.35u l=0.35u ad=1.2p pd=2u  as=1.2p ps=2u
m32 35 32 31 50 cmosp w=0.35u l=0.35u ad=1.2p pd=2u  as=1.2p ps=2u
m33 31 21 50 50 cmosp w=7u    l=0.7u  ad=20p  pd=40u as=20p  ps=40u
m35 35 32 36 50 cmosp w=0.35u l=0.35u ad=1.2p pd=2u  as=1.2p ps=2u
m36 60 8  36 50 cmosp w=0.35u l=0.35u ad=1.2p pd=2u  as=1.2p ps=2u
```

```
m37 36 21 50 50 cmosp w=7u    l=0.7u  ad=20p  pd=40u as=20p  ps=40u
m39 35 35 60 60 cmosn w=2u    l=0.7u  ad=5.2p pd=10u as=5.2p ps=10u
*
ibias1 23 60 dc  50u
vcomm1 32 0  dc  0.0
*
vdd    50 0  dc +1.25
vss    60 0  dc -1.25
*
cl7  7 0  5p
cl8  8 0  5p
*
*vip  1 0  dc 0 ac 1
vip 1 0 dc 0
vim  2 0  dc 0

******************
*unity-gain  amp
******************
*Rin1 1 101  1k
*Rin2 2 201  1k
*Rio1 1 7    1k
*Rio2 2 8    1k

*Vinp 101 0 0V pulse(-0.5 0.5 50ns 5ns 5ns 100ns 200ns)
*Vinn 201 0 0V

*.ac dec 10 1 1000meg
.dc vip -0.2 0.2 0.04
*.tran 1ns 250ns

.include modelcard.uscmos

.option gmin=1e-9
.option itl1=5000

.end
```

(D) Analog Comparator

```
**** Analog Comparator ****

M51 7 3 2 2  CMOSN W=10u L=0.25u
M52 8 4 2 2  CMOSN W=10u L=0.25u
M53 7 6 2 2  CMOSN W=20u L=0.25u
```

```
M54 8 5 2 2  CMOSN W=20u L=0.25u
M55 5 11 7 7 CMOSN W=20u L=0.25u
M56 6 11 8 8 CMOSN W=20u L=0.25u
M57 5 6 1 1  CMOSP W=50u L=0.25u
M58 6 5 1 1  CMOSP W=50u L=0.25u
M59 5 11 1 1 CMOSP W=20u L=0.25u
M60 6 11 1 1 CMOSP W=20u L=0.25u
M61 9 5 1 1  CMOSP W=25u L=0.25u
M62 10 6 1 1 CMOSP W=25u L=0.25u
M63 9 5 2 2  CMOSN W=10u L=0.25u
M64 10 6 2 2 CMOSN W=10u L=0.25u

VDD 1 0 1.5V
VSS 2 0 -1.5V

Vcomp 11 0 DC 0V pulse(-1.5 1.5 2ns 0ns 0ns 2ns 4ns)
Vinp 3 0 DC 0V pwl(0ns -1.5V 30ns 1V)
Vinn 4 0 DC 0V pwl(0ns 1.5V 30ns -1V)

.include modelcard.uscmos
.tran 0.1ns 30ns
.end
```

(E) Wide-Range Gilbert Multiplier

```
* Modified Wide Range Gilbert Multiplier
*.OPTIONS post ACCT OPTS $probe=1 dcon=1
*.print i(vi)
m1  15 16 13 0 cmosn w=0.5u  l=1.75u
m2   8 20 13 0 cmosn w=0.5u  l=1.75u
m3   1 15 15 1 cmosp w=0.5u  l=0.25u
m4   1  8  8 1 cmosp w=0.5u  l=0.25u
m5  13 14  0 0 cmosn w=0.5u  l=0.25u
m6  17 10 12 1 cmosp w=1.25u l=0.25u
m7  17 11  7 1 cmosp w=1.25u l=0.25u
m8   1 15 17 1 cmosp w=1.25u l=0.25u
m9   9 11 12 1 cmosp w=1.25u l=0.25u
m10  9 10  7 1 cmosp w=1.25u l=0.25u
m11  1  8  9 1 cmosp w=1.25u l=0.25u
m12  7  7  0 0 cmosn w=0.5u  l=0.25u
m13  6  7  0 0 cmosn w=0.5u  l=0.25u
m14 12 12  0 0 cmosn w=0.5u  l=0.25u
m15 18 12  0 0 cmosn w=0.5u  l=0.25u
m16 19  5  6 0 cmosn w=1.5u  l=0.25u
m17  3  5 18 0 cmosn w=1.5u  l=0.25u
m18  4  3  3 1 cmosp w=0.5u  l=0.25u
```

```
m19  2  3 19 1 cmosp w=0.5u  l=0.25u
m20  1  2  4 1 cmosp w=0.5u  l=0.25u
m21  1  2  2 1 cmosp w=0.5u  l=0.25u
vdd 1 0 5
v1 16 0 2.5
v2 20 0 2.5
v3 11 0 2.5
v4 10 0 2.5
vbb1 14 0 1.0
vbb2 5 0 2
vi 19 0 2.5

.include modelcard.uscmos
.dc v1 1.5 3.5 .01 v3 2.1 3.0 .1
.end
```

(F) DRAM Circuit

```
*  DRAM Circuit
*2-word x 1-bit DRAM circuit

m0 101 100 1 1 cmosp l=0.25u w=0.75uu
m1 102 101 1 1 cmosp l=0.25u w=2u
m2 101 100 0 0 cmosn l=0.25u w=0.5u
m3 102 101 0 0 cmosn l=0.25u w=1u
*
m29 122 112 1 1 cmosp l=0.25u w=0.75u
m30 123 122 1 1 cmosp l=0.25u w=2u
m31 122 112 0 0 cmosn l=0.25u w=0.5u
m32 123 122 0 0 cmosn l=0.25u w=1u
*
* write circuits
*
m4 104 103 1 1    cmosp l=0.25u w=1u
m5 105 106 1 1    cmosp l=0.25u w=1u
m6 107 105 1 1    cmosp l=0.25u w=1u
m7 100 104 107 1  cmosp l=0.25u w=1u
m8 104 103 0 0    cmosn l=0.25u w=0.5u
m9 105 106 0 0    cmosn l=0.25u w=0.5u
m10 108 106 0 0   cmosn l=0.25u w=0.5u
m11 100 104 108 0 cmosn l=0.25u w=0.5u
*
m21 118 117 1 1   cmosp l=0.25u w=1u
m22 119 106 1 1   cmosp l=0.25u w=1u
m23 120 119 1 1   cmosp l=0.25u w=1u
m24 112 118 120 1 cmosp l=0.25u w=1u
```

```
m25 118 117 0 0   cmosn l=0.25u w=0.5u
m26 119 106 0 0   cmosn l=0.25u w=0.5u
m27 121 106 0 0   cmosn l=0.25u w=0.5u
m28 112 118 121 0 cmosn l=0.25u w=0.5u
*
* precharging transistors
*
m33 112 125 124 1 cmosp l=0.25u w=2.0u
m36 128 129 127 0 cmosn l=0.25u w=0.5u
m38 128 129 131 0 cmosn l=0.25u w=0.5u
m40 100 125 124 1 cmosp l=0.25u w=2.0u
*
* sense amplifier and restoring circuit
*
m14 100 111 1 1   cmosp l=0.25u w=0.75u
m15 112 111 1 1   cmosp l=0.25u w=0.75u
m16 112 100 113 0 cmosn l=0.25u w=1.75u
m17 100 112 113 0 cmosn l=0.25u w=1.75u
m18 113 114 0 0   cmosn l=0.25u w=1.5u
*
* memory cells
*
m12 100 109 110 0 cmosn l=0.25u w=0.5u
m13 0 110 0 0 cmosn l=1.25u w=1.5u
m19 112 115 116 0 cmosn l=0.25u w=0.5u
m20 0 116 0 0 cmosn l=1.25u w=1.5u
m34 112 126 127 0 cmosn l=0.25u w=0.5u
m35 0 127 0 0 cmosn l=1.25u w=0.75u
m37 100 130 131 0 cmosn l=0.25u w=0.5u
m39 0 131 0 0 cmosn l=1.25u w=0.75u
*
* parasitic capacitance
*
c0 131 0 37f
c1 128 0 248f
** node: 128 = vdum
c2 129 0 200f
** node: 129 = pre0
c3 127 0 37f
c4 130 0 13f
** node: 130 = dumr
c5 126 0 13f
** node: 126 = duml
c6 124 0 461f
** node: 124 = vref
c7 125 0 335f
** node: 125 = pre
```

```
c8 123 0 117f
** node: 123 = vol
c9 122 0 66f
c10 121 0 12f
c11 120 0 23f
c12 118 0 63f
c13 119 0 57f
c14 117 0 17f
** node: 117 = vinl
c15 116 0 28f
c16 115 0 13f
c17 114 0 11f
** node: 114 = sel
c18 113 0 152f
c19 112 0 369f
** node: 112 = bitl
c20 111 0 12f
** node: 111 = restore
c21 110 0 28f
c22 109 0 13f
c23 108 0 12f
c24 107 0 23f
c25 104 0 63f
c26 105 0 57f
c27 106 0 276f
** node: 106 = write
c28 103 0 18f
** node: 103 = vinr
c29 102 0 117f
** node: 102 = vor
c30 101 0 66f
c31 100 0 378f
c32 1 0 666f

* voltage signals
*
vref 124 0 dc 2.5
vinl 117 0 dc 0 pwl(0 0 24ns 0 25ns 5)
vinr 103 0 dc 0
vpre 125 0 dc 5
+ pulse(5 0 0ns 0.5ns 0.5ns 3ns 12ns)
vpredum 129 0 dc 0
+ pulse(0 5 0ns 0.5ns 0.5ns 3ns 12ns)
vlw0 115 0 dc 0
+ pulse(0 5 5ns 0.5ns 0.5ns 6ns 12ns)
vdumr 130 0 dc 0
+ pulse(0 5 5ns 0.5ns 0.5ns 6ns 12ns)
```

```
vwrite 106 0 dc 0
+ pulse(0 5 4ns 0.5ns 0.5ns 7ns 24ns)
vsel 114 0 dc 0
+ pulse(0 5 17ns 0.5ns 0.5ns 6ns 24ns)
vrestore 111 0 dc 0
+ pulse(5 0 17.5ns 0.5ns 0.5ns 5.5ns 24ns)
vdum 128 0 dc 1.8v
vlw1 109 0 dc 0
vduml 126 0 dc 0
* power supply
vdd 1 0 dc 5
*
* analysis
*
.nodeset v(1)=5 v(100)=1.52 v(101)=4.87
+ v(102)=1.25e-8 v(103)=0 v(104)=5
+ v(105)=5 v(106)=0 v(107)=5 v(108)=1.52
+ v(109)=0 v(110)=4.45e-7
+ v(111)=5 v(112)=1.52 v(113)=8.83e-1
+ v(114)=0 v(115)=0 v(116)=4.45e-7
+ v(117)=0 v(118)=5 v(119)=5 v(120)=5
+ v(121)=1.52 v(122)=4.87
+ v(123)=1.25e-8 v(124)=2.5 v(125)=5
+ v(126)=0 v(127)=4.51e-7 v(128)=1.8
+ v(129)=0 v(130)=0 v(131)=4.51e-7
.tran 0.1ns 60ns
.include modelcard.uscmos
.end
```

Appendix F

List of Publications Achieved from Dissertation Work

(A) Journal Papers

A.1. **Steve H. Jen**, Bing J. Sheu, Yoichi Oshima, "A unified approach to submicron DC MOS transistor modeling for low-voltage ICs," *Journal of Analog Integrated Circuits and Signal Processing*, Kluwer Academic Publishers, vol. 12, no. 2, pp. 107-118, Feb. 1997.

A.2. **Steve H. Jen**, Bing J. Sheu, "A compact and unified MOS DC circuit model with highly continuous conductances for low-voltage ICs, " *IEEE Trans. on Computer-Aided Design for Integrated Circuits and Systems*, vol. 17, no. 2, pp. 169-172, Feb. 1998.

A.3. **Steve H. Jen**, Bing J. Sheu, "A unified submicron MOS transistor charge/capacitance model for mixed-signal ICs," *IEEE Journal of Solid-State Circuits*, accepted in 1998.

A.4. **Steve H. Jen**, Bing J. Sheu, " High-frequency MOS transistor model and its effects on radio-frequency circuits," submitted to *Journal of Analog Integrated Circuits and Signal Processing*, Kluwer Academic Publishers.

Magazine Article

A.5. Yoichi Oshima, Bing J. Sheu, **Steve H. Jen**, "High-speed computing memory architectures for multimedia applications," *IEEE Circuits and Devices Magazine*, vol. 13, no. 1, pp. 8-13, Jan. 1997.

Book Chapters

A.6. Yoichi Oshima, Bing J. Sheu, **Steve H. Jen**, Memory Architectures Technology for Multimedia Systems, Chapter 4 in *Multimedia Technology for Applications*, Editors: Bing J. Sheu and Mohammed Ismail, IEEE Press: Piscataway, NJ, 1998.

A.7. Yoichi Oshima, Bing J. Sheu, **Steve H. Jen**, DRAM Chips, *Encyclopedia of Electrical and Electronics Engineering*, Editor: John G. Webster, to be published by John Wiley & Sons, Inc..

(B) Conference Papers

B.1. **Steve H. Jen**, Bing Sheu, Yoichi Oshima, "An improved method for MOS transistor output conductance," IEEE International Symposium on Circuits and Systems, Proc., vol. 4, pp. 448-451, Atlanta, GA, May 1996.

B.2. **Steve H. Jen**, Bing J. Sheu, "Deep submicron silicon CMOS transistor model for low-voltage low-power mixed-signal VLSI," *Chinese-American Engineers and Scientists Association of Southern California Annual Convention and Technical Conference, Proc.*, pp. 32-33, Los Angeles, CA, Mar. 1997.

B.3. **Steve H. Jen**, Bing J. Sheu, Alex Y. Park, "An efficient MOS transistor charge/capacitance model with continuous expressions for VLSI," *IEEE International Symposium on Circuits and Systems, Proc.*, vol. 6, pp. 413-416, Monterey, CA, May 1998.

B.4. **Steve H. Jen**, Christian Enz, David R. Pehlke, Michael Schroter, Bing J. Sheu, "Accurate MOS transistor modeling and parameter extraction valid up to 10-GHz," accepted by European Solid-State Device Conference, France, Sept. 1998.

Related Work

B.5. Bing J. Sheu, **Steve H. Jen**, Richard H. Tsai, David C. Chen, "Multimedia for applications," tutorial of IEEE International Symposium on Circuits and Systems, Hung Kong, Jun. 1997.

B.6. Eric Y. Chou, Bing J. Sheu, **Steve H. Jen**, "A Compact VLSI design for recursive neural networks with hardware annealing capability," *IEEE International Conference on Neural Network, Proc.*, vol. 3, pp. 1650-1655, Perth, West Australia, Nov. 1995.

B.7. Richard H. Tsai, Bing J. Sheu, Michelle Y. Wang, **Steve H. Jen**, "Two-dimensional cellular neural networks for pre-processing in face recognition and digital library search," *IEEE International Symposium on Circuits and Systems, Proc.*, pp. 733-736 Hong Kong, Jun. 1997.