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S-CMOS: A Robust Deep-Submicron CMOS Transistor Model For Very Low-Power High-Frequency VLSI Application

by

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Abstract

A robust deep-submicron Short-Channel MOS transistor model (S-CMOS) is developed. All operation regions of MOSFET can be simulated with unified expression of S-CMOS model including the triode, saturation, subthreshold, weak and strong inversion regions. Temperature dependency on threshold voltage and effective mobility was investigated and efficient model was developed. Simple noise model was developed to describe the behavior of the noise in MOSFET devices. The effective mobility expression includes the effects of lateral and vertical electric fields in the channel efficient degradation factor which simplifies the expression and reduce the computation time. The unified drain current and terminal charge expressions, which provides a highly continuous behavior for the conductances and capacitances in all regions of operation are developed and the robustness was verified by simulating every mathematical components. The charge model uses the better expression of conductance degradation coefficient to model the channel charge density. The unified expressions of charge densities are valid for all operation regions, including the accumulation region. Non-quasi-static charge capacitance analysis is developed for radio frequency application and a unified first-order non-quasi-static expression including time constants for long-channel transistor and high frequency are derived. The

characteristics of time constants in all geometric regions are simulated and analyzed for high frequency Very large Scale Integration (VLSI) application. Efficient parameter extraction procedure was developed by using multiple-objective function which is able to include not only drain current but also conductance and transcoductance characteristic of the transistor and the extraction procedure of the S-CMOS model was implemented in MATLAB software. The accurate parameter values are extracted in accordance with the measurement data of 0.35μm technology transistors from MOSIS Service. The S-CMOS model is implemented into SPICE3f3 from U.C. Berkley successfully under SUN Solaris 2.6. and the performance comparison of S-CMOS, MOS Level2, Level3, BSIM, and BSIM3v3 models in circuits simulation including folded-cascode Op-Amp, analog multiplier, comparator, 8-bit carry-save adder, and 8-bitx8-bit carry-save multiplier are demonstrated. Detailed design and simulation results on efficient 8-bitx8bit divider design and simulation results are also included. The estimation methods of dc power dissipation of basic CMOS digital circuit blocks are also presented.

Chapter 1

Introduction

The idea of complementary MOSFET (Metal Oxide Semiconductor Field Effect transistor) was introduced in early 1960's. With the benefit of improvements in the Integrated Circuits(IC) fabrication technology in 1980's, Complementary Metal Oxide Semiconductor (CMOS) technology was widely accepted and used for VLSI system implementation. This acceptance was because of the unique advantages of CMOS circuits over nMOS and Bipolar junction transistor counterparts. CMOS technology consumes less power than other technologies and it is very suitable for battery-operated systems. Also, low cost, high-package density, large design margin (easy to design,) high noise margin, easy to scaling, wider temperature and voltage operation range make CMOS technology unique and promising for Very large-scale integration (VLSI) and Ultra large-scale integration (ULSI). VLSI circuits fabricated by metal-oxide-semiconductor (MOS) technologies are widely used in industry to implement high-performance computing, signal processing, multimedia, and telecommunication systems [1]. As the integrated-circuit industry continues its tremendous growth, a urgent concern is the industrial standard MOSFET models that can be commonly used in integrated-circuit simulation. MOSFET models are taken as representing the electrical behavior of a particular transistor fabrication technology and

provide the critical link, the "communication vehicle" between a foundry and its fabless customers. The emergence of CMOS as the main fabrication technology over the past decade has been accompanied by a reduction in feature size from 2.5μm to 0.18μm, an increase in chip area from $50mm^2$ to $300mm^2$, and an increase in the number of transistors from 100,000 to 1 billion for memories and from 60,000 to over 7 million for microprocessors [2], the further newest multi-chip-module (MCM) package technology can bind several chips in a single substrate with more than 20 million transistors, a drop in the on-chip gate delay from 1 nano-second to 10 pico-second and an increase in the chip clock frequency from 10 MHz to over 1 GHz [3]. In the competitive industrial environment, efficient design automation is invaluable in ensuring that high-quality products developed within a short period of time. In such an environment, circuit and system designs can take place simultaneously with continuous technology improvement. This requires closer relationship in the vertical integration from the device-level simulation through the circuit-level design to the system-level simulation. In recent years, concurrent engineering has been replacing traditional isolated design and manufacture approaches.

The level of circuit integration on a single chip has been greatly increased by new lithography and etching techniques. The increased use of deep-submicron technologies has created new challenges for researchers in mixed-signal VLSI hardware design, high-performance circuit simulation, and microelectronic system design. At the transistor level, detailed investigation of small-geometry effects on the behavior of transistors is required. Effects of coupling between interconnections and neighboring devices can be more significant due to compactness of the circuit. The degradation of device behavior with time of

operation can be more significant due to higher electrical stresses in the channel region of MOS transistors. At the circuit design level, accurate modeling of transistors is urgently needed so that special features of advanced technologies can be exploited to the greatest extent. Desirable features of the model include a compact set of parameters, continuity of the drain current and its derivatives across different regions of operation, and the ability to use a single parameter set over a large geometric design space. At the system design level, new architectures are required in order to utilize advanced technologies effectively and extend boundaries of achievable performance. Advanced computer architectures are likely to use superpipelined multiprocessors with distributed memories and optical interconnections. Nowadays, the integrated media systems combine all the advanced audio/video, telecommunication, and memory technologies to structure the information super-highway. Simultaneous efforts at the device, circuit, and system levels are essential in order to achieve the high performance computing and communication.

The main flowchart of mixed-signal VLSI circuit and system design is shown in Fig 1.1. Application is the first and most important issue, such as multimedia, telecommunication, microprocessor, hard disk drive, etc., which determines the aspect of the VLSI design. After that, the design methodology and algorithm should be determined to optimize the design cost and expected performance. During the circuit implementation period, simulation and verification are needed for each step to ensure the correction of the function and operation. In order to achieve the new generation of VLSI design which involves a very complex design procedure, the advanced computer-aided design (CAD) tools are required.

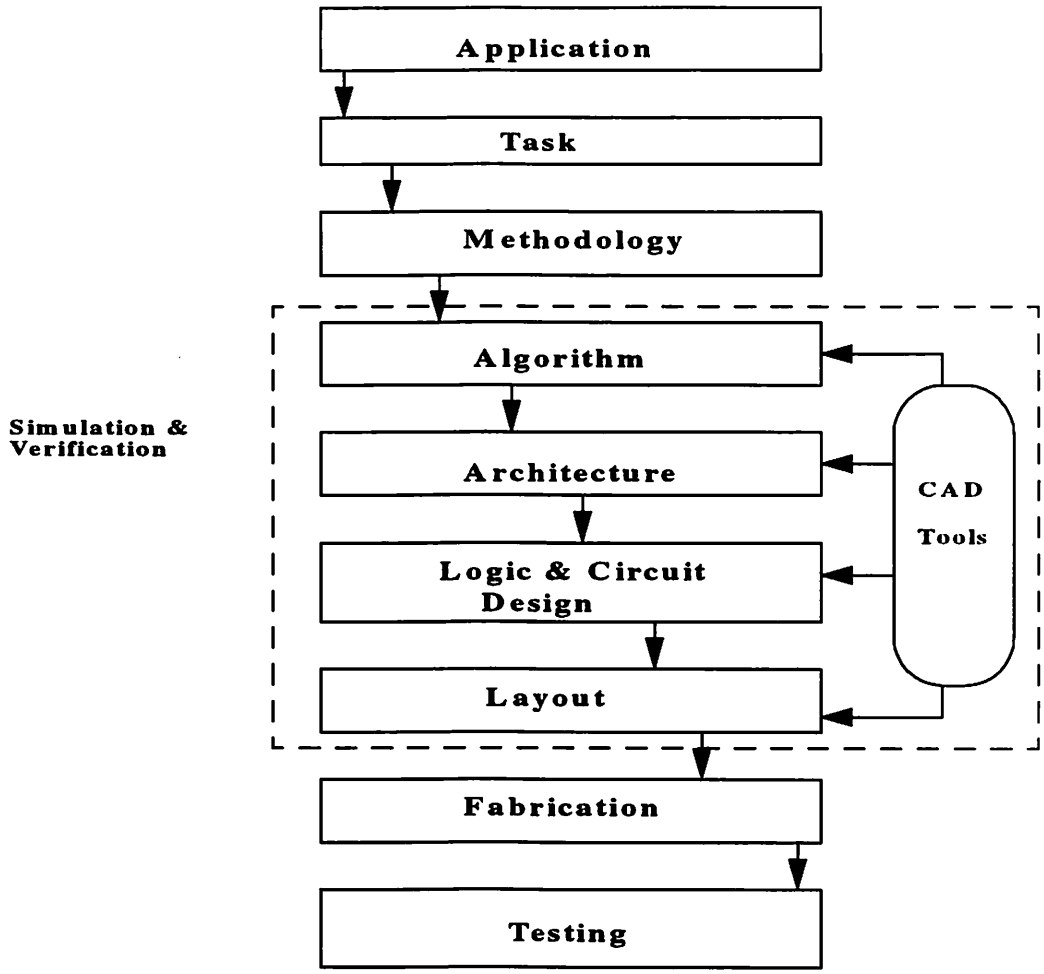

Figure 1.1: The main flowchart of mixed-signal VLSI circuit and system design

Fig.1.2. shows the main component of an advanced VLSI design environment. In the design and synthesis portion, the CAD tools for the digital domain are fairly well developed. However, the design of the analog sections often remains a bottleneck. To increase the efficiency of the design process, and reduce the design time for the mixed-signal VLSI, the analog CAD should be paid a lot of attention. Due to short prototype development time, device/process simulators such as SUPREM[9], SAMPLE and PISCES[10] from Stanford University can be used to analyze the effects of adjusting process variables,

and to predict detailed device behavior. Device simulators can be used to generate circuit-level parameters so that simulation can be performed for prediction of circuit performance. This link between device and circuit simulators enables optimization of fabrication processes based on circuit performance. The core of VLSI simulation environment contains circuit simulators such as SPICE from U.C. Berkeley [4], which use models of devices such as transistors to predict the detailed electrical behavior of analog and digital circuits.

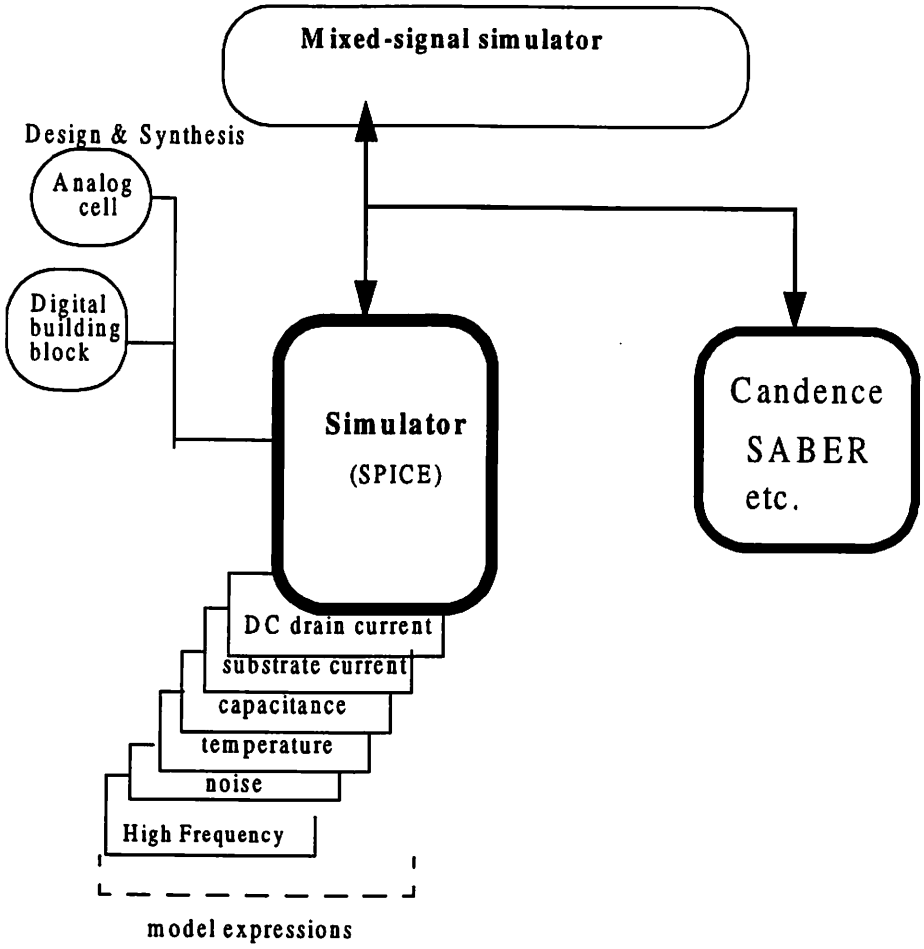

Figure 1.2: An advanced VLSI design environment

The model expressions calculate the terminal voltage and current waveforms of devices based on model parameters. Several commercial circuit simulators are based upon the SPICE program including HSPICE from Avant! Corp.[5]. and PSPICE from Microsim Corp. [6]. The use of macro-models increases the efficiency of these detailed circuit simulators. Some circuit simulators such as SPLICE from U.C. Berkeley [11] and iSPLICE from Univ. of Illinois, can perform simulation of mixed-signal circuits that contain substantial analog and digital circuitry. Other circuit simulators such as RELAX from U.C. Berkeley [12] and AWESIM from Carnegie Mellon University use waveform relaxation techniques to speed up simulation tasks. In addition to simulation results of the freshly manufactured circuit, the designer may require information about the degraded performance of a circuit after it has operated for some period of time, because the use of extremely small feature sizes causes concerns of transistor and interconnection reliability. Reliability simulators such as RELY from University of Southern California [7], BERT from U.C. Berkeley [14], and iSMILE from Univ. of Illinois, can be used to predict the lifetime of circuits based on technology-dependent degradation parameters. Reliability simulation results can be used to modify circuit designs for reliability enhancement before actually committing the circuit to fabrication. Reliability predictions are also useful in determining warranties to be given to customers using electronic products. At the highest level of abstraction in the simulation environment, logic and timing simulators use behavioral models of the circuit to predict and verify the functionality and speed performance of electronic sub-systems or systems. IC designers moving to deep submicron technologies face big challenges. Initial design projects have experienced unexpectedly long design cycles, a larger than expected number of design iterations, problems getting chips to oper-

ate at target clock speeds and surprises with die size late in the design cycle. The effects of deep submicron geometries, higher clock speeds, and soaring gate counts all create new design problems that are not addressed by existing tools and methodologies. The limitations of available tools and methodologies are clear. Logic designers, who once needed to know little about the physical implementation of their devices to successfully complete their designs, must now have access to key physical design information early in the design process. Without this information, timing delays, routability, and power dissipation are not accurately predicted and the logic designer has no way of knowing if basic design constraints such as functionality, cost, power, and speed are being met. The result is often big surprises late in the design cycle. Results from the circuit simulator affect crucial decisions that are made during architectural specification, circuit design, and chip fabrication. Accurate and efficient MOS transistor models are keys to the successful operation of such VLSI simulation environments. As the integrated-circuit industry continues its tremendous growth, an urgent concern is the Industrial Standard MOSFET models that can be commonly used in integrated-circuit simulation. MOSFET models are taken as representing the electrical behavior of a particular transistor fabrication technology and provide the critical link-the "communication vehicle" between a foundry and its fabless customers[16]. In the area of standard model testing, once a particular model is selected it should be tested using standard test cases. To cope with the urgent industrial demands, Compact Short-channel MOS Model (S-CMOS) will be completed for industrial application. With the growing use of portable and wireless electronic systems, reduction in power consumption has become more and more important in today's VLSI circuit and system designs. In CMOS digital circuits, power dissipation consists of dynamic and static components.

Since dynamic power is proportional to the square of supply voltage V_{dd} and static power is proportional to V_{dd}, lowering supply voltage is obviously the most effective way to reduce power consumption. With the scaling of supply voltage, transistor threshold voltage (Vth) should also be scaled in order to satisfy the performance requirements. Unfortunately, such scaling leads to an increase in leakage current which becomes an important concern in low voltage high performance circuit designs. Multiple thresholds can be used to deal with the leakage problem in low voltage high performance CMOS circuits. This technique has commonly been used in DRAM chips by raising threshold voltages of the array devices with a fixed body bias. Besides reducing threshold and supply voltages, other level of power reduction methodologies, such as; architecture, system or logic/circuit levels should be used during the design process for optimizing the power dissipation of digital systems. Because reducing threshold voltage causes in an exponential increase in the leakage current, DC power consumption of the CMOS circuits becomes more crucial for low-power, low-voltage CMOS circuits. Leakage current related power consumption analysis and optimization of the CMOS digital circuits was reported in the literature lately[17]. A model for deep-submicron CMOS digital circuits were examined and applied to basic CMOS digital building blocks. 0.35μm CMOS submicron process technology model parameters and SPICE3f3 circuit simulation program[4] is used.

According to the needs of the advance MOS transistor model for circuit designers and device engineers, a deep-submicron MOS transistor model for low-power and low-voltage mixed-signal circuit design is developed. The deep-submicron techniques and some interpolation and smoothing functions will be used to achieve accuracy and continuity of the

drain current, output conductance, transconductance, and their derivatives in all regions of transistor operation. Besides the drain current and charge/capacitance models, temperature and noise effects on circuit performance will also be considered in the new model. Based on the SPICE simulator structure, the new model will be designed to increase the accuracy, decrease the computational complexity, and avoid the non-convergence problem.

The MOS transistor modeling problem is described in Chapter 2. Literature publications in this area have been surveyed and significant results area briefly described. In this Chapter, an overview of MOSFET modeling for circuit simulation is presented. After discussing some of the implications of analog and low-power applications, the history of the MOS models commonly used in SPICE-like circuit simulators and the simulators are presented. In Chapter 3, based on the BSIM, drain current model structure described by unified expression is introduced. In Chapter 4, a newly developed Charge/Capacitance MOSFET model and the experimental results are presented. Non-quasi-static approach for high frequency application is proposed also in this Chapter. In Chapter 5 an efficient parameter extraction procedure and its strategies are presented. Accurate S-CMOS parameter values extracted with MOSIS 0.35μm tech. are introduced in this chapter. The implementation of the model in SPICE3f3 simulations are presented in Chapter 6. The performances comparison of S-CMOS, MOS Level2, Level, BSIM1, and BSIM3v3 models in circuits simulation including folded-cascode Op-Amp, analog multiplier, comparator, 8-bit carry save adder, and 8-bitx8bit carry save multiplier are presented in this chapter. Efficient 8-bitx8bit divider design and simulation results are included in this chapter also. Finally, Chapter 7. presents discussion and conclusion for implementation in the industrial application.

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Chapter 2

MOS Transistor Modeling

2.1 Overview

Rapid progress in VLSI technology have made the implementation of high density chips possible which contains multi-million transistors. Reducing feature size of the CMOS devices is the main way to increasing integration density in VLSI. New fabrication technologies, like CMOS Shallow Junction well FET (SJET) by Toshiba Corp., Twin-tub CMOS process with Lightly Doped Drain (LDD), and SOI (Silicon on Insulator)[1] have been developed for producing deep-submicron devices. When MOS transistors are made smaller (shorter or narrower) for VLSI circuits, several small-geometry effects arise, and two-dimensional effects near the edges of the smaller transistor become significant. Therefore, simple one dimensional gradual channel approximation (GCA)[2] no longer useful for explaining effect took place under the channel of the small geometry MOS device. Two-dimensional potential distribution in small-geometry MOSFETs, cause in reduction on threshold and punch-through voltages and cause in degradation on the sub-

threshold characteristics of the MOS devices. Also, reducing feature size and keeping supply voltage high, like 5V, cause in hot carrier generation and impact ionization which degrade device performance and characteristics. In the device design standpoint, proper design of the sub-micron devices become crucial for avoiding those short-channel effects. In the device model standpoint, short-channel effects such as carrier velocity saturation, carrier mobility degradation, and drain-induced barrier lowering (DIBL), should be included in the MOS transistor models. This kind of sophisticated models are available in today's technology and can be found in the literature [1],[2],[3]. Digital CMOS IC's have been the main driving force behind the VLSI technology for implementation of high-performance computing and other kinds of commercial or scientific applications. It seems that the demand of high density and high-performance digital CMOS IC's will be continually increased, because of the unique features of CMOS technology mentioned before. During last several years, tremendous amount of improvements have been seen in miniaturization of CMOS devices. Deep sub-micron CMOS devices were introduced and have become widely used in the market. However, as VLSI technology continuous to develop, power consumption, interconnection delay, and clock skew of the VLSI chips become crucial design considerations. Also keeping computing capacity high [4] and avoiding hot carrier effect in deep-submicron CMOS digital circuits, supply voltage of the system should be scaled down. With reducing V_{dd}, for keeping circuit speed the same and increasing the current drive capability of the logic gate or transistor, threshold voltage of the MOS transistor should be scaled down by keeping the ratio [5]. Three major criteria can be used to evaluate MOS transistor models for circuit simulation and circuit design: accu-

racy of simulation results, computational efficiency, and convenience of the model to circuit designers. The accuracy of circuit simulation results depends upon the ability of the model and the associated parameter set to simulate transistor characteristics including drain current, conductances, terminal charges and internodal capacitances over useful ranges of terminal voltages and transistor geometries that are used in the circuits. There is usually a balance between the accuracy and computational efficiency of a model, and clever handling of such a balance is an important engineering challenge. The usefulness of a device model to circuit designers depends upon several factors including the number of parameters, the different effects and features that are incorporated into the model, and how well the accuracy/efficiency balance is achieved. Significant results were reported over the past two decades from research on MOS transistor modeling. The tremendous advance achieved in improving the performance of these devices demands corresponding amount of efforts and progress in modeling their behavior. Three main categories of MOS transistor modeling research include:

type-1: investigation and modeling of specific important aspects of transistor behavior including threshold voltage, mobility, saturation velocity, and subthreshold conduction;

type-2: development of highly accurate and computational complex transistor drain current models that include many second-order and higher-order effects which are useful to device engineers; and

type-3: development of accurate and computationally efficient transistor models with compact parameter sets that closely address the needs of VLSI circuit designers.

For historical reasons, it is useful to classify the existing SPICE MOSFET models into three evolutionary generations[1]. The first-generation models were based on the simple

intention of physically-based analytical expressions, with all simple geometry dependence included in the model equations. These models concentrate on the description of the MOS transistor rather than the behavior of the model equations in a circuit simulator. This generation of models is comprised of Level-1, Level-2, and Level-3 models.

The second-generation models represented a major change from the philosophy for the first-generation ones. In this set of models, analytical equations are subject to extensive mathematical conditioning, with a clear focus on the circuit simulation usage. The parameter structure is twofold; there are individual device parameters, and there are also geometry-related (length and width) parameters. The model structure and its parameters take on considerable empirical character. This has the effect of shifting the challenge in the model to parameter extraction, which is imposed on a rather systematic formulation. This generation of models encompasses BSIM [7] and BSIM2, along with HSPICE Level-28 [21] which is based on BSIM. More recently, third-generation models started to emerge. The fundamental intent is to return to a simple model structure, possibly with a reduced number of parameters. These parameters are strongly physically-based, rather than being very empirical. Mathematical conditioning is also important in these models. However, in contrast to the polynomial functions which are heavily used in the second-generation models, the third-generation models employ more specialized smoothing functions which are mathematically well behaved. With the use of smoothing functions, the analytical equations for drain current and terminal charge and their derivatives are continuous and smooth. A single equation can be used for all regions of transistor operation. An overview of widely used MOS transistor models is presented here to provide the background of the new model development effort. The survey includes analytic models such as the MOS

Level-1, Level-2, Level-3, Level-6, BSIM, and BSIMplus [12] that are implemented in the SPICE3 circuit simulator, the ASIM model from AT&T Bell Laboratories, table look-up approach models, and the newest developed models, EKV model [13] from Europe and aMOS model from TI Inc..

2.2 MOS Transistor Models

The first-generation MOS transistor models were based on simple description of the device. The main focus is on the analytical description of the MOS transistor.

2.2.1 The First-Generation MOS Transistor Models

2.2.1.1 The Level-1 Model

The Level-1 MOS model is a first-order model that is useful for hand calculations when designing and analyzing new circuits. Simple expressions are used to describe the drain current characteristics. The Level-1 model applies well to large devices. The only geometric dependency is the inclusion of a simple l-expression for channel length modulation. Also, there is no subthreshold conduction expression.

2.2.1.2 The Level-2 Model

The Level-2 MOS model, reported by Vladimirescu and Liu [5], requires 18 parameters and includes many second-order effects suitable for in devices with channel length down to 1.2μm. The threshold voltage expression in the Level-2 MOS model included the substrate-bias and narrow-channel effects. The body-effect coefficient due to the depletion charge at the drain and source terminals was modified by correction factors. Depletion-

layer widths near the source and drain were calculated from the source and drain voltages, respectively. A single parameter with inverse-width dependence is used to model the drain-included barrier-lowering effect as well as the narrow-channel effect on the depletion charge-sharing coefficient. The channel length reduction was calculated from a complex expression that included the depletion layer width, the carrier mobility at the semiconductor surface, and the maximum carrier drift velocity at velocity saturation. The transition point between the weak and strong inversion regions was defined to be above the threshold voltage by a multiple of the thermal voltage value. The multiplication factor was calculated from the bulk depletion capacitance and a curve-fitting parameter that was related to the fast surface states at the oxide/silicon interface. A complex expression modeled the drain current in the weak-inversion region as an exponential function of the gate terminal voltage and the transition voltage. Continuity of drain current expressions was achieved at the transition point between weak and strong inversion. However, continuity of the first-order derivative of the drain current expressions was not achieved at this transition point.

2.2.1.3 The Level-3 Model

The Level-3 MOS model, which was also reported by Vladimirescu and Liu, is a semi-empirical model and can be used for technologies with feature sizes down to 1.0μm. The Level-3 model requires 18 parameters in the drain-current expressions that were mainly based on the curve fitting approach. The model took into account the two-dimensional nature of the potential distribution in the channel region. Geometrically dependent effects

were included to a limited extent in order to increase the accuracy of the model for technologies below 1.5μm. The threshold voltage in the Level-3 MOS model was calculated from the flat-band voltage and the surface inversion potential, and included the drain-induced barrier-lowering effect and the non-uniform substrate-doping effect. The drain-induced barrier-lowering effect was modeled with an inverse dependency on the cubed channel length. The non-uniform substrate doping effect included correction terms for the short-channel and narrow-channel effects. The correction factor for short-channel effects was calculated from the junction depth by using a trapezoidal approximation. The correction factor of narrow-channel effect was calculated from an inverse-width dependence and modeled the adjustment of depletion charges at the edge of the channel.

The surface carrier mobility was calculated from the intrinsic mobility in the channel region and an empirical fitting parameter. The effect of the vertical field on the intrinsic carrier mobility was modeled as a function of the gate voltage. The effective mobility also included the velocity saturation effect that was dependent upon the horizontal field in the channel and was calculated using the maximum carrier drift velocity parameter. The amount of channel-length reduction was calculated from the lateral electric field at the channel pinch-off point. The coefficient of depletion layer width which was calculated from the substrate doping concentration, and an empirical fitting parameter, was also used to determine the amount of channel-length reduction. The drain-current expression included a Taylor series expansion coefficient of bulk charge and the transconductance coefficient. The saturation voltage was defined as the drain voltage at which the carrier velocity approached the value of the maximum carrier drift velocity parameter. If this parameter was not given, the saturation voltage was determined from the maximum of the

drain-current equation. The weak-inversion drain current expression was similar to that used in the Level-2 MOS model. The Level-3 MOS model used a compact set of parameters. This was convenient for circuit designers who used the model, and also eased the parameter extraction task in which device engineers characterized the technology in terms of the model parameters. Since many model parameters were empirical, integration of the circuit simulator with device-level simulators that solve Poisson equations is quite difficult. Such integration includes determining the transistor parameter values from electronic quantities that are predicted by the device-level simulators. Empirical parameters are usually extracted to fit a limited voltage range or geometric space, while circuit designers could require simulations over a large voltage range and extensive geometric design space. The use of cubic inverse-length dependence for the drain-induced barrier-lowering term of the threshold voltage could limit the range of channel lengths over which a single parameter set is applicable. The use of a square-root dependence on $(V_{DS}-V_{DSAT})$ in the channel length modulation expression could cause discontinuity in derivatives of the drain-current expressions at the triode/saturation transition point. Such discontinuity could lead to non-convergence problems in the circuit simulation. The MOS Level-6 model was a simple model based on the n-th power law. The simulation times using this model were reported to be considerably better than the Level-3 model. Smooth drain current characteristics at the transition between the triode and saturation regions of operation improved the convergence of the circuit simulator. Parameters can be quickly calculated from a small number of data points. The model is general, and can also be applied to GaAs FETs.

2.2.2 The Second-Generation MOS Transistor Models

In the second-generation models, the device geometry is excluded in the basic model equations. In addition, an entirely separate parameter group is used solely to describe the geometric dependence. Independent parameters are extracted for each device. Then the geometry parameters are extracted to fit initial set of independent parameters across the length and width. The goal is to provide an apparatus in which the original independent device parameters can be reconstituted for any particular choice of channel length and width.

2.2.2.1 The BSIM Model

The BSIM(Berkeley Short-Channel IGFET Model)[7] is based on the device physics of small-geometry MOSFETs. It was a circuit-level MOS model with strong device physics emphasis which can accurately describe drain-current characteristics of transistors with channel lengths down to about 0.8μm[7]. The model used a total of 62 parameters in the drain-current expression. There were 24 electrical parameters, of which 19 were calculated from nominal, inverse-length and inverse-width coefficients. The simple framework of geometry dependence was a salient feature of the BSIM model. The parameter values were calculated by, length-dependent coefficient and width-dependence coefficient of the parameter respectively. The extracted parameters are in the form of a process file containing parameters for different layers including the NMOS and PMOS transistors, N-diffusion, P-diffusion, and metal layers showing a fully-integrated approach for computer-

aided parameter extraction and circuit design. The threshold voltage expression in the BSIM model included the effect of non-uniform substrate doping on the depletion charge term. The effect of extra bulk charge at the edge of narrow transistor channels was not explicitly modeled in the threshold voltage expression. The drain-induced barrier-lowering coefficient was calculated using zero-bias, substrate-voltage and drain-voltage dependence parameters, each of which has geometry dependency. The reduction of carrier mobility in the triode region due to vertical and horizontal electric fields was modeled by terms that were dependent upon the drain and gate voltages. The vertical field effect included only the gate voltage contribution explicitly. A second-order dependence upon the substrate voltage was included in the parameter that was used to model the vertical field effect. The parameter that describes the horizontal field effects was dependent upon the substrate and drain voltages. The drain-current expression in the saturation region included a body-effect coefficient term and a carrier saturation-velocity term. The drain current and its first-order derivatives were continuous at the transition between the triode and saturation regions. The subthreshold conduction expression in the BSIM model was dominated by the diffusion current component. The subthreshold slope was calculated using drain-voltage and substrate-voltage dependence coefficients. The diffusion component of the subthreshold current was modeled by using an exponential dependence on the gate and drain terminal voltages. The subthreshold current was limited in the strong-inversion region by clamping. The total drain current in all regions of transistor operations was expressed as the sum of weak-inversion and strong-inversion drain current components.

The simple geometric dependence framework included in the BSIM model was intended to increase accuracy of the model over a large geometric range. However, the number of

parameters that are to be extracted is quite large. As a result, only a small geometric region can be accurately characterized. Simulation of transistors beyond this characterized region can result in abnormal simulation results. due to exaggeration of second-order geometry-dependent effects. The technique used to model the non-uniform substrate doping effect can cause non-monotonic threshold voltage variation at high substrate voltages, resulting in simulation non-convergence problems. This happens because the terminal voltage during intermediate circuit simulation iterations sometimes take very high values beyond the power supply rails of the circuit. The drain current and the first-order derivatives are continuous at the triode/saturation transition and this is critical for circuit simulation purpose. However, the second derivative of the drain current is not continuous, resulting in poor output conductance behavior at the triode/saturation transition and in the saturation region.

2.2.2.2 HSPICE Level-28 Model

HSPICE Level-28 model [21] is a proprietary model which has used HSPICE as a vehicle to gain rather widespread acceptance. The model structure is based on BSIM, but has been extensively enhanced. Through extensive mathematical conditioning, HSPICE Level-28 has been made suitable for analog design. It is thus commonly employed in the IC industry. A unique feature of HSPICE Level-28 model is that the model structure is designed to accommodate model binning. Additional terms are introduced to provide the continuity of the model parameters at all four corners of a bin. In its structure, HSPICE Level-28 model enhances the quadratic expressions which appear in BSIM, so that they become less trou-

blesome. The drain-current expression contains very extensive conditioning of the various transition points. This foreshadows the structure of the third-generation models, and has led to very successful results. The saturation voltage model defines a transition region in addition to the normal use of the linear region and the saturation region, which produces good results. A similar conditioning approach is used on the subthreshold model, where several subregions are defined. In particular, the problems introduced in BSIM by the simple addition of the weak inversion current to the strong inversion current are eliminated. HSPICE Level-28 model maintains the clear focus of the second-generation models on the circuit design purpose. However, the model parameter set is very empirical. In addition, due to its roots, HSPICE Level-28 model carried virtually the entire BSIM mathematical structure. It can thus be slow in the simulation of large circuits. Due to its suitability for analog circuit design, HSPICE Level-28 model is commonly employed in the industrial circuit design environment.

2.2.2.3 The BSIM2 Model

The BSIM2 model from U.C. Berkeley [8] was a significant modification of the BSIM model. Several additional empirical parameters were added to model second-order effects of transistor behavior. By increasing the number of parameters, the accuracy of the model in the submicron region was improved. However, additional problems of complexity in circuit simulation and parameter extraction were created due to the very large parameter set. Extrapolating the process file from existing technologies to future technologies for all parameters that was used in BSIM, was retained in BSIM2. The threshold voltage in BSIM2 was very similar to that used in BSIM. The drain-voltage dependence of the drain-

induced barrier-lowering coefficient was removed in order to prevent the occurrence of negative output resistance at low current levels. The effect of the vertical field on the carrier mobility included a quadratic dependence upon the gate voltage in order to model the effect of large electric fields that occur in devices with thin gate oxides. The velocity saturation effect was modeled using the critical electric field parameter, which was calculated from a second-order dependence on the drain and saturation voltages. The effect of source/drain parasitic resistances were lumped with the mobility term during parameter extraction. The horizontal and vertical field effects on the mobility were combined as a summation of terms rather than as a product. The subthreshold drain current was calculated using the charge-sheet approximation. The depletion-layer capacitance and the surface potential at the channel/oxide interface were calculated as functions of the gate voltage. A transition region was defined around the threshold voltage and the effective gate voltage that was used in this region was generated using a cubic spline function in order to improve the transition between the weak-inversion and strong-inversion regions. The ability to handle analog design requirements is a major feature of BSIM2. In addition, the drain current model is more accurate, and provides better convergence behavior during circuit simulation. The main problem with BSIM2 is its complexity as it contains a very large number of parameters.

2.2.3 The Third-Generation Models

The third-generation MOS transistor models have started to emerge. The original intent was simplification of the MOS transistor model formulation, a reduction of the number of

model parameters, and the development of parameters which are physically-based rather than being empirical, as in the second-generation models. There is also extensive use of well-behaved mathematical smoothing functions, which allows for smooth and continuous expressions for model equations and their derivatives. The use of these smoothing functions usually leads to a combined equation which is valid for all regions of device operation.

2.2.3.1 The BSIM3 Model

The BSIM3 model from U.C. Berkeley [9], at present, has several different versions released. The original intent of BSIM3 was simplicity, with a simplified model structure and a small number of physically-based parameters. However, Versions 1 and 2 showed several shortcomings. An attempt to repair these problems is made in Version 3, but this is done with large infusion of empirical equations and new model parameters. The model has evolved into an extremely complex form with a very large number of parameters. This seems to deviate from the original intent of the third-generation models. In addition, the complexity of the model and the large number of parameters suggest that parameter extraction task for BSIM3 could be complicated. The BSIM3v3[24] has several new features as compared with BSIM3v2. A single I-V expression describes drain-current and output-conductance characteristics from the subthreshold to the strong inversion as well as from the triode to the saturation regions. Such formula guarantees continuities of I_{DS}, gds, gm and their derivatives throughout all V_{GS} and V_{DS} bias conditions. New width dependencies for bulk charge and source/drain resistance are included. This enhances the accu-

racy in modeling the narrow-width devices. The charge/capacitance model is still based on the BSIM1 structure including more high-order effects in modeling the saturation voltage and the active channel width and length. Non-quasi-static model expression is an option for charge/capacitances in BSIM3v3. It is based on the Elmore equivalent circuit to model the channel charge and channel time constant. However, the RC network and the time constant from gate to source and drain are not considered. The BSIM3v3 was originally intended for one set of parameter values fitting the whole designing geometry space. It has about 110 parameters. However, the extraction procedure is very complicated. Many parameters are difficult to extract and obtain the proper values. Therefore, the'binning" is still applied on BSIM3v3 and it results the number of parameters to be more than 300.

2.2.3.2 The MOS Model-9

The MOS Model-9 model was developed at Philips Laboratories [25]. Numerical smoothing functions are added to the MOS Model-9 model to allow for the use of a single expression for device characteristics, e.g. the drain current, conductances, or terminal charges, over the entire operating range of a transistor. The geometry dependence is included with an HSPICE-Level-28-like approach. However, unlike the second-generation models, this method is applied selectively to only certain parameters, and is used in different ways for different parameters. This makes the model more amenable to "binning". In the threshold-voltage modeling, besides the non-uniform doping effects, more efforts was spent on describing the drain-induced-barrier-lowering effect. The effect of static feedback on the threshold voltage is also considered. This effect is particularly important at large drain

biases, when the drain depletion region is a major portion of the total device depletion region. The effective carrier mobility only includes the first-order terms from the vertical and lateral field effects. The terminal charge is derived with gradual channel approximation for different operation regions, and the smooth functions are used to unify the expressions. With fewer number of parameters, the unified current and terminal charge expressions have a simpler format than BSIM3v3. It is easier to perform the "binning" parameter extraction.

2.2.3.3 The Enz-Krummenacher-Vittoz (EKV) Model

The Enz-Krummenacher-Vittoz (EKV) model [13] is clearly oriented toward use in low power analog circuit design. While it contains many third-generation features, the EKV model stands somewhat apart from other models, in that it employs a new and fresh approach to the study of the analytical modeling of the FET. Rather than use the source node as the voltage reference point, the substrate node serves this role; this allows the source and drain to be treated symmetrically, with separate voltages, which is particularly useful in circuits where the FET is used bi-directionally (a common practice in analog circuits). The EKV model develops a somewhat more involved and physically detailed description of the inversion charge. Like the third-generation models and other candidate models, it also uses one drain current equation and a number of smoothing functions, to ensure continuity of that drain current equation and its first derivatives. In contrast to the Power-Lane model and PCIM, which appear to be finished models, the EKV model is a work in progress, and continues to be improved and extended. Although the EKV model includes only two parameters for the description of short channel effects, it has

demonstrated good results using a single parameter set for all geometries for channel lengths as short as 0.7 μm [13].

2.3 Future Needs

As the CMOS technologies advance to the deep-submicron for low-voltage/low-power and high-speed/high-frequency applications, the accuracy and efficiency of MOS transistor models have to be improved. In the past, most of the MOS transistor modeling work was focusing on the drain current and the terminal charge behavior at the MHz range. Typically, model development was trying to improve the linkage between the technologies and the model behavior. However, the parameter extraction was usually not carefully considered during the model development. This results in a large number of parameters which can not be easily extracted, and the extracted results are highly user- and program-dependent. On the other hand, the charge/capacitance model was derived associated with the DC model and also affected by DC model parameters. Once the DC model parameters are extracted, the charge characteristic is determined accordingly. This leaves little room to match the charge/capacitance behavior, and the results, typically, may not be as good as DC model. For the digital circuits, it does not cause significant trouble, once good DC model behavior is obtained. However in analog circuit design, the charge/capacitance characteristics are as important as the DC part. For the high-frequency behavior, it is even more important to achieve accurate charge/capacitance modeling. Especially, in the low-voltage design, a transistor can be biased near the transition between different operation regions. Although the DC may have very good accuracy, the improper model of the charge

behavior may result in a significant error of the capacitance values in the transition region. Besides the intrinsic capacitance characteristics, as the channel length decreases to the deep-submicron range, the overlap capacitance and the space charge near the lightly-doped diffusion (LDD) portion become more important. The overlap capacitance also shows bias-dependency on the vertical field, as affected by the gate voltage and substrate voltage related to drain or source [22]. So far, only the BSIM3v3 model includes the gate-bias dependency on overlap capacitances. On the other hand, almost all the available MOS transistor model, do not consider the high-speed and high-frequency operation effects. The quarter-micron CMOS application has been pushed to GHz operation frequency, e.g. Personal Communication Services (PCS) at 1.9 GHz. Under that frequency range, the MOS transistor behavior is no longer dominated by the intrinsic behavior. The terminal resistance, especially the gate resistance, and substrate coupling and loss effects play very important roles. The model development can not just be looking to the bias geometry dependent characteristics of the transistor operation. The frequency effect has to be included and carefully considered. In either the high-speed large signal circuits or the high-frequency small-signal operation circuits design, the parasitic effects caused by substrate coupling and terminal resistances can result the error of the signal phase and the magnitude. The development of advanced MOS transistor model has to be focusing on the extrinsic components, including the bias-dependent overlap capacitances and the parasitics also. The representative models are compared with S-CMOS model in Table 2.1

Table 2.1 The representative models comparison with S-CMOS model

MOS Model	Level-3	HSPICE Level 28	BSIM3v3	S-CMOS
Number of parameters	18	37	109	35
Model expression in different regions	different expressions	different expressions	unified expression	unified expression
Continuity of conductance	discontinuous at transitions between different operation regions	continuous at transitions between different operation regions	continuous and smooth through all operation regions	continuous and smooth though all operation regions
Accuracy of drain current and conductances	moderate	good	good	good
Charge/capacitance model	separate equations for different region	separate equations for different region	unified terminal charge equations	single terminal charge equations
Applicable operation frequency	100 MHz range	several hundred MHz	several hundred MHz	up to 10 GHz
Applicable circuit type	Digital VLSI	Mixed signal VLSI	Mixed-signal VLSI	Mixed-signal VLSI
Applicable technology	1.2 μm	0.7 μm	deep-submicron	deep-submicron

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Chapter 3

S-CMOS DC Model

S-CMOS Model solves the continuity problems of the transition regions, and provides a good differentiable drain current expression. Typically, for the long-channel device, the channel-length reduction can be easily modeled by a function of drain voltage (V_{DS}). However, in the short-channel behavior, the channel-length reduction can be affected by the original channel length. This function, combined with the using of two drain-induced lowering effect parameters, and in threshold voltage prediction can perform the output conductance in the saturation region very well. In the transition between the triode and saturation regions, a hyperbola function [8] is applied to smooth out the abrupt transition. Therefore, the continuous drain current behavior in the strong-inversion region, including the triode and saturation regions, can be described by a single equation without any iteration steps. For the transconductance smoothing effect in the transition between weak- and strong-inversion regions, instead of the conventional technique, a new approach by using the interpolation [9] and sigmoid functions [17] to combine the diffusion and drift compo-

nents together is applied on S-CMOS Model. Thus, the Universal Expression of DC MOS transistor model can be constructed which provides good results of drain current, output conductance, and transconductance.

This development is based upon finding solutions to Poisson's equation using Gradual Channel Approximation (GCA) and Quasi–Static Two Dimensional Approximation (QTDA)[3]. It includes compact, analytical expressions for the following physical phenomenon observed in present day MOS devices [1]:

- Non–uniform doping effect (in both lateral and vertical directions),
- Short and narrow channel effects on threshold voltage,
- Mobility reduction due to vertical field,
- Bulk charge effect,
- Carrier velocity saturation. (Mobility Effect),
- Drain–induced barrier lowering (DIBL) Effect,
- Channel length modulation (CLM) Effect,
- Subthreshold conduction,
- Source/drain parasitic resistances.
- Temperature Dependency, and
- Noise Effects.

3.1 Threshold Voltage

Accurate modeling of threshold voltage (V_{th}) is one of the most important requirements for the precise description of electrical characteristics of a transistor. In addition, it serves

as a useful reference point for the evaluation of device operation voltage. The whole device operation region can be divided into three operational regions [10]. First, if the gate voltage is greater than the threshold voltage, the inversion charge density is larger than the substrate doping concentration. The MOSFET operates in the strong inversion region and drift current is dominant. Second, if the gate voltage is much less than the threshold voltage, the inversion charge density is smaller than the substrate doping concentration. The MOSFET operates in the weak inversion (or subthreshold) region. Diffusion current operates dominant. Lastly, if the gate voltage is very close to the threshold voltage, the inversion charge density is close to the doping concentration and the MOSFET is operating in the transition region. In such a case, both diffusion and drift currents are equally important.

3.1.1 Standard Expression

The standard threshold voltage of a MOSFET with long channel length/width and uniform substrate doping concentration is given by [3]

$$\begin{aligned} V_{th} &= V_{FB} + \phi s + \frac{\sqrt{2 \cdot \varepsilon_{si} \cdot q \cdot N_a \cdot (\phi s - V_{BS})}}{C_{OX}} \\ &= V_{tho} + \gamma(\sqrt{\phi s - V_{bs}} - \sqrt{\phi s}), \end{aligned} \tag{3.1}$$

where,
$$\gamma = \frac{\sqrt{2\varepsilon_{si} q N_a}}{Cox}, \tag{3.2}$$

and
$$\phi s = 2 \cdot \frac{K_B T}{q} \ln\left(\frac{N_a}{n_i}\right), \tag{3.3}$$

$$V_{FB} = \phi_{ms} - \frac{Q_{OX}}{C_{OX}} \quad . \tag{3.4}$$

Here, V_{FB} is the flat band voltage, V_{tho} is the threshold voltage of the long channel device at zero volt substrate bias, γ is the substrate bias effect coefficient, N_a is the substrate doping concentration, ϕ_{ms} is a work function difference between gate and substrate. In Eq.(3.1), it is assumed that the channel is uniform and makes use of the one dimensional Poisson's equation in the vertical direction of the channel. This expression is valid only when the substrate doping concentration is constant and the channel length is long. Under these conditions, the potential is uniform along the channel. But in reality, these two conditions are not always satisfied. Modifications have to be made when the substrate doping concentration is not uniform or and when the channel length is short and/or narrow.

3.1.2 Non–Uniform Doping Effect

The substrate doping level is not constant in the vertical direction. The substrate doping concentration is usually higher near the silicon to silicon dioxide interface (due to the threshold voltage adjust implant) than deep into substrate. The distribution of impurity atoms inside the substrate is approximately a half gaussian distribution [14,10]. This non–uniformity will make a function of the substrate bias. If the depletion width is less than x_t as shown in Fig.3.1., N_a in Eq.3.2 is equal to N_{ch}. Otherwise, it is equal to N_{sub}. The body effect coefficients are defined by

$$\gamma_1 = \frac{\sqrt{2\varepsilon_{si} q N_c}}{C_{ox}}, \tag{3.7}$$

$$\gamma_2 = \frac{\sqrt{2\varepsilon_{si} q N_s}}{C_{ox}}. \tag{3.8}$$

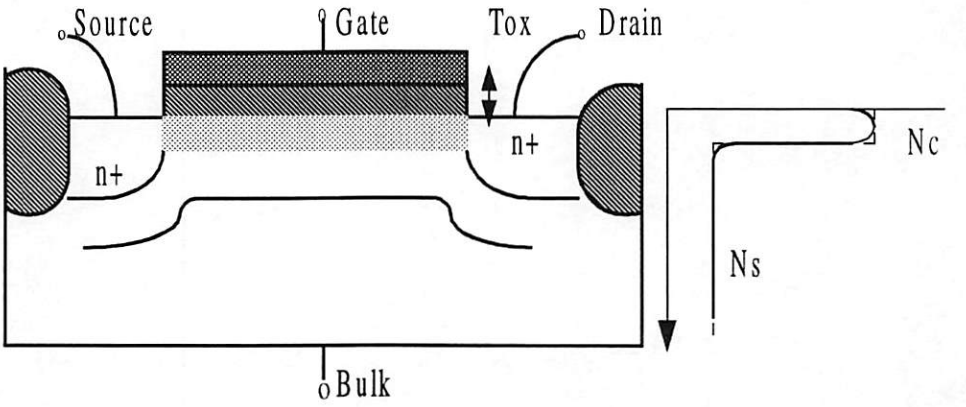

Figure 3.1. Schemetic of non-uniform doping concentration along the channel

3.1.3 Drain–Induced Barrier Lowering (DIBL)

Threshold voltage can be approximated as a linear function of the drain voltage. As the channel length L decreases, depletion is depleted more in the region under the inversion layer[3]. The channel layer are more attractive for electrons. As a result, the device can conduct more current than what would be predicted from long channel theory for a given V_{GS}.

3.1.4 Narrow Channel Effect

The actual depletion region in the channel is always larger than what is usually assumed under the one–dimensional analysis due to the existence of fringing fields [3]. This effect becomes very substantial as the channel width decreases and the depletion region underneath the fringing field becomes comparable to the "classical" depletion layer formed from the vertical field. In addition, we must also consider the narrow width effect for small channel lengths.

3.1.5 Short Channel Effect

The threshold voltage of a long channel device is independent of the channel length and the drain voltage. However, as the channel length becomes shorter and shorter, the threshold voltage shows a greater dependence on the channel length and the drain voltage. The dependence of the threshold voltage on the body bias becomes weaker as channel length becomes shorter, because the body bias has less control of the depletion region[3]. Short–channel effects must be included in the threshold voltage in order to model deep–submicron devices correctly. δVth is the threshold voltage reduction due to the short channel effect,

$$\Delta V_{th} = \frac{Q_{FS}}{C_{ox} L_{eff} W_{eff}}, \tag{3.9}$$

$$Q_{FS} = 2 W_{eff} Q_o K_o \left[1 - e^{-\frac{L_{eff}}{K_o}} \right]. \tag{3.10}$$

In MOSFET devices, the threshold voltage decreases monotonically with decreasing channel length due to charge-sharing effect by the drain and source terminals with the gate

terminal. This is called short-channel effects on threshold voltage. However, it has been observed that the threshold voltage in some devices increases with initial decreasing of the channel length. After it reaches a maximum value, it starts to decrease. Modeling of the reverse short-channel effects on threshold voltage was originally proposed by N. Arora and M. Sharma [1],

$$\Delta V_{th} = \frac{2Q_o K_o}{C_{ox} L_{eff}} \left[1 - e^{-\frac{L_{eff}}{K_o}} \right], \tag{3.11}$$

$$\eta_1 = K_1 \phi_s,$$

$$\eta_2 = \frac{2Q_o \eta_3}{C_{ox}} .$$

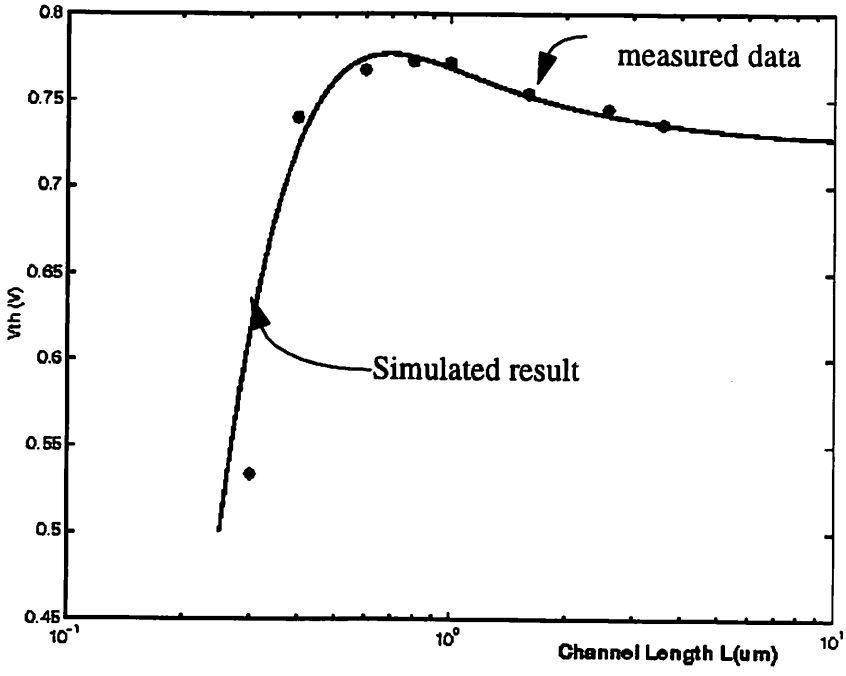

Figure 3.2 Reverse Short Channel Effect on Threshold Toltage

Including all the effects discussed above, V_{th} can be expressed as following [4]

$$V_{th} = V_{FB} + \phi_S + \left(\gamma_1 - \frac{\gamma_{1L}}{L}\right)\left(\sqrt{\phi_s - V_{bsh}} - \sqrt{\phi_S}\right) - \frac{Ks}{2}\left(\sqrt{\phi_s - V_{bsh}} - \sqrt{\phi_s}\right)^2 + \gamma_2\left(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s - V_{BSh}}\right) + \frac{K_{NZ}}{W} + \frac{K_{NB} \cdot V_{BS}}{W} - \left(\eta_Z + \frac{\eta_L}{L}\right)V_{DS} - \frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - \exp\left(-\frac{L}{\eta_3}\right)\right), \quad (3.12)$$

where,

$$V_{BSh} = \frac{1}{2}\left(V_{BS} + K_{BSh}V_{BST} + \sqrt{\left(V_{BS} + K_{BSh}V_{BST}\right)^2 - 4V_{BSh}V_{BST}}\right), \quad (3.13)$$

and

$$V_{BST} = \phi_s - \left(\frac{\gamma_1 - \gamma_2}{Ks} + \sqrt{\phi_s}\right). \quad (3.14)$$

3.1.6 Temperature dependency

Circuit designers require the ability to predict the variation of circuit performance with temperature. Typical temperature ranges used for performance verification are 0 ^{o}C to 70 ^{o}C for commercial applications and -55 ^{o}C to 125^{o}C for military applications. The changes in temperature predominantly affect the threshold voltage and carrier mobility of the transistors [3]. The S-CMOS Model uses the parameter B_{TH} to calculate the temperature dependence of the threshold voltage. The expression used to calculate the threshold voltage in the S-CMOS Model is given in Eq.(3.12) [17]. The threshold voltage changes with temperature because of changes in the energy required to move electrons into the

conduction band in order to form the channel. In all cases the gates were n-type doped polysilicon. The components of the threshold voltage expression that are highly sensitive to temperature include the flat-band voltage and the surface-inversion potential. The expression for the surface inversion potential of the p-type substrate of NMOS transistors can be rewritten as [16],

$$|\phi_s| \approx \frac{2kT}{q} \cdot \ln\left[\frac{N_{sub}}{n_i}\right]. \tag{3.15}$$

The doping concentration in the substrate is given by N_{sub}, and this is independent of the temperature. The relationship between the intrinsic carrier concentration and the temperature is given by,

$$n_i \propto T^{\frac{3}{2}} \cdot e^{-\frac{E_G}{2kT}} . \tag{3.16}$$

The energy band-gap of silicon as a function of temperature is given by[17],

$$E_G(T) = 1.16 - \frac{7.02 \times 10^{-4} \cdot T^2}{T + 1108} . \tag{3.17}$$

This expression has a negative temperature coefficient. The temperature dependence of the threshold voltage in the S-CMOS Model has been included by calculating the flat-band voltage and surface-inversion potential as temperature-dependent quantities. The nominal temperature, T_0, is the temperature at which the drain current parameter values were extracted. From Eq.(3.15) (3.16), we can write,

$$\frac{\phi_s(T)}{T} \approx \frac{2k}{q} \cdot \ln\left[\frac{N_{sub}}{n_i(T)}\right], \tag{3.18}$$

$$\frac{\phi_s(T_0)}{T} \approx \frac{2k}{q} \cdot \ln\left[\frac{N_{sub}}{n_i(T_0)}\right] . \tag{3.19}$$

Subtracting (3.18) from (3.19) and rearranging terms, we can write,

$$\phi_s(T) = \phi_s(T_0)\left[\frac{T}{T_0}\right] - \frac{2k}{q} \cdot \ln\left[\frac{n_i(T)}{n_i(T_0)}\right]. \tag{3.20}$$

Using the temperature dependence of the intrinsic carrier concentration given in Eq. (3.16), we can write,

$$\frac{n_i(T_0)}{n_i(T_0)} = \left[\frac{T}{T_0}\right]^{\frac{3}{2}} \cdot e^{-\frac{E_G(T)}{2kT} + \frac{E_G(T_0)}{2kT_0}}, \tag{3.21}$$

which can be written as,

$$-\frac{2kT}{q} \cdot \ln\left[\frac{n_i(T)}{n_i(T_0)}\right] = -\frac{2kT}{q} \cdot \frac{3}{2} \cdot \left[\frac{T}{T_0}\right] + E_G(T) - E_G(T_o)\left[\frac{T}{T_0}\right], \tag{3.22}$$

and

$$\phi_s(T) = \phi_s(T_0)\left[\frac{T}{T_0}\right] - \frac{3kT}{q} \cdot \ln\left[\frac{T}{T_o}\right] + E_G(T) - E_G(T_o)\left[\frac{T}{T_0}\right]. \tag{3.23}$$

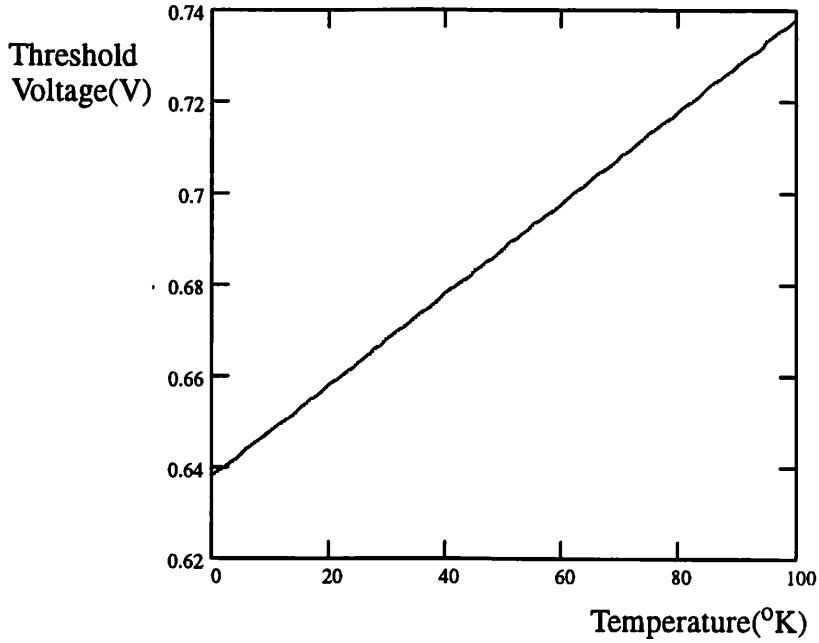

Figure 3.3 Temperature dependency on V_{th}: plot of the threshold voltage vs. temperature.

For an NMOS transistor which has a p-type substrate and an n-type polysilicon gate, the flat-band voltage is given by,

$$V_{FB} = -\frac{E_G}{2} - \frac{\phi_S}{2} - \frac{Q_o}{2} . \tag{3.24}$$

Based upon this expression, the temperature dependence of the flat-band voltage is given by,

$$V_{FB}(T) = V_{FB}(T_0) + \frac{E_G(T_0)}{2} + \frac{\phi_S(T_0)}{2} - \frac{E_G(T)}{2} - \frac{\phi_S(T)}{2} . \tag{3.25}$$

The temperature dependence of the threshold voltage can also be simulated by using a threshold-voltage temperature-coefficient, and the temperature-dependent threshold voltage can be calculated from,

$$V_{th}(T) = V_{th}(T_0) + B_{th}[T - T_0] . \tag{3.26}$$

The simulation result of temperature dependency of threshold voltage is shown in Fig. 3.3.

3.2 Mobility Model

3.2.1 Effective Mobility

An accurate model for surface carrier mobility is very critical to the accuracy of a MOSFET model. because carrier drift velocity is one of the most important parameters that affects device characteristics. S-CMOS Model uses a simple and semi–empirical saturation velocity model [17] given by:

$$v = \frac{\mu E}{1 + \frac{E}{E_{crit}}} \quad . \tag{3.27}$$

The parameter E_{crit} corresponds to the critical electrical field at which the carrier velocity becomes saturated in order to have a continuous velocity model at $E = E_{crit}$. The intrinsic carrier mobility at the siliccon/gate-oxide interface depends on temperature and can be considered as a fitting model parameter. During device operation, the mobility of carriers is reduced due to the transverse and lateral fields. Effective mobility is a function of (V_{gs}-V_{th}), V_{BS}, and V_{DS}. In S-CMOS Model a mobility reduction factor is used to improve accuracy of the effective mobility expression[4],

$$\mu_{eff} = \frac{\mu_o}{M_r}, \tag{3.28}$$

where,

$$M_r = \left[1 + \left(U_{GSZ} + \frac{U_{GSL}}{L}\right)(V_{GS} - V_{th}) + \left(U_{GSZ2} + \frac{U_{GSL2}}{L}\right)(V_{GS} - V_{th})^2 \right.$$
$$\left. - U_{BS}(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s}) + U_{DS}V_{DS} \right] \cdot \left[1 + \frac{V_{DS}(1 - f_s)}{E_{crit} \cdot L}\right]. \tag{3.29}$$

The simulation result of mobility reduction factor is shown in Fig. 3.4.

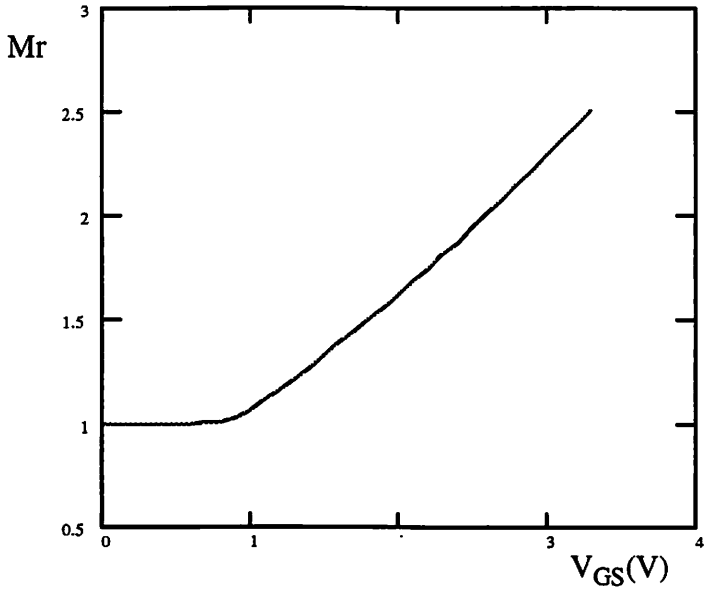

Figure 3.4 Plot of the mobility degradation factor(M_r) versus V_{GS} with V_{DS}=3.3V, V_{BS}=1V

3.2.2 Unified Expression

By including the continuity factor, unified expression of mobility degradation factor can be expressed by,

$$M_r = \left[1 + \left(U_{GSZ} + \frac{U_{GSL}}{L}\right)(V_{GSh} - V_{th}) + \left(U_{GSZ2} + \frac{U_{GSL2}}{L}\right)(V_{GSh} - V_{th})^2 - U_{BS}(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi_s}) + U_{DS}V_{DS}\right] \cdot \left[1 + \frac{V_{DS}(1-fs)}{E_{crit} \cdot L}\right], \quad (3.30)$$

where

$$V_{GSh} = \frac{1}{2}\left[V_{GS} + K_{GSh}V_{th} + \sqrt{(V_{GS} + K_{GSh}V_{th})^2 - 4V_{GS}V_{th}}\right]. \quad (3.31)$$

Here, parameters U_{GSZ}, U_{GSL}, and U_{BS} are used to model the reduction of mobility due to carrier scattering by the transverse electric field. The gate-voltage contribution to transverse field is modeled by U_{GSZ}, while the parameter U_{GSL} is a short-channel correction parameter. The parameter U_{DS} is used to model the effect by drain voltage. The continuous velocity saturation effect due to the influence of the lateral field in the channel on the carrier mobility is also included by the term, $\frac{V_{DS}(1-f_s)}{E_{crit}}$. Here, the critical field, E_{crit}, for velocity saturation is specified as a model parameter.

3.2.2 Temperature dependency

The carrier mobility has a logarithmic dependence on temperature and the electron mobility follows a $T^{-4.2}$ dependence, while the hole mobility follows a $T^{-2.2}$ dependence [16]. The effect of temperature on the mobility is calculated by using the parameter B_m and B_{ns}. In S-CMOS Model, the intrinsic carrier mobility depends upon the temperature as given by,

$$\mu(T) = \mu(T_0)\left[\frac{T}{T_0}\right]^{-Bm} . \tag{3.32}$$

where B_m is the slope of the $\log(\mu_0)$ vs. $\log(T)$ curve.

The saturation velocity has a $T^{-0.87}$ dependence for electrons and a $T^{-0.53}$ dependence for holes [22]. This can be written as,

$$V_{sat} \propto T^{-Bm} . \tag{3.33}$$

Since the saturation velocity, carrier mobility, and critical field for velocity saturation are related by,

$$E_{CRIT} \propto \frac{V_{sat}}{\mu_{eff}}, \tag{3.34}$$

Ecrit and the temperature dependence of the saturation velocity can be incorporated into the critical field for velocity saturation. In the S-CMOS Model this is. included as,

$$E_{CRIT}(T) \propto E_{CRIT}(T_0) \cdot \left[\frac{T}{T_0}\right]^{-Bns + Bm}. \tag{3.35}$$

where B_m is the S-CMOS Model parameter for the temperature dependence of the saturation velocity. The simulation result of reduction faction mobility is shown in Fig. 3.5.

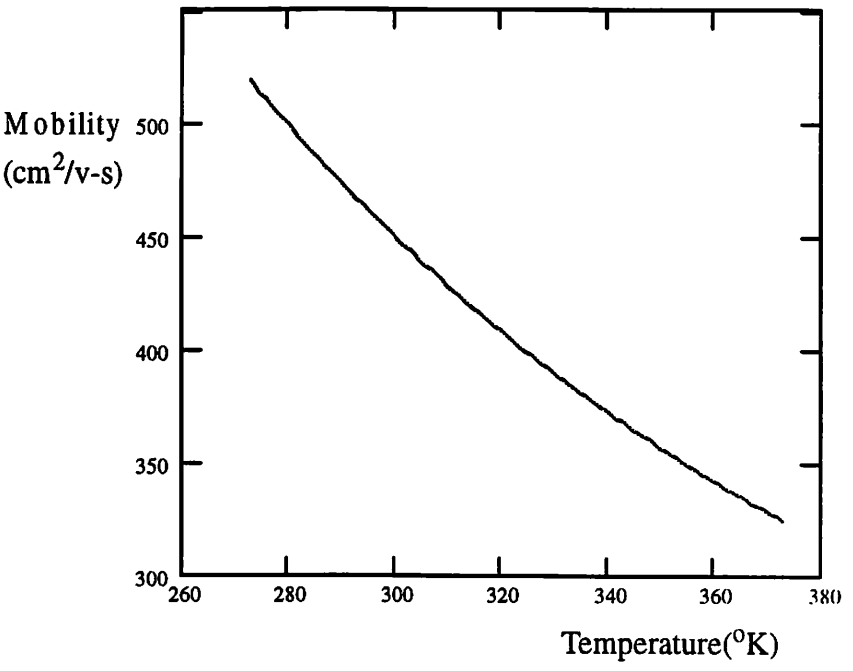

Figure 3.5 Graphical illustration of temperature dependency of the mobility.

3.3 Channel Length Modulation (CLM) Effect

In the saturation region, the effective channel length, L_{eff} = L-dL, determined from the channel-length modulation effect is reduced as the drain voltage increases. Due to this effect, the drain current is increased by a factor, L/L_{eff}. Typically, for the long channel length device, the channel-length reduction, dL, can be modeled by a function of V_D. However, for submicron devices, the channel length reduction effect should include the original channel length. So, instead of looking into the individual dL, the fraction of dL and L should be taken into account for modeling the channel-length modulation effect. By applying the Taylor series expansion on it, this factor can be approximated by,

$$\frac{L}{L_{eff}} = 1 + \frac{dL}{L} \quad . \tag{3.36}$$

Here, the term, dL/L, is a function of (V_{GS}-V_{th}), (V_{DS}-V_{DSAT}) and, V_{BS} [3, 4, 12]. In S-CMOS Model, the expression for the channel-length modulation effect is described by [3, 4, 7]:

$$f_L = \frac{dL}{L} = \frac{\lambda_D \cdot [\sqrt{\phi_D + V_{DS} - V_{DSAT}} - \sqrt{\phi_D}]}{L \cdot \left[(V_{GS} - V_{th})^{\frac{3}{2}} + \lambda_G \right] \cdot \left[\frac{\lambda_B^2 \cdot \lambda_{BS}}{\lambda_B - V_{BS}} \right]} \quad . \tag{3.37}$$

Here, λ_D, λ_G, λ_B, λ_{BS}, and ϕ_D are model parameters. V_{DSATh}, is used to replace V_{DSAT} to set f_L equal to zero in the triode region and Eq.(3.37) can be modified by

$$f_L = \frac{dL}{L} = \frac{\lambda_D[\sqrt{\phi_D + V_{DS} - V_{DSATh}} - \sqrt{\phi_D}]}{L \cdot \left[(V_{GSh} - V_{th})^{\frac{3}{2}} + \lambda_G\right] \cdot \left[\frac{\lambda_B^2 \cdot \lambda_{BS}}{\lambda_B - V_{BS}}\right]} \quad . \tag{3.38}$$

The simulation result of reduction faction mobility is shown in Fig. 3.5

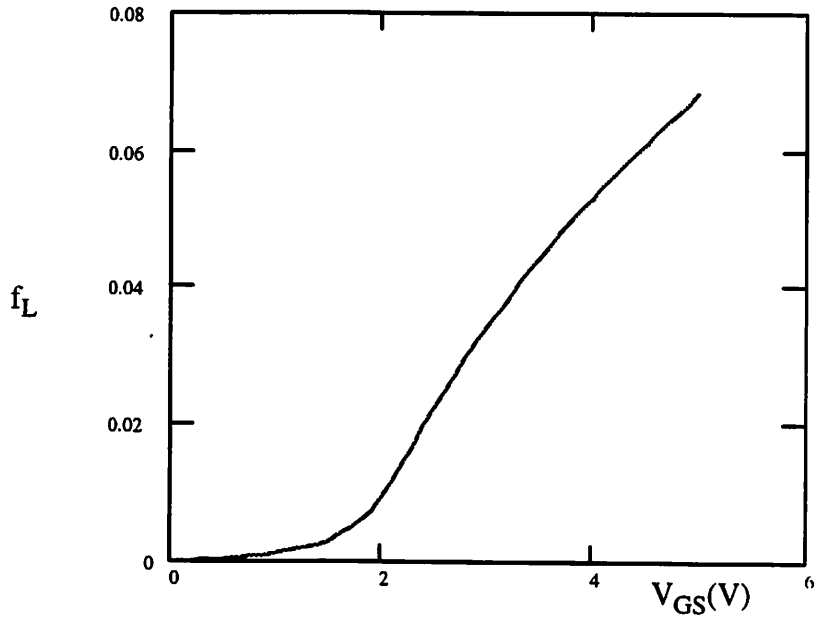

Figure 3.6 Plot of the f_L(channel length reduction factor) versus V_{GS} with V_{DS}=3V and V_{BS}=0V

3.4 Parasitic Resistances

The drain current expressions that have been derived in the previous sections are used to model the drain current within the intrinsic region of the MOS transistor. In deep-micron transistors, the parasitic source and drain resistances contribute a significant voltage drop that can affect the performance of the transistor. S-CMOS Model includes expressions to calculate the effect of these extrinsic parasitic resistances. The different components of the parasitic resistance in the source/drain region are shown in Fig. 3.7. The components

include, R_{CO}: the contact resistance, R_{sh}: the diffusion sheet resistance, R_{sp}: the spreading resistance, and R_{ac}: the accumulation layer resistance. The contact resistance, Rco, is the resistance between the metal contact and the diffusion layer under the contact window. When the length of the contact window is very small, the contact resistance is inversely proportional to this length. However, when the length of the contact window is sufficiently large, the contact resistance saturates at a minimum value which is independent of the length of the window.

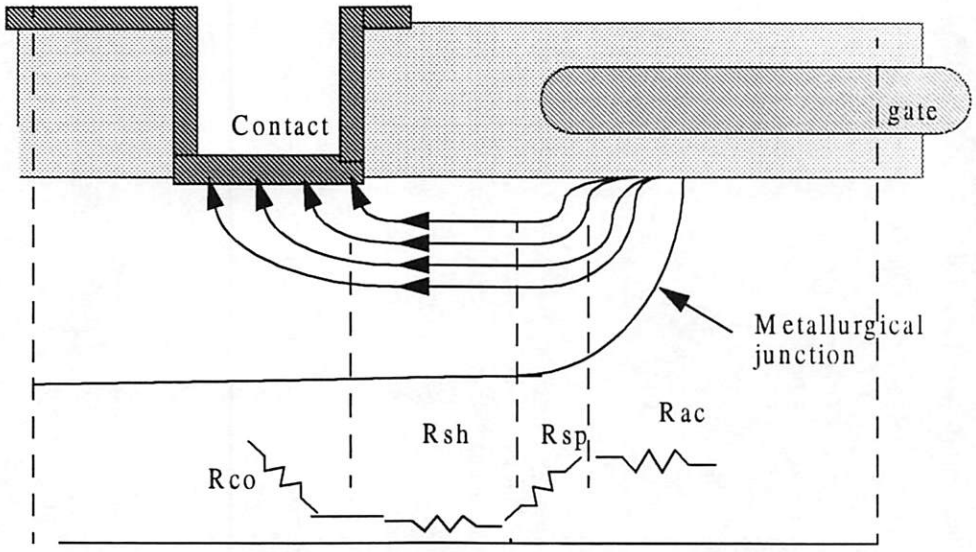

Figure 3.7 Components of parasitic resistance in source/drain regions [1]

The contact resistance is given by [5,18],

$$Rco \cong \frac{\sqrt{\rho_{sh}\rho_c}}{W}. \tag{3.39}$$

where ρ_{sh} is the sheet resistance per square of the source/drain diffusion layer, and ρ_c is the contact resistivity between the metal and diffusion layers. The minimum length of the

contact window that is required for the contact resistance to be independent of this length is frequently ensured by the design rules of the technology. The diffusion sheet resistance, R_{sh}, of the source/drain diffusion region can be calculated from ρ_{sh} and S, the spacing between the contact edge and the channel by [18],

$$Rsh \cong \frac{\rho_{sh} \cdot S}{W} . \tag{3.40}$$

The spreading resistance, R_{sp}, is due to the radially divergent pattern of the current as it flows from the thin channel region to the thicker source/drain diffusion layer. By assuming an abrupt doping profile at the edge of the source/drain diffusion layer, the spreading resistance is given by [16],

$$R_{sp} \cong \frac{0.64\rho_{s/d}}{W} \cdot \ln\left[\frac{0.37X_j}{X_c}\right] . \tag{3.41}$$

where the resistivity and thickness of the source/drain diffusion layer are given by $r_{s/d}$ and X_j, respectively, and X_c is the thickness of the channel. The additional component due to resistance of the accumulation layer, R_{ac}, is significant only in the case of a gradual doping gradient at the edge of the source/drain diffusion layer and goes to zero under the assumption of a step junction. Based upon this analysis, the extrinsic parasitic resistances in the source and drain regions are modeled with a constant term and an inverse width scaling term. The source and parasitic resistance is given by,

$$R_S = R_{SO} + \frac{R_{SW}}{W}, \tag{3.42}$$

$$R_D = R_{DO} + \frac{R_{DW}}{W}. \tag{3.43}$$

3.5 Noise Effect

Noise is caused by the small current and voltage fluctuation generated in the device. The noise generator may be represented as a voltage source in series with the gate of the transistor or as a current source in series with the transistor. The noise associated with these conductances can be represented as voltage sources in series with the conductances or current sources in parallel with the conductance

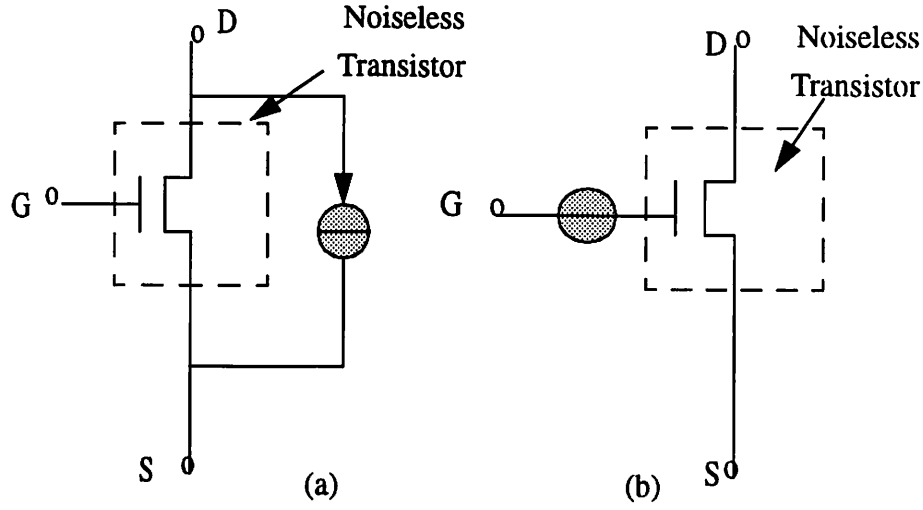

Figure 3.8: Noise mosel (a) Current source model (b) Voltage source model

3.5.1 Thermal Noise Effects

Thermal noise is a physical phenomenon associated with any conductor. This noise is due to the random motion of electrons in the conductor and is directly proportional to the absolute temperature of the conductor. The spectral density of thermal noise is independent of frequency. The thermal noise can be modeled as a current source between source and drain having a Power spectral density (PSD) and equivalent current source is given by:

$$S_{\Delta I_D} = 4kT \cdot \frac{\mu_n}{L^2} \cdot |Q_{inv}|, \tag{3.44}$$

$$\overline{i_{Tn}^2} = S_i(f) \cdot \Delta f = \frac{4kT}{R} \cdot \Delta f \tag{3.45}$$

where k is Boltzmann's constant and δf is the bandwidth.

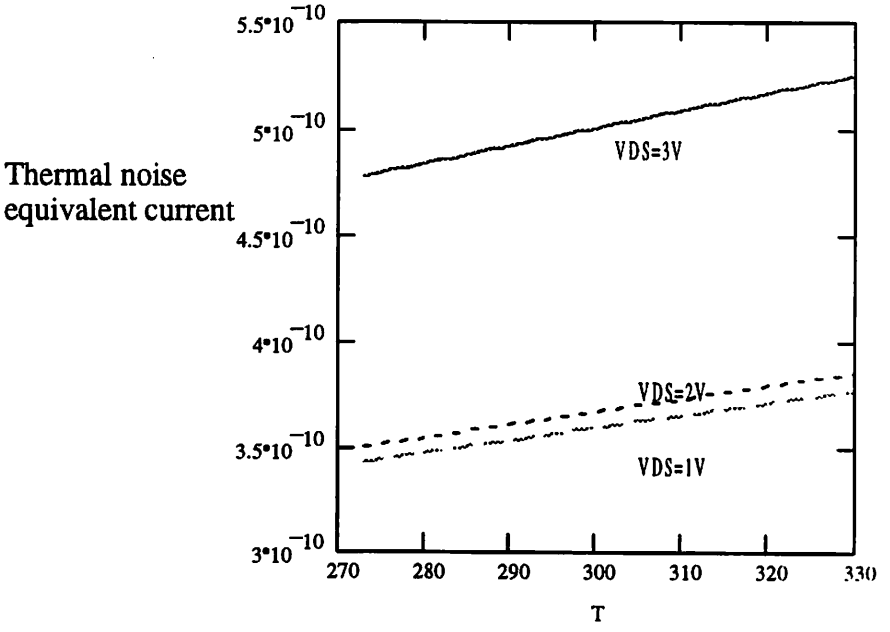

Figure 3.9: Simulation result of thermal noise equivalent current vs. temperature

3.5.2 Flicker (1/f) Noise Effects

Low-frequency noise due to fluctuation of the carrier density caused by trapping of carriers in traps in the oxide and close to Si-SiO2 interface via tunneling effect and fast surface states. Two theories have been proposed to explain the source of flicker noise. The Carrier Number Fluctuation Theory attributes this noise to the random trapping and de-training processes of charges near the oxide-semiconductor interface. The Mobility Fluctuation Theory proposes that the flicker noise is due to fluctuation in the bulk mobility of the car-

riers due to the scattering mechanism. In either case, the flicker noise is associated with the flow of current. The flicker noise also has an inverse dependence on the oxide capacitance since the time-varying component of the oxide interface charge causes changes in the threshold voltage that are inversely proportional to the oxide capacitance. The spectral density of flicker noise is found to have an inverse frequency dependence. Therefore it is frequently referred to as the 1/f noise.

$$\overline{i_{Fn}^2} = S_i(f) \cdot \Delta f = \frac{k_f \cdot I^{AF}}{fb} \cdot \Delta f \,. \tag{3.46}$$

3.5.3 Shot noise

Shot noise comes from the current flow in PN junction. The fluctuation of external current, I, consist of randum and independent current impules. Its mean square value can be expressed as

$$\overline{i_{Sn}^2} = S_i(f) \cdot \Delta f = 2q \cdot I \cdot \Delta f \,. \tag{3.47}$$

where df is the bandwidth, Si(f) is the power spectral density[11].

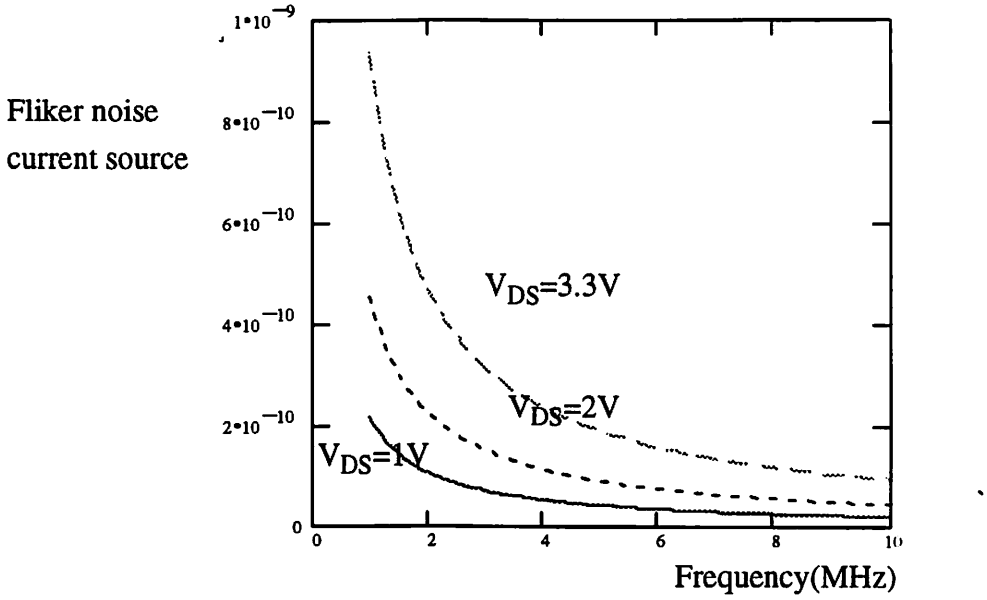

Figure 3.10: Simulation result of Fliker noise equivalent current vs. temperature

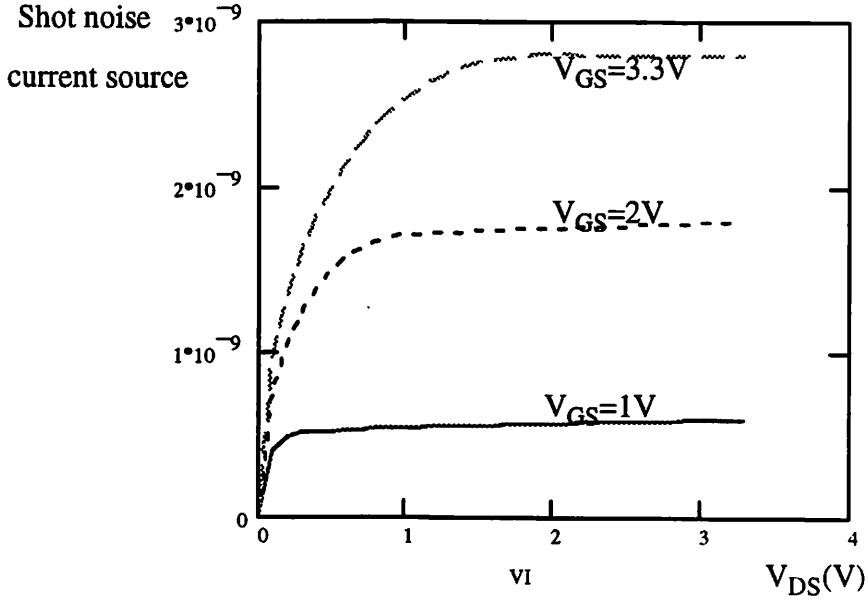

Figure 3.11: Simulation result of shot noise equivalent current vs. V_{DS}

3.5.4 Noise source

Noise can be implemented with the drain and source resistances, shot, and fliker noises The mean square noise current is given by,

$$\overline{i_N^2} = 2qI_{DS} + 4kT \cdot \frac{2}{3} g_m + 4kT \cdot g_D + 4kT \cdot g_S + \frac{Kf \cdot I_{DS}^{Af}}{f \cdot C_{ox} \cdot L_{eff}^2} \quad . \tag{3.48}$$

where g_m is the transconductance of the transistor, g_D and g_S are the conductances of the source and drain regions, Kf is flicker noise coefficient(10^{-19}~10^{-25}) and Af is the flicker noise exponent (0.5~2) [32].

3.6 Unified DC Current Model

3.6.1 Strong-Inversion Current

The transistor starts to operate in the strong-inversion region when the V_{GS}-V_{th} is greater than zero. The strong-inversion current can be obtained from the channel charge density, q_c, which can be expressed as [18]

$$q_C = -C_{OX}[(V_{GS} - \phi_S - V_{FB} - \phi_n) - \gamma_1 \sqrt{\phi_S + \phi_n - V_{BS}}], \tag{3.49}$$

where ϕ_n is the quasi-Fermi potential in the channel region. Therefore, the strong-inversion current can be described by the following expression,

$$I_{DSs} = \mu_{eff} \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \left[(V_{GS} - V_{th}) V_{DS} - \frac{a}{2} \cdot V_{DS}^{2} \right], \tag{3.50}$$

$$a = 1 + \frac{g \cdot \gamma_1}{2\sqrt{\phi_S - V_{BS}}}, \tag{3.51}$$

$$g = 1 - \frac{1}{1.744 + 0.8364(\phi_S - V_{BS})}. \tag{3.52}$$

Due to the change of the channel charge density, the saturation voltage, V_{DSAT} can be determined by,

$$V_{DSAT} = \frac{V_{GS} - V_{th}}{a\sqrt{K}}, \tag{3.53}$$

where

$$K = \frac{1 + V_c + \sqrt{1 + 2V_c}}{2}, \tag{3.54}$$

and

$$Vc = \frac{V_{GSh} - V_{th}}{aE_{critL}}. \tag{3.55}$$

V_{DSAT} determines the V_{DS} boundary between the linear and saturation regions of operation. In order to describe the drain current behavior after the transistor entering the saturation region, $V_{DS} > V_{DSAT}$, a hyperbola interpolation function, V_{DSATh}, proposed by A. Chatterjee, et al. [8] is used to smooth out the abrupt transition from the triode to the saturation regions. V_{DSATh} is given by

$$V_{DSATh} = f_2 - \sqrt{f_2^{\,2} - V_{DS} \cdot V_{DSAT}}, \tag{3.56}$$

$$f_1 = 1 + s, \tag{3.57}$$

$$f_2 = \frac{1}{2}(V_{DS} + f_1 \cdot V_{DSAT}) \quad . \tag{3.58}$$

V_{DSATh} is approximately equal to V_{DS} when the transistor operates in the triode region, while it will saturate at the value of V_{DSAT} in the saturation region. The difference between the function, V_{DSATh}, and the standard hyperbola function is that V_{DSATh} has to be exactly equal to zero at the starting point, $V_{DS} = 0$ in order to describe transistor current behavior properly in the low bias voltages region. This V_{DSATh} is used to replace all the V_{DS} terms of the effective mobility in Eq.(3.28), and drain current expression in Eq.(3.50). So the drain current saturating behavior can be described by the same current equation (3.50) when $V_{DS} > V_{DSAT}$. The smoothing parameter, s, controls the distances of the hyperbola from its asymptotes in order to make the derivative of V_{DSATh} continuous and smooth at the point of $V_{DS} = V_{DSAT}$. s can also be treated as a fitting coefficient for S-CMOS Model.

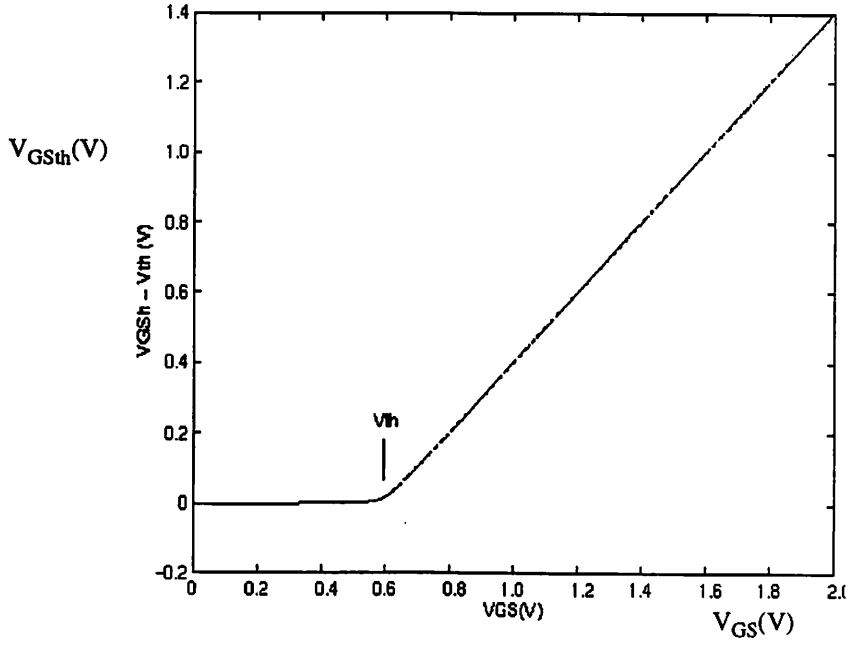

Figure 3.12 Graphical illustration of the function (V_{GSh}-V_{th}) which reduces to zero in weak inversion region

3.6.2 Sub-threshold Drain Current

When $V_{GS} < V_{th}$, the transistor operates in the weak-inversion region. Continuity of the drain current and its derivatives between weak-inversion and strong-inversion region is also highly desirable in low power design. The diffusion component is mainly dominant factor in the weak-inversion region, which can be expressed as [1,9]:

$$I_{DSw} = C_{OX} \cdot \mu_{eff} \cdot \frac{W_{eff}}{L_{eff}} \cdot n \cdot V_T^{\,2} \cdot e^{\frac{V_{GS}-V_{th}}{nV_T}} \cdot \left[1 - e^{-\frac{V_{DS}}{V_T}}\right]. \qquad (3.59)$$

This component increases exponentially with the V_{GS}. The parameter n, is used to model the slope of the diffusion drain current component.

3.6.3 Exponential interpolation Function

For the transconductance smoothing effect in the transition between weak- and strong - inversion regions, most of the models are using the equation, $I_{total} = I_{DSw} + I_{DSs}$, to sum the diffusion and drift components together. Because I_{DSs} is defined to be 0 in weak-inversion region, this equation, I_{total}, still can provide the continuity of drain current. However the derivative of the transconductance is not continuous at the point $V_{GS} = V_{th}$ with this approach. Since in strong-inversion region, the diffusion component of the drain current is much smaller than drift component and can be neglected, Eq.(3.50) and Eq.(3.59) can be combined by using a good and simple interpolation function [8],

$$V_{GSth} = 2 \cdot n \cdot V_T \cdot \ln\left(1 + e^{\frac{V_{GS}-V_{th}}{2nV_T}}\right). \qquad (3.60)$$

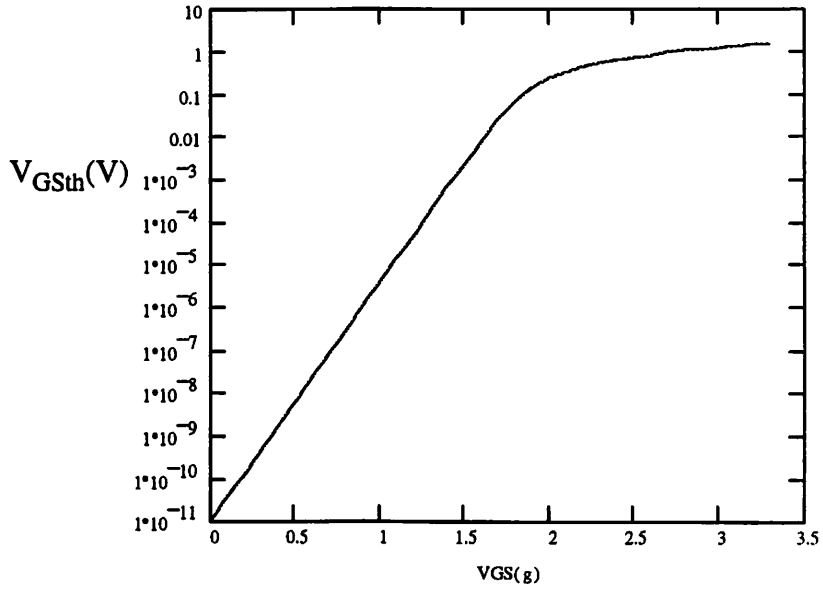

Figure 3.13 Plot of the V_{GSth} versus V_{GS} with V_{DS}=1V, V_{BS}=0V

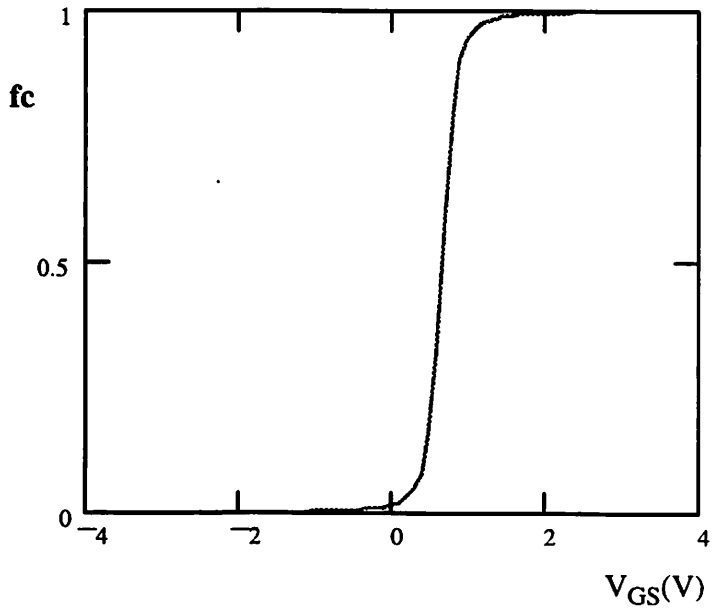

Figure 3.14 Plot of the fc versus V_{GS} with V_{DS}=1V, V_{BS}=0V

A sigmoid function is introduced in S-CMOS Model to smooth out the transitions of different effects from weak-inversion to strong-inversion regions, which is defined by.

$$f_s = \frac{1}{2}\left(1 - \frac{V_{GS} - V_{th}}{\sqrt{(V_{GS} - V_{th})^2 + K_{sig}}}\right). \tag{3.61}$$

3.6.4 Unified DC MOS Model Drain current Expression

The result of our new model shows a good and smooth behavior for the curve from weak- to strong-inversion Therefore, the complete single-equation current expression can be described as follows [17]:

$$I_{DS} = \frac{C_{ox} \cdot \mu_{eff} \cdot W_{eff}}{L_{eff}} \cdot \left[1 - fs \cdot e^{-\frac{V_{DS}}{VT}}\right] \cdot [1 - (1 - f_s) \cdot f_L + f_s \cdot K_{sub}] \cdot$$
$$\times \left[2 \cdot n \cdot V_T \cdot \ln\left(1 + e^{\frac{V_{GS} - V_{th}}{2 \cdot n \cdot V_T}}\right) \cdot V_{DSATh} - \frac{1}{2} \cdot V_{DSATh}^{\,2}\right] . \tag{3.62}$$

This single-equation MOS transistor current model has been successfully implemented to achieve higher accuracy and reduce the computational complexity for the simulation of the mixed-signal VLSI circuits. There are totally 29 parameters included. Since only one equation sets are used to apply on all the regions, the drain current can be calculated directly without any determination of the operation mode. Another advantage of this approach is that it also solves the non-convergence problem of the SPICE simulation. Because those non-convergence problems of the iteration process of the SPICE simulation are due to the discontinuity of the derivative of drain current in transition points from dif-

ferent operation regions. This single-equation expression provides a continuous behavior of all the derivative terms through the whole variables' domain.

3.7 Simulation and Experimental Results for DC Model

This drain current model combines all the effects from different operation regions into a single-equation expression. For the I-V characteristics, the drain current in the saturation region can be modeled accurately. The agreement with the measurement results is very good in both triode and saturation regions. In addition, the simulation results also provide an excellent transition from the triode to saturation regions for both the drain current and output conductance.

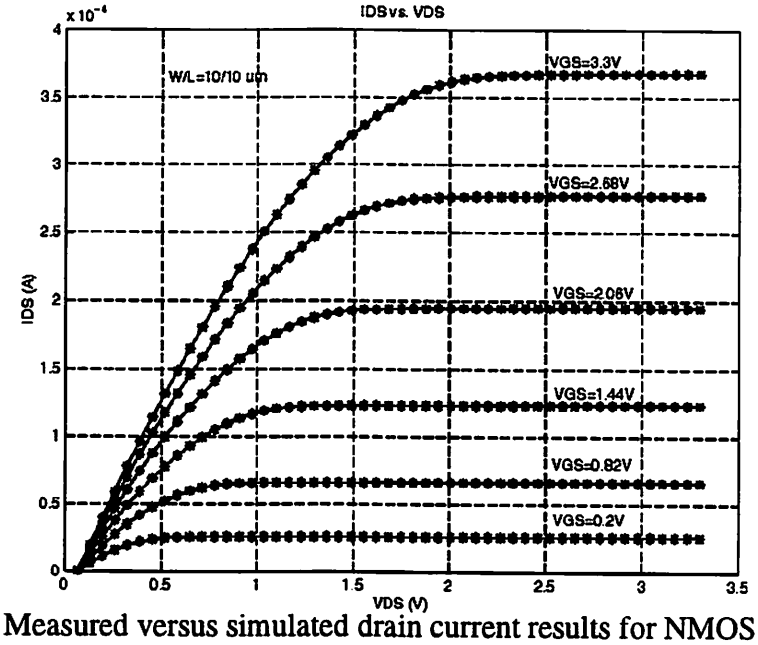

Figure 3.15: Measured versus simulated drain current results for NMOS Transistor with W/L=10μm/10μm, and V_{BS}=0V. [MOSIS 0.35μm Tech].

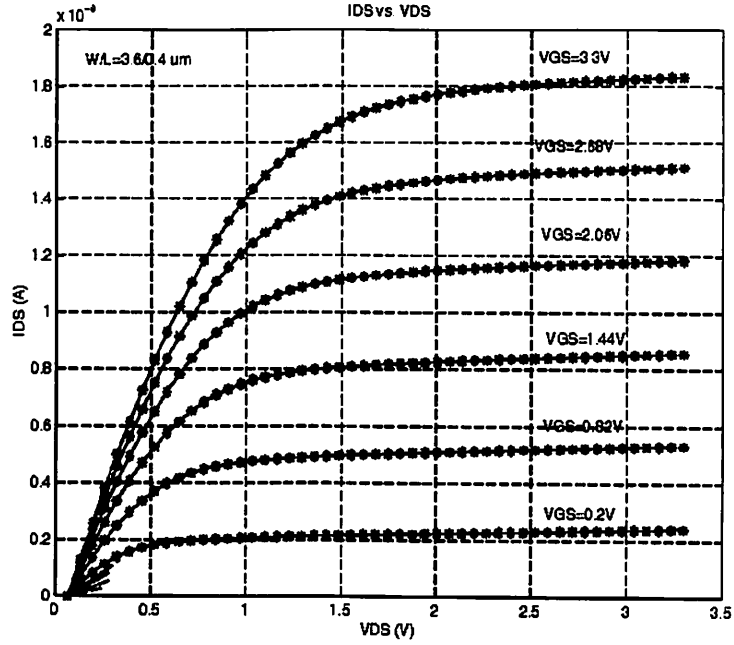

Figure 3.16: Measured versus simulated drain current results for NMOS Transistor with W/L=3.6μm/0.4μm, and V_{BS}=0V. [MOSIS 0.35μm Tech].

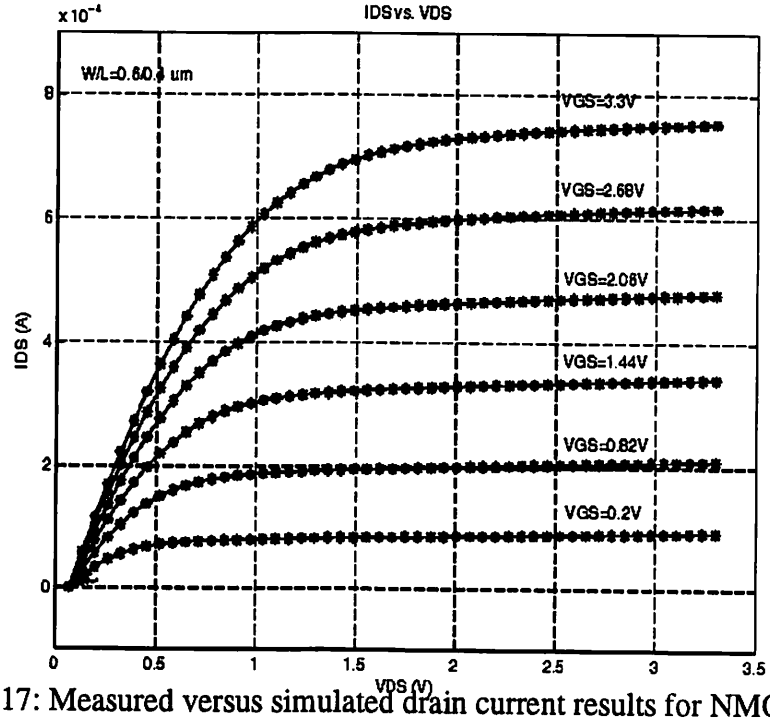

Figure 3.17: Measured versus simulated drain current results for NMOS Transistor with W/L=0.6μm/0.4μm, and V_{BS}=0V. [MOSIS 0.35μm Tech].

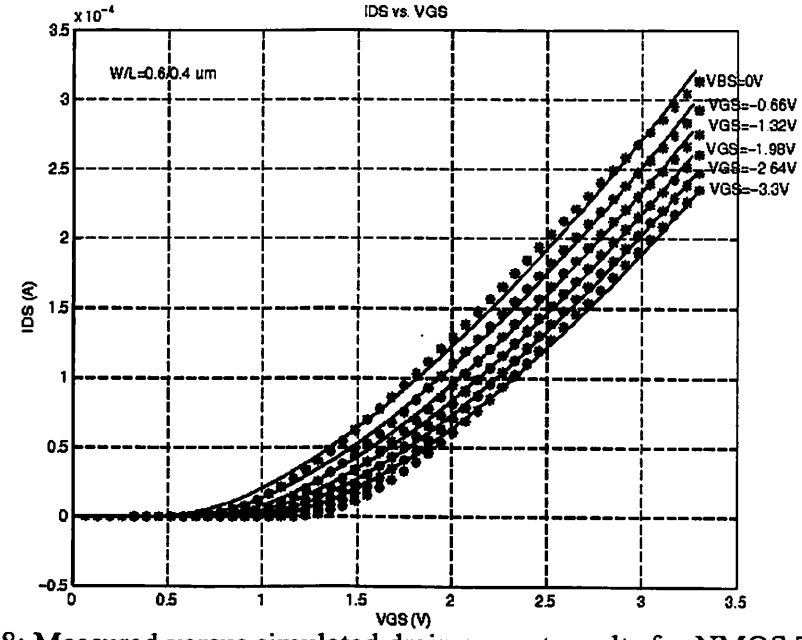

Figure 3.18: Measured versus simulated drain current results for NMOS Transistor with W/L=0.6μm/0.4μm, and V_{DS}=0.2V. [MOSIS 0.35μm Tech].

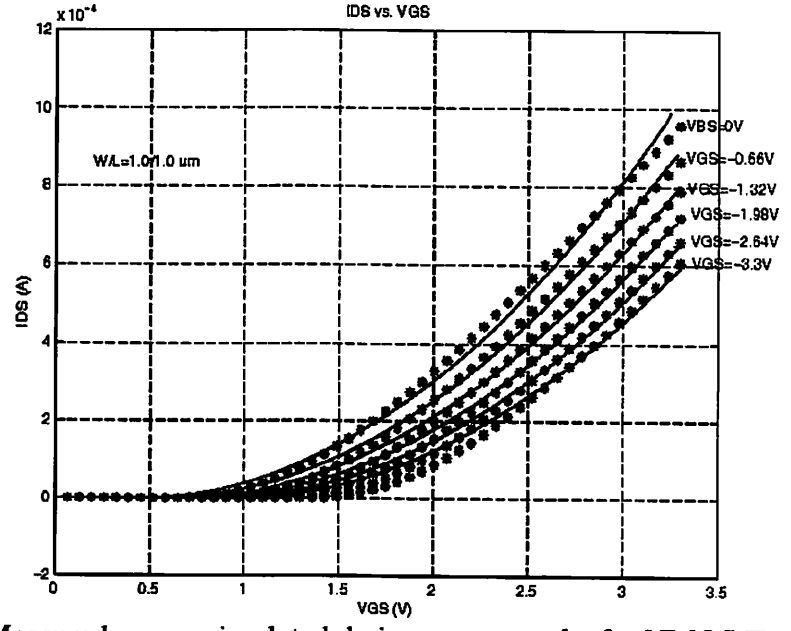

Figure 3.19: Measured versus simulated drain current results for NMOS Transistor with W/L=1.0μm/1.0μm, and V_{DS}=0.2V. [MOSIS 0.35μm Tech].

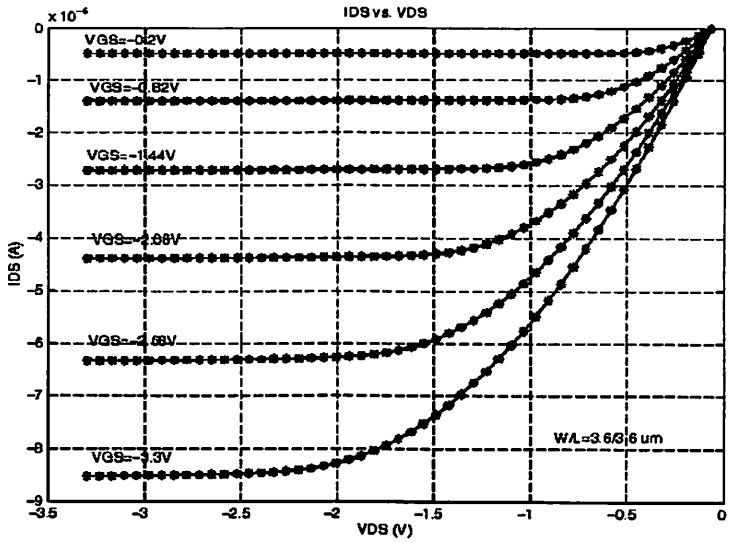

Figure 3.20: Measured versus simulated drain current results for PMOS Transistor with W/L=3.6μm/3.6μm, and V_{BS}=0V. [MOSIS 0.35μm Tech].

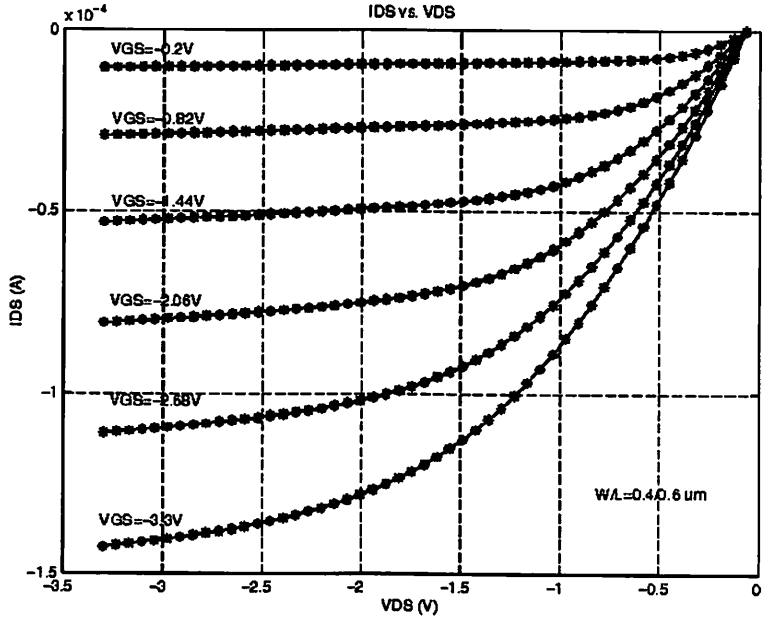

Figure 3.21: Measured versus simulated drain current results for PMOS Transistor with W/L=0.4μm/0.6μm, and V_{BS}=0V. [MOSIS 0.35μm Tech].

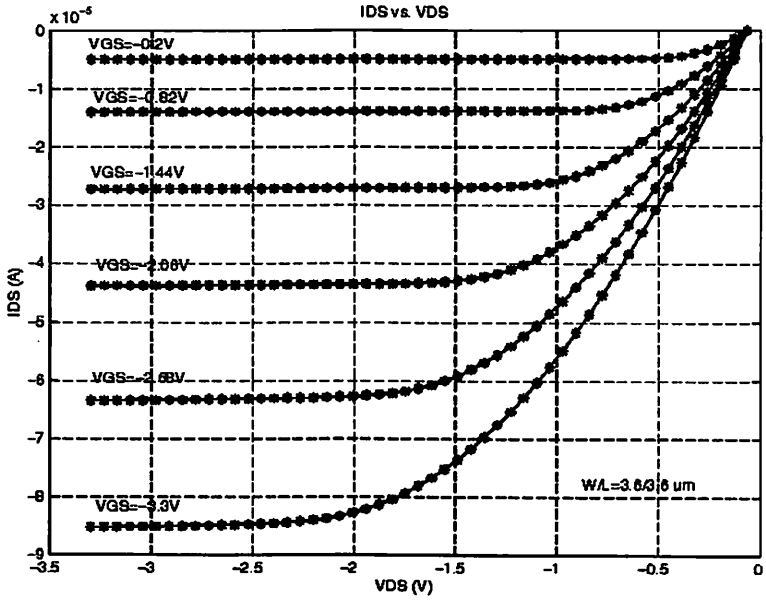

Figure 3.22: Measured versus simulated drain current results for PMOS Transistor with W/L=3.6μm/3.6μm, and V_{BS}=0V. [MOSIS 0.35μm Tech].

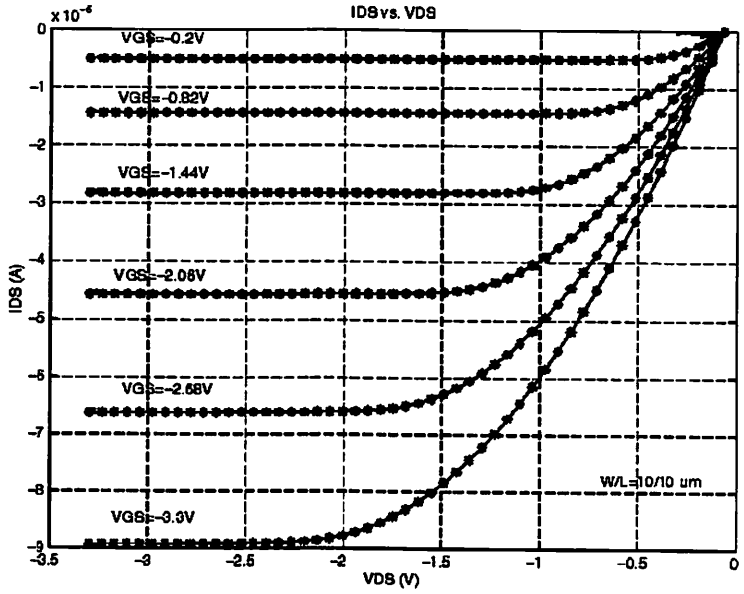

Figure 3.23: Measured versus simulated drain current results for PMOS Transistor with W/L=10μm/10μm, and V_{BS}=0V. [MOSIS 0.35μm Tech].

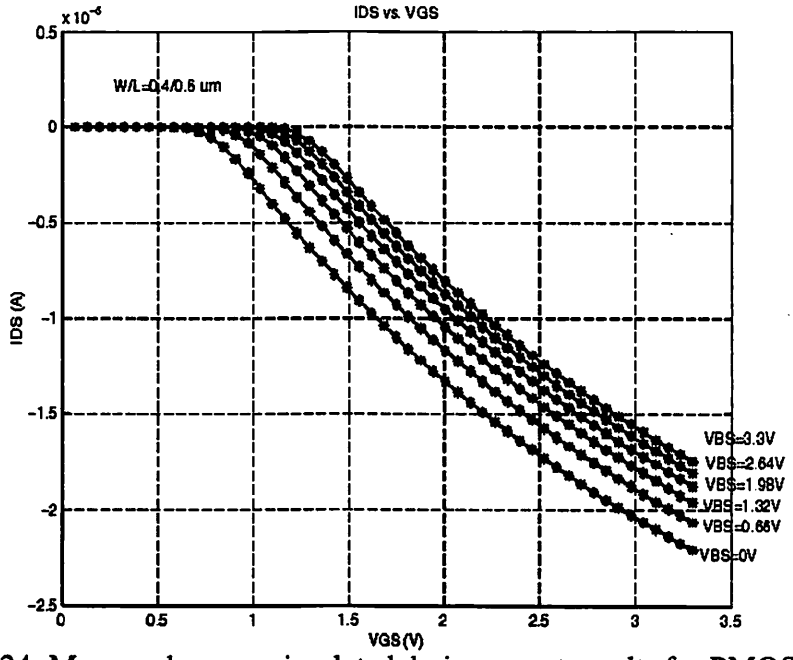

Figure 3.24: Measured versus simulated drain current results for PMOS Transistor with W/L=0.4μm/0.6μm, and V_{DS}=0.2V. [MOSIS 0.35μm Tech].

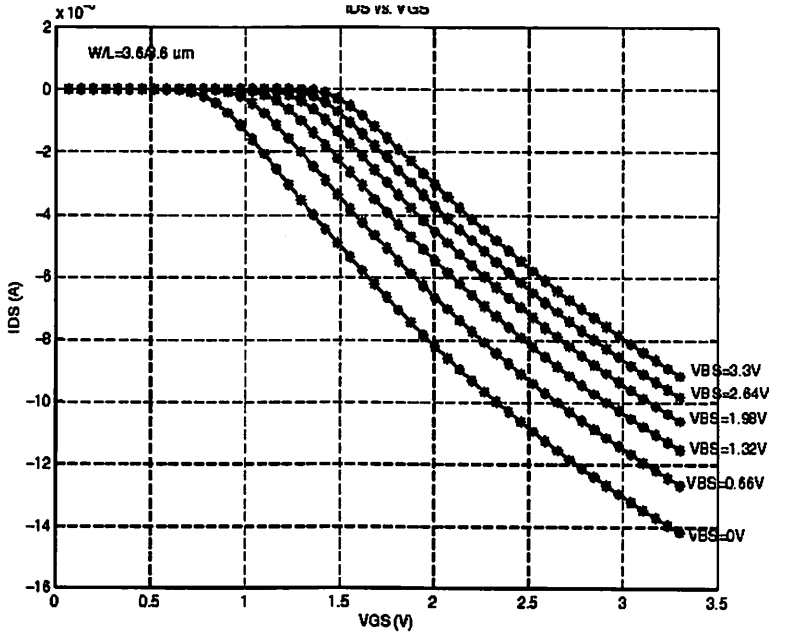

Figure 3.25: Measured versus simulated drain current results for PMOS Transistor with W/L=3.6μm/3.6μm, and V_{DS}=0.2V. [MOSIS 0.35μm Tech].

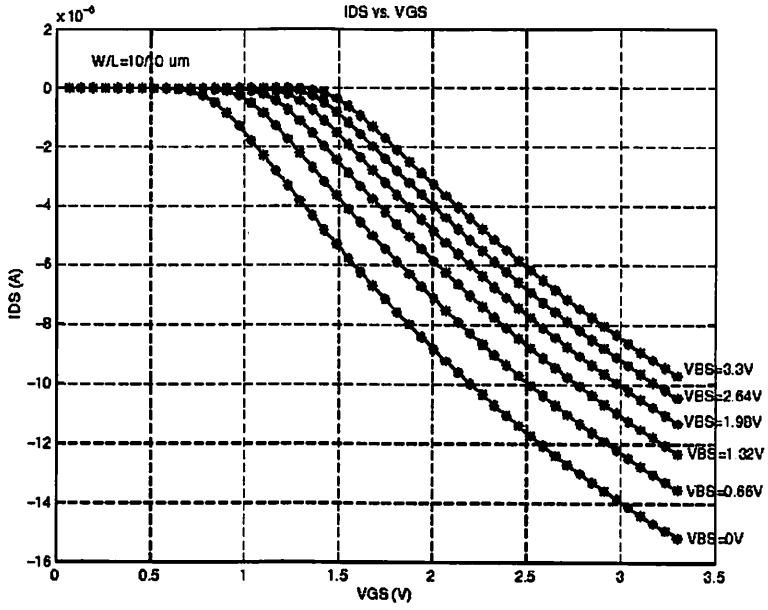

Figure 3.26: Measured versus simulated drain current results for PMOS Transistor with W/L=10μm/10μm, and V_{DS}=0.2V. [MOSIS 0.35μm Tech].

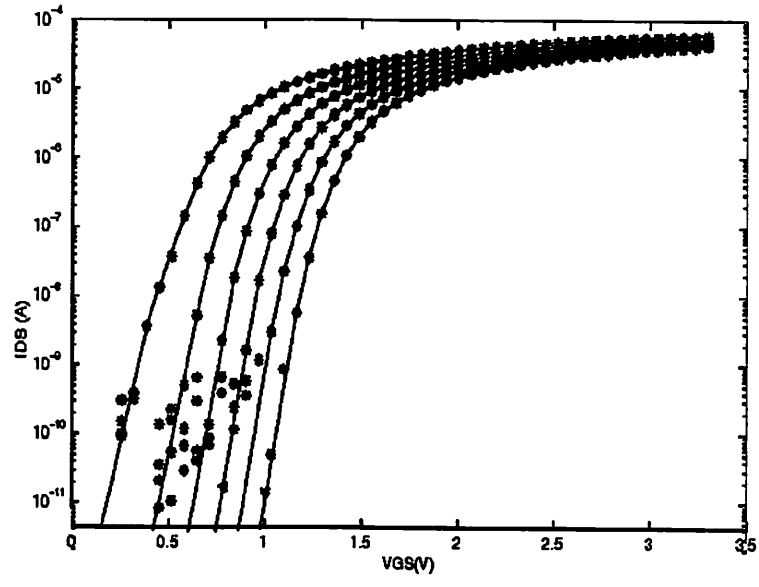

Figure 3.27 Measured versus simulated drain current results for NMOS Transistor with W/L=10μm/10μm, and V_{DS}=0.2V. [MOSIS 0.35μm Tech].

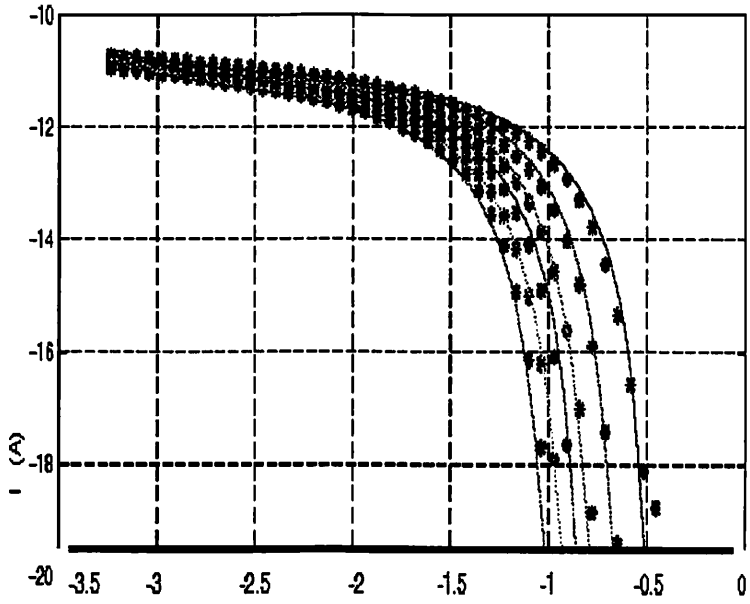

Figure 3.28: Measured versus simulated drain current results for PMOS Transistor with W/L=10μm/10μm, and V_{BS}=0V. [MOSIS 0.35μm Tech].

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Chapter 4

Charge/ Capacitance Model

In this chapter, a unified MOS transistor Charge/Capacitance model valid in all operation regions is described. Instead of calculating the surface potential by solving the Poisson equation directly, charge density approximation is used to obtain the gate, channel, and bulk charge densities to reduce the complexity of the expressions. The sigmoid function and hyperbola techniques are used in S-CMOS Model to unify the charge density expressions, and provide the smooth transition between different operation regions. The terminal charges are calculated by integrating the charge densities across the channel area. Good agreement between the measured data and simulation results is obtained.

4.1 Charge Model

4.1.1 Terminal Charge Expression

To ensure charge conservation, terminal charges instead of the terminal voltages are used as state variables. The terminal charges Q_g, Q_b, Q_s, and Q_d are the charges associated with the gate, bulk, source, and drain, respectively. The charge of an MOS transistor is made up

of three fundamental components: the charge residing on the gate electrode, qg, the fixed charge residing in the bulk depletion layer, q_b, and the mobile channel charge residing in the channel region, q_c. The charge densities are derived by using gradual-channel approximation and depletion approximation. The charge densities in strong inversion region can be expressed [5],

$$q_g = C_{ox}(V_{GB} - V_{FB} - \phi_S - V_{ch}), \tag{4.1}$$

$$q_c = -C_{ox} \cdot [V_{GS} - V_{th} - \alpha_x V_{ch}], \tag{4.1}$$

$$q_b = -C_{ox}[V_{th} - V_{FB} - \phi_s - (1 - \alpha_x)V_{ch}] \ . \tag{4.3}$$

In the weak inversion region

$$q_g = C_{ox} \cdot \frac{\gamma_1^2}{2}\left(-1 + \sqrt{1 + \frac{4(V_{GS} - V_{FB} - V_{BS})}{\gamma_1^2}}\right). \tag{4.4}$$

In the accumulation region

$$q_g = C_{ox} \cdot (V_{GS} - V_{FB} - V_{BS}). \tag{4.5}$$

4.1.2 Transition from linear to saturation region

A hyperbola function is used to smooth out the transition between linear and saturation regions. To unify the (V_{GS} - V_{th}) effects for both strong-and weak-inversion regions, a very popular interpolation function is used [17]. This function has the same linear behavior as (V_{GS}-V_{th}) in the strong-inversion region, and reduces to the exponential decay in the weak-inversion region [1,3].

$$V_{DSAT} = \frac{V_{GS} - V_{th}}{\alpha x}, \tag{4.6}$$

$$V_{DSAT} = V_{GS} - \phi_s - V_{FB} + \frac{\gamma_1^2}{2} - \gamma_1^2 \cdot \sqrt{V_{GS} - V_{FB} - V_{BS} + \frac{\gamma_1^2}{4}} \ . \tag{4.7}$$

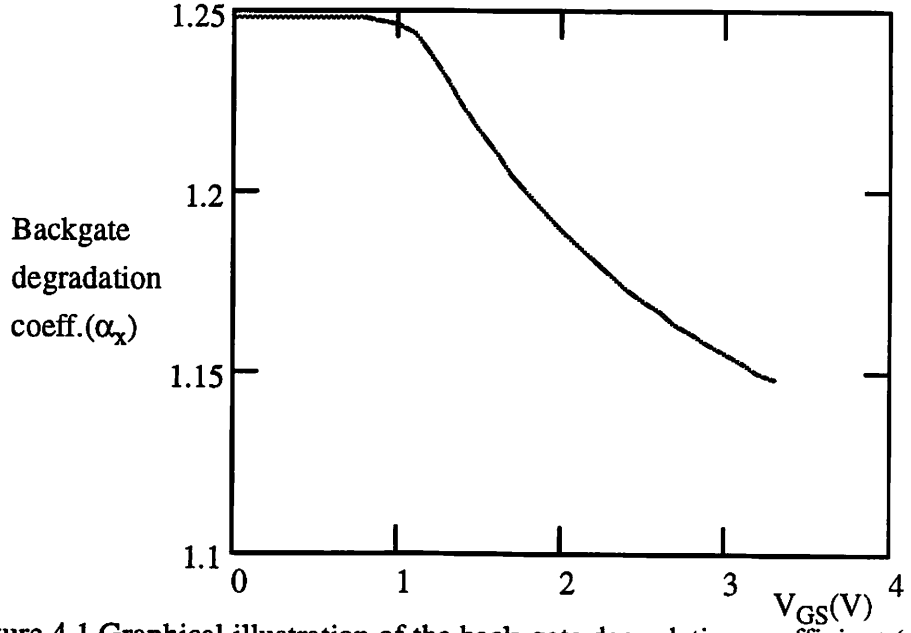


Figure 4.1 Graphical illustration of the back-gate degradation coefficient (α_x) versus V_{GS} with V_{BS}=0, V_{DS}=1V.

The back-degradation coefficient, α_x is obtained by taking inverse value of the differential term of saturation voltage, V_{DSAT}, with respect to the gate voltage, and the expression is

$$\alpha_x = \left(\frac{\partial V_{DSAT}}{\partial V_{GS}}\right)^{-1}$$

$$= \left(1 - \frac{\gamma_1^2}{2\sqrt{V_{GSth} + V_{th} - V_{FS} + \frac{\gamma_1^2}{4}}}\right)^{-1} . \tag{4.8}$$

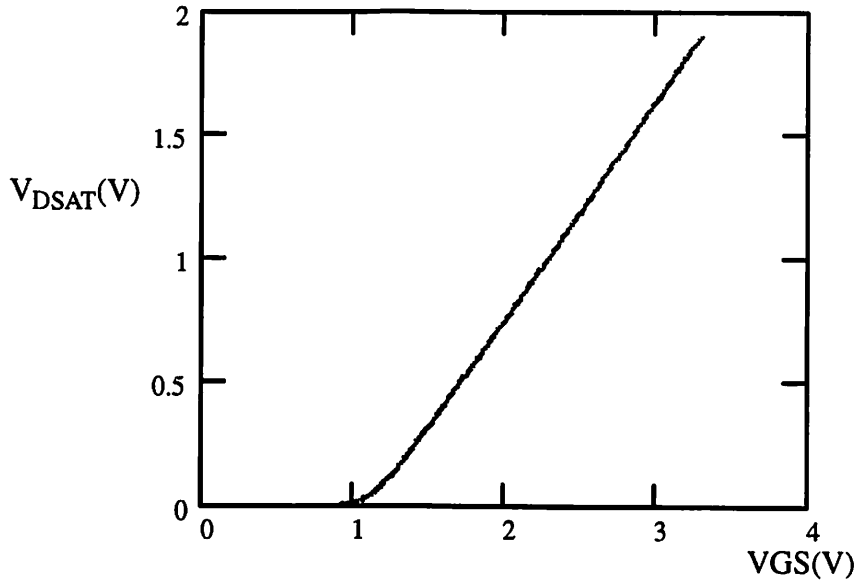


Figure 4.2 Plot of V_{DSAT} versus V_{DS} with V_{DS}=1V, V_{BS}=0V

The saturation voltage, $V_{DSAT} = V_{GSth}$, is valid for both the weak- and strong-inversion regions. The hyperbola function [18], V_{DSATh}, is used to describe the saturation behavior of the charge expression when the transistor operates in the saturation regions [4]

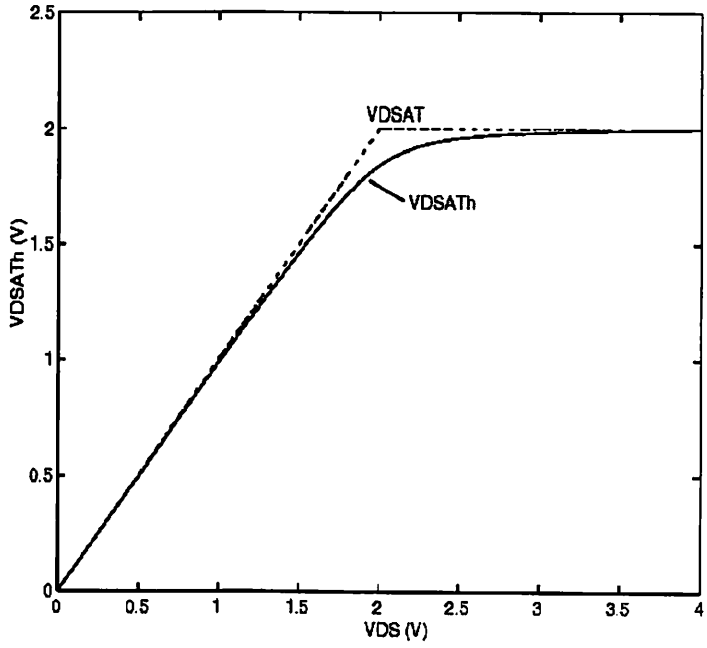
$$q_g = C_{ox}(V_{GSth} + (1-f_s)V_{th} - V_{FB} - \phi_s - (1-f_s)V_{ch}) + \frac{C_{ox}\gamma_1^2}{2}\cdot\left(-1+\sqrt{1+\frac{4(V_{GFh}-V_{GSth}-V_{FB})}{\gamma_1{}^2}}+V_{GS}-V_{GFh}\right), \quad (4.9)$$

$$q_c = -C_{ox}(V_{GSth} - \alpha_x(1-f_s)V_{ch}), \quad (4.10)$$

$$q_b = -(q_g + q_c), \quad (4.11)$$

where

$$V_{GFh} = \frac{1}{2}\left(V_{GS} + K_{GFh}V_{FS} + \sqrt{(V_{GS} + K_{GFh}\ V_{FS})^2 - 4V_{GS}V_{FS}}\right) . \qquad (4.12)$$



V_{DSATh}

Figure 4.3 Graphical illustration of the function V_{DSATh} vs.V_D which reduces to V_{DSAT} in the saturation region

Here, V_{FB} is the flat-band voltage, $V_{FS} = V_{FB} + V_{BS}$ is defined as flat-band voltage referring to source terminal potential, and f_C is a sigmoid function which has the value of 1 in the strong-inversion region and smoothly transits to 0 in the weak-inversion region. In S-CMOS Model, K_c is defined as a model parameter to accurately predict the behavior at the transition between the weak- and strong-inversion regions [17]. The total charge stored in each of the gate, channel, and bulk regions is obtained by integrating the distributed charge densities, q_g, q_c, and q_b, over the channel area.

$$Q_c = W_{eff} \cdot \int_0^L q_c(y)dy = W_{eff} C_{ox} \cdot \int_0^L (V_{GT} - \alpha_x V_y) \cdot \quad dy, \tag{4.13}$$

$$Q_g = W_{eff} \cdot \int_0^L q_g(y)dy = W_{eff} C_{ox} \cdot \int_0^L (V_{GT} + V_{th} - V_{FB} - \phi_s - V_y) \cdot \quad dy, \tag{4.14}$$

$$Q_b = W_{eff} \cdot \int_0^L q_b(y)dy = -W_{eff} C_{ox} \cdot \int_0^L (V_{th} - V_{FB} - \phi_s - (1-\alpha_x)V_y) \cdot \quad dy. \tag{4.15}$$

We have the following expressions upon integration:

$$Q_G = W_{eff} L_{eff} C_{ox} \cdot \left[V_{GSth} + (1-f_s)(V_{th} - V_{FB} - \phi_s) - (1-f_s) V_{DSATh} \frac{4T_c - 1}{6T_c} \right.$$
$$\left. + \frac{\gamma_1^2}{2} \left(-1 + \sqrt{1 + \frac{4(V_{GFh} - V_{GSth} - V_{FS})}{\gamma_1^2}} \right) + V_{GS} - V_{GFh} \right], \tag{4.16}$$

$$Q_c = -W_{eff} L_{eff} C_{ox} \cdot \left(V_{GSth} - \left(\alpha_x \cdot (1-f_s) \cdot V_{DSATh} \cdot \frac{4T_c - 1}{6T_c} \right) \right), \tag{4.17}$$

Where

$$T_c = 1 - \frac{\alpha_x}{2} \cdot \frac{V_{DSATh}}{V_{GSth}}, \tag{4.18}$$

and

$$V_{DSATh} = \frac{1}{2}(V_{DS} + K_{DSATh} V_{DSAT} + \sqrt{(V_{DS} + K_{DSATh} V_{DSAT})^2 - V_{DS} V_{DSAT}}). \tag{4.19}$$

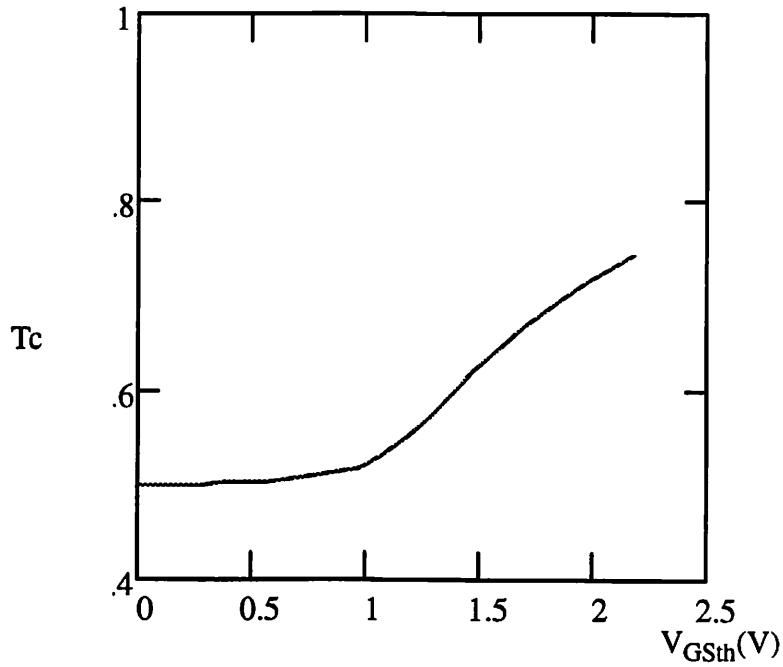


Figure 4.4 : Plots of the Tc versus V_{GS}-V_{th} with V_{DS}=1V and V_{BS}=0V.

4.2 Channel Charge Partitioning Methods

The inversion charges are supplied from the source and drain electrodes such that Q_{inv} = Q_s+Q_d. The ratio of Q_d and Q_s is the charge partitioning ratio. Existing charge partitioning schemes are 0/100, 50/50 and 40/60 which are the ratios of Q_d to Q_s in the saturation region[5]. To complete the charge model, expressions for the drain and source terminal charges should also be included. This can be done by channel charge partitioning.

4.2.1 The 40/60 Channel–charge Partition

This is the most physical model of the three partitioning schemes in which the channel charges are associated to the source and drain electrodes by assuming a linear dependence to the distance.

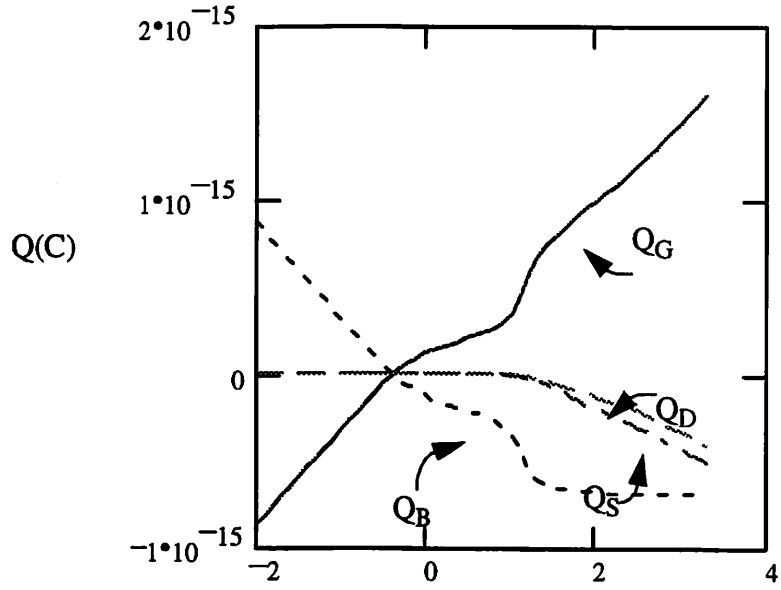


Figure 4.5: Plots of the Terminal charges versus V_{GS} with V_{DS}=1V and V_{BS}=0V.

A physically meaningful 40/60 partitioning scheme for drain and source terminal charges, developed by Ward is used [12]. By carrying out the integration, the charges associated with the drain and source terminals are obtained [17]

$$Q_D = -W_{eff}L_{eff}C_{ox}V_{GSth}\left(-\frac{1}{2}+T_c+\frac{(1-T_c)(1+3T_c+6T_c^2)}{30T_c^2}\right), \tag{4.20}$$

$$Q_S = -W_{eff}L_{eff}C_{ox}V_{GSth}\left(\frac{1}{2}+\frac{(1-T_c^2)}{3Tc}+\frac{(1-T_c)(1+3T_c+6T_c^2)}{30T_c^2}\right). \tag{4.21}$$

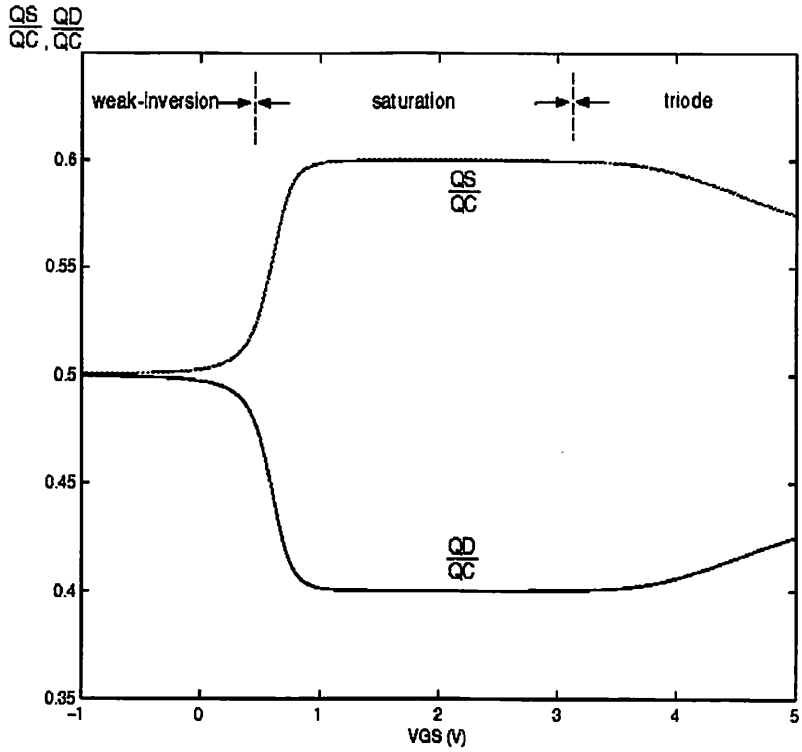


Figure 4.6: Plots of the charges versus V_{GS} with V_{DS}=1V and V_{BS}=0V.

4.2.2 0/100 Channel Charge partitioning

In fast transient simulations, the use of a quasi–static model may result in a large unrealistic drain current spike. This partitioning scheme is developed to artificially suppress the drain current spike by assigning all inversion charges in the saturation region to the source electrode. Notice that this charge partitioning scheme will still give drain current spikes in the linear region and aggravate the source current spike problem [1,4].

$$Q_D = -W_{eff} \cdot L_{eff} \cdot C_{OX} \cdot V_{GSth} \cdot \left(-1 + \frac{3Tc}{2} + \frac{(1-Tc)^2}{30Tc^2} \right), \tag{4.22}$$

$$Q_S = -W_{eff} \cdot L_{eff} \cdot C_{OX} \cdot V_{GSth} \cdot \left(1 + \frac{Tc}{2} + \frac{(1-Tc)^2}{6Tc^2} \right). \tag{4.23}$$

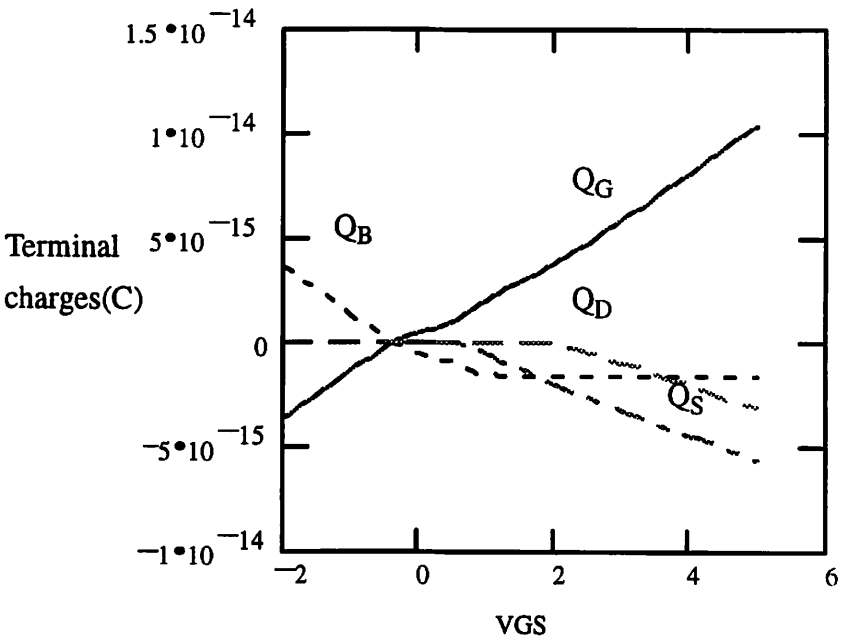


Figure 4.7: Plots of the terminal charges versus V_{GS} in different operation regions with V_{DS}=3.3V and V_{BS}=1V.

4.2.3 50/50 Channel Charge partitioning

This is the simplest of all partitioning schemes in which the inversion charges are assumed to be contributed equally from the source and drain nodes. Despite it's simplicity it is found to approximate the simulation data well [1,4].

$$Q_D = -\frac{1}{2}W_{eff}\cdot L_{eff}\cdot C_{ox}\cdot\left(V_{GSth}+-\alpha_x(1-f_s)V_{DSATh}\frac{4T_c-1}{6T_c}\right), \qquad (4.24)$$

$$Q_S = -W_{eff}\cdot L_{eff}\cdot C_{ox}\left(V_{GSth}+-\alpha_x(1-f_s)V_{DSATh}\frac{4T_c-1}{6T_c}\right). \qquad (4.25)$$

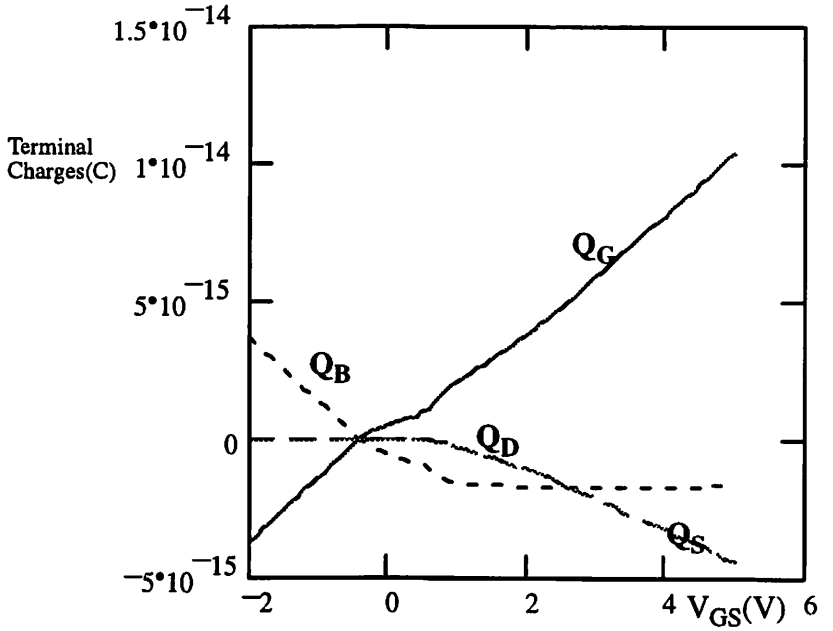


Figure 4.8: Plots of the terminal charges versus V_{GS} in different operation regions with V_{DS}=1V and V_{BS}=0V.

4.3 Capacitance Model

One bottleneck is the difficulty in capacitance measurement, especially in the deep micron regime. At very short channel lengths, the MOSFET intrinsic capacitance is very small yet the conductance is large. The large conductance results in large in–phase currents during high frequency measurement and overloads the C–V meter. Also the effects of the parasitic inductance in the experimental setup will be more profound. Moreover, since charge can only be measured at high impedance nodes (i.e. the gate and substrate nodes), only 8 of the 16 capacitance components in an intrinsic MOSFET, can be directly measured. Another reason for the lack of development work is the observation that most circuits used to be dominated by interconnect and junction capacitance. An exact model for the intrinsic

transistor capacitance is of lesser importance. However, this may no longer be true with the continuous shrinking of design rules. Also, a well behaved capacitance model will help circuit simulation convergence. In low power and analog applications, designers are interested in device operation near threshold voltage. Thus, the model must also be accurate in transition regions as well. To ensure proper behavior, both the I–V and C–V model equations should be developed from an identical set of charge equations so that C_{ij} /I_d is well-behaved. Similar to the I–V model, the development of the capacitance model was carried out with an effort to balance physics with simulation efficiency.

For capacitance modeling considerations, a transistor can be divided into 2 regions: intrinsic and extrinsic. The intrinsic part is the region between the metallurgical source and drain junction when the gate to S/D region is at flat band voltage. All capacitances are derived from the charges to ensure charge conservation. There are 4 nodes, altogether 16 components. The effects of body bias and DIBL is included in the capacitance model by modifying the threshold voltage to make it consistent with the I–V model. In deriving the capacitances additional differentiations are needed to account for the dependence of threshold voltage on drain and substrate biases. The intrinsic capacitances can be derived based on the above charge equations. The inter-nodal capacitances are represented as derivatives of the terminal charges, Q_G, Q_B, Q_D, and Q_S, with respect to the terminal voltages, i.e

$$C_{ij} = x_{ij}\frac{\partial Qi}{\partial Qj}, \tag{4.26}$$

where the indices i and j represent any of the four terminals, gate, bulk, drain, or source.

$$x_{ij} = -1 \quad \text{for} \qquad i \neq j,$$

$$x_{ij} = 1 \quad \text{for} \qquad i = j.$$

The differentiation of these charge expressions is also unified through all operation regions. Previous capacitance models used long-channel charge models in which the ratio of C_{ij}/L_{eff} (where i and j are the transistor nodes) did not scale with L_{eff}. This resulted in an overestimation of capacitance values for devices smaller than a L_{drawn} of 2μm. This effect was particularly severe at low drain biases. In addition, previous capacitance models also showed appalling discontinuity for the gate capacitance at threshold voltage. These factors as wells as others necessitated the development of a new charge and capacitance model. In S-CMOS, a new capacitance formulation addresses the above concerns. In the old formulation, the capacitance is divided into four regions. There were separate equations modeling the nodal charge expressions in each region. From one region to another the charges were continuous, but not their slopes. Therefore, the capacitances in some of these transitions were discontinuous. In the S-CMOS model, a single equation is used to model each terminal charge for all regions.

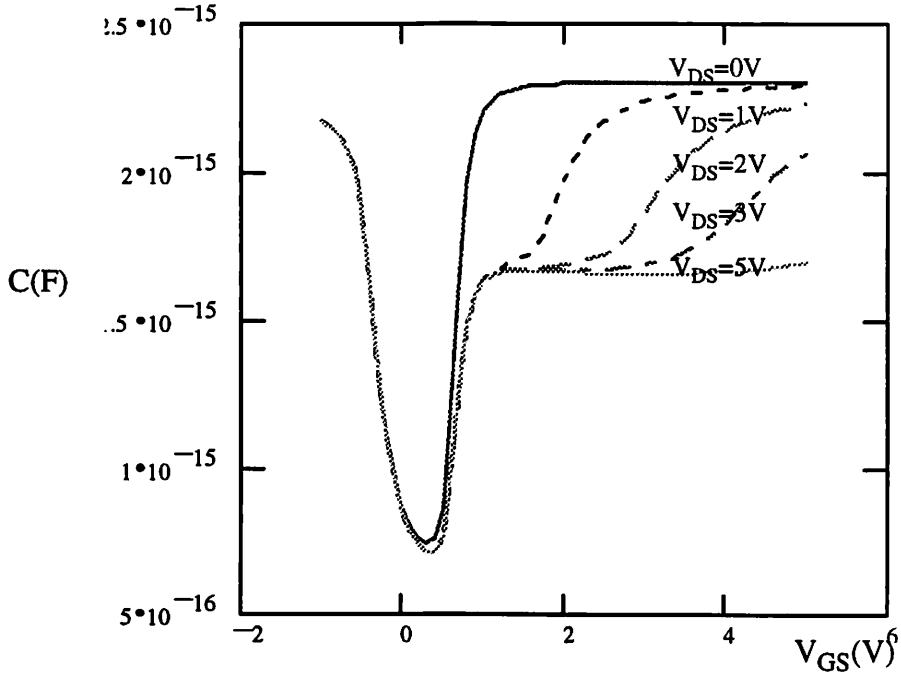


Figure 4.9: Gate capacitances versus gate voltage for V_{DS}=0, 1, 2, 3, 5V, and V_{BS}=0V

$$C_{GB} = W_{eff}L_{eff}C_{ox}\cdot\left(\frac{f_S}{\sqrt{1+\frac{4(V_{GFh}-V_{FS})}{\gamma^2_1}}}+\frac{f_C(\alpha_X-1)}{3\alpha_X}\cdot\frac{(1-T_C)^2}{T_C}\right), \quad (4.27)$$

$$C_{GD} = W_{eff}L_{eff}C_{ox}\cdot\left(\frac{2f_C}{3}+\frac{4T_C{}^2-1}{4T^2{}_C}\right), \quad (4.28)$$

$$C_{GS} = W_{eff}L_{eff}C_{ox}\cdot\left(\frac{2f_C}{3}+\frac{4T_C-1}{4T^2{}_C}\right), \quad (4.29)$$

$$C_{BD} = W_{eff}L_{eff}C_{ox}\cdot\left(\frac{2f_C\cdot(\alpha_X-1)}{3}+\frac{4T_C{}^2-1}{4T^2{}_C}\right), \quad (4.30)$$

$$C_{BS} = W_{eff}L_{eff}C_{ox} \cdot \left(\frac{2f_C \cdot (\alpha_X - 1)}{3} + \frac{4T_C - 1}{4T^2_C} \right). \tag{4.31}$$

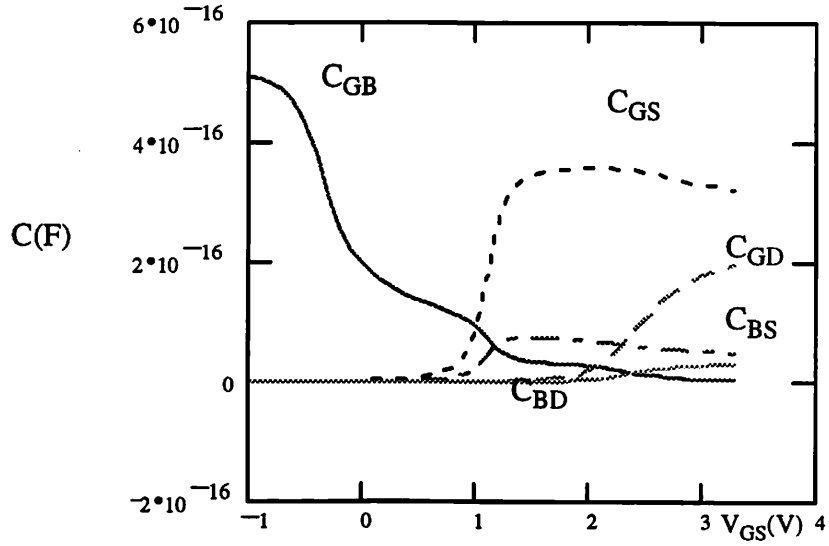


Figure 4.11: Terminal capacitances versus gate voltage for V_{DS}=1V and V_{BS}=0V

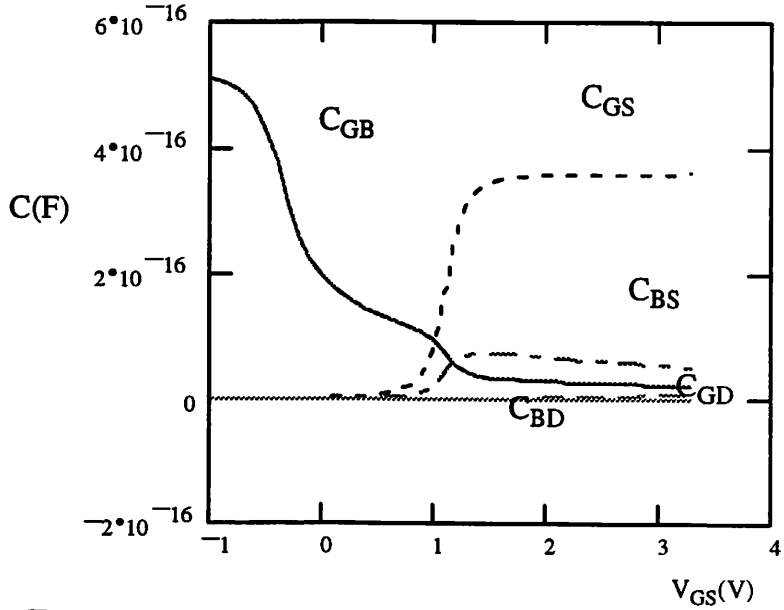


Figure 4.11: Terminal capacitances versus gate voltage for V_{DS}=3.3V and V_{BS}=0V

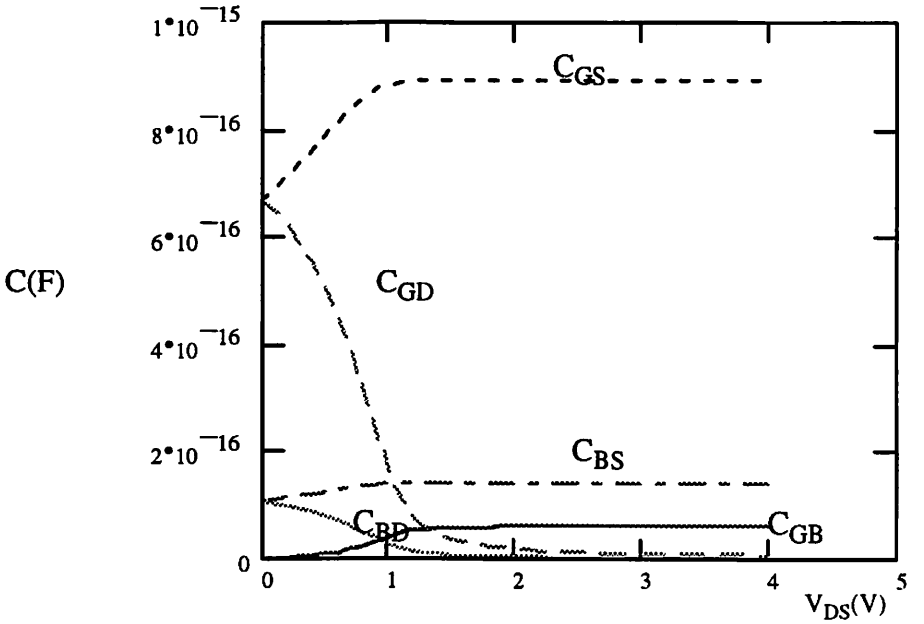


Figure 4.12: Terminal capacitances versus drain voltage for V_{GS}=2V and V_{BS}=-1V

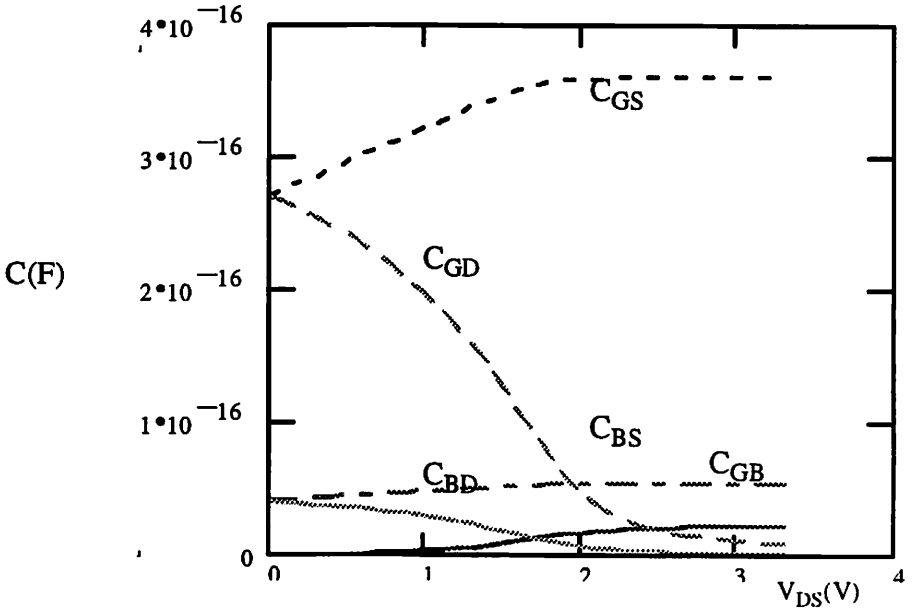


Figure 4.13: Terminal capacitances versus drain voltage for V_{GS}=3.3V and V_{BS}=0V

To form the matrix, nine of the 16 capacitances are independent. The plots of nine capacitances versus the gate voltage and drain voltage are showed, respectively.

4.4. Small signal equivalent circuit

In order to properly describe the MOS transistor from DC to high operation frequency, the choosing of small-signal equivalent circuit is very important. The analysis can be done by four-terminal y-parameter analysis. As shown in Fig.1[11], where all the components include the frequency-dependent terms and real terms. For the circuit simulation purpose, considering the model complexity and accuracy issues, the approximation of all the y parameters can be used by first-order approximation[11,7]. Therefore,

$$-y_{gs} = j\omega C_{GS\omega} = j\omega \cdot \frac{C_{gs}}{1+j\omega\tau_s}, \tag{4.32}$$

$$-y_{bs} = j\omega C_{BS\omega} = j\omega \cdot \frac{C_{bs}}{1+j\omega\tau_s}, \tag{4.33}$$

$$-y_{gd} = j\omega C_{GD\omega} = j\omega \cdot \frac{C_{gd}}{1+j\omega\tau_d}, \tag{4.34}$$

$$-y_{bd} = j\omega C_{BD\omega} = j\omega \cdot \frac{C_{bd}}{1+j\omega\tau_d}, \tag{4.35}$$

$$-y_{gb} = j\omega C_{GB\omega} = j\omega \cdot C_{gb}, \tag{4.36}$$

$$y_{dg} - y_{gd} = g_{m\omega} = \frac{g_d}{1+j\omega\tau_d}, \tag{4.37}$$

$$-y_{sd} = g_{d\omega} = \frac{g_d}{1+j\omega\tau_d}, \tag{4.38}$$

$$y_{db} - y_{bd} = g_{mb\omega} = \frac{g_{mb}}{1 + j\omega\tau_d} \cdot \tag{4.39}$$

At low frequencies where the quasi-static assumption is satisfied, since $\omega\tau_{c(s,d)} << 1$, all the terms are reduced to the frequency-independent components:

$$C_{GS\omega} = C_{gs}, \tag{4.40}$$

$$C_{BS\omega} = C_{bs}, \tag{4.41}$$

$$C_{GD\omega} = C_{gd}, \tag{4.42}$$

$$C_{BD\omega} = C_{bd}, \tag{4.43}$$

$$C_{GB\omega} = C_{gb}. \tag{4.44}$$

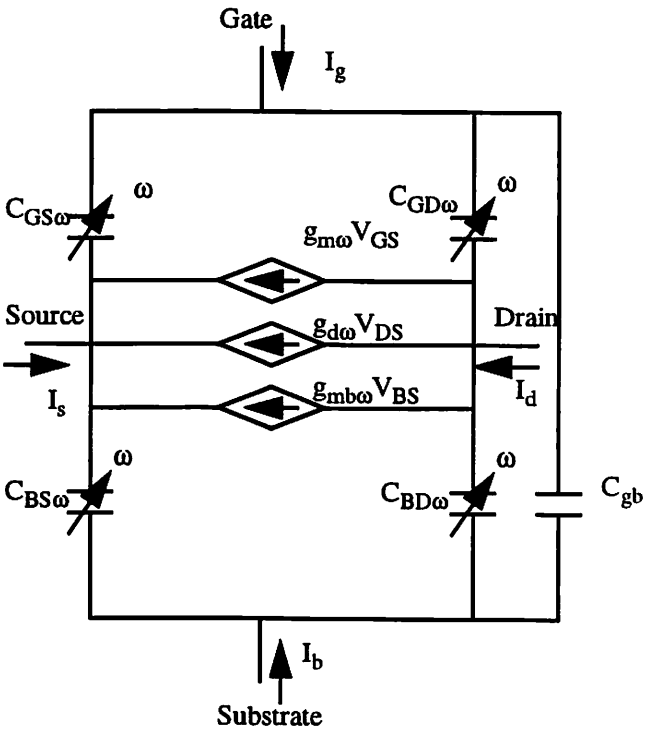


Figure 4.14 : The small-signal equivalent circuit of MOS transistor by y-parameter representation

Therefore, the five capacitance C_{gs},C_{bs},C_{gd},C_{bd} and C_{gb} can be derived directly from quasi-static assumption terminal charges. At high frequencies, there exist the transmission effects between the four transistor terminals. The channel, drain, and source time constants, τ_c,τ_d and τ_s can be derived from the first order quasi-static analysis.

The low-frequency dynamic properties of MOS transistors can be represented by analytical capacitance model based on quasi-static assumption.

4.5 A first order Non–Quasi Static Analysis

It is usually assumed that the charge state of the FET is an instantaneous function of the terminal voltages. This assumption allows the charge-voltage relationships which follow naturally from the current model to be employed in describing the node charge values. The quasi-static approximation for MOS charge models was stated to be valid for terminal voltages that varied sufficiently slowly. Of course, to determine the limits of usefulness of the quasi-static approximation, some method of quantifying sufficiently slowly would be useful. Not unexpectedly, there are no hard and fast rules for determining a particular limit, outside of which non-quasi-static effects will have to be considered. A general rule of thumb for the usefulness of the quasi-static approximation has been found to be [5]

$$\tau_r > 20 \cdot \tau_t \tag{4.45}$$

where τ_r is the rise time of a waveform, and τ_t is the transit time for carriers which leave the source and arrive at the drain. The use of 20 is ad hoc, and cases can be made for values from 15-25 [5],

$$\tau_t = \frac{L_{eff}}{v_{sat}} . \tag{4.46}$$

The quasi-static approach can break down for very high frequencies, or for very long-channel lengths. For submicron technologies, the frequency at which the quasi-static approximation breaks down is well into the GHz range, so it is not likely that this situation will be encountered in most digital circuit designs. However, if a very long channel length is used in an analog circuit design, it is possible that a non-quasi-static approach may be required. This indicates that for a given frequency, the greatest vulnerability to non-quasi-static effects will be found in longer channel devices. Of course, a decreasing channel length implies a higher operating frequency, so it is more instructive to estimate the frequency where the quasi-static approximation begins to break down for a given channel length. The non-quasi-static effects are most likely to be encountered in microwave devices [16]. This discussion applies quite well to digital circuit design, where the shortest available channel lengths are generally used. These conditions are found in some analog and signal processing circuits [30]. Circuits of this type are likely to be the first to require a non-quasi-static charge model. There are additional special circumstances that may require non-quasi-static charge models for silicon MOS technology. As the MOS transistor becomes more performance–driven, the need to accurately predict circuit performance operating near device cut–off frequency becomes more essential as well. However, most device models available in circuit

simulators such as SPICE fall short from this need. They include models which are formulated upon Quasi–Static(QS) assumptions [3]. In other words, the finite charging time for the inversion layer is ignored. When these models are used with the common 40/ 60 charge partitioning option, unrealistically large drain current spikes frequently occur. In addition, the inability of these models to accurately simulate channel charge re–distribution causes problems in fast switched–capacitor type circuits. S-CMOS Model includes a physical NQS transient model which alleviates the above problems. Although it is a physical model that takes in account velocity saturation Model Formulation effects, it is conceptually simple to understand because its formulation is based on familiar channel relaxation principles. When the MOS transistor operates at high frequencies, there are the transmission line effect through the channel and between the device terminals [31]. Those effects can be modeled by time constants, τ_c, τ_s, and τ_d, which denote the time delay in the channel, source to gate (bulk), and drain to gate (bulk), and can be derived by solving the following equations [31].

$$\tau_c = \tau_o \cdot \frac{4\left(1 + 3a_\tau + a_\tau^2\right)}{15(1 + a_\tau)^3}, \tag{4.47}$$

$$\tau_s = \tau_c - \frac{\tau_o}{15(1 + a_\tau)} \frac{\left(2 + 8a_\tau + 5a^2\tau\right) \cdot F_S + \left(5a_\tau + 8a^2\tau + 2a^3\tau\right) \cdot F_L}{(1 + 2a_\tau) \cdot F_S + \left(2a_\tau + a^2\tau\right) F_L}, \tag{4.48}$$

$$\tau_d = \tau_c - \tau_o \cdot \frac{5 + 8a_\tau + 2a^2\tau}{15(1 + a_\tau)^2 \cdot (2 + a_\tau)}, \tag{4.49}$$

where,

$$F_s = -Vt\left(\frac{dU_{SS}}{dV_{GS}} + \frac{dU_{SS}}{dV_{BS}} + \frac{dU_{SS}}{dV_{DS}}\right), \tag{4.50}$$

$$F_L = -Vt\left(\frac{dU_{SL}}{dV_{GS}} + \frac{dU_{SL}}{dV_{BS}} + \frac{dU_{SL}}{dV_{DS}}\right). \tag{4.51}$$

and a_τ is defined as the boundary charge ratio of inversion layer at drain and source boundaries. In order to calculate τ values, it requires to solve the surface potentials at the channel boundaries. The nomalized surface potential can be obtained by the following relationship [29].

$$\frac{V_t}{\gamma^2}(U_g - U_s)^2 = e^{-Us} - 1 + e^{Uc - \frac{2\phi_F}{Vt}}(e^{Us} - 1) + U(s), \tag{4.52}$$

where Us=Uss, for Uc=V_{SB}/V_t, V_{DB}/V_t, respectively, and U_g is defined by $(V_{GB}-V_{FB})/V_T$. In strong-inversion region, the boundaries surface potential can be approximated by

$$U_{SS} = \frac{V_{SB} + 2\phi_F}{V_t}, \tag{4.53}$$

and

$$U_{SL} = \frac{V_{DB} + 2\phi_F}{V_t}, \tag{4.54}$$

Thus, F_S=1, F_L=0, and

$$\tau_S = \tau_c - \tau_o \times \frac{2 + 8a_\tau + 5a^2_\tau}{15(1 + a_\tau)^2(1 + 2a_\tau)}. \tag{4.55}$$

In weak inversion region, by directly solving the derivatives of boundary surface potentials as in Eq.(4.17), we can obtain [29]:

$$\frac{V_t}{\gamma^2}(U_g - U_s)^2 = e^{-Us} - 1 + e^{Uc - \frac{2\phi_F}{Vt}}(e^{Us} - 1) + U_S, \tag{4.56}$$

$$F_S = \frac{-(e^{Uss} - 1)\cdot e^{-\frac{V_{SB} - 2\phi_F}{Vt}}}{2\cdot\frac{V_t}{\gamma^2}(U_g - U_{SS}) - e^{Uss} + e^{-U_{SS} - \frac{V_{SB} + 2\phi_F}{V_T}} + 1}, \tag{4.57}$$

$$F_L = \frac{-(e^{U_{SL}} - 1)\cdot e^{-\frac{V_{DB} - 2\phi_F}{Vt}}}{2\cdot\frac{V_t}{\gamma^2}(U_g - U_{SL}) - e^{U_{SL}} + e^{-U_{SL} - \frac{V_{DB} + 2\phi_F}{V_T}} + 1}. \tag{4.58}$$

Since in weak inversion region, the surface potential at source boundary is almost equal to drain boundary. This results a_τ=1. Therefore, the following simplified results can be obtained. In the MOS device operation, the behavior is smoothly continuous in all operation regions from DC to high frequencies. The frequency-dependent terms should also be determined without specifying the operation region. The unified time constants, τ_c, $\tau_{s,\text{ and}}$ τ_d can be calculated using Eq(4.47), (4.48), and (4.49) by the unified expressions of τ_0 and a_τ which are given as,

$$\tau_0 = \frac{L^2}{\mu_{eff}} \cdot \frac{\alpha_x}{(V_{GSh} - V_{th}) + \alpha_x \cdot V_t}, \tag{4.59}$$

$$a_\tau = 1 - \frac{V_{DSATh}}{V_{DSAT} + K_\tau} \quad . \tag{4.60}$$

where K_τ=0.01.

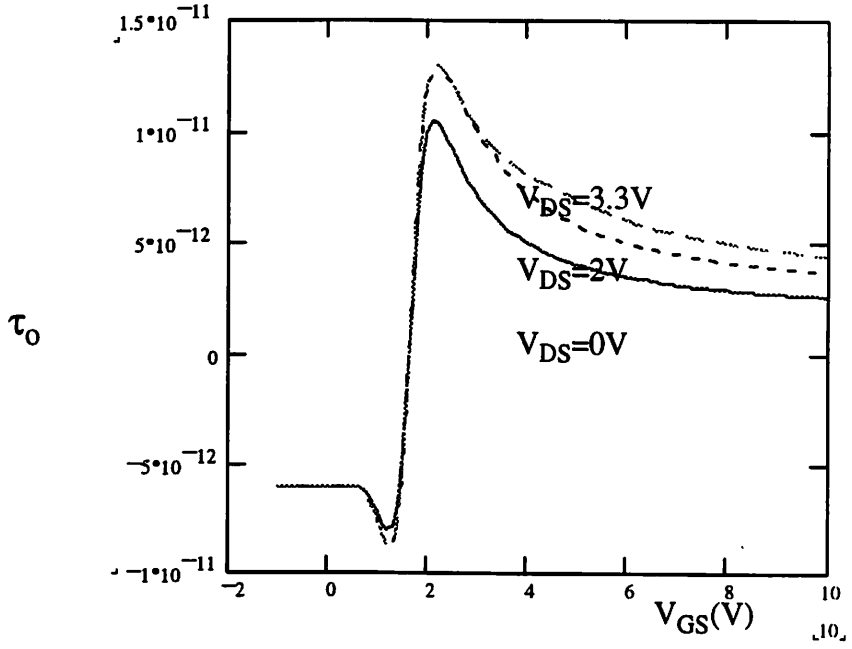


Figure 4.15: The plots of τ_0 versus V_{GS} for V_{DS}=3.3, 2, 0V and V_{BS}=1V for W/L= 1μm/0.5μm NMOS Transistor.

Notice that the time constant curves in various bias condition are smooth throughout all operation regions as shown in Fig.4.16 to Fig.4.25. The time constant values can be obtained according to the bias condition of V_{DS}, V_{GS}, and V_{BS}.

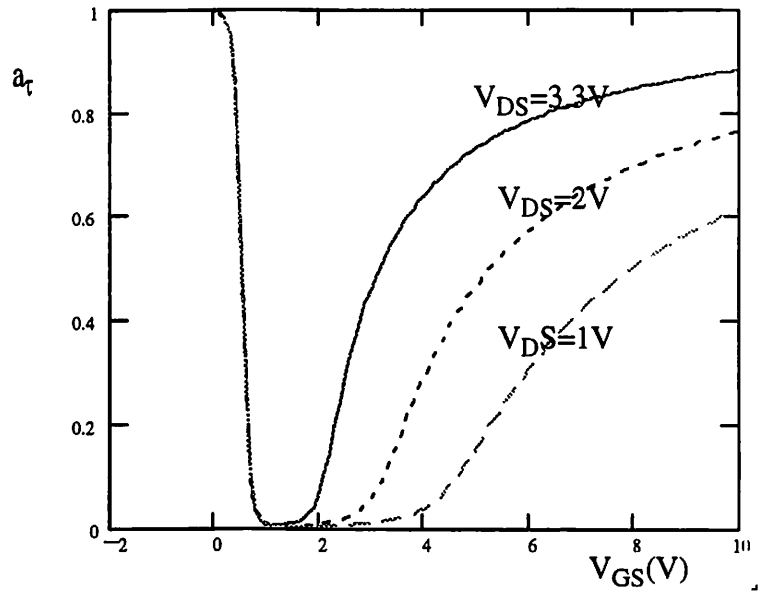


Figure 4.16: Plots of a_τ versus V_{GS} for V_{DS}=1, 2, 3.3V, and V_{BS}=1V for W/L=1.0μm/0.5μm NMOS Transistor.

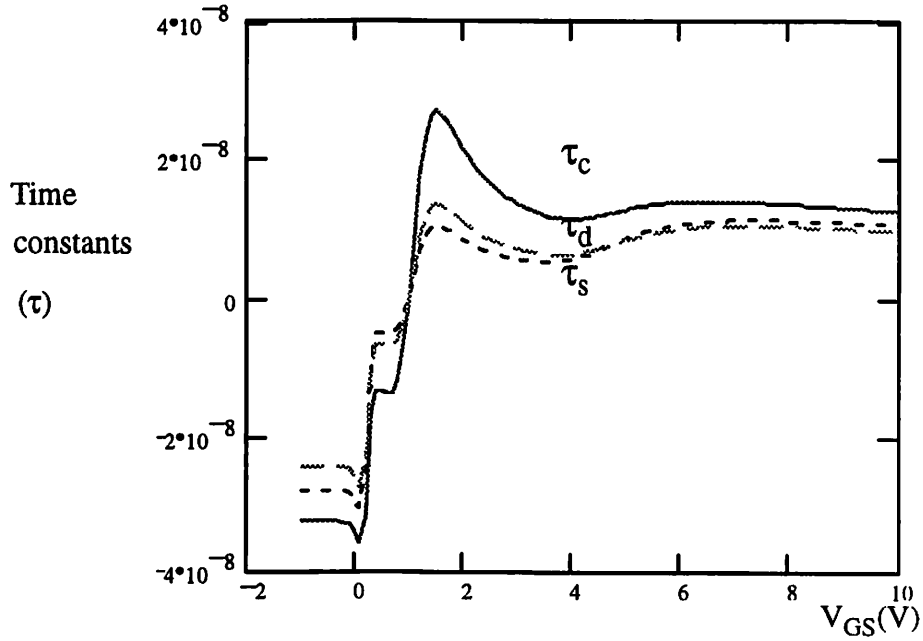


Figure 4.17: Plots of time constants versus gate voltage for V_{DS}=3.3V and V_{BS}=1V. for W/L=50μm/50μm NMOS Transistor.

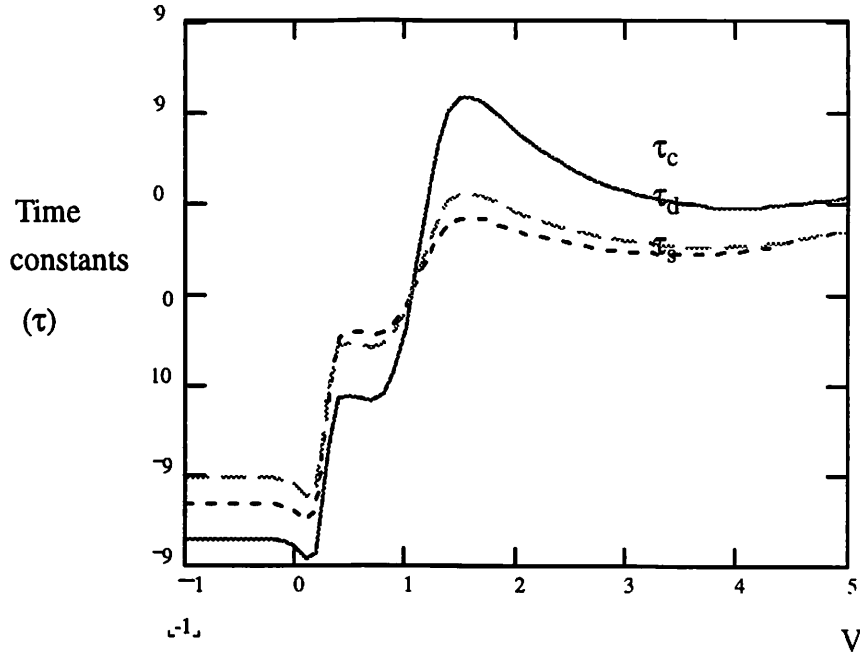


Figure 4.18: Plots of time constants versus gate voltage for V_{DS}=3.3V and V_{BS}=1V. for W/L=10μm/10μm NMOS Transistor.

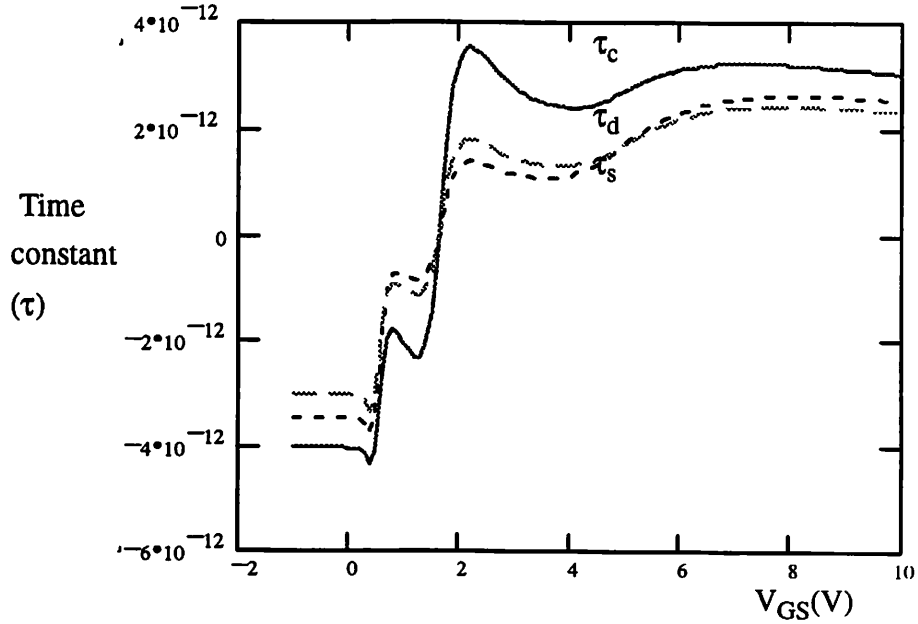


Figure 4.19: Plots of time constants versus gate voltage for V_{DS}=3.3V and V_{BS}=1V. for W/L= 1μm/0.5μm NMOS Transistor.

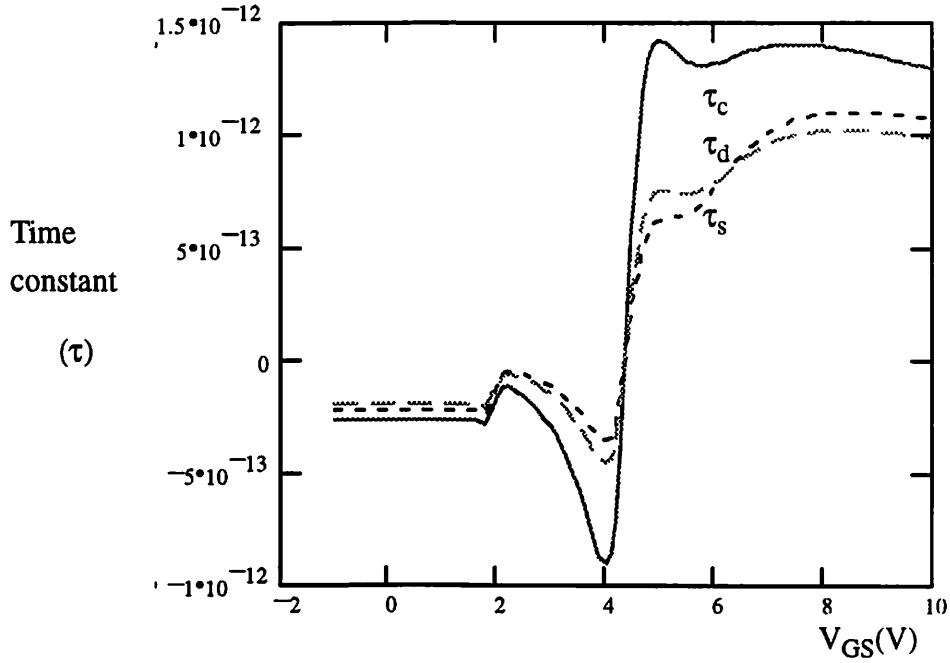


Figure 4.20: Plots of time constants versus gate voltage for V_{DS}=3.3V and V_{BS}=1V. for W/L= 0.18μm/0.18μm NMOS Transistor.

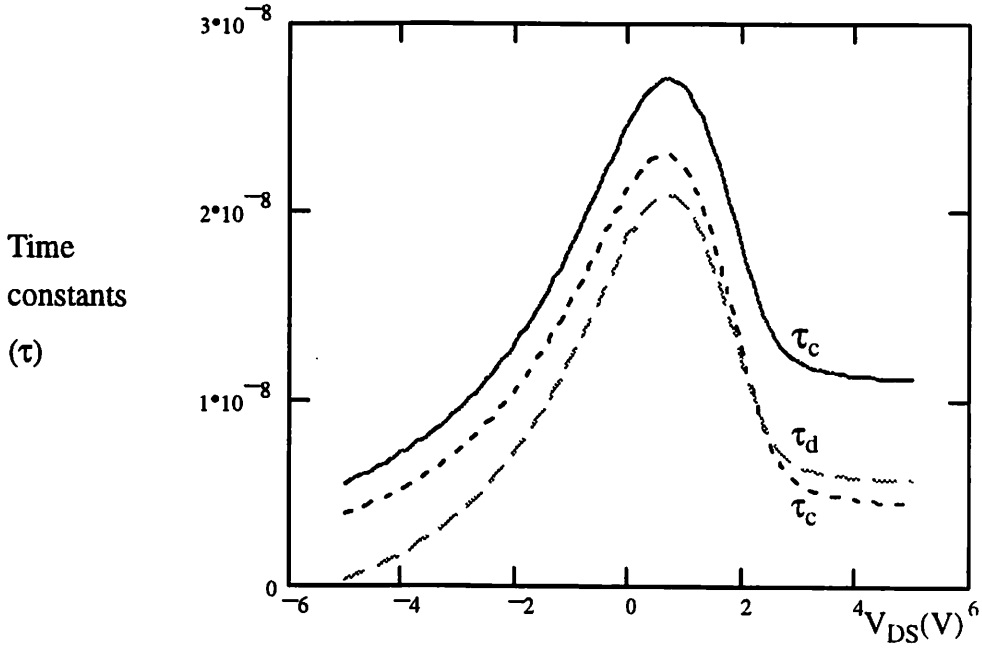


Figure 4.21: Plots of time constants versus drain voltage for V_{GS}=3.3V and V_{BS}=0V. for W/L= 50μm/50μm NMOS Transistor.

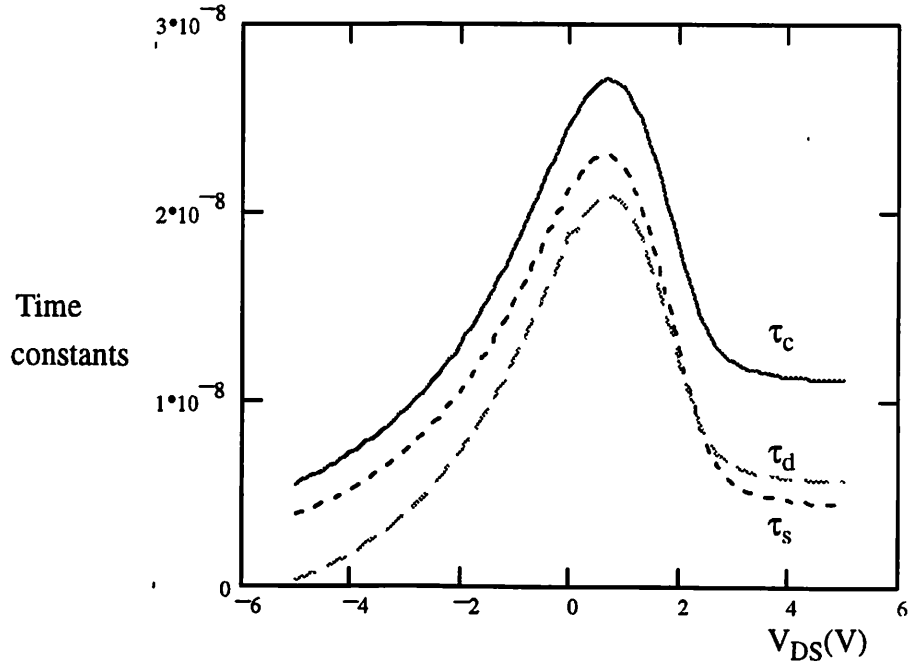


Figure 4.22: Plots of time constants versus drain voltage for V_{GS}=3.3V and V_{BS}=0V. for W/L= 10μm/10μm NMOS Transistor.

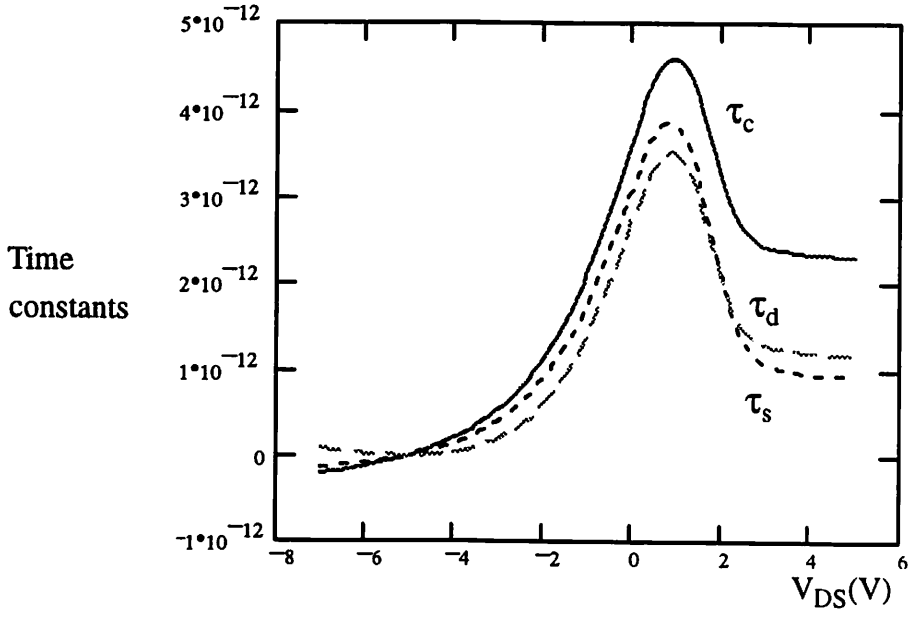


Figure 4.23: Plots of time constants versus drain voltage for V_{GS}=3.3V and V_{BS}=0V. for W/L= 1.0μm/0.5μm NMOS Transistor.

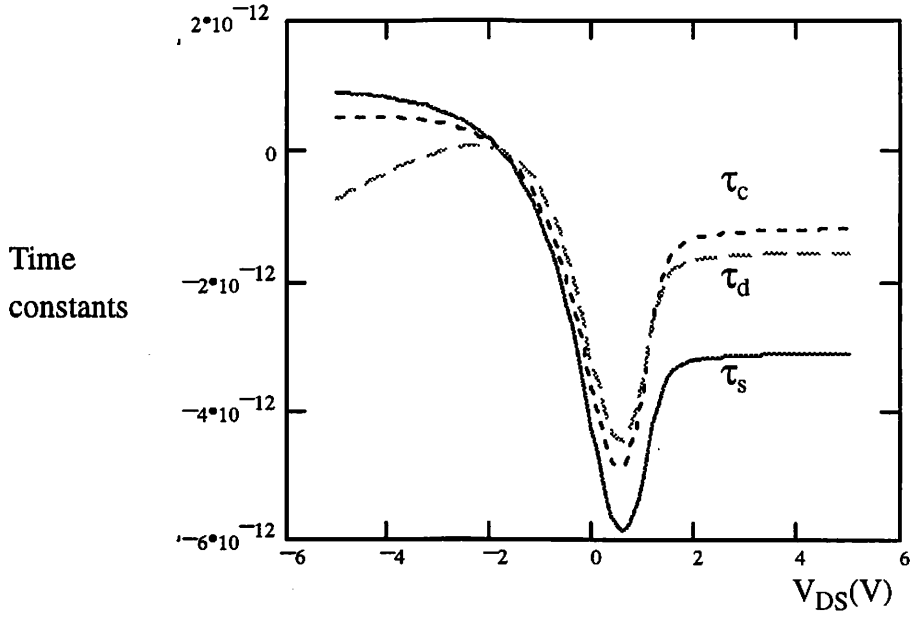


Figure 4.24: Plots of time constants versus drain voltage for V_{GS}=3.3V and V_{BS}=0V. for W/L= 0.18μm/0.18μm NMOS Transistor.

The simulation results of time conatants and applicable frequency limit in S-CMOS Model in different channel lengthes are summrized in Table 4.1

Table 4.1 The simulation results of time conatants in differenr channel lengthes

Device size(μm)	tc(sec)	Frequency limit
50/50	26.99ns	1.85MHz
10/10	1.08ns	46.22MHz
1.0/0.5	3.54ps	14.96GHz
0.18/0.18	1.41ps	35.31GHz

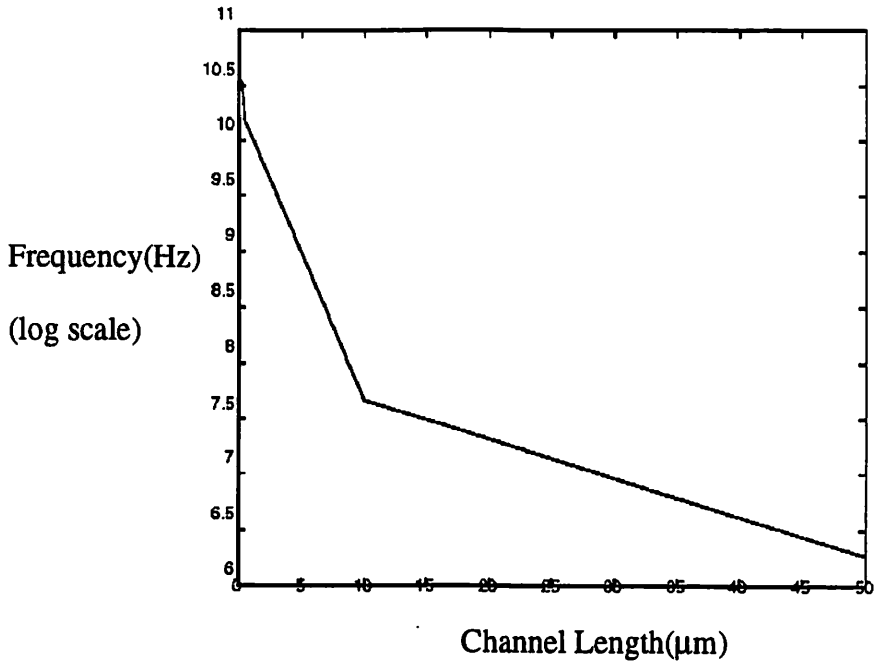


Figure 4.25 The simulation results of time conatants in different channel length

4.6 Experimental Results for Charge/Capacitance Model

The S-CMOS transistor charge/capacitance model has been simulated and compared to the measured data. Fig 4.26 shows the normalized plots of the four terminal charges of a short-channel MOS transistor with the 40/60 channel-charge partitioning method. The normalization factor is ($W_{eff}L_{eff}C_{ox}$). Notice that the unified charge expressions are continuous over all operation regions. In the time-domain large-signal analysis and frequency-domain small-signal analysis for the charge-based approach, 16 charge derivatives are needed in the assembly of the nodal admittance matrix. These derivatives may be regarded as inter-nodal capacitances. Notice that the capacitance curves are smooth throughout all

operation regions. Comparison of measured and calculated results of the capacitances associated with gate and bulk terminals for an L_{eff} = 0.5 μm transistor is shown in Fig.4.27. Good agreement between the measured data and calculated result as been obtained.

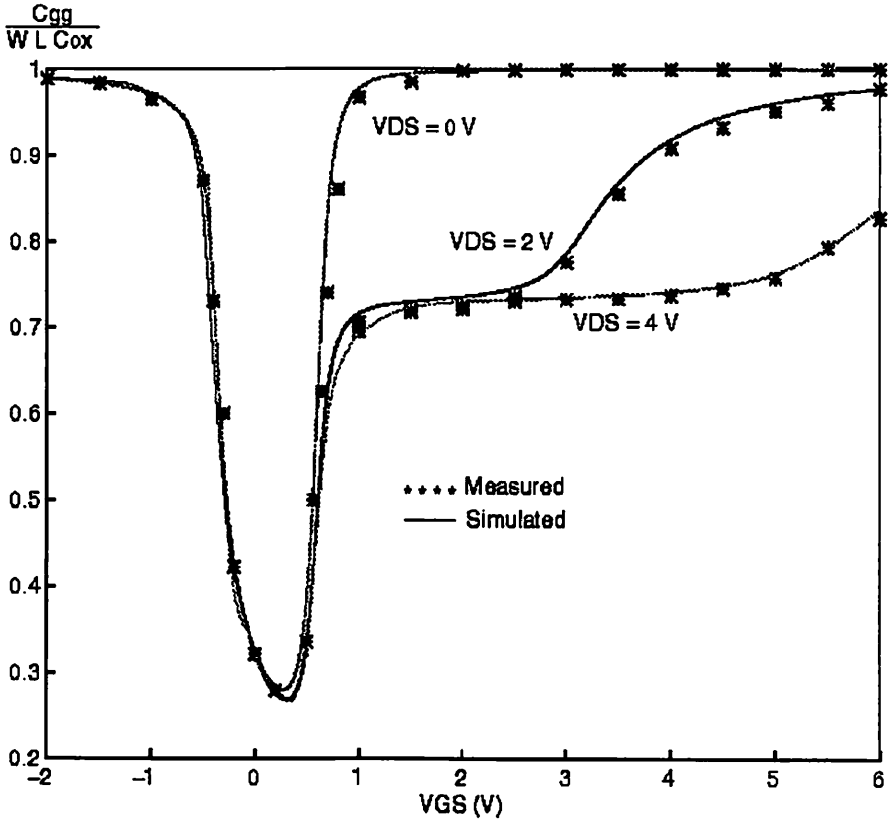


Figure 4.26: Plots of nomalized capacitances versus V_{DS} of an NMOS Transistor

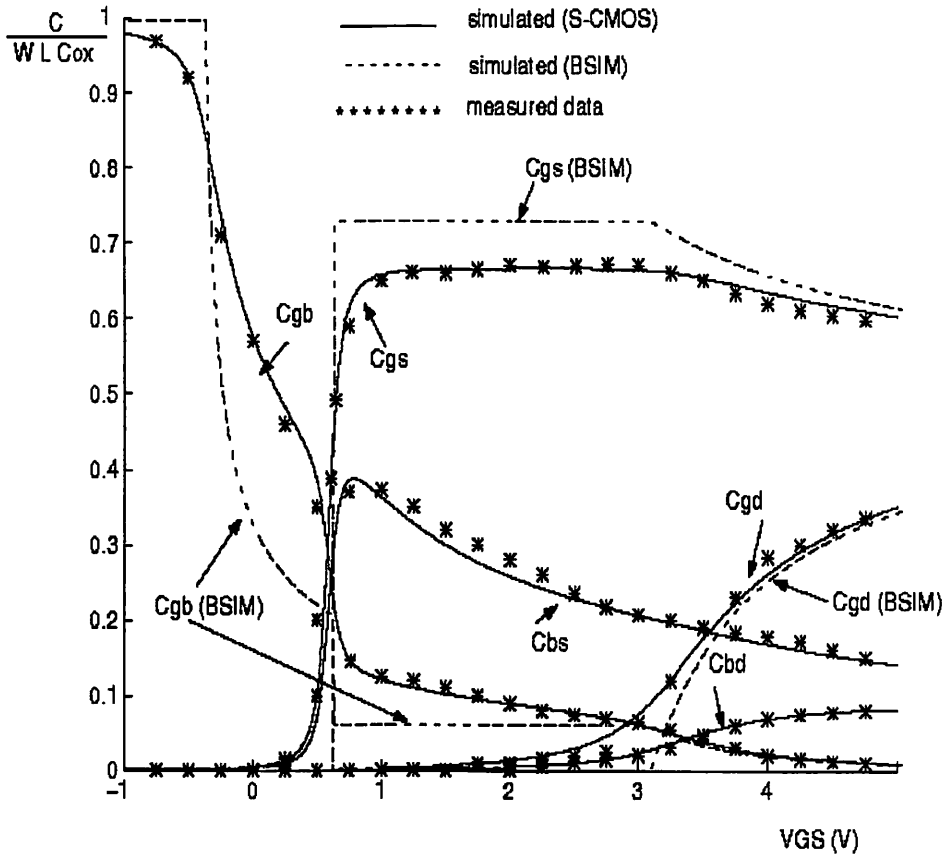


Figure 4.27: Plots of nomalized capacitances versus V_{GS} of an NMOS Transistot of W/L=25μm/0.5μm

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Chapter 5

S-CMOS Model Parameter Extraction

In this chapter, an efficient MOSFET model parameter extraction program is described, proper error function is defined, and a good initial guess algorithm is provided to initiate the optimization process. Based on the properties of the S-CMOS, a combination of a local optimization and the group device extraction strategy is adopted for parameter extraction.

CMOS design has advanced remarkably in the last few years, due to the trend toward mixed signal chips, to low-voltage low-power high-frequency application. Adequate device models for circuit simulators are required in the design of IC's, especially in analog design, because the accuracy of simulation results is closely related to model which is used in the simulation. Parameter extraction is an important part of model development. Many different extraction methods have been developed. The appropriate methodology depends on the model and on the methods the model is applied. Reliable analog IC design requires reliable and accurate device models. An analytical device modeling can be classified by following several methods[13].

(A) Physics-based method

One of the most widely used methods is a "physics-based approach". This approach is highly desirable since model parameters are closely related to the device structure and fabrication processing. However, due to the difficulty in solving fundamental semiconductor equations to obtain a solution, this method can be applied only to very simple device structures.

(B) Best-fitting method

Another method is the "**best fitting**" of data derived from measurements. A empirical method in MOSFET modeling has many advantages over physics-based modeling, is the appropriate for circuit simulation.

(C) Combined method

Above two methods can be combined to improve the performance of the model. In this case a physics-based model is derived by solving very simple equations. The unknown "physical parameters" can be derived by a "fitting" procedure.

5.1 Parameter classification

The MOS transistor model described in this research includes several important effects of submicron technology from different operation regions. It is equipped with 35 model parameters, as listed in Table 5.1. The parameters can be summarized into three subgroups

as the primary physical parameters, secondary physical parameters for fitting, and smooth function parameters.

5.1.1 Primary Physical Parameters

The primary physical parameters strongly represent the key device behavior. Most of the parameters in this category can be determined directly from local extraction of measured data without global optimization. The parameters can be used to determine characteristics of transistors with large channel length and width. The gate-oxide thickness, t_{ox}, can be directly determined from the devices measured data from the beginning. Inversion potential, ϕ_s are the main contribution to the zero-bulk-bias threshold voltage, V_{tho}, which can be extracted by calculating the threshold voltage from the low drain-bias measurement. The intrinsic surface mobility, μo, can be extracted from the drain current behavior with respect to the gate voltage between the measured data and modeled results under the zero-substrate-bias and low drain voltage conditions.

5.1.2 The Fitting Parameters

Fitting parameters are used to model the device effects including short-channel/reverse short-channel effects, narrow-channel effects, body-effect, velocity saturation effects, mobility reduction due to the transverse and lateral electric fields, and channel-length modulation effects. The optimization steps are usually used to extract the fitting parameter values. We have to pay attention to three key issues for this type of extraction: optimization algorithm, bias conditions of measured data and modeled results, and the number of

transistors and the transistor sizes chosen for optimization. Twenty-four secondary physical parameters are used to properly model deep-submicron MOS transistors. In the S-CMOS model, the goal of the secondary physical parameters is to enhance the model accuracy for deep-submicron applications. Therefore, accurate extraction of the secondary physical parameters is very important to ensure the model applicability for advanced technologies.

5.1.3 The Smooth-Function Parameters

In order to unify the model expressions to be valid for all operation regions, several smooth functions are applied to achieve better transitions between different operation regions. In S-CMOS model, there are three types of smooth functions: sigmoid function, hyperbola function, and exponential interpolation function. The exponential interpolation function is widely used to model V_{GS}-V_{th} from the weak-inversion region to subthreshold and approaches square term in strong-inversion region. There is no parameter required in this function. The sigmoid function, f_s, is also used to smooth out the transition between the weak- and strong-inversion regions for high-order effects, and is equipped with one parameter. The hyperbola function is used to achieve better transition between the triode and saturation regions, and is equipped with another parameter. In S-CMOS Model, all the smooth function parameters are first set to the default values while extracting other model parameters. The extraction of those parameters is done at the latter step by optimizing the transitions between different operation regions. The effect of this step is to achieve better fitting at those transitions between different operation regions.

5.2 Optimization Techniques

5.2.1 Error Functions

All extraction algorithms that are based on optimization techniques try to minimize an error function, also called objective function or cost function. The value of the error function is a measure of the distance between measured and calculated data points. Even after the error function has been minimized, there will be a difference between measured and calculated data points since the model always is an approximation to reality and the data points also contain measurement noise. A simple commonly used error function is given by [8]

$$\left\| e(p_k) \right\|^2 = \sum_{i=1}^{N} e(p_k)^2 = \sum_{i=1}^{N} \left(\frac{I_i(p_k) - I_{i(measured)}}{max(I_i, I_{min})} \right)^2, \qquad (5.1)$$

where p_k is the parameter vector during the k-th iteration, $Ii(p_k)$ the calculated drain current at data point number i, $I_{i(measured)}$ the measured drain current, and N, the number of data points. I_{min} is the current limit above which the relative error is used and below which the absolute error (scaled by I_{min}) is used in the error function. With this error function, the relative differences between measured and simulated currents are minimized. The absolute differences between measured and simulated currents can also be minimized. These two different error functions have slightly different behaviors. While the absolute error function favors large currents at the expense of the smaller currents, the relative error function behaves in the opposite way. Therefore the current difference in Eq (5.1) is

divided by the maximum value of $I_{i(measured)}$ and I_{min} to prevent the differences in the sub-threshold region from dominating. For simulation of digital circuits it is usually sufficient to minimize the errors in the currents but for simulation of analog circuits it is not only the current level is important but also for instance the transconductance and the output conductance. These are the derivatives of the current with respect to the gate-source and drain-source voltages, respectively. Therefore it is important to include the difference between measured and simulated derivatives of the current in the error function. The different types of errors can be weighted differently through weighting factors. In the error functions described above the variables are divided into two groups: independent and dependent variables. The independent variables are usually the terminal voltages and the dependent variables are the measured currents, transconductances, etc. It is assumed that the independent variables are known exactly while the dependent variables contain all simulation errors. This means that the sum of the errors in the dependent variables is minimized.

5.2.2 Optimization Methods

The objective of the optimization routine is to find a set of parameter values which will minimize the error function. There are two classes of gradient methods for optimizing the Newton (or quasi-Newton) methods and the modified Gauss methods [7]. The most widely used general-purpose optimization method is the Davidon-Fletcher-Powell (DFP) algorithm which belongs to the class of the quasi-Newton methods. However, for the MOSFET model parameter extraction the DFP algorithm is not the proper choice. Since

the error function ERR is a sum of squares of nonlinear functions, the MOSFET model parameter extraction is a nonlinear least square fit problem. The advantage of error function is that it provides a percentage error and does not give too much emphasis either on low currents or on high currents. One advantage of these general optimization techniques is that the model parameters for new or modified models are easy to extract. The algorithms can be classified into the following categories:

- Gradient following methods,
- Direct searching methods,
- Combined methods (combination of above).

(A) Gradient Following Method

The most commonly used gradient following methods are the **steepest descent**, the **Gauss-Newton**, and the **Levenberg-Marquardt methods**. In the steepest descent method, a search for the minimum of the error function is performed along a direction defined by the gradient of the norm. This is a one dimensional search where numerical search methods are used. The great advantage of this method is its stability for points far from the minimum but its drawback is its slow convergence. In the Gauss-Newton method, not only the slope of the error function but also its curvature are used to determine the direction of the search. This method converges rapidly for points close to the minimum, but convergence is not guaranteed for points far from the optimum solution. The Levenberg-Marquardt algorithm is a combination of the steepest descent and the Gauss-Newton methods. This algorithm is based on the assumption that the optimal search direction lies between the steepest descent direction and the direction of the Gauss-Newton

method. With the combination of the two methods both stability and rapid convergence can be reached.

(B) Direct Searching Method

The direct searching optimization methods take a different approach to determine the updated parameter vector. Some of the large number of direct searching methods that exist have been used for extraction of model parameters. This algorithm uses a series of geometrical operations called reflection, expansion and contraction to improve the parameter vector. The error function is evaluated for each parameter vector and the parameter vector with the largest error.

(C) Combined Methods

Wang, et al [11] proposed a combination of a gradient following algorithm and a direct searching process. The algorithm starts with the Gauss-Newton method. It continues with the Gauss-Newton method as long as the value of the error function for the updated parameter vector is smaller than the value for the old parameter vector. If a better parameter vector cannot be found by the Gauss-Newton method, a minimum search process is performed. First, a minimum search is carried out along a search path with the highest possible probability of intersecting the valley of the error function. The error function is calculated for a number of points along the curve. If a parameter vector with a smaller error function than the original parameter vector is found, this vector becomes the new parameter vector and the algorithm continues with the Gauss-Newton method from this vector. The error function is evaluated for this parameter vector and if a smaller value is

obtained the algorithm continues with the Gauss-Newton method from this vector. Otherwise, a minimum search along the direction of the Gauss-Newton method is performed. If this search along the direction of the Gauss-Newton method also fails to improve the parameter vector, a search is performed along the direction defined by the steepest descent method. A reduced value of the error function can always be obtained along the direction defined by the steepest descent method.

5.2.3 Least Square Fitting Techniques

Least square fitting techniques uses the saturation voltage in order to separate the data points in the linear and saturation regions. Parameters were obtained from data points in the linear region measured with a small drain-source voltage. The gain and the mobility reduction factors due to the gate-source and the bulk-source voltage can be obtained. The drain current equation was re-arranged to depend linearly on the unknown parameters. These were then calculated using least square fitting techniques. The linearized drain current equation contains a small remainder that depends on the unknown parameters. Therefore the parameters are determined by using an iterative procedure. Another extraction algorithm which is based on a combination of least square fitting techniques and Newton-Raphson iterations can also be regarded as belonging to this approach [13]. The parameters were divided into smaller groups and extracted in the region of operation where they have the most significant influence on the device characteristics.

5.3 Parameter Extraction in S-CMOS Model

Parameter extraction is a very critical part for VLSI circuits development. Parameter extraction performance of the MOS transistor model during circuit simulation depends on the parameter set that is used with the model. Parameter extraction for the MOS transistor model is a complicated task due to the large number of parameters that need to be optimized over a wide range of bias conditions and transistor geometries for the design space. The appropriate extraction methodology depends on the model and is sometimes influenced by particular applications. There are several issues that affect the accuracy of the extraction results, including the optimization strategy, device sizes selected to be optimized, and the number of parameters to be optimized. The important issues that must be resolved in the parameter extraction procedure include: number of transistors and the transistor geometries for which measured data are required, terminal voltage biases for which data are required, and choice of transistor characteristics to be optimized. Some strategies available for extraction parameters: the single device extraction strategy and group device extraction strategy; the extraction for global parameter values and "binning" extraction strategy. In single device extraction strategy, experimental data from a single transistor are used to extract a complete set of model parameters. This strategy will fit on one device very well, but it does not fit other devices with other sizes. Furthermore, single device extraction strategy can not guarantee that the extracted parameters have strong physical meaning. On the other hand, for the short-channel or narrow-channel effects, if we just use the "corner" devices in the extraction, the results might not be properly for the devices with the intermediate geometries. The group device extraction usually requires a device with large channel length and width, one set of devices with different channel length, and one set of devices with different channel width. However, the results might not be the best

"fitting" for each individual device. Furthermore, this type of extraction consumes more computer time for the optimization. The number of devices and their sizes in each set have to be properly determined in order to achieve a good accuracy with reduced extraction time.

5.3.1 Optimization Method

There are two different optimization strategies: local determination and global optimization. Global optimization relies on the explicit use of computer software to find one set of model parameters which will best fit the experimental data. This methodology may produce the minimum average error between measured and simulated data points.

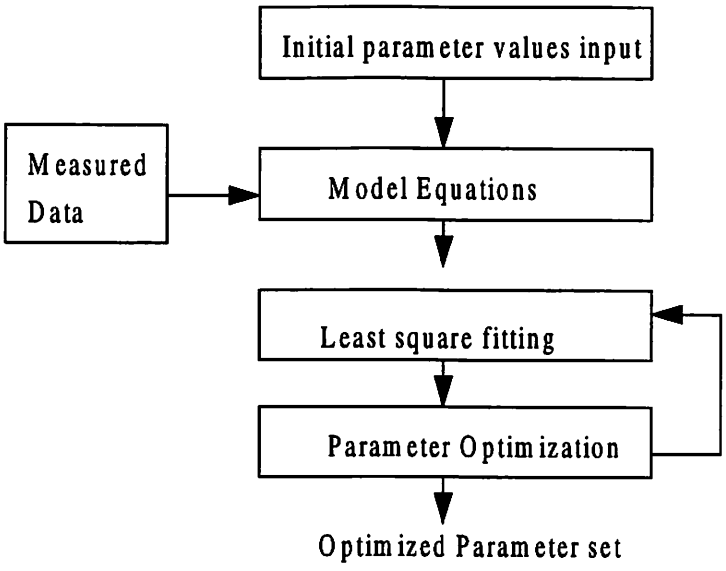


Figure 5.1 Flow of the parameter extraction optimization procedure in S-CMOS

But it also treats each parameter as an empirical parameter without strong consideration of their physical meaning. In the local determination approach, many parameters are extracted independently. Parameters are extracted from unique bias conditions which correspond to the dominant physical mechanisms. To properly execute the local determina-

tion, the bias condition has to be carefully selected for each extraction step. A combination of the local determination and global optimization will be most suitable. To estimate a desired random vector from observable random vector, minimum mean squared error estimation (MMSE) is used.

5.3.2 Multi-objective parameter extraction

Conventional techniques are based one I_{DS} optimization because digital circuit designers need to accurately predict the drain current of transistors in circuit simulation. However, output conductance affect accurate prediction of voltage gain and frequency-domain behavior in analog circuit design. A multi-objective function was proposed by Gowda, et al [4]. In this work, more simple and efficient function is implemented in parameter extraction program.

$$\left\|e(p_k)\right\|^2 = \sum_{i=1}^{N} e(p_k)^2 = \sum_{i=1}^{N} \left(\frac{I_i(p_k) - I_{i(measured)}}{max(I_i, I_{min})} \right)^2$$

$$+ W_{gd} \sum_{i=1}^{N} \left(\frac{g_{ds_i}(p_k) - g_{ds_{i(measured)}}}{max(g_{ds_i}, g_{ds_{min}})} \right)^2$$

$$+ W_{gm} \sum_{i=1}^{N} \left(\frac{g_{m_i}(p_k) - g_{m_{i(measured)}}}{max(g_{m_i}, g_{m_{min}})} \right)^2 . \qquad (5.2)$$

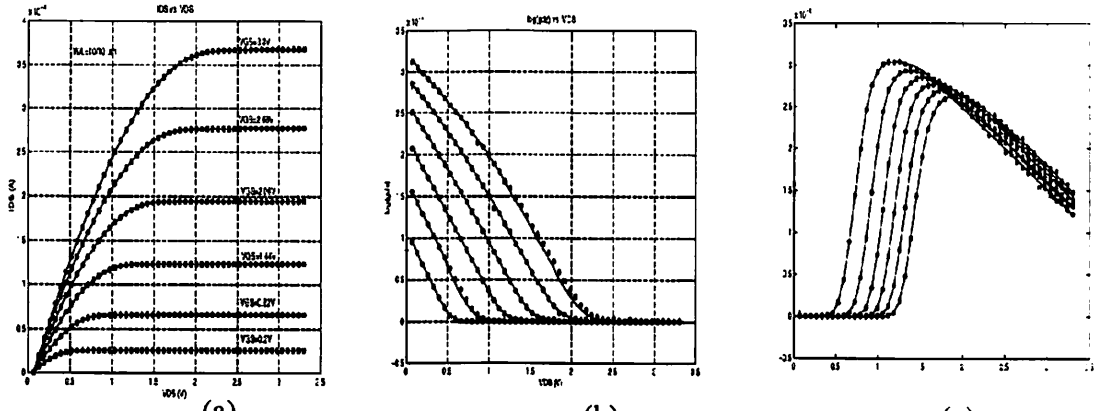


Figure 5.2: Measured versus simulated results for NMOS Transistor (a)I_{DS} vs. V_{DS} (b) g_{ds} vs. V_{DS} (c) g_m vs. V_{GS} with W/L=10μm/10μm.

5.3.3 Extraction Strategies

Two different strategies are available for extracting parameters: the single device extraction strategy and group device extraction strategy. In single device extraction strategy, experimental data from a single device are used to extract a complete set of model parameters. This strategy will fit one device very well but will not fit other devices with different geometries. Furthermore, single device extraction strategy can not guarantee that the extracted parameters are physical. If only one set of channel length and width is used, parameters related to channel length and channel width dependencies can not be determined. S-CMOS uses group device extraction strategy. This requires measured data from devices with different geometries. All devices are measured under the same bias conditions.

5.3.4 Geometric Space

Most of the MOS models were developed to cover all the device geometries of the design space with one set of parameter values. However, the extraction accuracy is usually not suitable for various applications. The key reasons are improper inclusion of higher-order effects in the model expressions and selection of parameters. A very common solution used in the microelectronics industry is "binning", which breaks the whole geometry space into sub-regions. The extraction is done within each sub-region. shows an example of binning sub-regions. Partitioning of the sub-regions depends on the specific application and the given fabrication technology. This approach provides higher accuracy but requires more extraction time. In order to accommodate the binning for better results, there is an explicit formula for parameters which is introduced by HSPICE Level-28 model as an extension to the original BSIM model, The reference geometries which are the right-upper corner devices of the sub-regions are introduced to enhance the accuracy. By doing so, the number of parameters becomes quadrupled. In fact, it is not necessary to apply this structure to all the parameters. Advanced digital and analog VLSI circuits could require the use of transistors that are distributed over a large geometric space. In general, only a small region of the geometric design space is characterized in the laboratory in order to extract parameter values. The transistor model must enable circuit designers to explore the geometric space beyond the region of characterization. One conventional approach to providing transistor model parameter values over a large geometric space involves partitioning the geometric space into several bins as shown in Fig.5.3. In each bin, a parameter set is extracted with the intention of providing maximum accuracy within that bin. In this way, high accuracy can be achieved over a large geometric space without producing abnormal results in any of the bins where parameters are extracted. However, the problem in this

approach lies in the transition from one geometric bin to another. Since the parameter sets used in two adjacent bins are extracted separately using data from different sets of transistors, the drain current may not vary monotonically across the boundary between the two bins.

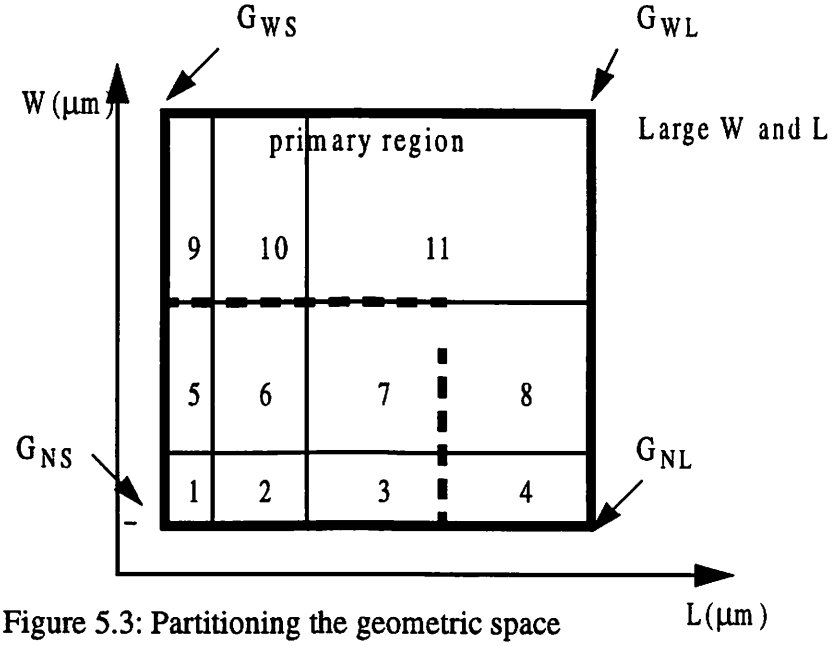


Figure 5.3: Partitioning the geometric space

This is in contradiction to the principles of device operation and observations of measurement results. Such non-monotonically can also cause convergence problems in automatic circuit synthesis programs that use circuit simulation results to search across the geometric design space. The multiple-bin approach also fails to address the problem of modeling transistors beyond the periphery of the characterized region. These include long-channel transistors used in the design of analog circuits, wide-channel transistors used in special digital driver circuits, and small-geometry transistors that can be used to predict the effect of using next-generation technologies. The method involves clamping the evaluation of second-order effects at the boundaries of a primary region as shown in Fig. 5.3 [4]. The primary region is determined by using the criterion that abnormal drain current character-

istics are not produced during simulation of transistors within this region. The upper and lower length bounds of the primary region are L_{lng} and L_{sht}, while the corresponding width bounds are W_{wid} and W_{nrw}, respectively. The first-order scaling of the drain current with geometry is done by the W/L term that is given in the following saturation drain current expression. The effective channel width and length of the transistor are used in the calculation of this W/L term over the entire geometric design space. In the evaluation of other second-order geometric dependencies, the length and width to be used are determined according to,

$$L = \begin{cases} L_{NS}, & if\ L \le L_{SN} \\ L_{WL}, & if\ L > L_{LN} \end{cases}, \tag{5.3}$$

$$W = \begin{cases} W_{NS}, & if\ W \le W_{NS} \\ W_{WL}, & if\ W > W_{WL} \end{cases}. \tag{5.4}$$

This is a set of conditional constraints that modifies the geometric dependence scheme in order to extend the use of a parameter set. For transistors beyond the primary region, the second-order effects are evaluated at the boundaries of the primary region. The effectiveness of the this method depends upon the suitable determination of the bounds L_{sht}, L_{lng}, W_{nrw}, and W_{wid}. The upper length and width bounds of the primary region, L_{lng} and W_{wid}, can be defined as the longest length and widest width of the transistors used for actual parameter extraction. The lower length and width bounds are L_{sht} and W_{nrw}. L_{sht} and W_{nrw} represent the geometries at which physical constraints are violated and abnormal results are produced by the geometry dependence terms of the model. Choosing the

lower bounds in this manner allows increased exploitation of the accuracy that is included in the small-geometry effect terms of the model.

5.4 S-CMOS Parameter Extraction Phases

5.4.1 Parameter Extraction Phase

Parameter extraction proceeds in three distinct phases. A long, wide device is once again used as a base, to which small geometry effects are added as corrections. Here parameter extraction will proceed as follows: The oxide thickness and the differences between the drawn and effective channel dimensions are provided as process input. In the first phase of parameter extraction, a long, wide device is used to determine some base parameters, which are used as the starting point for each individual device extraction of the second phase. In the second phase, a set of parameters is extracted independently for each device, using the parameter results of the first phase as the starting point for each particular device. Once again, this phase represents the fitting of the data for each independent device to the intrinsic equation structure of the model. In the third phase, the compiled parameters from the second phase are used to determine the geometry parameters; this represents the imposition of the extrinsic structure onto the model.

(A) The First Phase

In this phase of parameter extraction, a long, wide device is used to determine a set of base parameters, which is used as the starting point for the second-phase extractions. In the first step, fitting is done to the linear characteristic with no substrate biases applied. In

the second step, the linear characteristic is employed with substrate biases applied. For the third step, the linear characteristic is once again used with substrate biases applied, to extract the parameter.

(B)The Second Phase

The second phase of parameter extraction involves the independent fitting of each device to the intrinsic model structure. The procedure described here is repeated for each device that is being used. For the first step, fitting is done for the linear characteristic with substrate biases applied. This step uses a longer (10/1.0)μm device, and a narrow (0.4/ 3.6)μm device. The option is used here of extracting a value of the low field mobility MUO for each device. In the second step, the saturation characteristic is used with no substrate biases applied. Once again, the results represent an improvement over the situation with BSIM; however, some minor fitting difficulties are still present in the short (10/0.4)μm device and the narrow (0.4/3.6)μm device. The third step makes use of the saturation characteristic with substrate biases applied. In a submicron channel length (3.6/ 0.4)μm device, the result (in contrast to BSIM) is qualitatively correct. In a longer channel (10/10)μm device, the result is quantitatively better. The subthreshold characteristics are used in the fourth step. The final step involves the fitting of the output conductance characteristics. A slight improvement can be obtained by extracting the output conductance fitting parameters.

(C) The Third Phase

The third phase of parameter extraction involves using the compiled list of independent device parameters, which were determined during the second phase, as data for the extraction of the length and width parameters that form the extrinsic part of the model structure. In the third phase of model construction, the parameters compiled for each device in the second phase are used to build the extrinsic model structure. This involves the determination of the geometry parameters for each bin.

The S-CMOS model uses a selective way to include the geometry dependence only in certain parameters, e.g., γ_{1L}, K_{NZ}, etc. With this development technique, the model parameter set can be minimized while includes most of the small-geometry effects. The efficient DC parameter extraction is designed based on the properties of the CMOS model by considering the physical behavior of each parameter in the model equations.

5.4.2 Data Measurement

In general, the procedure consists of measuring the output of three devices:

- a large device with a long channel and wide channel,
- a wide channel a narrow channel device
- a short channel device

The measurement on these three devices provides sufficient information for extracting a full set of model parameters, including the channel length and width dependence. As previously noted, this measurement is performed only on the short channel device. This measurement provides the information in the saturation region, and is used to extract the

saturation parameters. After completing the measurement procedure, execute the extraction command on the same Setups. In DC parameter extraction, the extracted parameters are directly related to the geometries of the devices. To extract DC model parameters, it must have the correct L (drawn or mask channel length) and W (drawn or mask channel width) device parameters with which to work. Before executing an extraction or simulation, to make sure the L and W parameters are correct. Before starting the extraction, enter several process parameters.

5.5 S-CMOS Parameter Extraction Process

5.5.1 The Parameter Extraction procedure

In order to simplify the initial extraction condition, the extraction should be started from a large device to exclude the short-channel and narrow-channel effects. The threshold voltage is the first step to be focused. The parameters, γ_1, and $V_{FB,}$ can be extracted. The zero-bulk biased threshold voltage, $V_{tho} = V_{FB} + \phi_s$, is extracted from the I_{DS} vs. V_{GS} measurement. The short-channel and narrow-channel effects on the threshold voltage are extracted by optimizing the expression with the measured data of the threshold voltages on different transistors with different channel lengths, and channel widths, respectively. The reverse short-channel effect modeled by η_1, η_2, and η_3 is extracted from the threshold voltages with different channel lengths.

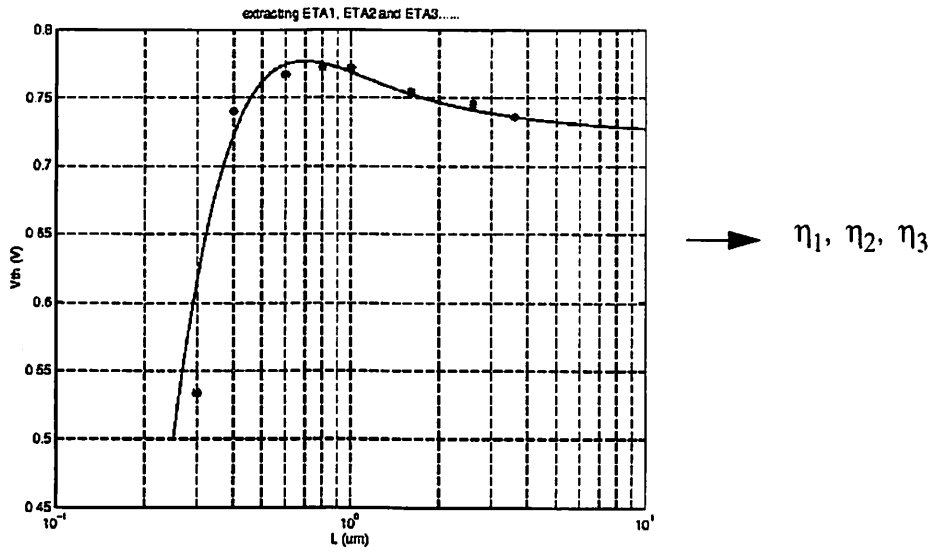


Figure 5.4 : Parameter extraction step for reverse short channel effects

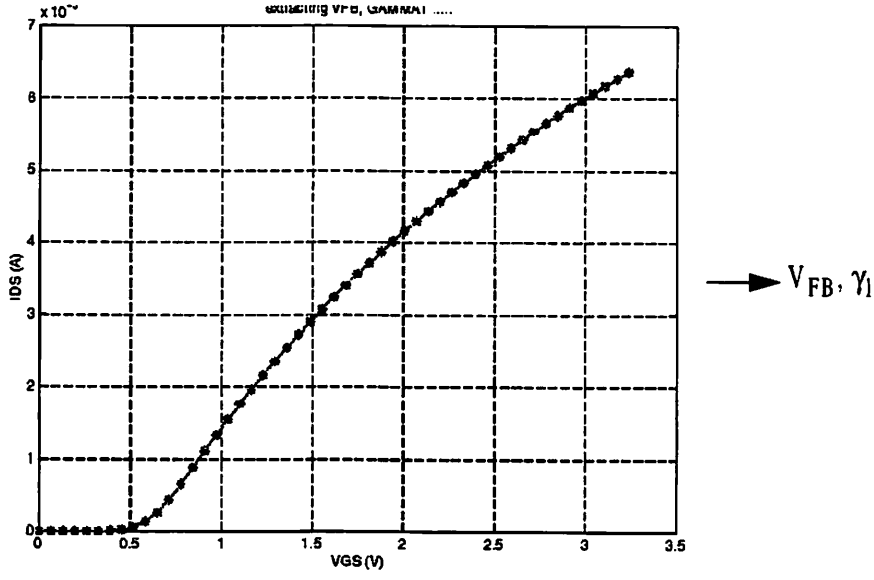
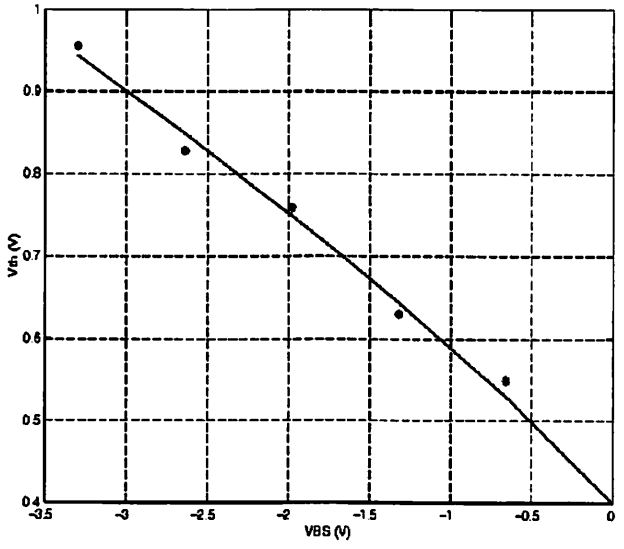


Figure 5.5 : Parameter extraction step for flat band voltage and zero-bias body effect

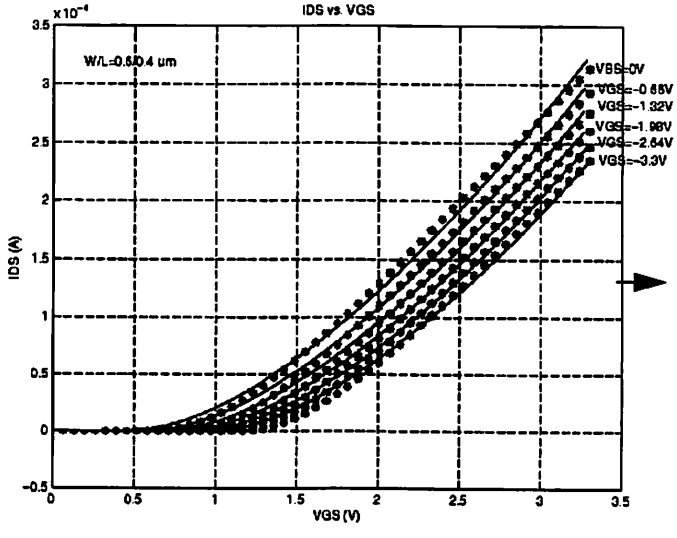
The extraction of non-uniform substrate doping effect parameters, γ_2, K_S, is done by curve fitting. In order to extract the intrinsic mobility and vertical field-effect parameter values,

the measured data have to be done with a small V_{DS} value to reduce saturation-region effects.



→ K_S, γ_2

Figure5.6 : Parameter extraction step for depletion charge sharing and high-bias body-effect



→ $\mu 0$, U_{GSZ}, U_{GSG2}, U_{BS}

Figure 5.7: Parameter extraction step for mobility degradation effect

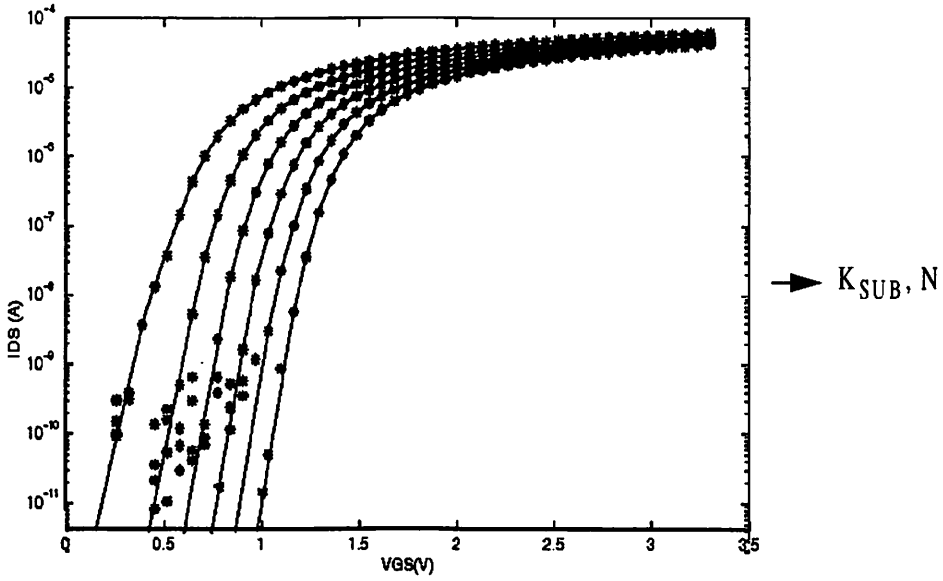


Figure 5.8: Parameter extraction step for subthreshold current shifting

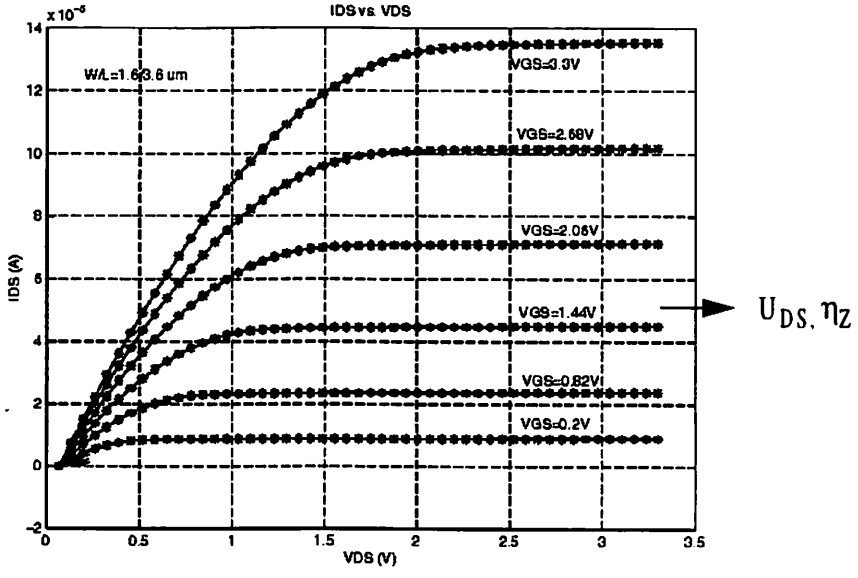


Figure 5.9: Parameter extraction step for Drain induced barrier lowering effect

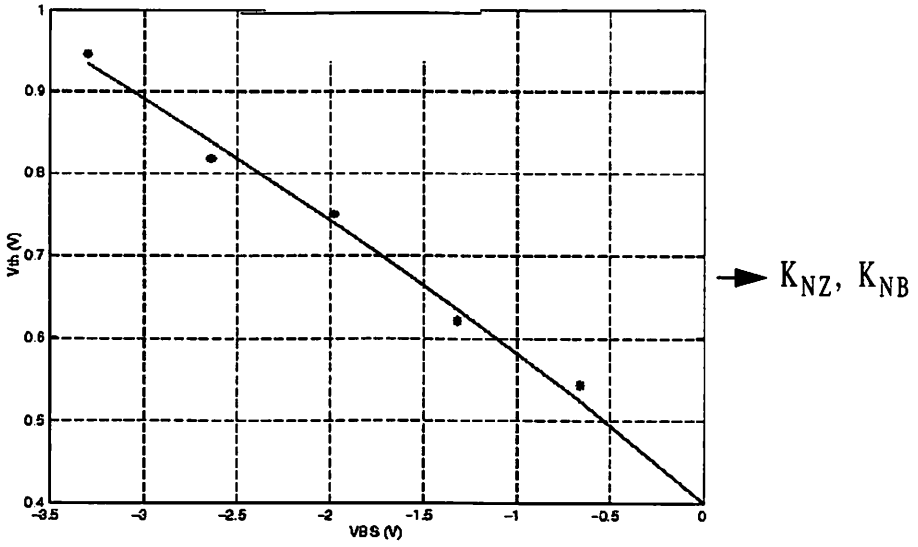


Figure 5.10: Parameter extraction step for narrow channel threshold voltage

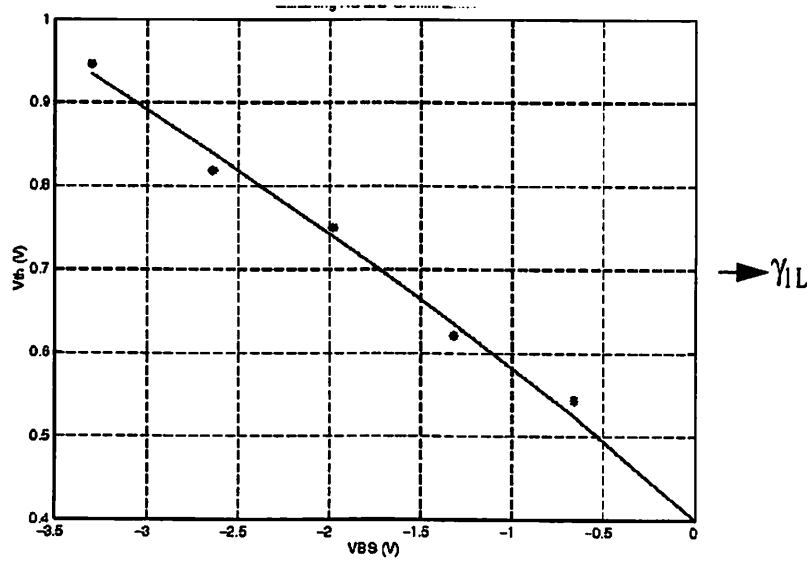


Figure 5.11: Parameter extraction step for short channel body effects

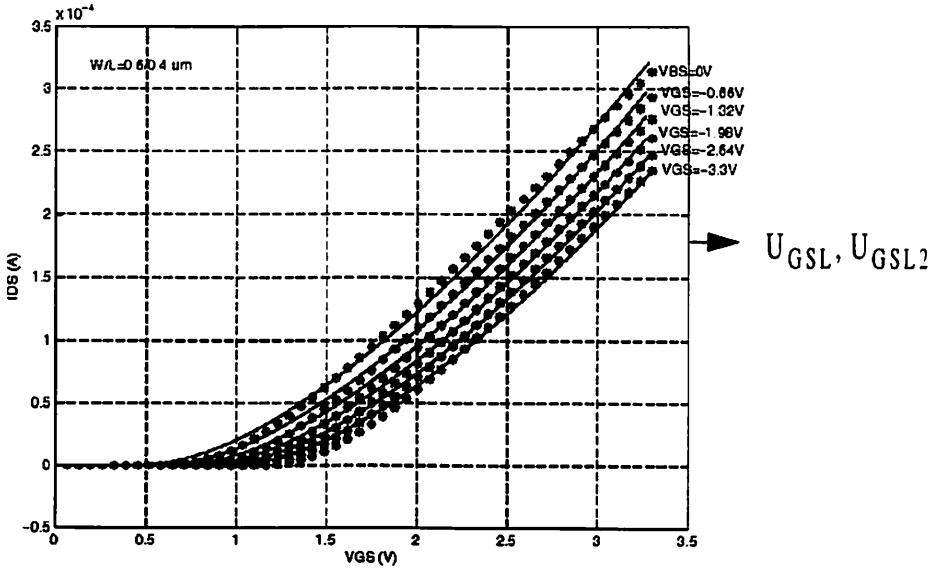


Figure 5.12 : Parameter extraction step for gate-voltage mobility degradation

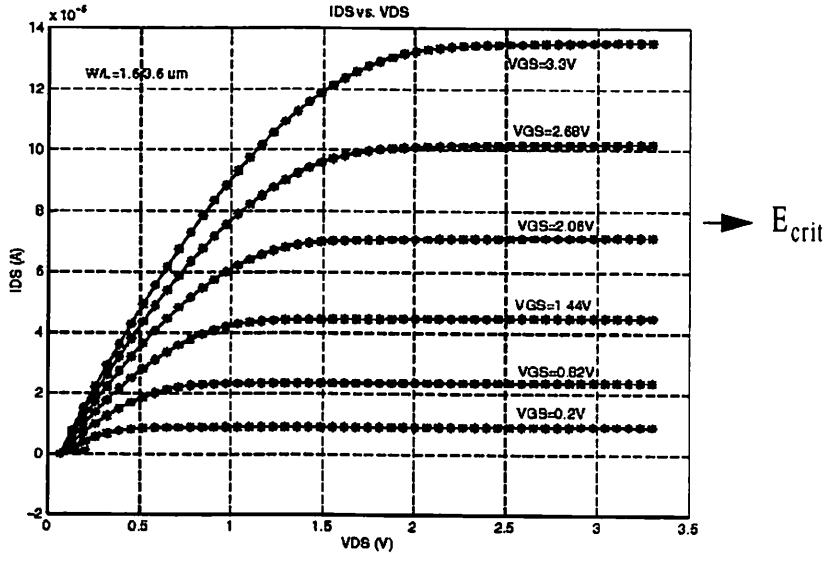


Figure 5.13 : Parameter extraction step for critical electrical field

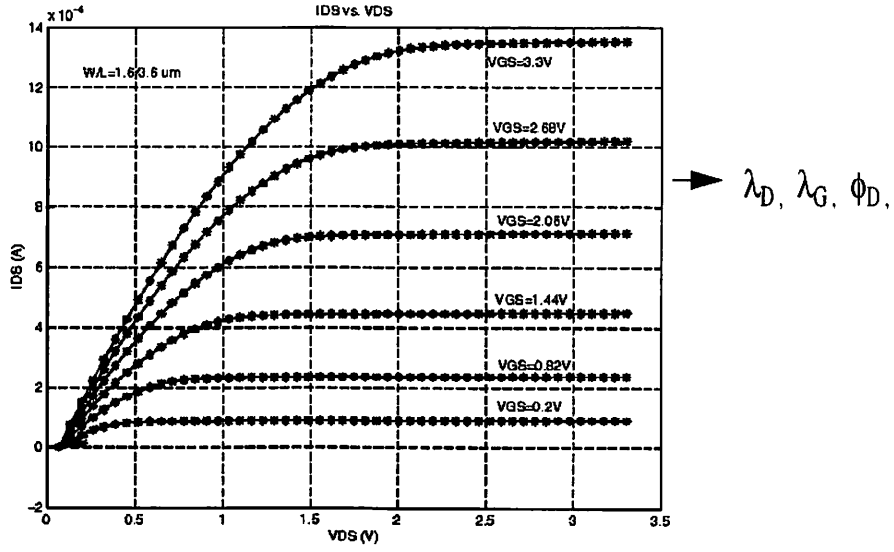


Figure 5.14 : Parameter extraction step for Channel Length Modulation Effects

The subthreshold parameters, K_{sub} and N, are extracted by optimizing the I_{DS} characteristics in the weak-inversion region. The critical field parameter, E_{crit}, affects the saturation voltage and velocity saturation effect. It can be extracted by optimizing the I_{DS} vs. V_{DS} characteristics. The channel-length modulation effect parameters are used to model the output conductance characteristics in the saturation region especially for short-channel devices. Therefore the extraction should be done by fitting drain current and output conductance curves in the saturation regions. All the smooth function parameters are extracted at the last step to fine-tune the behavior at the transitions between different operation regions.

5.5.2 Model Parameter Extractor in MATLAB

In most of model extractions, either the specific extraction software or the interface between the optimization program and SPICE simulator are required in order to extract the parameters of a specific model. Usually, the extraction program is implemented by the user instead of the model developer. This may result in user-dependent parameter values and accuracy due to the understanding of model characteristics. All the measured data are stored in the data bank. The MOS model equations, parameter set, and all the optimization steps are implemented in the separate m-code functions. The minimum set of transistors for the complete extraction includes a large transistor, a short-channel transistor, and a narrow-channel transistor. All of those transistors should include the measured data of V_{DSAT} versus V_G, I_{DS} versus V_{GS} with different V_{BS}'s, and I_{DS} versus V_{DS} with different V_{GS}'s. For extracting the reverse short-channel effect and accurately of threshold voltage for different channel lengths has to be performed. The extraction starts from the zero-bias threshold voltage, Vth, which can be obtained from V_{DSAT} versus V_{GS} measurement, i.e., $V_{th} = V_{GS}$, $V_{DSAT} = 0$. As shown in Fig.5.4, parameters, η_1, η_2, and η_3, can be extracted by fitting the threshold voltage behavior with $V_{BS} = 0V$ and V_{DS} being close to 0V.

The flat-band voltage, V_{FB}, and body-effect coefficient, γ_1, are the major parameters affecting the saturation voltage behavior, V_{DSAT}. Therefore, they can be extracted from a large transistor, as shown in Fig. 5.5. The non-uniform substrate doping effect causes the change of threshold voltage with different V_{BS} biases. This effect is modeled by parameters, γ_1, γ_2 and K_S to include the second-order term. Fig 5.6 shows the extraction of γ_2 and K_S values from Vth versus V_{BS} with a small V_{DS} to exclude the drain-induced barrier

lowering effect. Once the threshold voltage characteristics of a large device are determined, the drain current characteristics can be used to extract the effective mobility. In MOSFET, the effective mobility is described by a reduction factor to include the vertical- and horizontal-field effects. With a large device, the effects of the mobility reduction are observed. To extract the vertical-field effect, the I_{DS} versus V_{GS} characteristics with different V_{BS} biases are used to determine the intrinsic mobility, μ_0, and parameters, U_{GSZ}, U_{GSZ2} and U_{BS}. Notice that, in this step, the horizontal-field effect has to be excluded by setting V_{DS} = 0.05V. The results of this step are shown in Fig.5.9. The horizontal-field effect on effective mobility modeling by parameter, U_{DS}, as well as the drain-induced-barrier-lowering effect by parameter η_z, therefore, can be seen and extracted from the I_{DS} versus V_{DS} characteristics. In the weak-inversion operation, the drain current is contributed by the diffusion current, which is modeled, in logarithmic domain, by a slope factor, n, and an offset factor, Ksub. Thus, those two parameters are extracted by optimizing the weak-inversion current characteristics. In the short-channel and narrow-width transistors, the body effect is affected by the channel width and length. Those effects are modeled by parameters, K_{NZ}, K_{NB}, and γ_{1L}, and can be extracted from the behavior of V_{th} versus V_{BS}, as shown in Fig. 5.10. and Fig. 5.11. To analyze the short-channel effect on effective mobility and velocity saturation, the I_{DS} versus V_{GS} and the I_{DS} versus V_{DS} characteristics of a short-channel transistor have to be used. The vertical-field effects on the effective mobility for short-channel transistors are modeled by parameters U_{GSL} and U_{GSL2} as shown in Fig. 5.12, and the velocity saturation effect is modeled by the critical field, Ecrit as shown in Fig. 5.13. The channel-length modulation effect is more significant for the

short-channel transistors, and is to be extracted from the I_{DS} versus V_{DS} in the saturation region. All the smooth function parameters are fine-tuned in the last step by optimizing the transition portion between different operation regions as shown in Fig. 5.14. The parameters are extracted in the following procedure as shown in Fig. 15. These procedures are based on understanding of physical meaning of the model and based on local input parameters names.

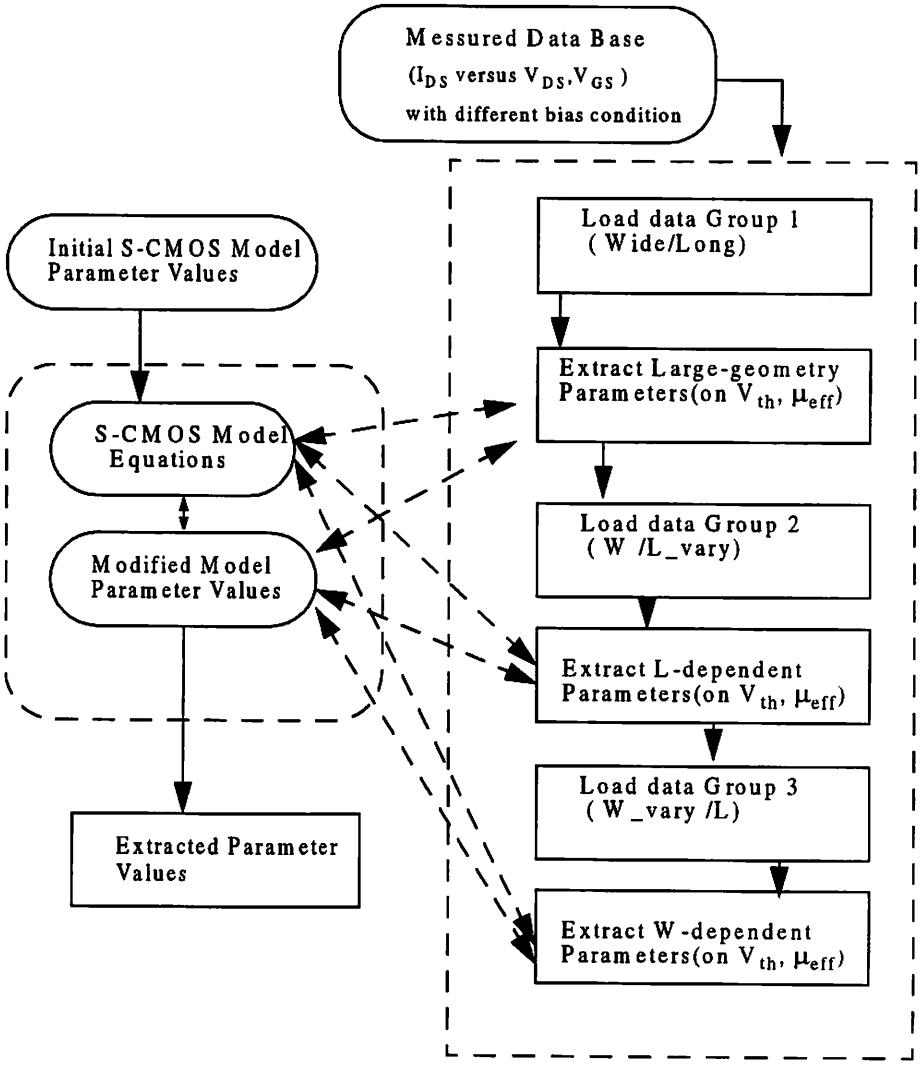


Figure 5.15 Parameter extraction procedure of S-CMOS Model

TABLE 5.1 S-CMOS Default Model Parameter Values

Name	Description	Unit	NMOS (value)	PMOS (value)
ϕs	Surface inversion potential	V	0.36	0.32
V_{FB}	Flat band voltage	V	-0.4	-0.43
Tox	Gate oxide thickness	nm	79	79
μ_0	intrinsic surface mobility	$cm^2/v.s$	450	130
δL	Channel length reduction	μm	0	0
δW	Channel width reduction	μm	0	0
γ_1	Zero-bias body-effect coefficient	$V^{0.5}$	0.421	0.563
γ_{1L}	Zero-bias short channel body-effect coefficient	$V^{0.5}\mu m$	0.03	0.06
γ_2	High-bias body-effect coefficient	$V^{0.5}$	0.328	0.309
Ks	depletion charge-sharing coeff.	-	2.7	34
Knz	Narrow width threshold voltage coeff.	$V^{0.5}\mu m$	0.244	0.217
Knb	Narrow width threshold voltage sub-strate coeff.	μm	5.4e-4	-3.9e-4
ηz	Drain induced barrier lowering coeff.	-	0.002	-0.005
ηL	Short channel drain induced barrier lowering coeff.	μm	0.001	0.083
$\eta 1$	Short channel threshold voltage reduction coeff.	$V.\mu m$	0.3277	0.3577
$\eta 2$	Characteristics length of reverse short channel effect	$V.\mu m$	0.3755	0.4355
$\eta 3$	reverse short channel effect coeff.	μm	0.3555	0.2205
Ugsz	Gate-voltage mobility degradation coeff.	V^{-1}	0.02	0.1
Ugsz2	Gate-voltage mobility degradation 2nd order coeff.	V^{-1}	0.02	0.1

TABLE 5.1 S-CMOS Default Model Parameter Values

Name	Description	Unit	NMOS (value)	PMOS (value)
UgsL	Short channel adjustment of Ugsz	$V^{-1}\mu m$	0.06	-0.1
U_{GSL2}	Second order Short channel adjustment of Ugsz	$V^{-1}\mu m$	0.06	-0.1
U_{DS}	Drain voltage mobility degradation coeff.	$V^{-1}\mu m$	0.08	0.01
U_{BS}	Substrate voltage mobility degradation coeff.	V^{-1}	0.005	0.02
N	Substrate drain current slope	-	1.5	1.5
K_{SUB}	Subthreshold current shifting coefficient	-	5	0.1
Ecrit	Critical electrical field for velocity saturation	V/μm	10	10
λd	Drain voltage dependent CLME coeff	V^{-1}	0.01	1.15
λg	Gate voltage dependent CLME coeff	$V^{3/2}$	0.1	3.5
λb	Substrate voltage shifting CLME coeff	-	2	2
λbs	Substrate voltage dependent CLME coeff	V	1	1
ϕd	Drain voltage related CLME potential	V	0.5	0.1
K_{BSh}	Bulk bias hyperbola function coeff.	-	1.01	1.01
K_{DSATh}	Strong inversion hyperbola function coeff.	-	1.03	1.05
K_{GSh}	Gate threshold hyperbola function coeff.	-	1.01	1.01
K_{sig}	Sigmoid function coeff.	-	1.01	1.01
Bm	Mobility temperature dependency coeff	-	1.5	1.5
Bvth	Threshold voltage temperature dependency coeff	-	1e-6	1e-6

TABLE 5.1 S-CMOS Default Model Parameter Values

Name	Description	Unit	NMOS (value)	PMOS (value)
Af	Noise effect exponent coeff.	-	1.5	1.5
Kf	Fliker noise effect coeff.	-	1e-19	1f-19

Table5.2.Extracted parameter for CMOS 0.35μm Tech. (10/10, 0.6/10, 10/0.4)

No	Name	Unit	Values	No	Name	Unit	Values
1	V_{FB}	V	-0.7043	11	U_{DS}	V^{-1}	-0.0334
2	ϕs	V	1.2626	12	ηz	-	4.539e-9
3	γ_1	$V^{0.5}\mu m$	0.8345	13	Knz	$V^{-}\cdot\mu m$	-0.0780
4	Ks	-	-0.2511	14	Knb	$\cdot\mu m$	-0.0476
5	γ_2	$V^{0.5}$	0.328	15	γ_{1L}	$V^{0.5}\mu m$	0.12207
6	μ_0	$cm^2/v.s$	444	16	U_{GSL}	$V^{-1}\cdot\mu m$	-0.090
7	Ugsz	V^{-1}	0.8345	17	U_{GSL2}	$V^{-1}\cdot\mu m$	0.0479
8	U_{BS}	V^{-1}	-0.1341	18	Ecrit	V/μm	10.799
9	K_{SUB}	-	-0.97111	19	λd	V^{-1}	0.0667
10	N	-	1.6	20	λg	$V^{3/2}$	-0.1145

Table5.3. Extracted parameter for CMOS 0.35μmTech.(10/10, 0.6/10, 10/0.4).

No	Name	Unit	Values	No	Name	Unit	Values
1	V_{FB}	V	-0.704	11	U_{DS}	V^{-1}	-0.03348
2	ϕs	V	1.262	12	ηz	-	8.48e-9
3	γ_1	$V^{0.5}\mu m$	0.825	13	Knz	$V^{-}\cdot\mu m$	-0.0752
4	Ks	-	-0.2511	14	Knb	$\cdot\mu m$	-0.0465
5	γ_2	$V^{0.5}$	0.328	15	γ_{1L}	$V^{0.5}\mu m$	0.328
6	μ_0	$cm^2/v.s$	447	16	U_{GSL}	$V^{-1}\cdot\mu m$	0.2093
7	Ugsz	V^{-1}	0.20938	17	U_{GSL2}	$V^{-1}\cdot\mu m$	0.0479

Table5.3. Extracted parameter for CMOS 0.35μmTech.(10/10, 0.6/10, 10/0.4)

No	Name	Unit	Values	No	Name	Unit	Values
8	U_{BS}	V^{-1}	-0.1341	18	Ecrit	V/μm	12.5
9	K_{SUB}	-	-0.96114	19	λd	V^{-1}	0.0101
10	N	-	1.6	20	λg	$V^{3/2}$	1.1759

Table5.4.Extracted parameter for CMOS 0.35μm Tech.(10/0.4,0.6/0.4, 5/0.4)

No	Name	Unit	Values	No	Name	Unit	Values
1	V_{FB}	V	-0.033	11	U_{DS}	V^{-1}	-0.09979
2	φs	V	0.717	12	ηz	-	3.11e-8
3	γ_1	$V^{0.5}\mu m$	0.9790	13	Knz	$V^{-1}\cdot\mu m$	0.0469
4	Ks	-	-0.3966	14	Knb	$\cdot\mu m$	0.03576
5	γ_2	$V^{0.5}$	0.328	15	γ_{1L}	$V^{0.5}\mu m$	0.328
6	μ_0	$cm^2/v.s$	458	16	U_{GSL}	$V^{-1}\cdot\mu m$	0.0158
7	Ugsz	V^{-1}	0.1635	17	U_{GSL2}	$V^{-1}\cdot\mu m$	0.0479
8	U_{BS}	V^{-1}	-0.0839	18	Ecrit	V/μm	21.82
9	K_{SUB}	-	-0.1998	19	λd	V^{-1}	0.02365
10	N	-	1.69	20	λg	$V^{3/2}$	0.514

Table5.5. Extracted parameter for CMOS 0.35μmTech.(10/0.4, 0.6/0.4,1.2/0.4)

No	Name	Unit	Values	No	Name	Unit	Values
1	V_{FB}	V	0.0233	11	U_{DS}	V^{-1}	0.13254
2	φs	V	0.7037	12	ηz	-	1.15e-8
3	γ_1	$V^{0.5}\mu m$	0.8634	13	Knz	$V^{-1}\cdot\mu m$	0.11429
4	Ks	-	-0.3832	14	Knb	$\cdot\mu m$	0.04768
5	γ_2	$V^{0.5}$	0.328	15	γ_{1L}	$V^{0.5}\mu m$	0.328

Table5.5. Extracted parameter for CMOS 0.35μmTech.(10/0.4, 0.6/0.4,1.2/0.4)

No	Name	Unit	Values	No	Name	Unit	Values
6	μ_0	$cm^2/v.s$	444.7	16	U_{GSL}	$V^{-1}\cdot\mu m$	0.5165
7	Ugsz	V^{-1}	0.26496	17	U_{GSL2}	$V^{-1}\cdot\mu m$	0.0479
8	U_{BS}	V^{-1}	-0.0734	18	Ecrit	V/μm	9.98
9	K_{SUB}	-	-1.4597	19	λd	V^{-1}	0.1484
10	N	-	1.39	20	λg	$V^{3/2}$	0.48566

Table5.6. Extracted parameter for CMOS 0.35μmTech.(10/10, 0.6/10, 5/0.4)

No	Name	Unit	Values	No	Name	Unit	Values
1	V_{FB}	V	-0.7043	11	U_{DS}	V^{-1}	-0.0334
2	φs	V	1.262	12	ηz	-	-3.66e-8
3	γ_1	$V^{0.5}\mu m$	0.8345	13	Knz	$V^{-}\cdot\mu m$	-0.0476
4	Ks	-	-0.0780	14	Knb	$\cdot\mu m$	0.00977
5	γ_2	$V^{0.5}$	-0.2511	15	γ_{1L}	$V^{0.5}\mu m$	0.328
6	μ_0	$cm^2/v.s$	900	16	U_{GSL}	$V^{-1}\cdot\mu m$	-0.0267
7	Ugsz	V^{-1}	0.1053	17	U_{GSL2}	$V^{-1}\cdot\mu m$	0.0479
8	U_{BS}	V^{-1}	-0.13410	18	Ecrit	V/μm	9.55
9	K_{SUB}	-	2.0	19	λd	V^{-1}	5.88e-8
10	N	-	1.6003	20	λg	$V^{3/2}$	-0.03797

Table5.7. Extracted parameter for CMOS 0.35μmTech.(10/10, 0.6/10, 10/0.4)

No	Name	Unit	Values	No	Name	Unit	Values
1	V_{FB}	V	-0.599	11	U_{DS}	V^{-1}	-0.096
2	φs	V	1.146	12	ηz	-	-0.107e-8
3	γ_1	$V^{0.5}\mu m$	1.646	13	Knz	$V^{-}\cdot\mu m$	-0.03127
4	Ks	-	-0.343	14	Knb	$\cdot\mu m$	0.00894
5	γ_2	$V^{0.5}$	0.328	15	γ_{1L}	$V^{0.5}\mu m$	0.328

Table5.7. Extracted parameter for CMOS 0.35μmTech.(10/10, 0.6/10, 10/0.4)

No	Name	Unit	Values	No	Name	Unit	Values
6	μ_0	$cm^2/v.s$	600.7	16	U_{GSL}	$V^{-1}\cdot\mu m$	0.2505
7	Ugsz	V^{-1}	0.2615	17	U_{GSL2}	$V^{-1}\cdot\mu m$	0.0479
8	U_{BS}	V^{-1}	-0.31377	18	Ecrit	V/μm	17.53
9	K_{SUB}	-	-0.8519	19	λd	V^{-1}	0.1883
10	N	-	1.759	20	λg	$V^{3/2}$	1.337

Table5.8. Extracted parameter for CMOS 0.35μmTech.(2.5/1, 0.6/1, 2.5/0.4)

No	Name	Unit	Values	No	Name	Unit	Values
1	V_{FB}	V	0.2521	11	U_{DS}	V^{-1}	-0.0139
2	φs	V	0.8339	12	ηz	-	-4.09e-8
3	γ_1	$V^{0.5}\mu m$	0.9659	13	Knz	$V^{-}\cdot\mu m$	-0.0317
4	Ks	-	-2.4421	14	Knb	$\cdot\mu m$	0.0178
5	γ_2	$V^{0.5}$	0.3280	15	γ_{1L}	$V^{0.5}\mu m$	0.328
6	μ_0	$cm^2/v.s$	596	16	U_{GSL}	$V^{-1}\cdot\mu m$	1.589
7	Ugsz	V^{-1}	0.3870	17	U_{GSL2}	$V^{-1}\cdot\mu m$	0.0479
8	U_{BS}	V^{-1}	-0.217	18	Ecrit	V/μm	14.68
9	K_{SUB}	-	-1.194	19	λd	V^{-1}	-0.21624
10	N	-	1.39	20	λg	$V^{3/2}$	0.48566

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Chapter 6

S-CMOS Model Implementation

In this chapter, the implementation of the model in SPICE3f3 and is presented The performances comparison of S-CMOS, MOS Level2, Level, BSIM1, and BSIM3v3 models in circuits simulation including folded cascode Op Amp, analog multiplier, comparator, 8-bit carry save adder, and 8-bitx8bit carry save multiplier is demonstrated. Efficient 8-bitx8bit divider design and simulation results are included.

6.1 Implementation to SPICE3f3 Simulator

During the 1960's, two complementary trends combined to provide both the requirements and abilities to simulate electronic circuits. As circuits grew larger and more complex, it became desirable to simulate their behavior on an electronic computer, rather than through the traditional bread board evaluation. This was particularly true as the integrated circuit appeared on the scene; with hundreds and then thousands of transistors, the task of setting up a circuit on a breadboard was becoming complicated to

the point of impossibility. At the same time, as computational power was increasing, it became possible to create a simulation program that would provide accurate answers in a reasonable amount of time. In the best engineering tradition, growing complexity led to a clever solution. Although this approach is taken for granted now, at the time of its introduction, the concept was somewhat revolutionary. Rather than employing an iterative succession of breadboarding and testing of designs, a circuit would be designed, evaluated, and redesigned using only computer simulation. The Simulation Program with Integrated Circuit Emphasis (SPICE) circuit simulator was the result of this new approach to circuit design [12,13]. The original SPICE core was developed at the University of California/Berkeley in the late 1960's, as a successor to a first attempt at a computer-aided circuit simulator with the somewhat egregious name of Computer Analysis of Nonlinear Circuits Excluding Radiation (CANCER) [14]. In SPICE, any circuit is treated in a node/element fashion; the circuit is depicted as a collection of various elements (e.g., resistors, capacitors, etc.) connected at numbered nodes. The circuit is described in its entirety by the number of nodes and elements it contains, and by the nodes to which each particular element is connected. In a circuit with n nodes, the SPICE representation can be thought of as an nxn matrix. If two nodes are connected by some element, the corresponding matrix element will be nonzero. By defining one or more state variables (such as the voltage) at each node, and fixing the state variables at external nodes (such as the power supply, ground, etc.), the matrix can be solved to determine the values of the state variables at the various internal circuit nodes. To reach a solution, models specific to any particular circuit element are required. In this form, the circuit can be handled by the main program, while the element models are subroutines

that are called when the behavior of an element must be evaluated. In addition to SPICE, there are a number of circuit simulation programs which employ the same basic approach. However, SPICE has become the dominant circuit simulator for two reasons. First, the entire SPICE package, including the program code itself, was (and continues to be) made available by the University of California/Berkeley for a very small nominal fee. Thus, it was obtain to purchase ready-to-run SPICE for circuit simulation, or to acquire the core program and customize it for the user's own purposes. Second, SPICE became available in the right place at the right time. Its availability coincided with the nearby growth of the integrated circuit industry, and was thus easily adopted as the circuit simulation standard.

Because of this widespread adoption, SPICE has become the most popular circuit simulator in the integrated circuit industry. A circuit designer may encounter SPICE in any one of three different groups. The first incarnation is the basic SPICE that is still maintained and updated by the University of California /Berkeley. In addition, there are also enhanced versions of SPICE available with numerous additional features, developed with the industrial circuit designer, in mind. The most common such package is HSPICE [15] from Avant! Corp., which is used extensively on UNIX workstations in the integrated circuit industry. Another package is PSPICE [16], which was developed for personal computers. Finally, many firms maintain their own internally modified and continually developing version of SPICE, based on the original Berkeley core. In all these versions of SPICE, the basic method of describing and simulating a circuit is the same; in general, the circuit description can be entered into any of these versions of SPICE for simulation. The differences exist beneath the surface, in the mathematical

methods used for circuit simulation, and in the element models which are called during circuit simulation. Therefore, to describe the use of SPICE to simulate integrated circuits, the problem can be separated into three distinct levels. The first level involves the basic methods of using SPICE to simulate various circuits. This subject is well covered in a number of texts and is not described here. At the second level, there is a variety of issues revolving around the mathematical and numerical methods involved in simulating circuits, where the focus is on ensuring the convergence of the simulation while making efficient use of computing resources, so that a useful simulation result may be obtained in a reasonable time. Due to the present overwhelming dominance of CMOS technology, the vast majority of industrial use of SPICE concerns the simulation of FET-based circuits. In addition, FET technology is evolving rapidly, which provides impetus for evaluating how available models describe that technology, while also demonstrating what requirements must be imposed on new FET models. To make effective use of the FET models available in SPICE, the user must understand the construction and implementation of those models.

6.1.1. SPICE Analysis

(A) DC Analysis

SPICE determines the dc operating point of the circuit with inductors shorted and capacitors opened. A dc analysis is automatically performed prior to a transient analysis to determine the transient initial conditions, and prior to an ac small signal analysis to determine the linearized, small signal models for nonlinear devices. If requested, the dc small signal

value of a transfer function (ratio of output variable to input source), input resistance, and output resistance is also computed as a part of the dc solution.

(B) AC Small Signal Analysis

SPICE computes the ac output variables as a function of frequency. The program first computes the dc operating point of the circuit and determines linearized, small signal models for all of the nonlinear devices in the circuit. The resultant linear circuit is then analyzed over a user specified range of frequencies. The desired output of an ac small signal analysis is usually a transfer function (voltage gain, transimpedance, etc).

(C) Transient Analysis

The transient analysis portion of SPICE computes the transient output variables as a function of time over a user specified time interval. The initial conditions are automatically determined by a dc analysis.

(D) Convergence

Both dc and transient solutions are obtained by an iterative process which is terminated when both of the following conditions hold[34]:

- The nonlinear branch currents converge to within a tolerance of 0.1 percent or 1 picoamp (10^{-12} Amp), whichever is larger.
- The node voltages converge to within a tolerance of 0.1 percent or 1 microvolt (1.0e - 6 Volt), which ever is larger.

Although the algorithm used in SPICE has been found to be very reliable, in some cases it fails to converge to a solution. When this failure occurs, the program terminates the job. Failure to converge in dc analysis is usually due to an error in specifying circuit connections, element values, or model parameter values.

6.1.2 Primary functions in SPICE3f3

A brief description of the primary functions[9] served by the files contained in these directories follows.

conf/default file contains several variables that are used during the compilation of the program which need to be set according to the environment in which the program is being compiled. These variables include the command to run the C-language compiler, the paths to the libraries that are required during compilation, the directories containing the source files, intermediate files and output files, the default editor when using SPICE interactively, the analyses that the program is to perform, and the device models that the program is to be capable of simulating.

The file was modified to include the S-CMOS Model as In addition to the defaults file, the directory also contains files for different computer systems that include special definitions that are required by the given system and which do not appear in the **defaults** file. The **util** directory contains the command which is used to compile the program.

The **src/lib** contains the C-language files that constitute the program. The include directory contains C-language preprocessor files that are required by the program. Several variables including index numbers, values of physical constants, and sizes/types of data

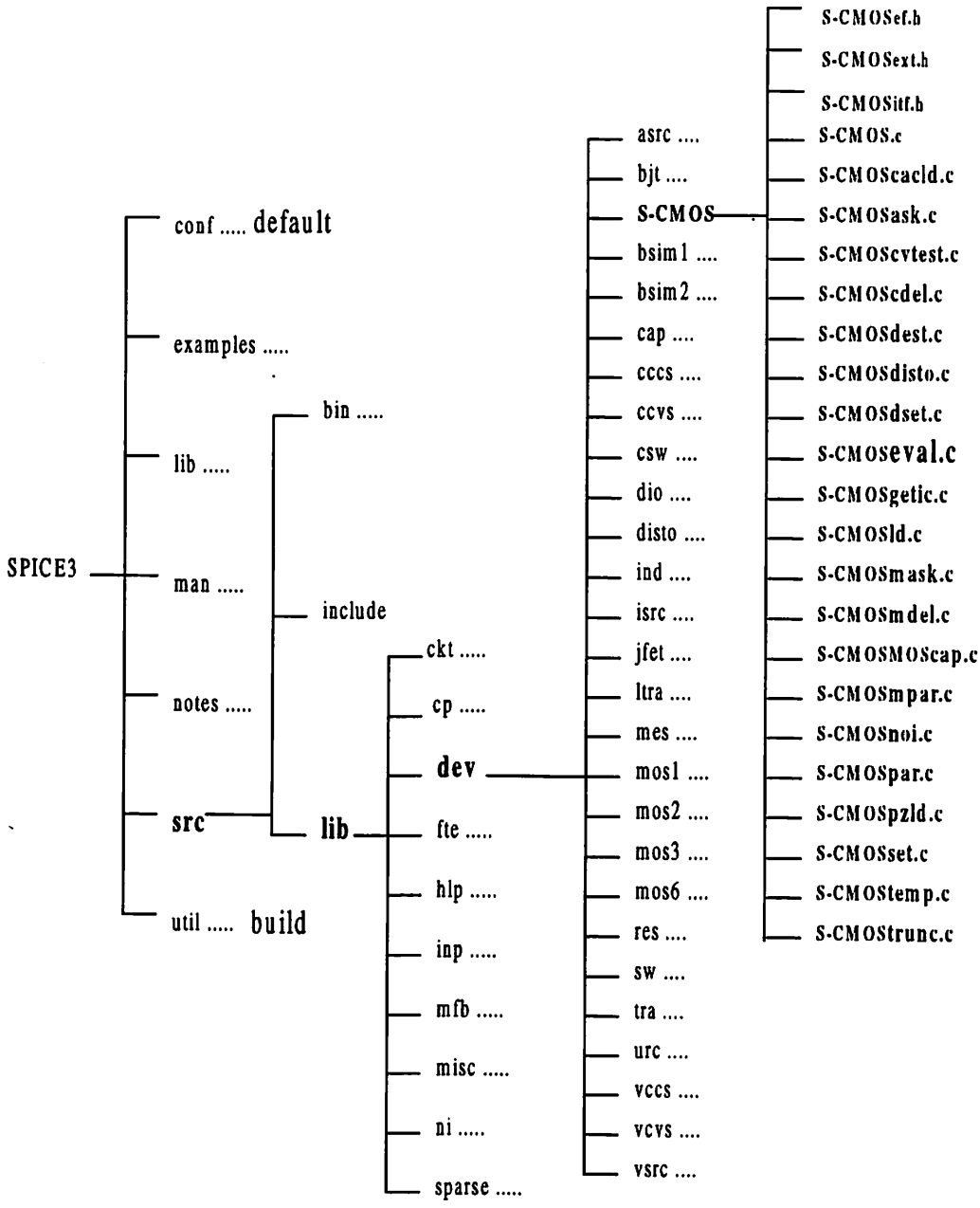


Figure 6.1 UNIX-based organization of the SPICE3f3P program

structures used by the programs are defined in files that are in S-CMOS Model directory. These files are then included in the headers of the C-language program files by using the "#include" command. After the program is compiled, the executable file of the simulation program is placed in the src/bin directory.

The **ckt** directory contains routines that link the entire structure of the program and serve as interface points between different functions in the program. Some of these routines implement the front-end interface of the simulator. Other routines are used to bind the various components of the program together by stepping through device dependent subroutines and calling instances that have been defined or that are needed for the operations to be performed. Routines implementing the various analyses such as the D.C., A.C. and transient analyses that are to be performed by the program are contained in S-CMOS Model directory. Simple utilities that are used to manipulate the data structures in SPICE are also contained in this directory.

The "**ni**" directory contains the numerical algorithms that are used by the SPICE program. These include routines that initialize and load matrices, compute time step and integration-method dependent terms, and perform voltage/current equation convergence tests. Routines that perform numerical integration, Newton-Raphson iterations, finding roots of complex polynomials, and computing determinants for the pole-zero analysis are also contained in this directory. The directory contains functions of a specialized sparse matrix package that is use to manipulate the sparse matrices generated during simulation.

The directory **"inp"** contains the routines necessary to parse the input format and produce the subroutine calls that are required by the front-end to simulator interface. These include routines that parse the model definitions and descriptions of various active and passive

elements in the input decks. The directory also contains files defining the front end of the simulator.

The "**dev**" directory contains routines that define and evaluate the different devices and models that have been implemented in SPICE.

6.1.3 SPICE-3f3s implementation of S-CMOS model

The S-CMOS model was developed to enhance the capability of circuit simulation for high-performance VLSI design in deep-submicron technologies. In order to enable circuit designers to use the model, it was necessary to implement it into a popular circuit simulator. The SPICE-3f3 simulation program[12] was selected for the implementation of S-CMOS model and the modified version with the S-CMOS model is called SPICE-3f3. The structure of the SPICE-3f3s program for the new model implementation is shown in Fig. 6.1. A brief description of the primary functions served by the files contained in these directories and the S-CMOS model implementation procedure are given as following. The implementation of a new device model into the SPICE-3f3 program requires three types of changes:

- new routines written specifically to support the device,
- modifications of existing routine to include knowledge required for parsing, and
- changes to integrate the new device model into the main loops of the simulation algorithm.

The C-language files that were created to support the S-CMOS model were placed in the **src/lib/dev/S-CMOS** directory. The main files and a brief description of the routines contained in them are listed below:

S-CMOSdef.h: This file contains two data structures, one for the device model and one for a specific instance of model.

S-CMOSitf.h: This file contains pointers to routines that are used to interface with the device model, as well as a number of tables and constants.

S-CMOSext.h: This file declares the different routines associated with the S-CMOS model.

S-CMOSc.c: This file contains two parameter descriptor arrays that list the parameters along with the type of values that can be assigned to the parameters, as well as integers that can be used to refer to the parameters in other routines.

S-CMOSacld.c: This routine is used to load the sparse matrix during A.C. analysis where complex quantities may need to be loaded.

S-CMOSask.c: This routine allows users to access internal values of S-CMOS devices instances. Certain parameters of instances can be passed to it in order to compute and return the values of such parameters.

S-CMOScvtest.c: This routine performs the convergence test for each device.

S-CMOSdel.c: This routine deletes a single instance of the S-CMOS model from the data structures, leaving everything else alone.

S-CMOSdest.c: This routine is used to dismantle the data structure and free all space used by S-CMOS model and instances.

S-CMOSeval.c: This routine contains the S-CMOS model expressions. The drain current, terminal charges, their derivatives with respect to drain, gate, source, bulk voltages are evaluated in this routine.

S-CMOSgetic.c: This routine gets the initial conditions of S-CMOS devices from the node initial conditions.

S-CMOSld.c: This routine is used in the D.C. and transient analyses to load the sparse matrix.

scmask.c: This routine allows users to access internal values of S-CMOS model parameters.

S-CMOSmdel.c: This routine is used to dismantle data structures and free space occupied by a specific S-CMOS model and all instances of that model.

scmoscap.c: This routine calculates and assigns values of equivalent conductances and total terminal charge.

S-CMOSmpar.c: This routine assigns a value to a specific S-CMOS model parameter.

scnoi.c: This routine calculates the thermal noise due to the source/drain and channel conduct dances, as well as the flicker noise.

S-CMOSpar.c: This routine assigns a value to a specific parameter field of a device instance.

S-CMOSpzld.c: This routine is used for evaluating and loading the matrix during pole-zero analysis.

S-CMOSset.c: This routine is called once during parameter preprocessing, and all the one-time operations such as allocating sparse matrix entries and getting pointers to them are done here.

S-CMOStemp.c This routine is used to preprocess the S-CMOS model parameters.

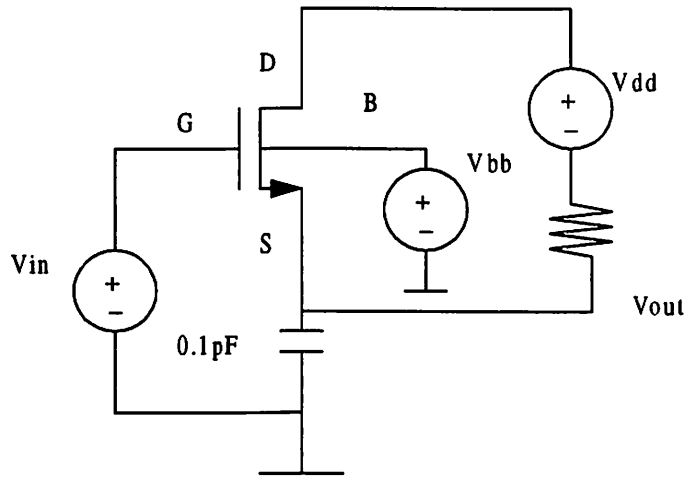
S-CMOStrunc.c: Calculation of truncation errors on energy storage elements or components of elements is done here.

The S-CMOS model has been implemented in the SPICE-3f3 version of the circuit simulation program to give VLSI designers the ability to use the model for design of low-power high-performance circuit in advanced deep-submicron technologies.Several conventional and advanced CMOS circuit blocks were simulated by using SPICE-3f3 to demonstrate the capability of S-CMOS model in different types of circuit simulation. The SPICE program was also used to simulate several conventional and advanced CMOS circuit blocks.

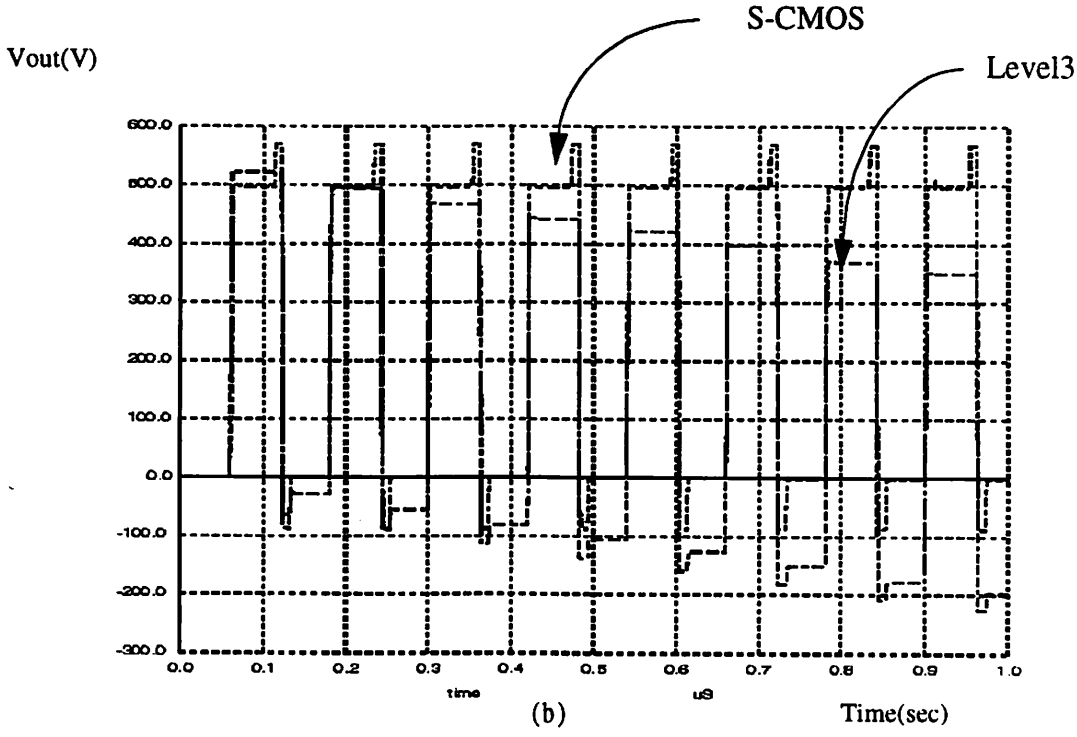
6.2 Charge Conservation

The first generation MOSFET model, Level2 and Level3 models are highly empirical and contained discontinuity in their dc and capacitance analysis. They did not conserve charge and incorporate in the deep submicron devices. In addition to the issue of how the node charges are simulated at the device level, there are a number of concerns at the circuit simulation level. These difficulties are quite subtle, and may at first glance appear to actually be device level issues. However, as will be shown here, implementation at the circuit simulation level is actually the most important constraint on the ability to conserve charge. As originally implemented in SPICE, the voltage is specified as the state variable at each circuit node; that is, at each node, if the voltage is not fixed by connection to an

external node (such as the power supply or ground), it is the item which the matrix circuit solution produces. Once the voltage is determined at each node, the circuit behavior is computed from knowledge of all the node voltages. In the most general case, either the voltage or the charge could be specified as the state variable at each node. However, it has been shown [15] that due to the highly nonlinear relationship between the voltage and the charge in MOSFETS, charge conservation can only be ensured by using the charge as the state variable in MOS simulation. If the voltage is specified as the state variable, the charge must be computed by integrating the voltage, which will lead to incorrect results. Consider the computation of a node charge during SPICE circuit simulation. The Meyer model computes capacitance values, which are made available at the circuit simulation level; what follows is the case for any model which provides capacitance (rather than charge) to the circuit simulator. The charge on any particular node is found by integrating the transient current [15]:A single MOS transistor was simulated to ensure charge conservation property. For the comparison purpose, S-CMOS and Level-3 model are simulated and compared. as shown in Fig. 6.14(a) and (b).



(a)



(b)

Figure 6.2 (a) Charge conservation test circuit (b) S-CMOS Model and Level3

6.3 Comparison of Circuit Simulation Performance

The S-CMOS, MOS Level2, Level3, BSIM, and BSIM3v3 models were used to simulate circuits including folded cascode Op-Amp, analog multiplier, comparator, 8-bit carry save adder, 8-bit x8bit carry-save-multiplier

6.3.1 Folded-Cascode Operational Amplifier

A folded-cascode operational amplifier[10] was designed with a 0.35μm technology. The circuit schematic diagram of the amplifier is shown in Fig.6.3. The amplifier was designed to operate with a power supply voltage of 3.3V. A bias current of 10μA was used in the simulation. The output range was also determined with the amplifier in the open-loop configuration. Fig 6.4 shows the voltage gain and phase characteristics of the simulation result by using S-CMOS Model.

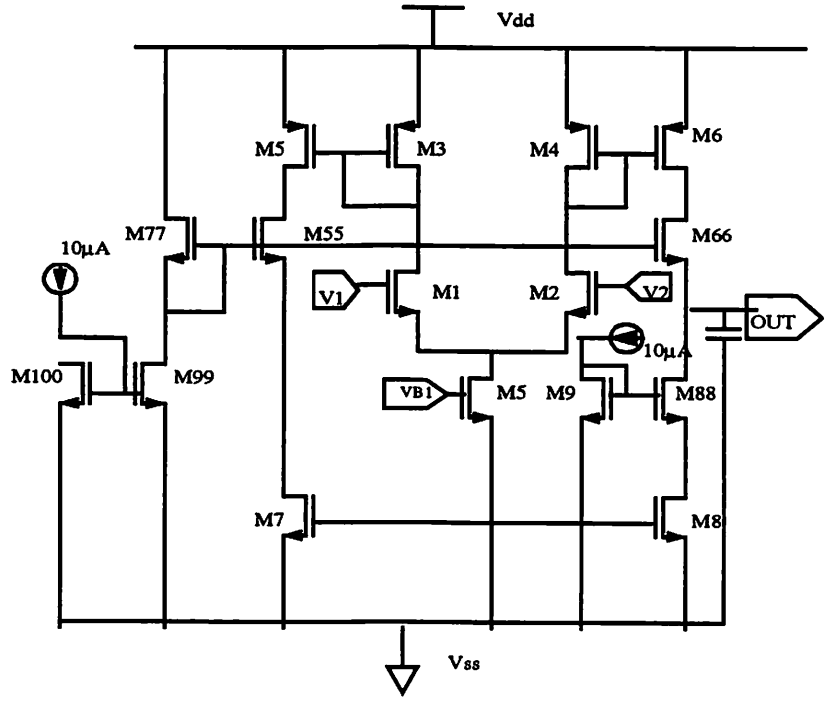
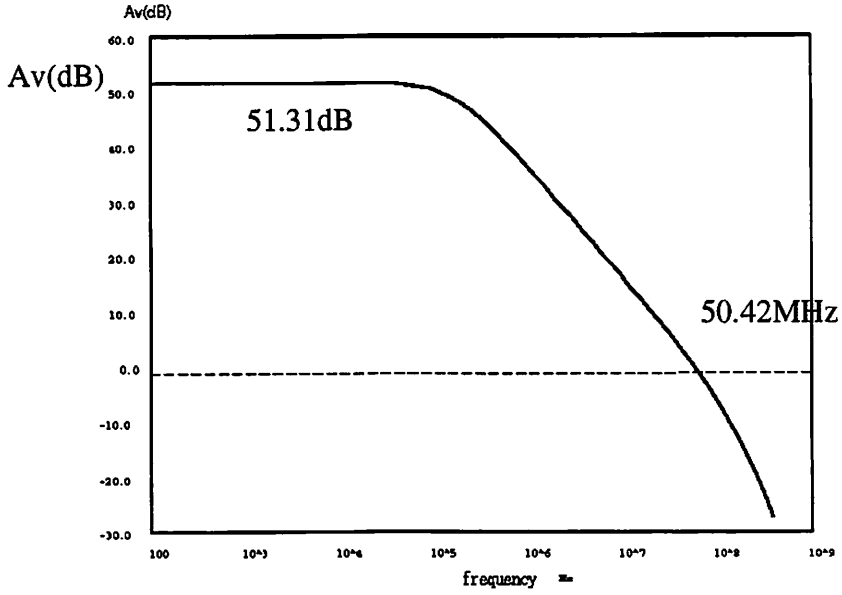
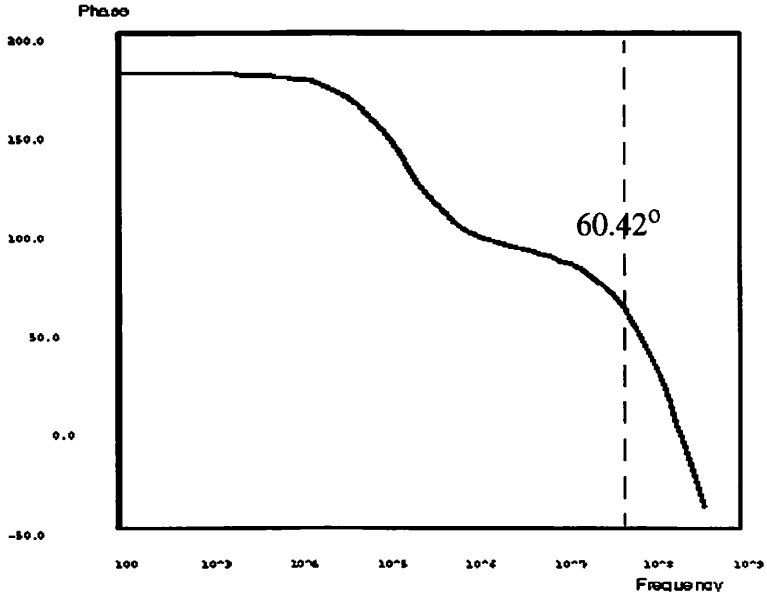


Figure 6.3: The schemetic of a folded-cascode OP amp



(a)



(b)

Figure 6.4 Simulation result by S-CMOS model (a) Gain characteristics
(b) Phase characteristics

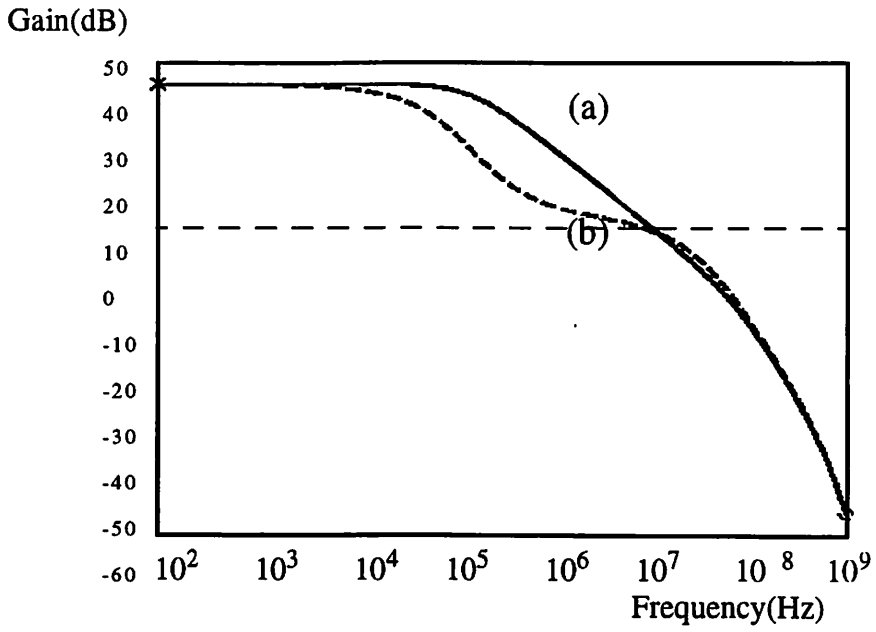


Figure 6.5 Simulation result by Level2 model (a) Gain characteristics
(b) Phase characteristics

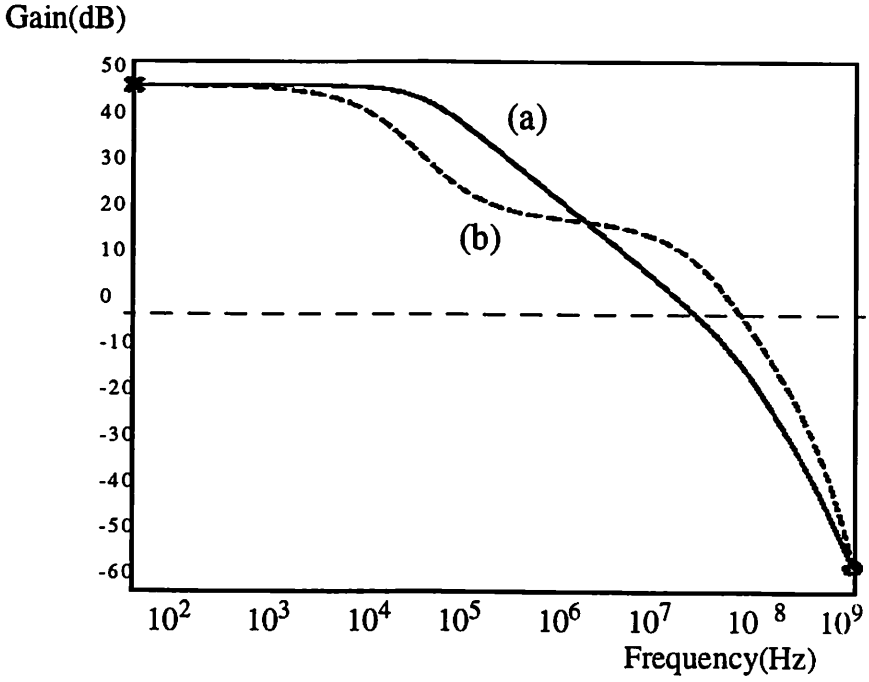


Figure 6.6 Simulation result by Level3 model (a) Gain characteristics
(b) Phase characteristics

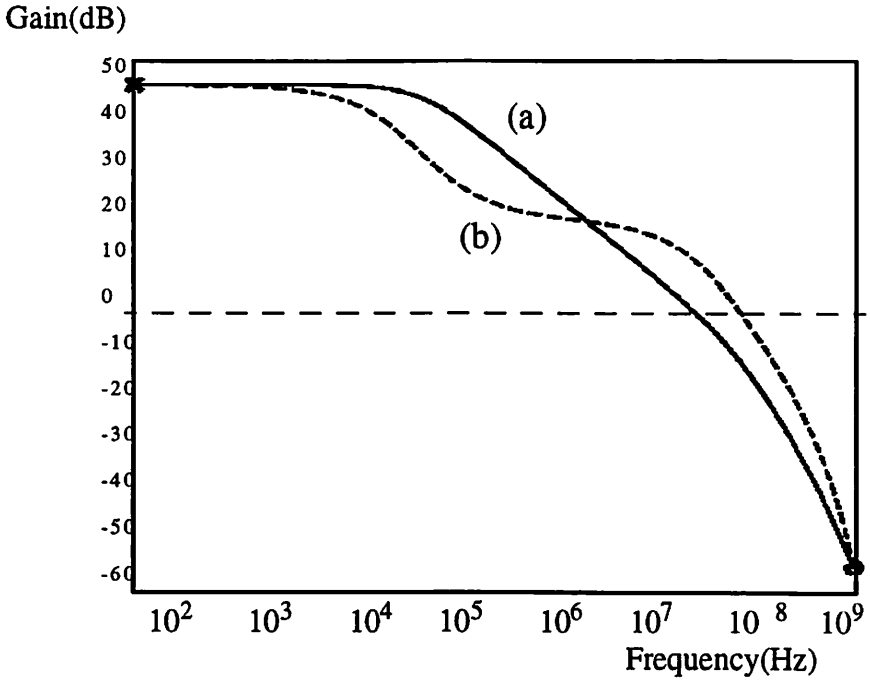


Figure 6.7 Simulation result by BSIM model (a) Gain characteristics
(b) Phase characteristics

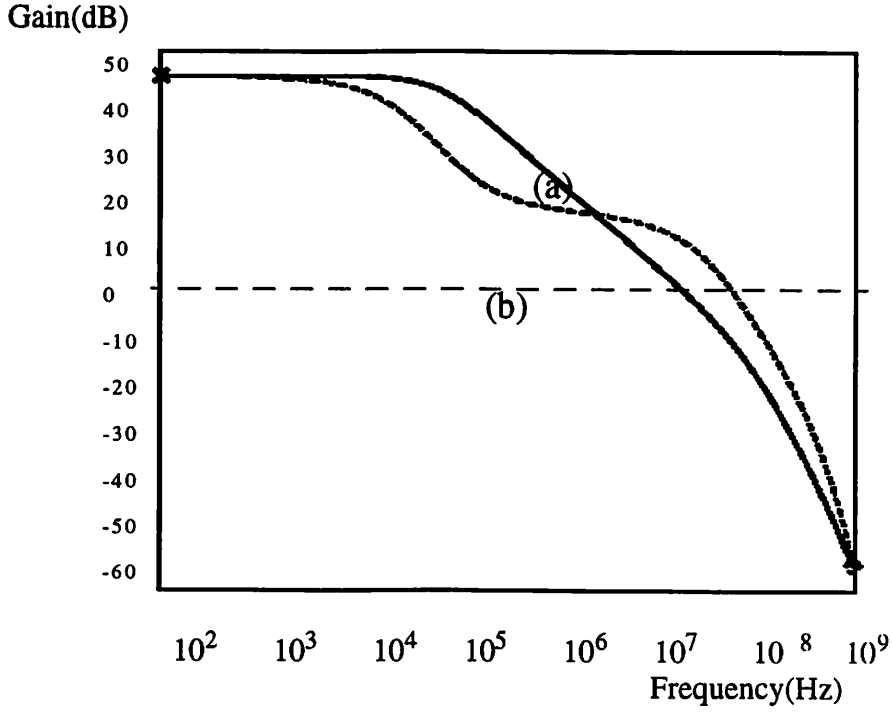


Figure 6.8 Simulation result by BSIM3v3 model (a) Gain characteristics
(b) Phase characteristics

Table 6.1 Simulated performance characteristics pf the single stage folded cascode op amp

Characteristics	Level2	Level3	BSIM	BSIM3v3	S-CMOS
CPU time(sec)	0.49	0.66	0.61	0.88	0.43
DC gain(dB)	49.4	51.11	51.1	52.1	51.31
Unity gain Frequency (MHz)	41.6	34.5	36.5	21	50.42
Phase Margin (degree)	55.4	75.2	74.2	67.7	60.42
3dB frequency (KHz)	158	97	62.64	59.4	171
Applicable Tech.(μm)	0.8	0.8	0.8	0.35	0.35

The simulations were concluded and the expected result were obtained with S-CMOS and BSIM3v3 model in 0.35μm technology. However, convergence problems occured due to the minimum effective channel length error in the simulation with level3, Level2, and BSIM model. When the design scaled up from 0.35μm to 0.8μm technologies and simulated using MOS Level-2, Level3, and BSIM models, the expected results were obtained. Therefore, different channel lengths were used in this simulation comparison. The comparison on Table 6.1 shows that S-CMOS simulation is faster than those of other models in CPU time.

6.3.2 Gilbert Multiplier

In Fig. 6.8 M_1, M_2, M_6, M_7, M_9, and M_{10}, form the conventional Gilbert multiplier structure This circuit uses two PMOS transistor pairs for the inputs V_3 and V_4 to realize large operation range of input voltages from very close to V_{DD} to very close to ground. In order to have a more precise current mirror between two output stages in both sides of the circuit, M_{18}-M_2 are used as a cascode structure. The output current is proportional to (V_1 - V_2)* (V_3 - V_4). The simulated result of the output current over a wide range of V_1 for several fixed values of differential input V_3-V_4 by using S-CMOS model is shown in Fig 6.9.

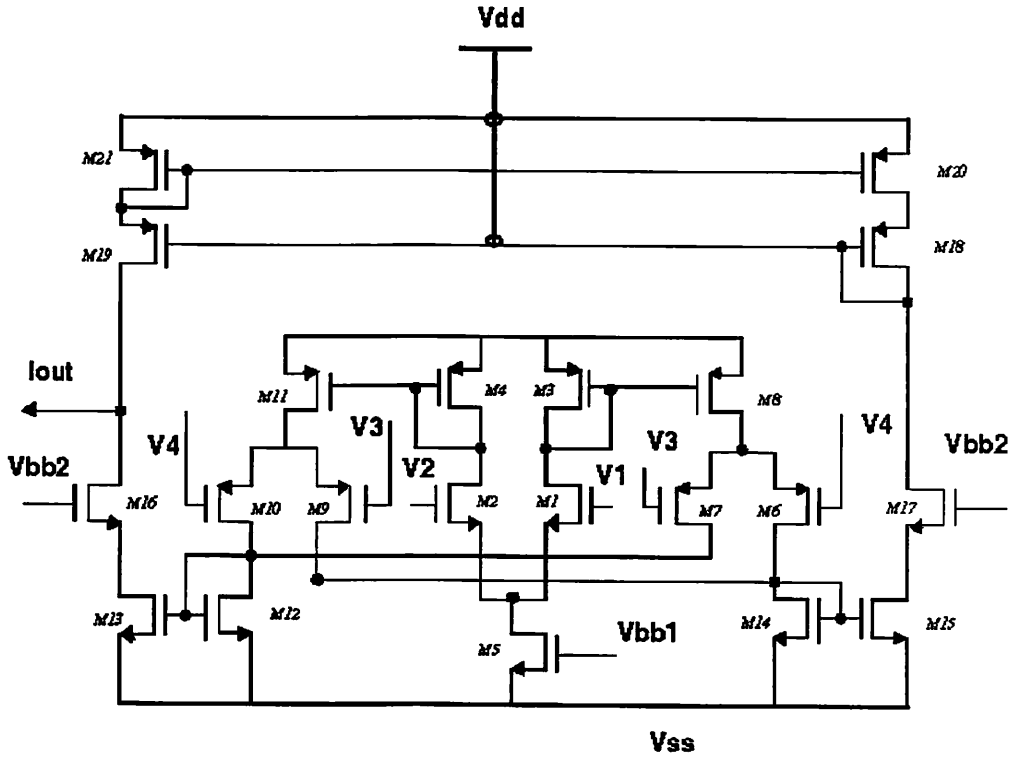


Figure 6.8: Modified Gilbert multiplier for a wide operation range

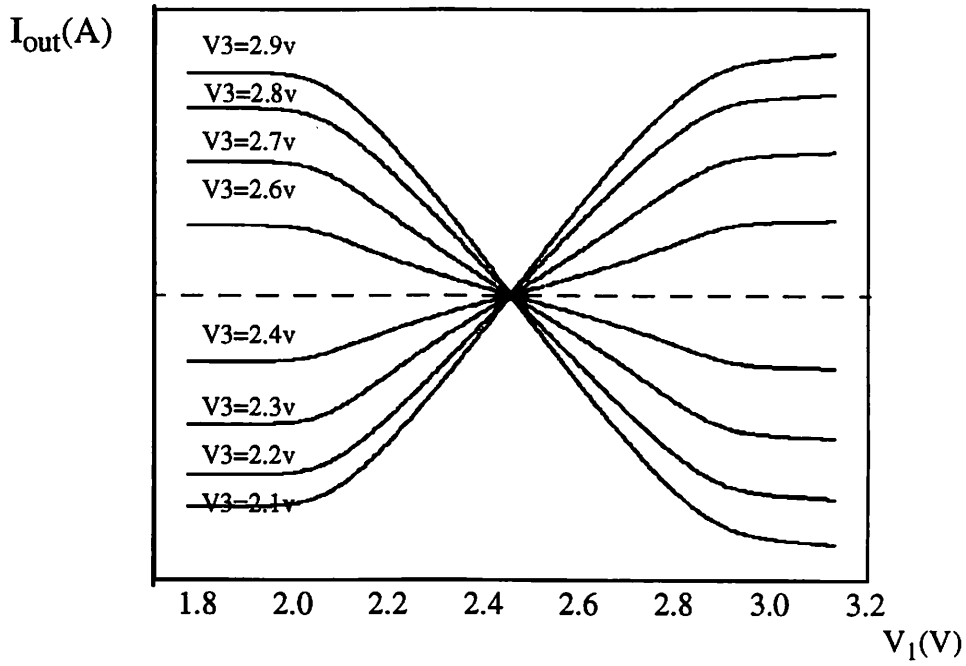


Figure 6.9: Simulation output result by using S-CMOS model

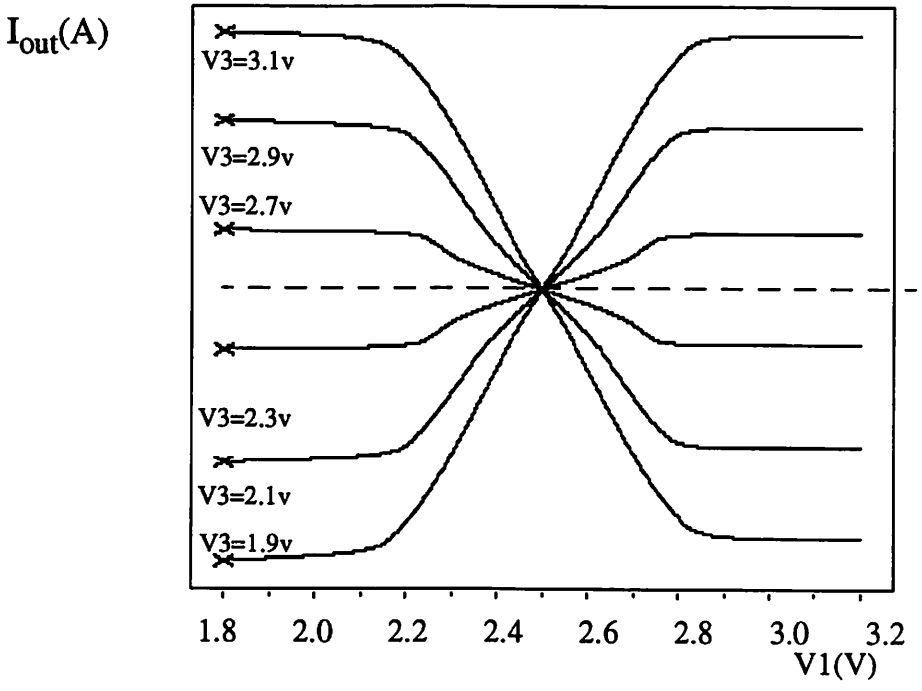


Figure 6.10: Simulation output result by using Level2 model

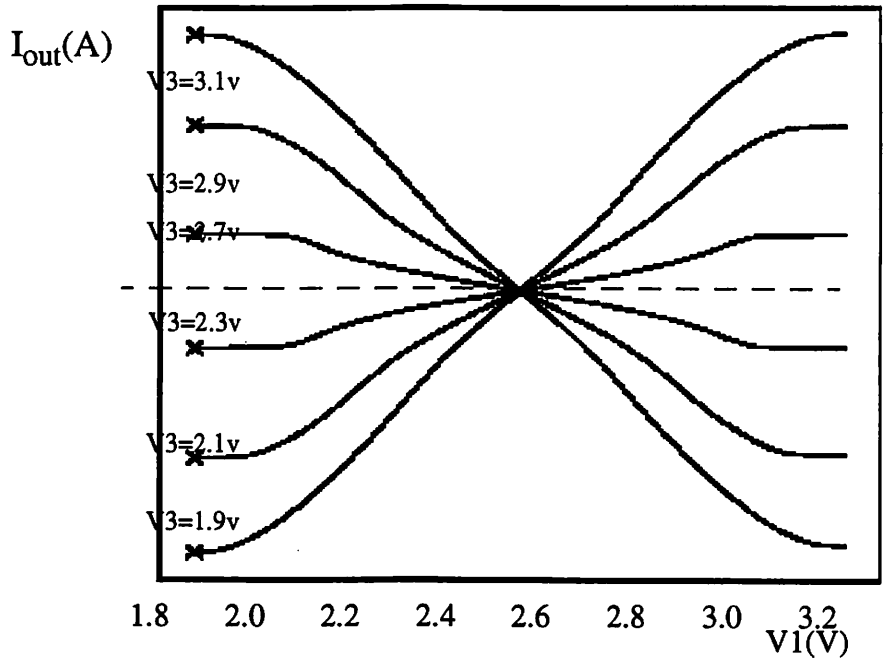


Figure 6.11: Simulation output result by using Level3 model

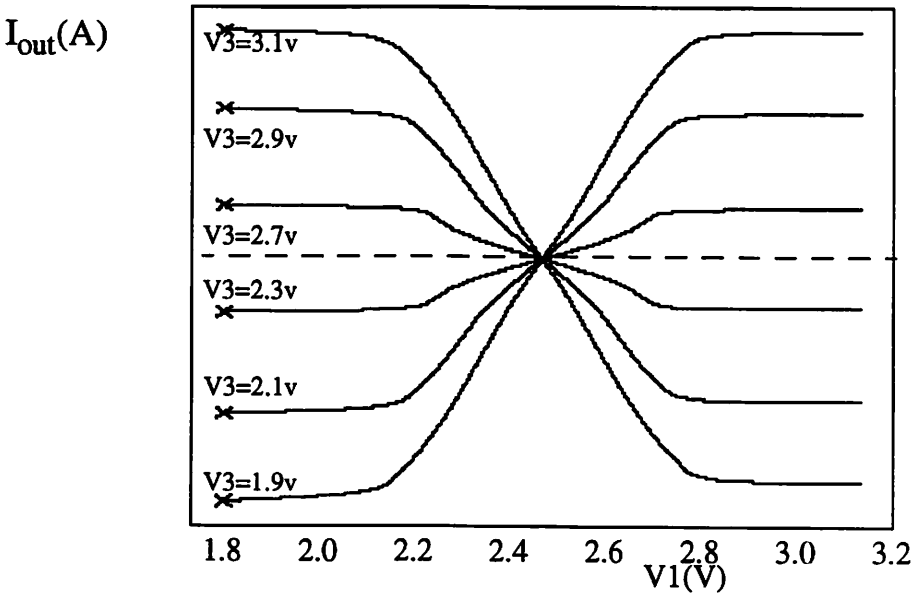


Figure 6.12: Simulation output result by using BSIM model

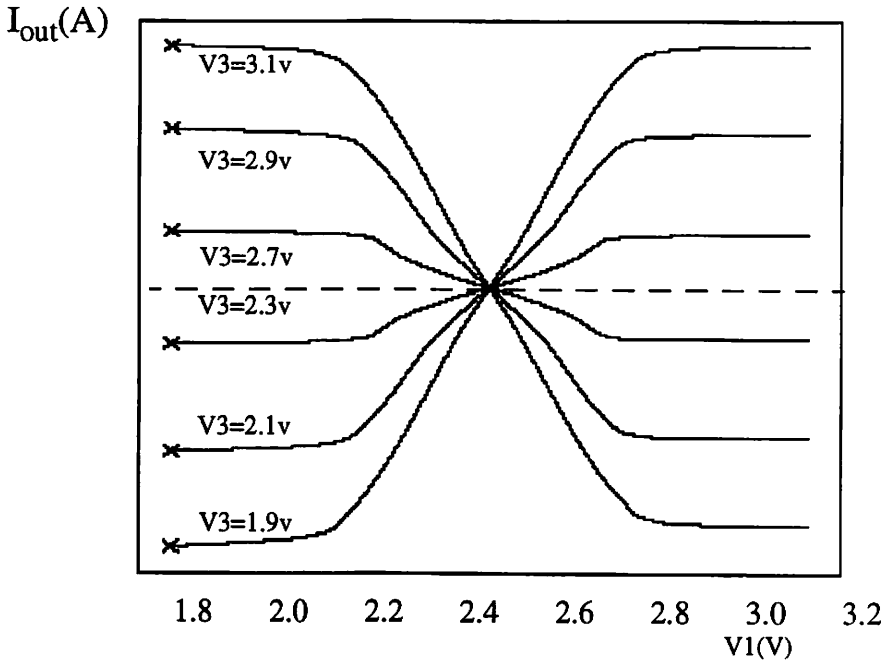


Figure 6.13: Simulation output result by using BSIM3v3 model

Table 6.2 Simulated performance characteristics of Gilbert multiplier

	Level2	Level3	BSIM	BSIM3v3	S-CMOS
CPU time(sec)	15.65	12.78	12.38	9.45	9.78
Total memory used	185K	185k	168k	168k	367k
Iteration	16922	16914	5364	4314	5364
Applicable tech.(μm)	0.8	0.8	0.8	0.35	0.35
MOSFET #	21	21	21	21	21

The simulations were concluded and the expected result were obtained with S-CMOS and BSIM3v3 Model in 0.35μm technology. During the simulations, minimum effective

channel length error were occured and abolted in the simulation with MOS level2, Level3, and BSIM model. When the design of the multiplier scaled up from 0.35μm to 0.8μm technologies and simulated using MOS Level-2, Level3, and BSIM models, the expected results were obtained. The result shows that BSIM3v3 and S-CMOS model are useful in deep-submicron technologies. The simulation time using S-CMOS model were equivalent to BSIM3v3 model and quicker than those of the other models. The comparison on this simulation is shown in Table 6.2.

6.3.3 Carry Save Multiplier

Multiplications are complex adder arrays and expensive slow operations. An efficient carry save multiplier is considered to do the simulation comparison of the models. The multiplication result in the carry save multiplier does not change when the output carry bits are passed diagonally downward. A 8-bit carry save adder and 8-bit x 8-bit carry save parallel multiplier were designed using transistors with L=0.5μm. Figure 6.28 shows 8-bit carry save adder. The multiplier can be implemented by AND gates, half and full adder cell[6]. Sixty four AND gates were used to calculate the partial products of all pair-wise combinations of the input bit in parallel. Single-bit adder cells were used for the accumulation of shifted partial-product terms. The resulting sum and carry terms rippled across the array of multiplier cell shown in Fig. 6.14.

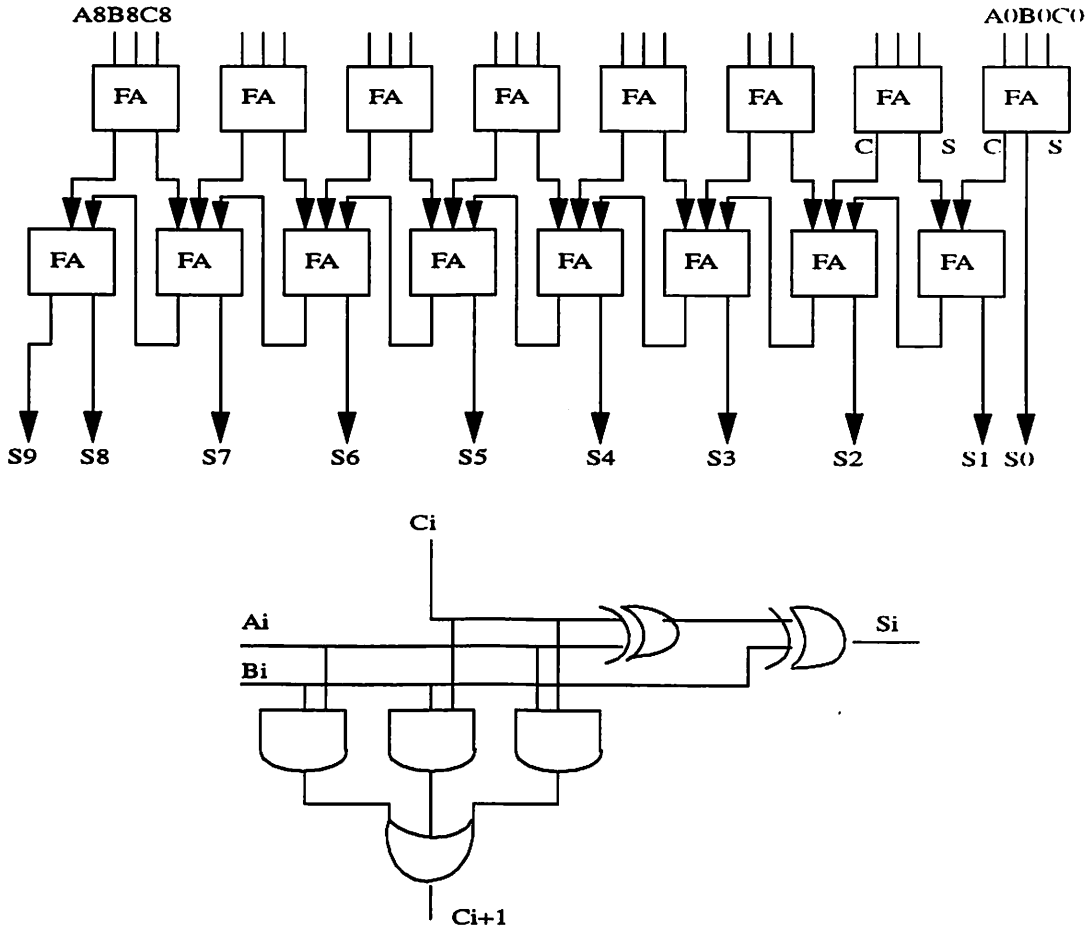
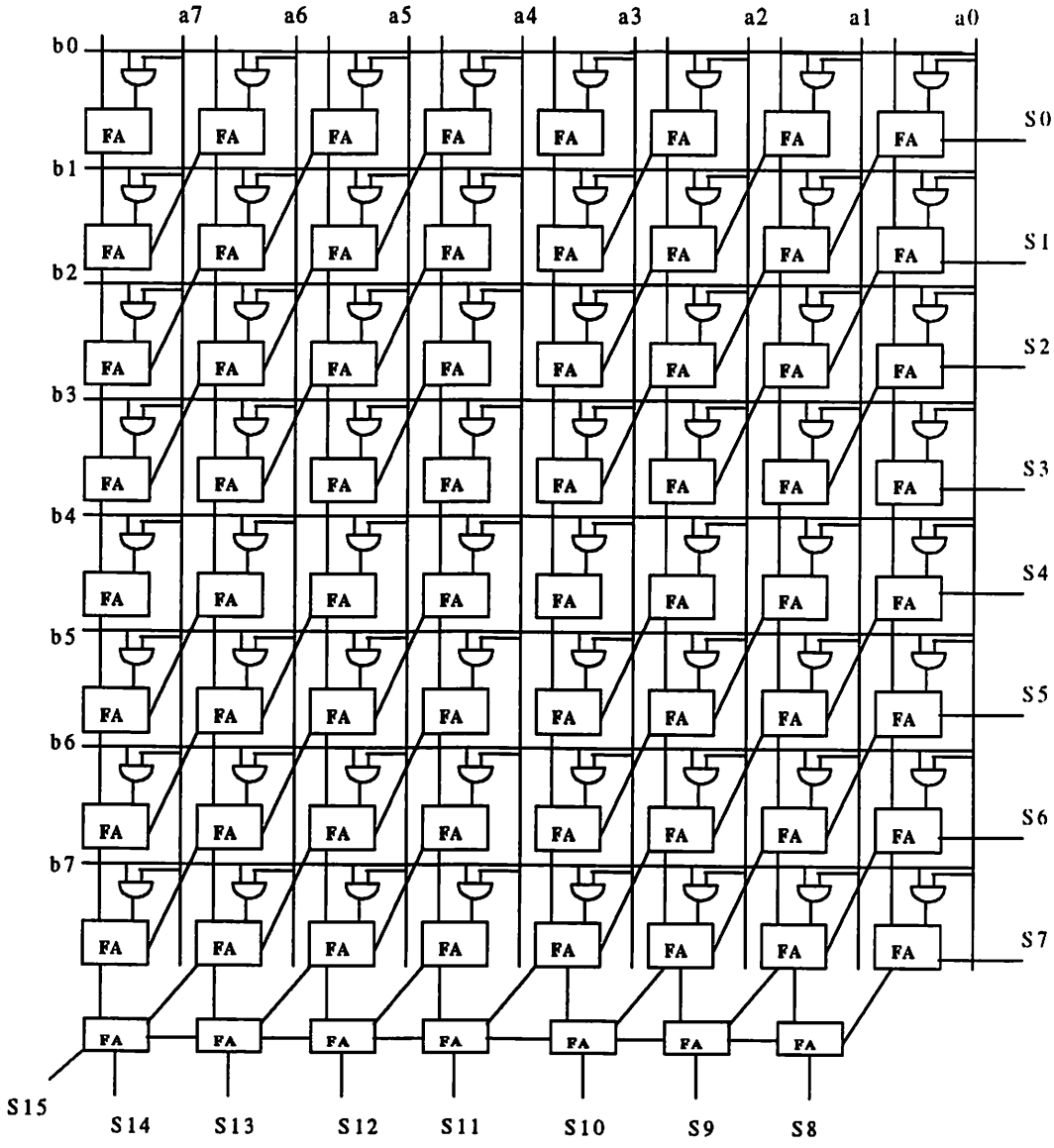


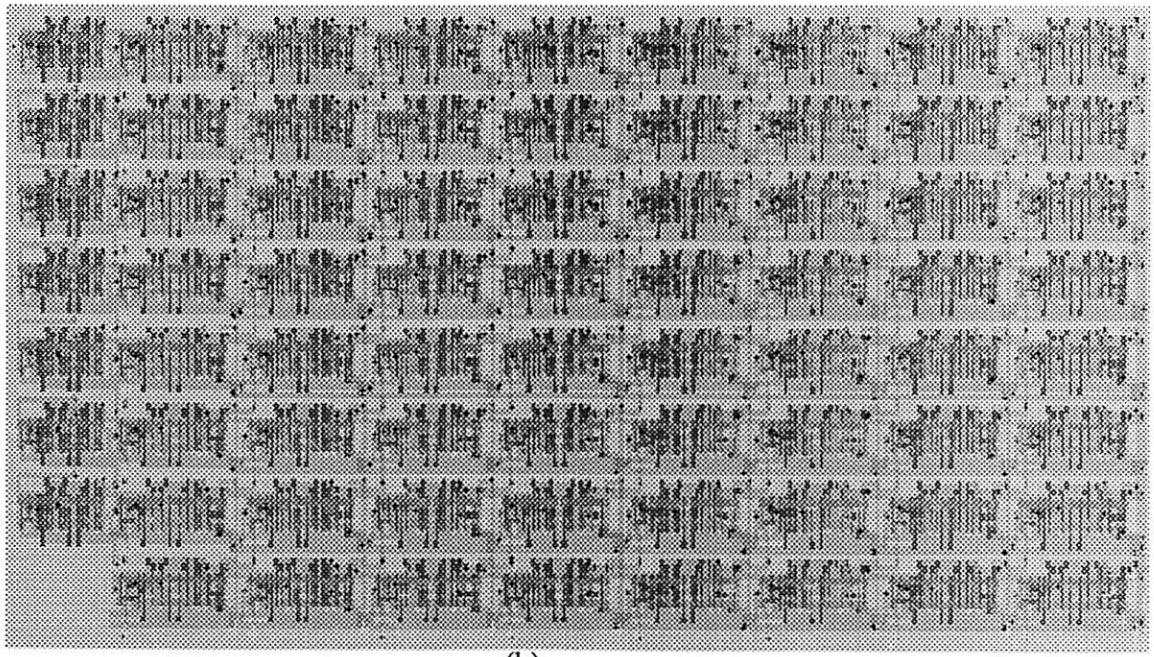
Figure 6.14 The structure of 8-bit Carry Save adder

The multiplier results were generated at the outputs of the adder cells on the boundary of array. In this design, sixty four AND gates and sixty three full adders were used. MOS Level-2, Level3, BSIM, BSIM3v3 and S-CMOS simulation results are compared on the Table 6.4. Simulations times using the S-CMOS model compare favorably with those of the other four models. Convergence performance of S-CMOS model is equivalent to BSIM3v3 model and better than the other three models. The simulation results were

similar. The simulation time using S-CMOS model were quicker than the simulations using the other models.



(a)



(b)

Figure 6.15 The design of 8-bit Carry Save Multiplier (a) Block digram of the multiplier (b) Layout of the multiplier

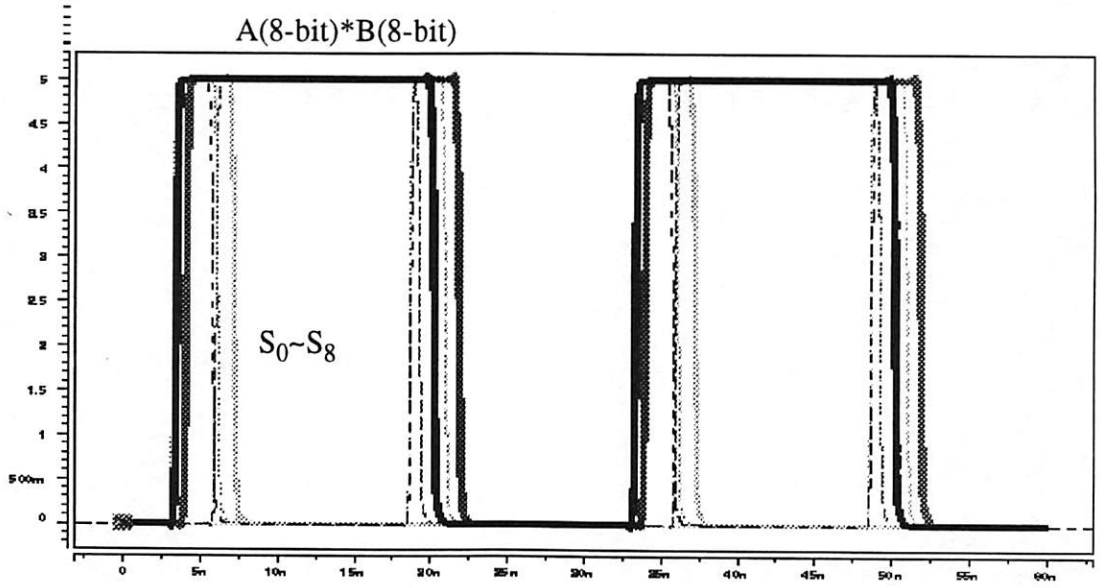


Figure 6.16 : Simulation output result of the 8-bit carry save multiplier

Table 6.3 Simulated performance characteristics of 8-bit Carry save multiplier

	Level2	Level3	BSIM	BSIM3v3	S-CMOS
CPU time(sec)	224.98	199.74	207.67	256.76	250.32
Total memory Used(Kbit)	4784	4784	4783	8559	9235
Iteration	3924	3980	4033	3127	3824
MOSFET #	2372	2732	2732	2732	2732

The simulations were concluded and the expected result were obtained with S-CMOS and BSIM3v3 model in 0.35μm technology. However, convergence problems occured due to the minimum effective channel length error in the simulation with level3, Level2, and BSIM model. When the design of the multiplier scaled up to 0.8μm technologies and simulated using MOS Level-2, Level3, and BSIM models, the expected results were obtained. The comparison on this simulation is shown in Table 6.3. The simulation time using S-CMOS model were quicker than BSIM3v3 model and equivalent to the simulations using the other models. A 8-bit divider was designed with the carry save 8-bit multipliers and adders to implemented A/B calculation. Fig 6.17 and 6.18 show the algorithm and layout of the divider respectively. Simulation computation CPU time and applicable chennel length are compared in Table 6.4.

Algorithm

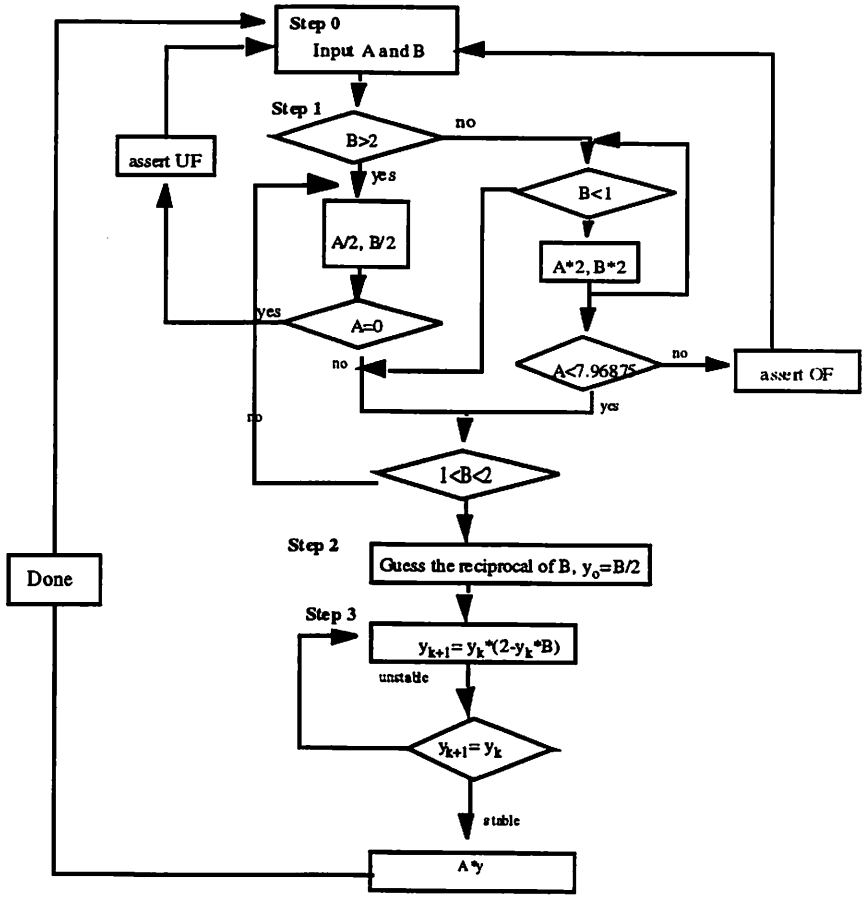


Figure 6.17: The flow chart of 8-bit divider algorithm

Table 6.4 Simulation comparison of the models

Simulation characteristics/ time(sec)	Level-2	Level-3	BSIM	BSIM3v3	S-CMOS
Op Amp	0.49	0.66	0.61	0.88	0.43
Gilbert Multiplier	15.65	12.78	12.38	9.45	9.78
Conventional Adder	0.71	0.72	0.77	0.72	0.92
Analog Comparator	16.42	20.38	14.83	13.63	16.47
8-bit Carry save multiplier	224.98	199.74	207.67	256.76	250.32
Applicable technology(μm)	0.8	0.8	0.8	0.35	0.35

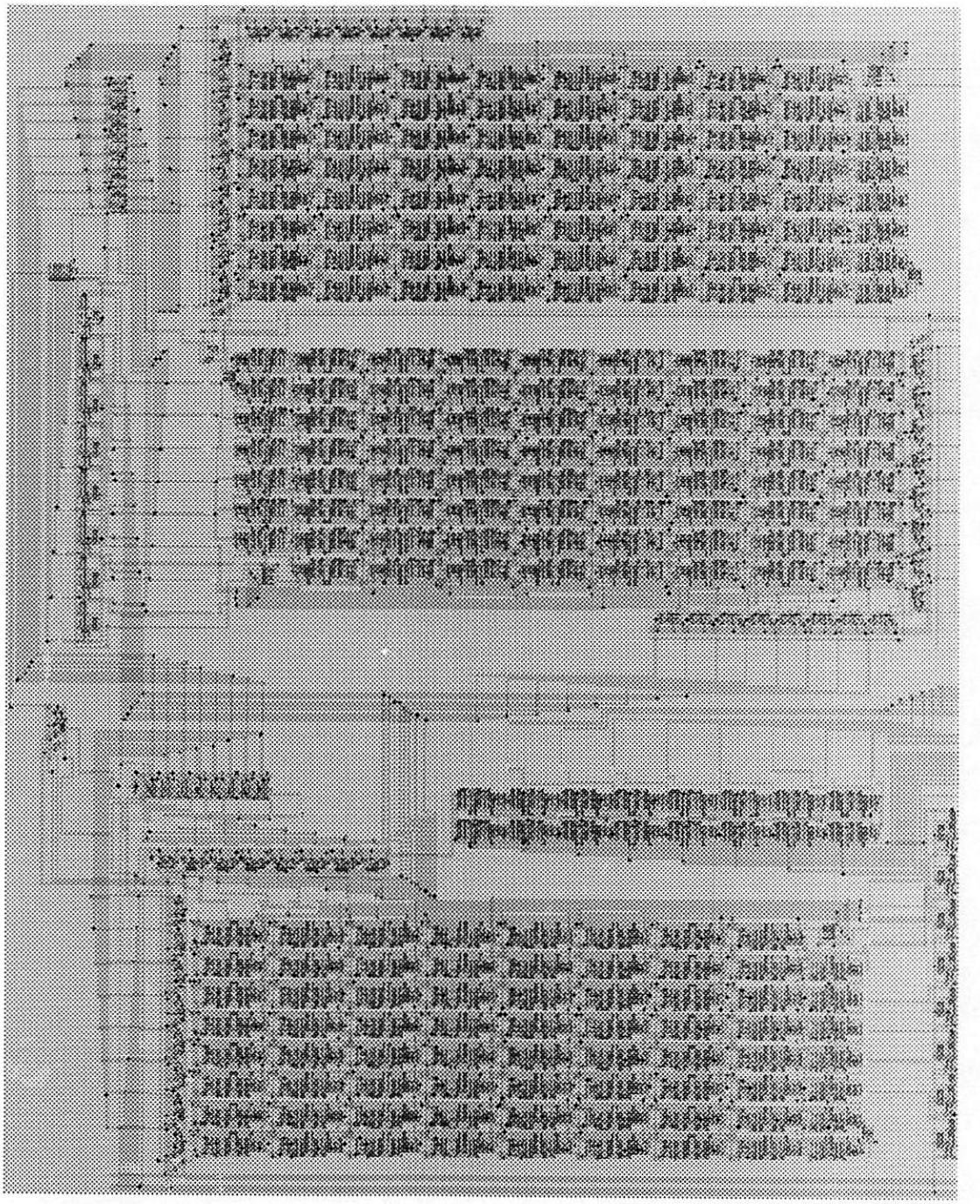


Figure 6.18 : The layout of 8-bit divider

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Chapter 7

Conclusion

An accurate, physically based compact model, S-CMOS, is developed and implemented to the circuit simulator to provide the VLSI designers with the efficient tool to simulate very low power high speed deep submicron technologies. It has been demonstrated that S-CMOS model ensures the continuities in high-order derivatives of the current and charges in the boundaries between different regions. Introductory Non-quasi-static approximation is introduced for high frequency application. Efficient parameter extraction program by using simplified data structure is presented. The proposed model is based on BSIM model and accomplished continuity in all the region of the transistor operation. Selected analog circuits and digital block simulation are demonstrated and these results are compared.

The key features of the model that make it very valuable include:

- compact set of physic-based parameters
- use of three smoothing functions, hyperbola, exponential interpolation, and sigmoid functions, for the drain current and terminal charge provides excellent transitions without discontinuity between different operation regions in the unified expressions.
- unified drain current and terminal charge expressions in all regions of operation.

- accurate modeling of charge densities by the better expression of conductance degradation coefficient.
- unified first-order non-quasi-static time constants for long-channel transistor at high frequency
- a compact set of physically-based parameters and efficient parameter extraction strategy.
- integration of MOS transistor characteristics from DC to high frequency.
- the effective mobility expression includes the effects of lateral and vertical electric fields in the channel.
- the hyperbola and exponential interpolation functions provides the effective mobility expression valid for both weak- and strong-inversion regions.
- the charge model uses the better formulation of conductance degradation coefficient to model the channel charge density.
- the unified expressions of charge densities are valid for all operation regions, including the accumulation region.
- the use of a compact set of 33 parameters, including 29 physics-based parameters and 4 smoothing function parameters.

The Important features in many properties of the S-CMOS model are summurized in Table 7.1

Table 7.1 The Important features in many properties of the S-CMOS model

MOS Model	Level-3	BSIM	BSIM3v3	S-CMOS
Number of parameters	18	62	109	35

MOS Model	Level-3	BSIM	BSIM3v3	S-CMOS
Model expression in different regions	different expressions	different expressions	unified expression	unified expression
Continuity of conductance	discontinuous at transitions between different operation regions	discontinuous at transitions between different operation regions	continuous and smooth through all operation regions	continuous and smooth though all operation regions
Accuracy of drain current and conductances	moderate	moderate	good	good
Charge/capacitance model	separate equations for different region	separate equations for different region	unified terminal charge equations	single terminal charge equations
Applicable operation frequency	100 MHz range	100 MHz range	several hundred MHz	up to 10 GHz
Applicable circuit type	Digital VLSI	Digital VLSI	Mixed-signal VLSI	Mixed-signal VLSI
Applicable technology	1.2 μm	0.8 μm	deep-submicron	deep-submicron

The S-CMOS model was implemented into the simulators including SPICE3f3 from Berkeley and the extraction procedure of the S-CMOS model was implemented in MATLAB software which is one of the most popular math tool to engineers. Parameter set were extracted from MOSIS 0.35mm technology. An expriment to demonstrate the charge conservation property of S-CMOS model was presented. Simulation of mixed-signal circuits including folded-cascode operational amplifier, analog comparator, wide-range Gilbert multiplier, and 8-bit carry save multiplier circuit were done to observe the performance of the circuit simulator and the new model. Comparison of simulated results and measured data of transistors was done to demonstrate the accuracy of the S-CMOS model and its strong capability in the deep-submicron technologies. These cir-

cuits were simulated using MOS level2, Level3, BSIM, and BSIM3v3 to demonstrate the improved circuit simulation convergence properties of the S-CMOS model. The comparison in simulated computation time and applicable technologies(channel length) are summurized in the Table 7.2

Table 7.2 The comparison in computation time and applicable technologies

Simulation characteristics	Level-3	BSIM	BSIM3v3	S-CMOS
Op Amp	0.66	0.61	0.88	0.43
Gilbert Multiplier	12.78	12.38	9.45	9.78
Comparator	20.38	14.83	13.63	16.47
8-bit Carry save multiplier	199.74	207.67	256.76	250.32
Applicable technology(μm)	0.8	0.8	0.35	0.35

Circuit simulation is an integral part of the IC design process and simulation provides an accurate, simple, and efficient tools in circuit design. The accuracy of circuit simulations is determined by the models used to describe the operation of the MOSFETs. It is apparent that accurate MOSFET models are essential to VLSI industry. Although many compact models for MOSFET's have been introduced to the public, their drawbacks limit the accuracy and convergence in specific operation regions. The first generation model, Level2 and Level3 models are highly empirical and contained discontinuity in their dc and capacitance analysis. They did not conserve charge and incorporate in the deep submicron devices. Most of these earlier problems which related which related with discontinuity in conductances at the boundaries between linear and saturation region or at the boundary between weak and strong inversion regions. These problems was resolved with imple-

menting single expression for all operation region by using three smoothing functions, hyperbola, exponential interpolation, and sigmoid function into the model expressions. The continuity of the current and its derivatives are ensured.

The S-CMOS model serves as the keystone of VLSI design which includes very lower and low voltage circuit circuits operating at 1.8V which are essential for the potable wireless communication and signal image processing including wireless video communication technologies.

At the most basic level, the circuit designer is the model consumer. Therefore, every circuit designer should be an educated model consumer. In presentation situation, closer interaction between modeling activities and the users of those activities, circuit designers, is needed. Also, since no analytical FET model is perfect, models can be more carefully built to address specific circuit design needs, while avoiding the wasting of time required to achieve model accuracy where it is not needed. Mixed signal deep-submicron circuit with analog and digital block have much challenges to VLSI designers.

Appendix A

Low Power Application for Digital CMOS Circuits

A.1. Power consumption Estimation

(A) Dynamic Power Estimation

Ignoring power dissipation due to direct path short circuit current, dynamic power of a CMOS circuit is due to the charging and discharging of load capacitances and internal node capacitances, which can be evaluated as follows[11],

$$P_{dyn} = P_{dyno} + P_{dynj}$$
$$= \frac{1}{2} \cdot f_{clk} \cdot \left(V_{dd}^2 \sum_i (\alpha_i \cdot C_{Li}) + V_{dd} \cdot \sum_i \sum_j (\alpha_i \cdot C_{Li} \cdot V_{ij}) \right) \quad \text{(A.1)}$$

where P_{dyno} and P_{dynj} are the dynamic power due to the load capacitances and the dynamic power due to the internal node capacitances, respectively. f_{clk} is the clock frequency. i represents the gate i and j denotes the jth internal node in a gate. V_{ij} is the voltage swing of the jth internal node of gate i, which equals to Vdd capacitance of gate i, respectively.

(B) Static Power Estimation

The leakage power of a CMOS circuit is determined by the leakage current through each transistor, which has two main sources: reversed biased diode junction leakage current and subthreshold leakage current. Diode leakage current is approximately $I_L=A_DJ_S$. A_D is the drain diffusion area of the device and J_S is the leakage current density of the device which is set by the technology. Diode leakage current is very sensitive for temperature and increase drastically with increasing temperature. Sub-threshold leakage current of deep-submicron MOS transistor is exponentially depend on the gate-source voltage under the subthreshold working condition. Under the standby working condition of the digital circuits; V_{GS}=0V and V_{DS}> 0V, there is a leakage current flow through the ground. For low threshold voltage deep-submicron devices, V_{th} <0.4V, sub-threshold leakage current become bigger than diode leakage current and behave the important role in DC power consumption of the digital circuits. Diode junction leakage is very small and can be ignored. Subthreshold leakage exponentially increases with the reduction of threshold voltage, making it critical for low voltage circuit design. Therefore, in our simulation, we focus on sub threshold leakage power estimation. In order to estimate leakage power accurately, a general transistor model, which considers subzero gate to source voltage (V_{GS}) for NMOS and super zero V_{GS} for PMOS (occurs when multiple series connected transistors are turned off), body effect and drain induced barrier lowering (DIBL), is used. The following analysis is done for NMOSFETs, but is equally applicable to PMOSFETs. If transistors are connected in parallel and are both turned off (such as in the pull down network of a NOR gate), then the values of V_{DS} and V_S are the same for each transistor. The leakage contribution of each transistor can be calculated separately and added together.

However, things become more complicated if they are in series. Consider the pull down network of an N input NAND gate. Without loss of generality, we consider the case where all N NMOS transistors are turned off. The quiescent subthreshold leakage through each transistor must be identical, given that other leakage components are negligible.

(C) DC (Standby) power consumption

For establishing a theoretical DC power model for the static CMOS circuits, one, two and three stack NMOS structures' standby currents should be examined for biasing condition as seen in Fig A.2. Drain induced barrier lowering (DIBL) is one of the important parameters for low-power applications. During subthreshold working of deep-submicron devices, flow of carriers under the influence of channel electrical field become more complicated and it is controlled by both drain-source voltage and gate-source voltage. When drain-source voltage was increased or the length of the channel was reduced, the depletion regions of the source and drain move closer, even overlap (punchthrough). This results in a field penetration from drain to source. This penetration causes the potential barrier at the source junction to be lowered. This effect is called drain-induced barrier lowering (DIBL) effect and increases with increasing gate oxide thickness and junction depth. DIBL effect could be reduced by increasing the surface and/or the substrate doping concentration, and reducing oxide thickness and junction depth. However, increasing doping concentration of the channel for short-channel devices cause in Hot Carrier Degradation[7].

A.2 Power Estimation Model

In S-CMOS model, total drain current is modeled as the linear sum of a strong inversion and weak inversion components which are expressed as;

$$I_{DS} = \frac{C_{OX} \cdot \mu_{eff} \cdot W}{L} \cdot \left[1 - fs \cdot e^{-\frac{V_{DS}}{V_T}}\right] \cdot [1 - (1 - fs) \cdot f_L + f_s \cdot K_{sub}] \cdot \times \left[2 \cdot n \cdot VT \cdot \ln\left(1 + e^{\frac{V_{GS} - V_{th}}{2 \cdot n \cdot V_T}}\right) \cdot V_{DSATh} - \frac{1}{2} \cdot V_{DSATh}^{\,2}\right] \quad \text{(A.2)}$$

$$I_{DSw} = C_{OX} \cdot \mu_{eff} \cdot \frac{W_{eff}}{Leff} \cdot n \cdot e^{1.8} \cdot V_T^{\,2} \cdot e^{\frac{V_{GS} - V_{th}}{nV_T}} \cdot \left(1 - e^{-\frac{V_{DS}}{VT}}\right) \quad \text{(A.3)}$$

$$I_{DSo} = C_{OX} \cdot \mu_{eff} \cdot \frac{W_{eff}}{Leff} \cdot n \cdot e^{1.8} \cdot V_T^{\,2} \quad \text{(A.4)}$$

$$_{th} = V_{FB} + \phi_S + \left(\gamma_1 - \frac{\gamma_{1L}}{L}\right)(\sqrt{\phi_s - V_{bsh}} - \sqrt{\phi s}) - \frac{Ks}{2}(\sqrt{\phi_s - V_{bsh}} - \sqrt{\phi_s})^2 + \gamma_2(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s - V_{BSh}}) + \frac{K_{NZ}}{W} + \frac{K_{NB} \cdot V_{BS}}{W} - \left(\eta z + \frac{\eta_L}{L}\right)V_{DS} - \frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - \exp\left(-\frac{L}{\eta_3}\right)\right) \quad \text{(A.}$$

For establishing a theoretical DC power model for the static CMOS circuits, one, two and three stack NMOS structures' standby currents should be examined for biasing condition as seen in Fig A.2.

A. ONE TRANSISTOR STRUCTURE

Standby current of one NMOS structure shown in Fig A.2(a). can be found using Eq. (A.3). For; and, Eq. (A.3) become,[5];

$$I_{S1} = I_o \cdot e^{-\frac{V_{th}}{n \cdot V_T}}$$

$$= I_o \cdot e^{-\frac{V_{th1}}{n \cdot V_T}} \qquad \text{(A.8)}$$

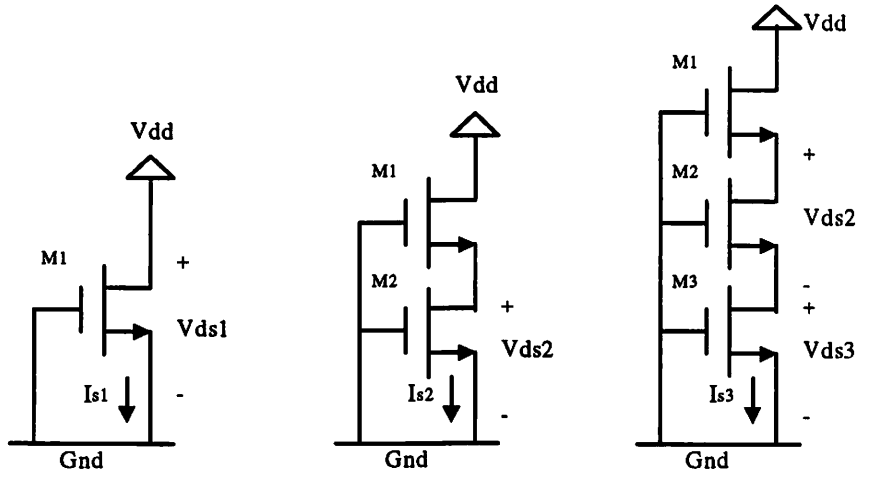


Figure A.2: (a) One NMOS , (b) two stack NMOS transistor, (c) three stack NMOS transistor configurations.

(B) TWO STACK TRANSISTORS STRUCTURE

Standby current of the two stack NMOS transistor structure seen in Fig.A. 1(b) can be written as;

$$I_{S2} = I_o \cdot e^{-\frac{V_{th1}}{n \cdot V_T}\left(1 - e^{-\frac{V_{ds1}}{V_T}}\right)} \qquad \text{(A.9)}$$

$$I_{S2} = I_o \cdot e^{-\frac{V_{th2}}{n \cdot V_T}\left(1 - e^{-\frac{V_{ds2}}{V_T}}\right)} \qquad \text{(A.10)}$$

where

$$V_{th1} = V_{FB} + \phi_S + \left(\gamma_1 - \frac{\gamma_{1L}}{L}\right)\left(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi s}\right) - \frac{Ks}{2}\left(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi_s}\right)^2 + \gamma_2\left(\sqrt{\phi_s - V_{BS}}\right.$$

$$\left. - \sqrt{\phi_s - V_{BSh}}\right) + \frac{K_{NZ}}{W} + \frac{K_{NB} \cdot V_{BS}}{W} - \left(\eta Z + \frac{\eta_L}{L}\right)V_{DS1} - \frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - \exp\left(-\frac{L}{\eta_3}\right)\right) \quad \text{(A.1}$$

and

$$V_{th2} = V_{FB} + \phi_S + \left(\gamma_1 - \frac{\gamma_{1L}}{L}\right)\left(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi s}\right) - \frac{Ks}{2}\left(\sqrt{\phi_s - V_{BSh}} - \sqrt{\phi_s}\right)^2 + \gamma_2\left(\sqrt{\phi_s - V_{BS}}\right.$$

$$\left. - \sqrt{\phi_s - V_{BSh}}\right) + \frac{K_{NZ}}{W} + \frac{K_{NB} \cdot V_{DS2}}{W} - \left(\eta Z + \frac{\eta_L}{L}\right)V_{DS2} - \frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - e^{\left(-\frac{L}{\eta_3}\right)}\right) \quad \text{(A.1}$$

$$= -Vds2 + V_{FB} + \phi_S + \left(\gamma_1 - \frac{\gamma_1}{L}\right) \cdot \left(\sqrt{\phi_S + V_{DS2}} - \sqrt{\phi s}\right) - \frac{Ks}{2}\left(\sqrt{\phi_S + V_{DS2}} - \sqrt{\phi_S}\right)^2$$

$$\gamma_2\left(\sqrt{\phi_S + V_{DS2}} - \sqrt{\phi s}\right) + \frac{K_{NZ}}{W} + \frac{K_{NB} \cdot V_{DS2}}{W} - \left(\eta Z + \frac{\eta_L}{L}\right)V_{DS2} - \frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - e^{\left(-\frac{L}{\eta_3}\right)}\right) \quad \text{(A.13)}$$

We can equate the current of the first (top) and second transistor. Eq. (A.14) can be obtained by solving for V_{DS2} in terms of Vdd (assume that $V_{S1} << V_{dd}$)[13].

$$V_{DS2} = \frac{nV_T}{(1 + 2\eta + \gamma)} \ln\left(\frac{I_{o1}}{I_{o2}} \cdot e^{\frac{\eta V_{dd}}{nV_T}} + 1\right) \quad \text{(A.14)}$$

$$V_{DSi} = \frac{nV_T}{(1 + \gamma)} \ln\left(\frac{I_{o,i-1}}{I_{o,i}}\left(1 - e^{\frac{V_{DS(i-1)}}{V_T}}\right) + 1\right) \quad \text{(A.15)}$$

$$P_{leak} = \sum_i I_{DSqi} \cdot V_{DSqi} \quad \text{(A.16)}$$

The general method of computing leakage power for a large circuit involves the following steps. Given a particular set of circuit input values, determine which pullup and pulldown networks are turned off. Within each network, the transistors which are turned on can be treated as short circuits. Transistors that are parallel to a transistor that is turned on can be eliminated from the leakage calculation. Given the resulting simplified network, estimate V_{DS} for the remaining transistors using Eq.(A.9) and (A10.). Finally, the magnitude of leakage current and resulting leakage power can be computed. The above method is very suitable for leakage power estimation during standby mode. In active mode, the time required for the leakage current in transistor stacks to con verge to its final value is determined by the internal node capacitance, input conditions, and subthreshold leakage current. Subthreshold leakage current strongly depends on the threshold voltage and temperature. If the in terminal node capacitance is small and active temperature is high, the given method can also be used to estimate active leakage power of low Vth circuits, especially at low switching activities. Considering the fact that standby leakage current depends on input signal levels, the average leakage power can be evaluated with random patterns applied to primary inputs. Ratio of drain source voltage to thermal voltage was found bigger than 2. Therefore, we can neglect the second exponential terms of Eq. (A.9) and (A.10). Since, typically, surface inversion potential (f_s) is between 0.7 and 1.5, we can write;

$$\sqrt{1+\frac{V_{ds2}}{\phi_s}} \cong 1+\frac{V_{ds2}}{\phi_s} \qquad \text{(A.17)}$$

So, we can extract voltage from Eq. (A.9) and (A.10)using the assumptions given above.

$$V_{ds2} = \frac{\left(\eta_Z + \frac{\eta_L}{L}\right)V_{dd}}{1 + \eta_Z + \frac{\eta_L}{L} + \frac{\gamma_1 + \frac{\gamma_{1L}}{L}}{2\sqrt{\phi_S}} - K_S} = \frac{\left(\eta_Z + \frac{\eta_L}{L}\right)V_{dd}}{K} \qquad \text{(A.18)}$$

where

$$K = 1 + \eta_Z + \frac{\eta_L}{L} + \frac{\gamma_1 + \frac{\gamma_{1L}}{L}}{2\sqrt{\phi_S}} - K_S$$

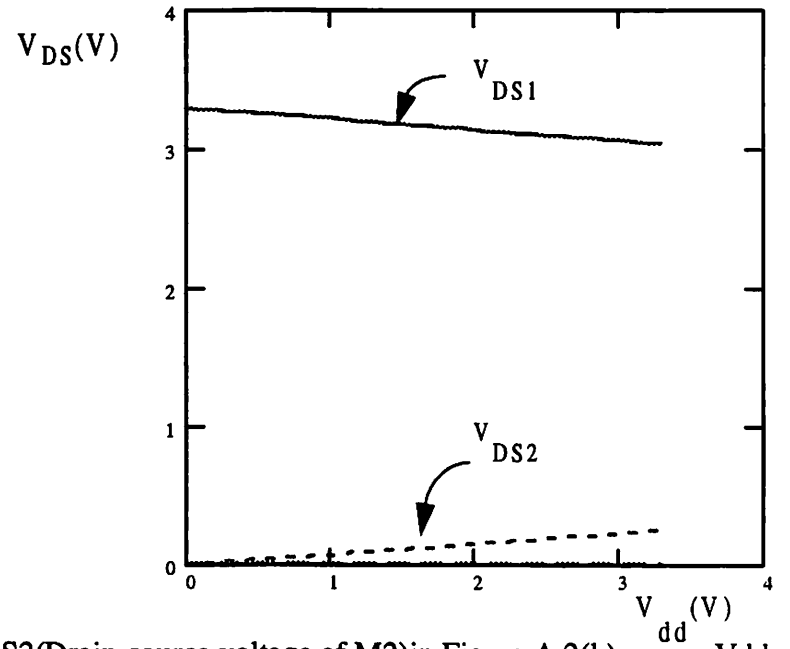


Figure A.3. VDS2(Drain-source voltage of M2)in Figure A.2(b) versus Vdd voltage (W=1.0μm, L=0.35μm)

(C) THREE STACK TRANSISTORS STRUCTURE

For three stack transistors structure, seen in Fig A.2(c), we can write the standby current, I_S, as seen below.

$$I_{S3} = I_o \cdot e^{-\frac{V_{th3}}{n \cdot V_T}}\left(1 - e^{-\frac{V_{ds3}}{V_T}}\right) \tag{A.19}$$

$$I_{S3} = I_o \cdot e^{-\frac{V_{th2}}{n \cdot V_T}}\left(1 - e^{-\frac{V_{ds2}}{V_T}}\right) \tag{A.20}$$

$$I_{S3} = I_o \cdot e^{-\frac{V_{th1}}{n \cdot V_T}}\left(1 - e^{-\frac{V_{dd}-V_{ds2}-V_{ds2}}{V_T}}\right) \tag{A.21}$$

Where

$$V_{th3} = V_{FB} + \phi_S + \left(\gamma_1 - \frac{\gamma_{1L}}{L}\right)\left(\sqrt{\phi_s - V_{bsh}} - \sqrt{\phi s}\right) - \frac{Ks}{2}\left(\sqrt{\phi_s - V_{bsh}} - \sqrt{\phi_s}\right)^2 + \gamma_2\left(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s - V_{BSh}}\right) + \frac{K_{NZ}}{W} + \frac{K_{NB} \cdot V_{BS}}{W} - \left(\eta Z + \frac{\eta_L}{L}\right)V_{DS3} - \frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - \exp\left(-\frac{L}{\eta_3}\right)\right) \tag{A.22}$$

and

$$V_{th2} = V_{FB} + \phi_S + \left(\gamma_1 - \frac{\gamma_{1L}}{L}\right)\left(\sqrt{\phi_s - V_{bsh}} - \sqrt{\phi s}\right) - \frac{Ks}{2}\left(\sqrt{\phi_s - V_{bsh}} - \sqrt{\phi_s}\right)^2 + \gamma_2\left(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s - V_{BSh}}\right) + \frac{K_{NZ}}{W} + \frac{K_{NB} \cdot V_{BS}}{W} - \left(\eta Z + \frac{\eta_L}{L}\right)V_{DS2} - \frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - e^{\left(-\frac{L}{\eta_3}\right)}\right)$$

$$= -V_{ds3} + V_{FB} + \phi_S + \left(\gamma_1 - \frac{\gamma_{1L}}{L}\right) \cdot \left(\sqrt{\phi_S + V_{ds3}} - \sqrt{\phi s}\right) - \frac{Ks}{2}\left(\sqrt{\phi_S + V_{ds3}} - \sqrt{\phi_S}\right)^2$$

$$\gamma_2\left(\sqrt{\phi_S + V_{ds2}} - \sqrt{\phi s}\right) + \frac{K_{NZ}}{W} + \frac{K_{NB} \cdot V_{ds2}}{W} - \left(\eta Z + \frac{\eta_L}{L}\right)V_{ds2} - \frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - e^{\left(-\frac{L}{\eta_3}\right)}\right) \tag{A.23}$$

and

$$V_{th1} = V_{FB} + \phi_S + \left(\gamma_1 - \frac{\gamma_{1L}}{L}\right)(\sqrt{\phi_s - V_{bsh}} - \sqrt{\phi s}) - \frac{Ks}{2}(\sqrt{\phi_s - V_{bsh}} - \sqrt{\phi_s})^2 + \gamma_2(\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s - V_{BSh}}) + \frac{K_{NZ}}{W} + \frac{K_{NB} \cdot V_{BS}}{W} - \left(\eta Z + \frac{\eta_L}{L}\right)V_{DS2} - \frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - e^{\left(-\frac{L}{\eta_3}\right)}\right)$$

$$= -V_{ds3} - V_{ds2} + V_{FB} + \phi_S + \left(\gamma_1 - \frac{\gamma_{1L}}{L}\right) \cdot (\sqrt{\phi_S + V_{ds2} + V_{ds3}} - \sqrt{\phi s}) - \frac{Ks}{2}(\sqrt{\phi_S + V_{ds2} + V_{ds3}} - \sqrt{\phi_S})^2$$

$$+ \gamma_2(\sqrt{\phi_S + V_{ds3} + V_{ds2}} - \sqrt{\phi s}) + \frac{K_{NZ}}{W} + \frac{K_{NB}(V_{ds2} + V_{ds3})}{W} - \left(\eta Z + \frac{\eta_L}{L}\right)V_{dd} - \frac{\eta_1}{L} + \frac{\eta_2}{L} \cdot \left(1 - e^{\left(-\frac{L}{\eta_3}\right)}\right) \quad \text{(A.24)}$$

Since $V_{ds} > V_T$ and $V_{dd} - V_{ds2} - V_{ds3} > V_T$, second exponential terms of the Eq. (A.20), and (A.21) could be neglected. For simplifing Eq. (A.19), (A.20), and (A.21) and estimating voltage, SPICE simulation was conducted, Fig A.4. It was found that V_{ds3} is smaller than V_T. Thus, second exponential term of the Eq. (A.19) should be reduced as given below.

$$\exp\left(-V_{ds3}/V_T\right) \cong 1 - \frac{V_{ds3}}{V_T} \quad \text{(A.25)}$$

From Eq.A (19).Eq.A (24), VDS3 can be expressed by

$$\log\left(\frac{V_{ds3}}{V_T}\right) + \frac{K}{n} \cdot \frac{V_{ds3}}{V_T} = \frac{\eta^2 \cdot V_{dd}}{C \cdot n \cdot V_T} \quad \text{(A.26)}$$

For typical deep-submicron devices, the term in the right side of the Eq. (A.25) is of the order of 0.1, [5]. Also the parameters, n and K are in the same order and they cancel each other in the Eq. (A.26), [5]. As a result, in general, Eq. (A.26) could be written as seen below.

$$\log\left(\frac{V_{ds3}}{V_T}\right)+\frac{V_{ds3}}{V_T}=0 \tag{A.27}$$

From Eq.(A.27) V_{ds3} can be found;

$$V_{ds3}\approx 0.4V_T\approx 11mV \tag{A.28}$$

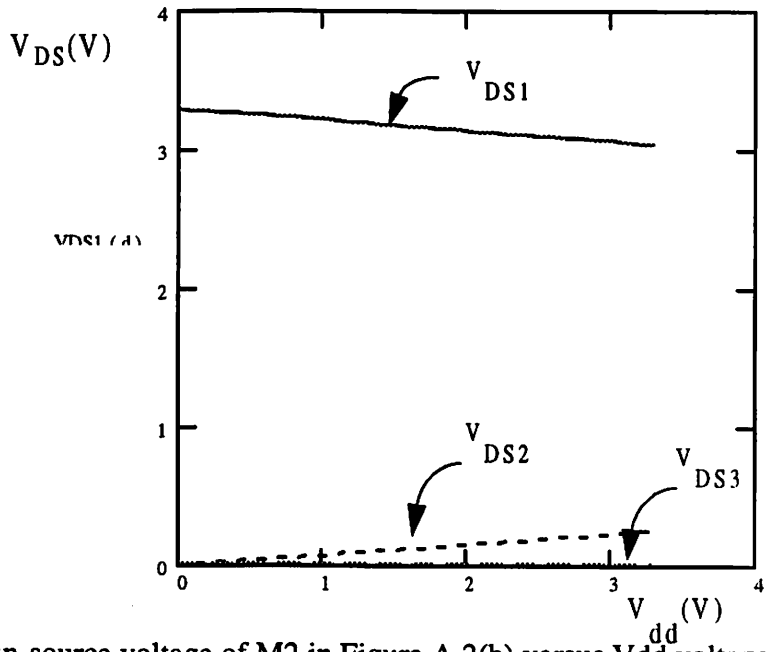


Figure A.4. Drain-source voltage of M2 in Figure A.2(b) versus Vdd voltage (W=1.0μm, L=0.35μm)

As seen in Fig. A.4., V_{ds3} seems slightly depended on the supply voltage. This dependency will be extracted for specific technology. But in this level, it will be assumed that current is independent from the supply voltage. Using this assumption, threshold voltage should be written as seen below.

$$V_{th}\cong V_{tho}-\left(\eta_Z+\frac{\eta_L}{L}\right)V_{dd} \tag{A.29}$$

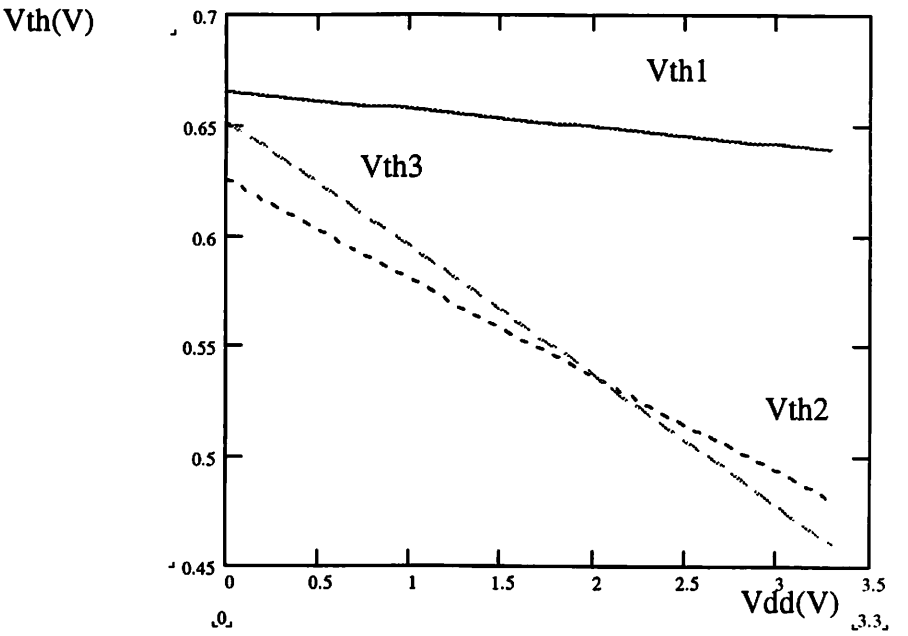


Figure A.5. Drain-source voltage of M2, M3 in Figure A.2(c) versus Vdd voltage

We can arrange the standby current of one, two, and three stack transistors as given below.

$$I_{S1} = I_o \cdot e^{\frac{V_{dd} \cdot \eta_Z}{n \cdot V_T}} \tag{A.30}$$

$$I_{S2} = I_o \cdot e^{\frac{V_{dd} \cdot \eta_Z^2}{n \cdot V_T \cdot K}} \left(1 - e^{-\frac{V_{ds3}}{V_T}}\right) \tag{A.31}$$

$$I_{S3} = I_o \cdot e^{\frac{V_{ds3}}{n \cdot V_T}} \left(1 - e^{-\frac{V_{ds3}}{V_T}}\right) \tag{A.32}$$

where

$$K = 1 + \eta_Z + \frac{\eta_L}{L} + \frac{\gamma_1 + \frac{\gamma_{1L}}{L}}{2\sqrt{\phi_S}} - K_S \tag{A.33}$$

and

$$V_{ds3} \approx 0.4 V_T \approx 11mV \tag{A.34}$$

$$V_{tho} = \gamma_Z \sqrt{\phi_S} - K_S \phi_S \tag{A.35}$$

$$I_o^{'} = C_{OX} \cdot \mu_o \cdot \frac{W_{eff}}{Leff} \cdot e^{1.8} \cdot V_T^{\,2} \cdot e^{\left(-\frac{V_{tho}}{V_T}\right)} \tag{A.36}$$

$$P_{dc,av.} = \left(\sum_{i=1}^{N} \alpha_i \cdot A_i \right) \cdot I_0^{'} \cdot V_{dd} \tag{A.37}$$

Since each deep-submicron technology has different process parameters, Eq. (A.34) should be different for different processes. As seen in Fig A.4., V_{ds3} is depended on the supply voltage, threshold voltage and other process parameters. As seen in Eq.'s (A.30), (A.31), and (A.32) drain induced barrier lowering (DIBL) effect is key parameter for reducing standby current and DC (standby) power consumption of the system.

A.3 DC (Standby) Power Consumption of Static CMOS Circuits

Using the expressions found in section A.2.2, DC power consumption of different type of logic gates could be found, if the S-CMOS parameters of the deep-submicron process are known. In the next sections, during examining the DC power of the static gates, it will be assumed that the standby current of the PMOS devices and the NMOS devices are same in the circuits. Since standby current is become negligible when the number of stacked transistors are more than three, we can use this model up to 3 input logic gates. Under these assumptions, average DC power consumption of an m-input static logic gate written as[11];

where, a_i is the product of transition probability of inputs for the state i. N is the number of input combination (2^m). A_i is the standby current normalization factor of the input combination i. $I_0^{'}$ is the current given in Eq. (A.36). If transition probability of the input states are same, Eq. (34) become;

$$P_{dc,av.} = \frac{1}{2^m} \cdot \left(\sum_{i=1}^{N} A_i \right) \cdot I_0^{'} \cdot V_{dd} \qquad \text{(A.38)}$$

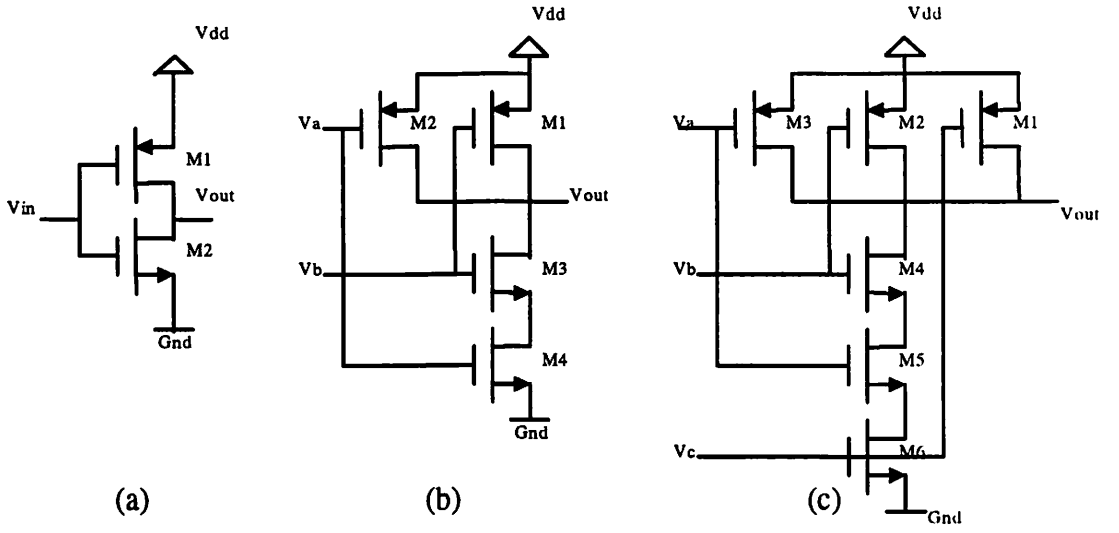


Figure A.6 (a). Static CMOS inverter, (b).2-Input NAND gate, (c) 3-Input NAND gate.

A.4 DC Power Consumption of two and three-input static CMOS gates.

Since the number of transistors in 2-input NAND and NOR gates are equal, their average standby currents and DC power consumption are found same for equal logic-1 and logic-0 input probabilities as seen in Table A.1. Same situation is valid for 3-input NAND and NOR gates under the same assumptions as seen in Table A.6. Using Eq. (A.38), average DC (standby) power consumption of the inverter, 2- and 3-input NAND and NOR gates for different input logic level probabilities could be calculated as seen in Fig A.6. Also, using S-CMOS parameters given, I_{s1},I_{s2}, and I_{s3} were found by using Eq.'s (A.30)...(A.36) for 1V supply voltage.

$$I_{s1} = 7.778 \cdot I_o^{'}$$

$$I_{s2} = 1.115 \cdot I_o^{'}$$

$$I_{s3} = 0.633 \cdot I_o^{'} \qquad \text{(A.39)}$$

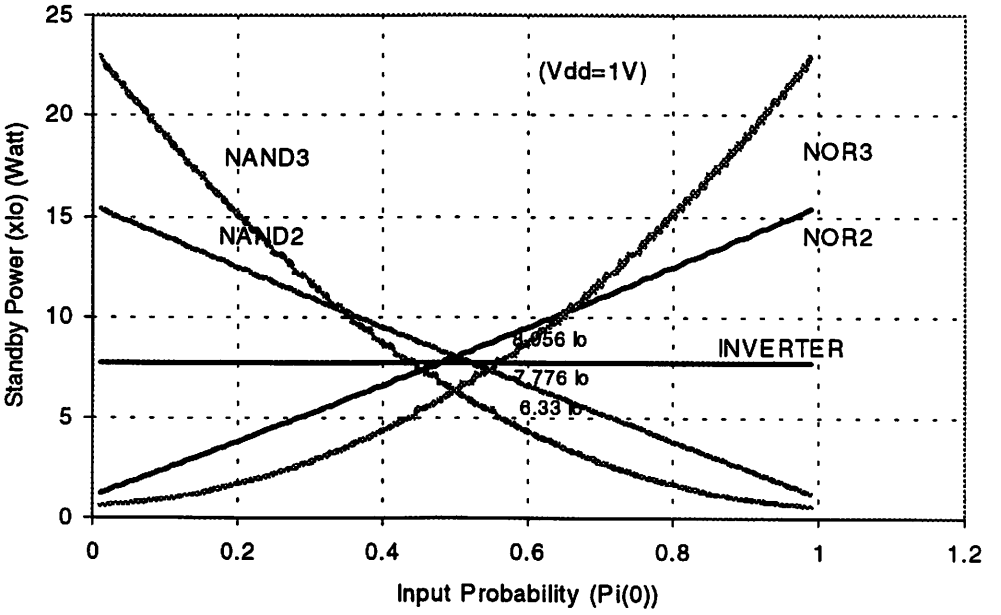


Figure A.7 Standby current of 2 and 34 input NAND and NOR gate vs. input probability

CMOS inverter's average standby current is independent from the probabilities of the inputs and equal to the sextets. Average DC power dissipation of 2- and 3-input NAND and NOR gates for equal input probabilities are found as seen below.

Table A.1 Standby current of 2-input NAND and NOR gates

A	B	NAND2	NOR2
0	0	I_{s2}	$2I_{s1}$
0	1	I_{s1}	I_{s1}
1	0	I_{s1}	I_{s1}
1	1	$2I_{s1}$	I_{s2}

(Inverter)

$$P_{dc,av.} = I_{s1} \cdot V_{dd} \tag{A.40}$$

(NAND2 and NOR2 gates)

$$P_{dc,av.} = 0.25 \cdot \left(4 \cdot I_{s1} + I_{s2}\right) \cdot V_{dd} \tag{A.41}$$

(NAND3 and NOR3 gates)

$$P_{dc,av.} = 0.125 \cdot \left(6 \cdot I_{s1} + 3 \cdot I_{s2} + I_{s3}\right) \cdot V_{dd} \tag{A.42}$$

Table A.2 Standby current of 3-input NAND and NOR gates

A	B	C	NAND3	NOR3
0	0	0	I_{s3}	$3I_{s1}$
0	0	1	I_{s2}	I_{s1}
0	1	0	I_{s2}	I_{s1}
0	1	1	I_{s1}	I_{s2}
1	0	0	I_{s2}	I_{s1}
1	0	1	I_{s1}	I_{s2}
1	1	0	I_{s1}	I_{s2}
1	1	1	$3I_{s1}$	I_{s3}

Average DC power consumption of the gates were found for equal input probabilities;

(Inverter)

$$P_{dc,av.} = 7.778 \cdot I_0^{'} \tag{A.43}$$

(NAND2 and NOR2 gates)

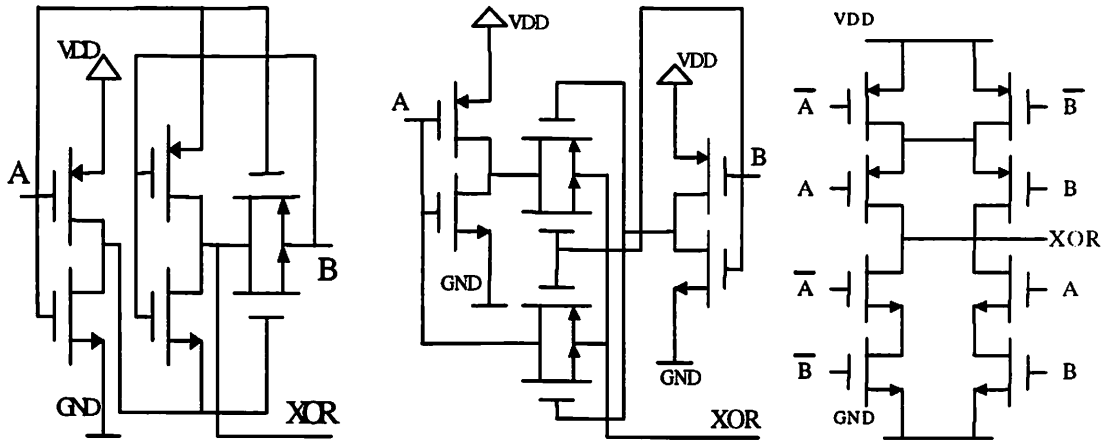
$$P_{dc,av.} = 8.056 \cdot I_0^{'} \tag{A.44}$$

(NAND3 and NOR3 gates)

$$P_{dc,av.} = 6.330 \cdot I_0^{'} \tag{A.45}$$

A.5 DC Powwer Consumption of XOR gates

The exclusive-OR (XOR) and exclusive-NOR (XNOR) gates are main building blocks of digital circuits, such as comparator, parity checker, full adder. Thus, their DC (standby) power dissipation are worth to be examined. For examining DC (standby) power dissipation of XOR gates, three different kinds of well known and used XOR structures were chosen which are 6 and 8 transistors transmission gate (TG) XOR, and conventional CMOS XOR structures as seen in Fig A.7, [8],[9]. Under the equal input logic probabilities, standby current performance of the XOR gates are given in Table A.3 for 1V supply voltage (Vdd=1V).



(a) (b) (c)

Figure A.8.a) 6-tr. XOR gate, b) 8-tr. XOR gate, c) Complementary XOR gate .

Table A.3 Standby current of 6 tr. XOR and 8 tr. XOR gates

A	B	XOR (6-tr.)	XOR(8-tr.)	XOR(Conv.)
0	0	$2I_{s1}$	$4I_{s1}$	$4I_{s1}$
0	1	$4I_{s1}$	$4I_{s1}$	$4I_{s1}$
1	0	$2I_{s1}$	$4I_{s1}$	$4I_{s1}$
1	1	$4I_{s1}$	$4I_{s1}$	$4I_{s1}$

(6-tr. TG-XOR)

$$P_{dc,av.} = 3 \cdot I_{s1} \cdot V_{dd} = 23.334 \cdot I_0' \tag{A.46}$$

(8-tr. TG-XOR, Conv.CMOS XOR)

$$P_{dc,av.} = 4 \cdot I_{s1} \cdot V_{dd} = 31.112 \cdot I_0' \tag{A.47}$$

For different input logic probabilities, DC power performance of the chosen XOR gates are found by using Eq. (A.37). It is shown in Fig A.8.

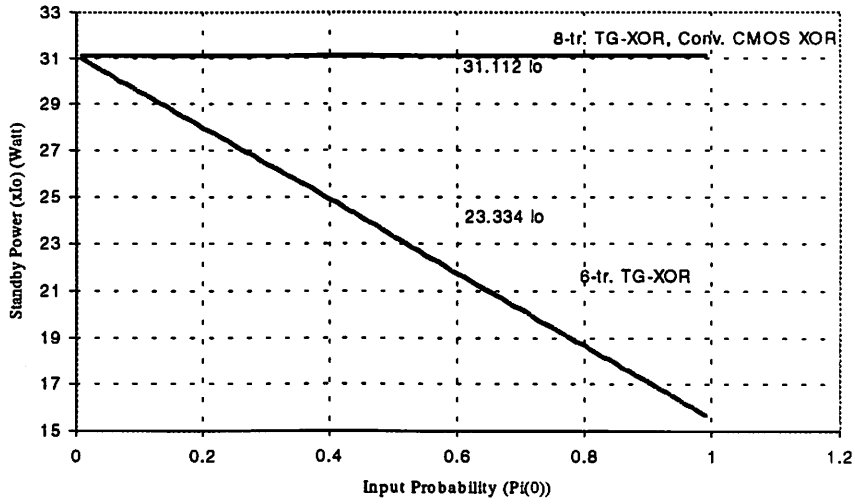
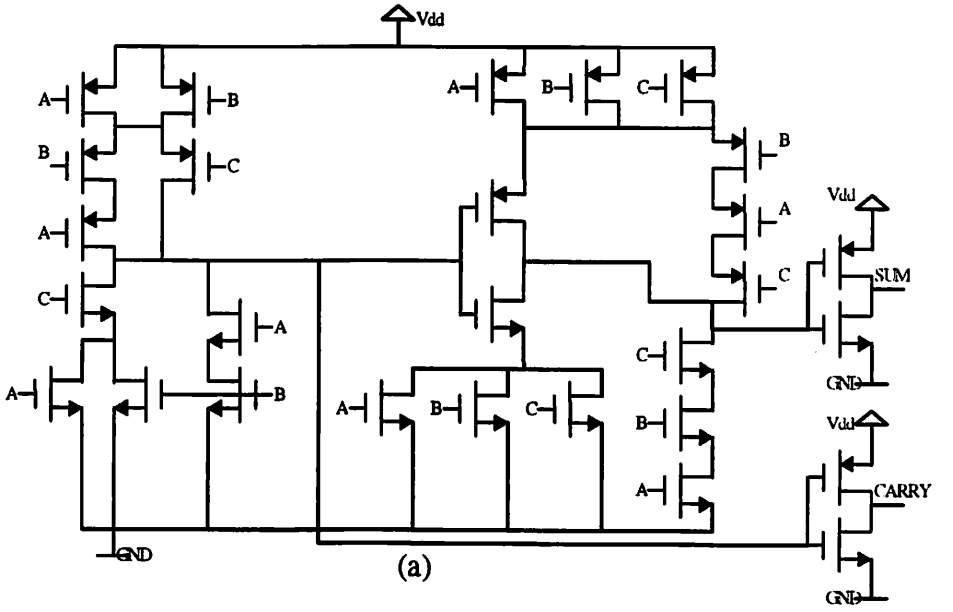


Figure A.9. DC (standby) Power dissipation of 8-tr. and 6-tr. TG XOR and conventional CMOS XOR gates for different input probabilities.(Vdd=1V)

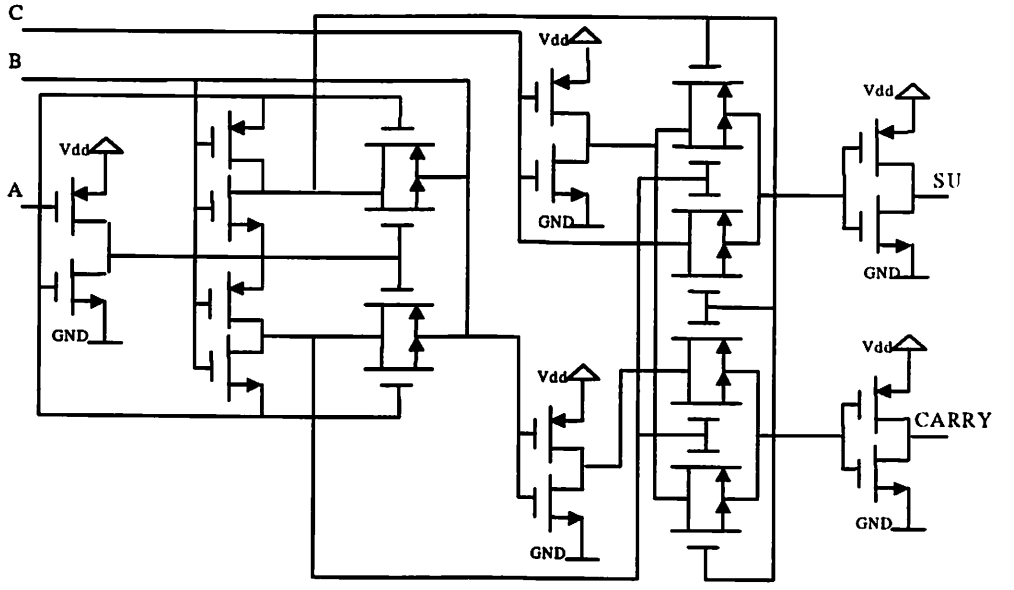
As seen in Fig A.9., for equal input level probabilities, DC power dissipation of 6-transistors TG XOR gate is better than the conventional CMOS and 8-transistors TG- XOR gates.

A.6. DC Power Dissipation of full adders

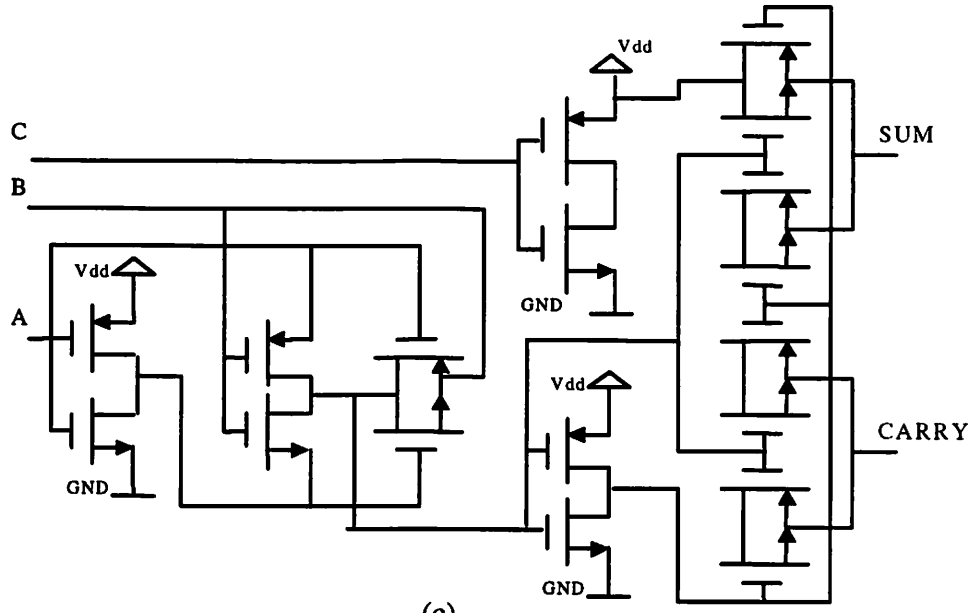
Since full adders are the main units of the arithmetic operations, and most of the portable systems have embedded arithmetic units, their DC power consumption are also to be analyzed and optimized in logic and process level. For this purpose, three types of full adder structures which are conventional CMOS full adder, TG full adder, and optimized TG full adder were chosen for DC power consumption analysis as seen in Fig. A.10 [9],[10]. Their standby power consumption of the circuits for different input level probabilities are given in Fig. A.11.



(a)

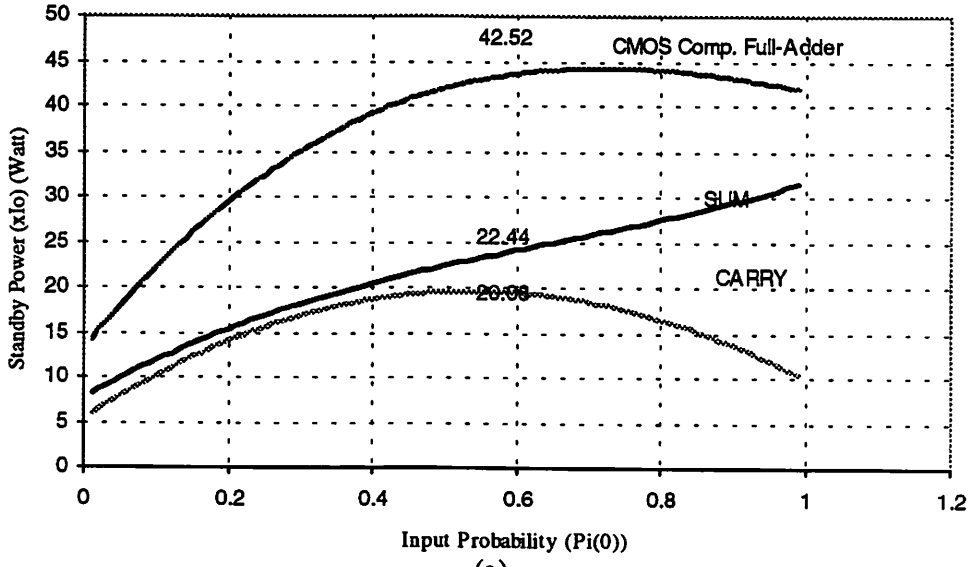


(b)

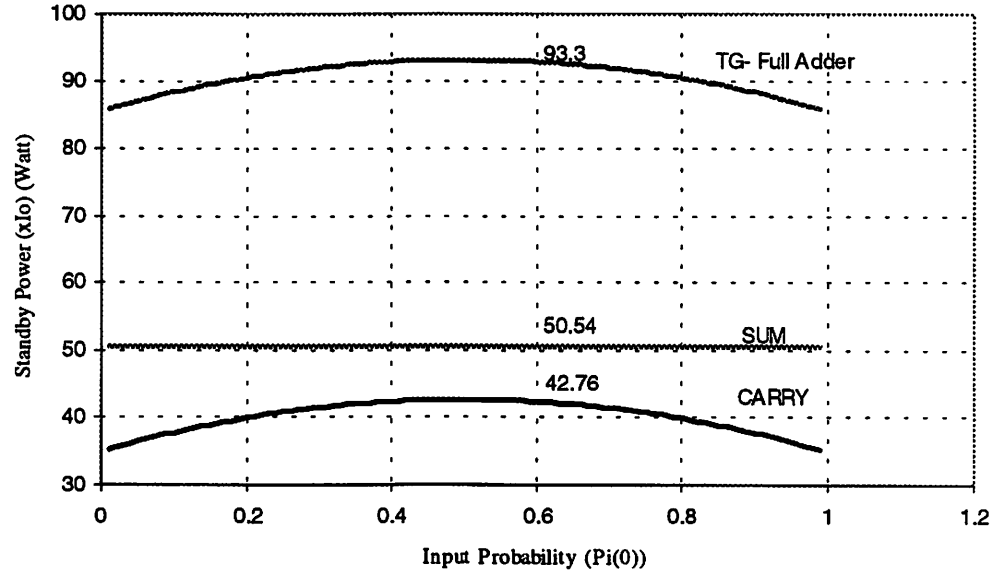


(c)

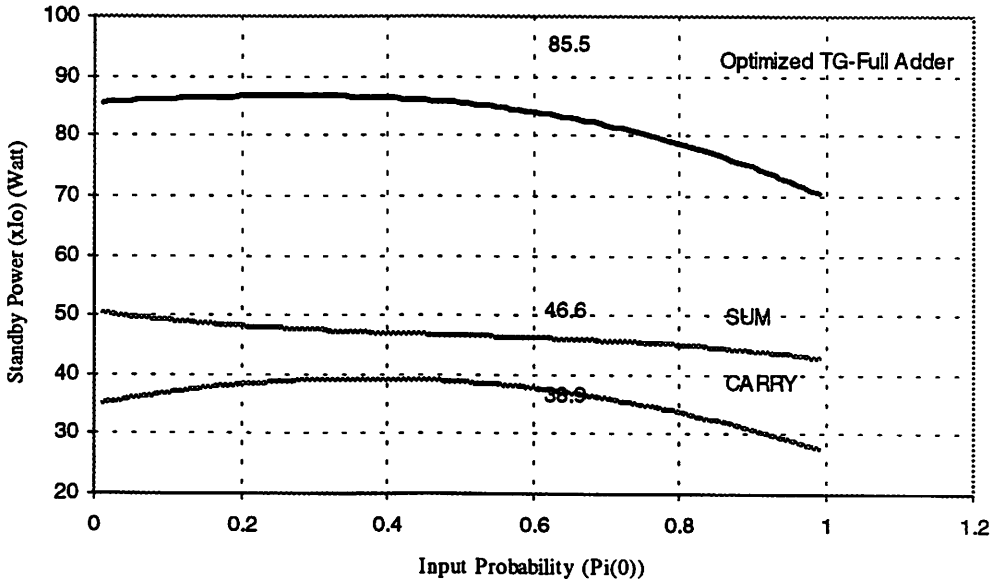
Figure A.10: (a) CMOS Complementary Full-Adder, (b) TG-Full Adder, (c) Optimized TG-Full Adder



(a)



(b)



(c)

Figure A.11 DC (Standby) Power Dissipation of (a) CMOS Complementary Full-Adder, (b) TG Full-Adder,(c).Optimized TG Full-Adder for different input probabilities

Table A.4 Standby current of adders

INPUTS			CMOS Comp. Full-Adder		TG Full Adder		OPT.-TG Full Adder	
C	B	A	CARRY	SUM	CARRY	SUM	CARRY	SUM
0	0	0	$2I_{s2} + I_{s1}$	$4I_{s1} + I_{s3}$	$4.5I_{s1}$	$6.5I_{s1}$	$3.5I_{s1}$	$5.5I_{s1}$
0	0	1	$3I_{s1}$	$3I_{s1}$	$4.5I_{s1}$	$6.5I_{s1}$	$4.5I_{s1}$	$6.5I_{s1}$
0	1	0	$3I_{s1}$	$3I_{s1}$	$6.5I_{s1}$	$6.5I_{s1}$	$5.5I_{s1}$	$6.5I_{s1}$
0	1	1	$3I_{s1}$	$3I_{s1}$	$6.5I_{s1}$	$6.5I_{s1}$	$6.5I_{s1}$	$5.5I_{s1}$
1	0	0	$3I_{s1} + I_{s2}$	$3I_{s1}$	$6.5I_{s1}$	$6.5I_{s1}$	$5.5I_{s1}$	$5.5I_{s1}$
1	0	1	$3I_{s1}$	$3I_{s1}$	$6.5I_{s1}$	$6.5I_{s1}$	$6.5I_{s1}$	$6.5I_{s1}$
1	1	0	$3I_{s1}$	$3I_{s1}$	$4.5I_{s1}$	$6.5I_{s1}$	$3.5I_{s1}$	$5.5I_{s1}$
1	1	1	$I_{s1}+I_{s2}+I_{s3}$	I_{s1}	$4.5I_{s1}$	$6.5I_{s1}$	$4.5I_{s1}$	$6.5I_{s1}$

Standby currents of carry and sum lines for different input combinations are given in Table A.4. Average standby current of the circuits for equal input level probabilities are;

$$P_{dc,av.}(CARRY) = \begin{cases} 0.125 \cdot \left(20 \cdot I_{s1} + 4 \cdot I_{s2} + I_{s3}\right) \cdot V_{dd} & (Conv.CMOS) \\ 5.5 \cdot I_{s1} \cdot V_{dd} & (TG) \\ 5 \cdot I_{s1} \cdot V_{dd} & (OPT.\text{–}TG) \end{cases} \tag{A.48}$$

$$P_{dc,av.}(SUM) = \begin{cases} 0.125 \cdot \left(23 \cdot I_{s1} + I_{s3}\right) \cdot V_{dd} & (Conv.CMOS) \\ 6.5 \cdot I_{s1} \cdot V_{dd} & (TG) \\ 6 \cdot I_{s1} \cdot V_{dd} & (OPT.\text{–}TG) \end{cases} \tag{A.49}$$

For the S-CMOS parameters., DC power dissipation of the adders for equal input probabilities are;

$$P_{dc,av.}(CARRY) = \begin{cases} 20.08 \cdot I_0' & (Conv.CMOS) \\ 42.76 \cdot I_0' & (TG) \\ 38.9 \cdot I_0' & (OPT.-TG) \end{cases} \quad \text{(A.50)}$$

$$P_{dc,av.}(SUM) = \begin{cases} 22.44 \cdot I_0' & (Conv.CMOS) \\ 50.54 \cdot I_0' & (TG) \\ 46.66.9 \cdot I_0' & (OPT.-TG) \end{cases} \quad \text{(A.51)}$$

Also for different input level probabilities, total DC (standby) power dissipation of the adders are shown in Fig A.12.

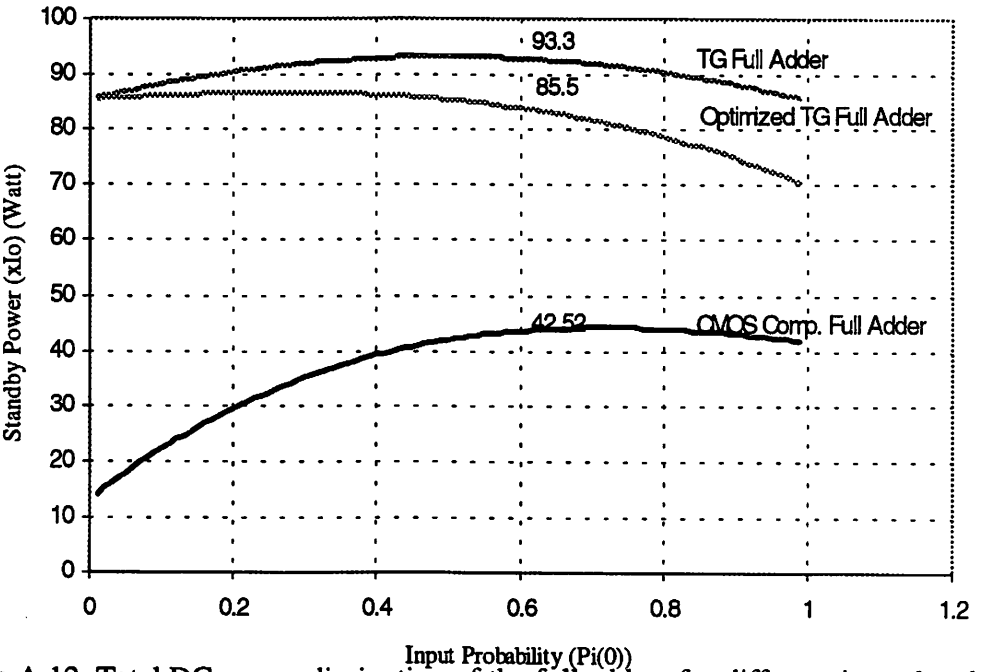


Figure A.12. Total DC power dissipation of the full adders for different input level probabilities

As clearly seen in the Fig A.11, DC (standby) power dissipation of the conventional CMOS full adder is better than both TG and optimized-TG full adders.

A.7 Optimizing power delay product of CMOS digital circuits

In this section, it will be established an optimization method for DC power consumption. This method will be applied to the process parameters. For different supply voltages, normalization factors of I_{s1}, I_{s2}, and I_{s3} are given in Table A.5. As clearly seen in the Table A.5, biggest standby current is one stack transistor current I_{s1}. Therefore, this standby current is dominant factor for the DC power consumption of the basic digital building blocks. Optimum supply voltage, threshold voltage and other device parameters which are play important role on the DC power consumption can be obtained by optimizing the power delay product of a simple inverter which basically is one stack transistor structure. Power delay product of MOS digital circuits is given as;

$$PDP_t = \left(I_{s1} \cdot V_{dd} + P_{dyn.}\right) \cdot t_d = PD_{s1} + PD_{dyn.} \tag{A.52}$$

where is the delay time of an inverter, [11];

$$t_d = \frac{C_L \cdot V_{dd}}{I} = \frac{C_L \cdot V_{dd}}{\frac{\mu \cdot C_{ox}}{2}(W/L)(V_{dd} - V_{tho})^2} = k_d \cdot \frac{V_{dd}}{(V_{dd} - V_{tho})^2} \tag{A.53}$$

and PD_{dyn} is dynamic power dissipation of inverter.

$$P_{dyn.} = C_L \cdot f \cdot V_{dd}^{\ 2} \tag{A.54}$$

Table A.5 Nomalization factors of I_{s1}, I_{s2}, and I_{s3} (η=0.08)

Standby Current	Vdd (V)			
	2.0	1.5	1.0	0.7
I_{s1}	60.495	21.691	7.778	4.203
I_{s2}	1.268	1.195	1.115	1.087
I_{s3}	0.671	0.652	0.633	0.501

I_{s1} is;

$$I_{S1} = I_o' e^{\frac{\left(\eta_Z + \frac{\eta_L}{L}\right)V_{dd}}{nV_T}} \tag{A.55}$$

The power delay product(PDP) can be derived by setting the derivatives of PD_{s1} and PD_{dyn} with respect to V_{dd} to zero

$$\frac{d}{dV_{dd}} PD_{s1} = 0 \tag{A.56}$$

and

$$\frac{d}{dV_{dd}} PD_{dyn} = 0 \tag{A.57}$$

Vdd can be expresed by

$$V_{dd} = 3 \cdot V_{th} \tag{A.58}$$

and

$$V_{dd}^2 - \left(V_{tho} + \frac{n \cdot V_T}{\eta}\right) \cdot V_{dd} - \frac{n \cdot V_T \cdot V_{tho}}{\eta} = 0 \qquad \text{(A.59)}$$

From Eq.(A.59), Vdd can be found by[11],

$$V_{dd} = \frac{1}{2}[V_{tho} + p + \sqrt{(V_{tho} + p)^2 + 4p \cdot V_{tho}}] \qquad \text{(A.60)}$$

where

$$p = \frac{nV_T}{\eta_Z + \frac{\eta_L}{L}} \qquad \text{(A.61)}$$

Fig A.13 is shows the dependency of V_{dd} to V_{th} and η. As seen in Fig A.13, DIBL parameters of the MOS device plays important role for optimizing PDP of the digital circuits. Intersections of PD_{s1} and PD_{dyn}. lines are the optimum supply and threshold voltages for given DIBL parameters.

Three optimum values were found which are;

Vdd=0.78V, Vtho =0.260V, $\eta = 0.1$

Vdd=0.94V, Vtho =0.317V, η =0.08

Vdd=1.27V, Vtho =0.425V, η =0.06

Here, Vdd is 1 Volt, and the standby currents are;

$Is1=7.778I_o'$

$Is2=1.115I_o'$

$$Is3=0.633I_o'$$

Optimized standby currents are found for =0.94V, which are

$$Is1=6.877I_o'$$

$$Is2=1.08\ I_o'$$

$$Is3=0.563I_o'$$

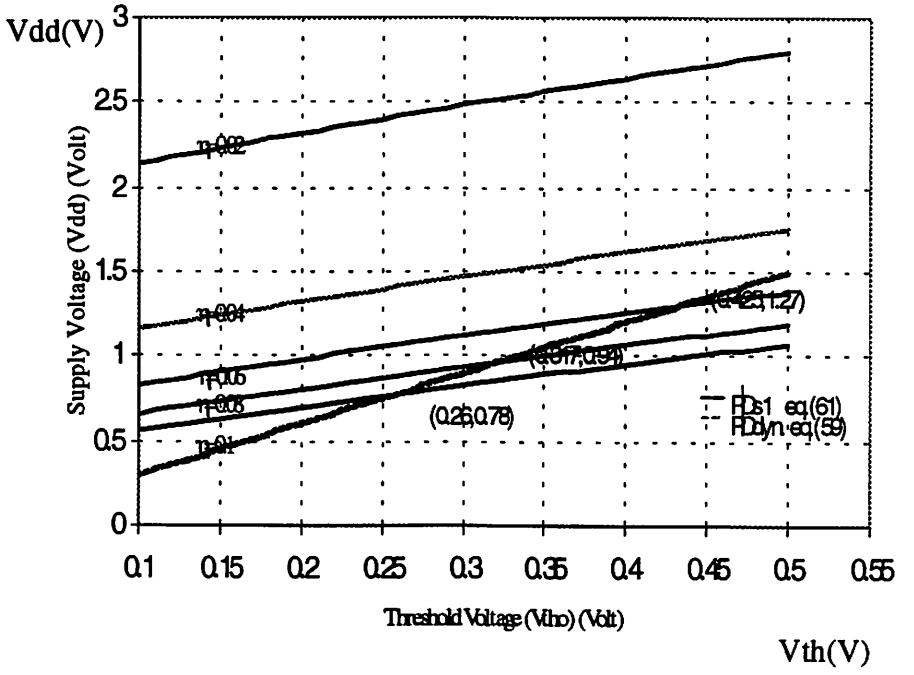


Figure A.13: Supply voltage versus threshold voltage for optimum Power Delay Product.

Total power reduction of the digital building blocks are given in Table A.6 for equal input logic probabilities. After the optimization, 11 percent power saving was accomplished in average for the digital building blocks.

Table A.6 Nomalized DC power dissipation before and after the optimization

	DC Power (normalized)		
Digital Building Blocks	Before Opt.	After Opt.	Reduction (%)
Inverter	7.778	6.877	11.6
NAND2,NOR2	8.056	7.147	11.3
NAND3,NOR3	6.330	5.633	11.0
Conv. CMOS XOR, 8-tr TG-XOR	31.112	27.508	11.6
6-tr. TG-XOR	23.334	20.631	11.6
CMOS Full Adder	42.520	37.644	11.5
TG Full Adder	93.300	85.524	11.6
Opt.-TG Full Adder	85.500	75.640	11.6

DC (Standby) power dissipation optimization of the CMOS digital circuits was examined by using the model introduced in [5]. Beside other parameters, it was found that DC power dissipation of the CMOS digital circuits are depended on the input logic probabilities. This dependency was formulated for the DC power dissipation model and applied to basic CMOS digital building blocks. It was found that DIBL effect is play an important role on the standby power. Standby current is exponentially depend on both supply voltage and the DIBL parameter. For reducing DC power dissipation, DIBL parameter (η) should be reduced while increasing supply voltage. Appropriate threshold voltage and DIBL parameters could be found using the optimization method given this work. In the logic level, more stacked structures should be used. Because, leakage current of two and three stacked transistor are much more smaller than that of the one stack transistor's. Also input logic level probabilities of the circuits are worth to be considered during power optimization process.

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Appendix B

User guide for SPICE3f3 implementation

This User's Guide is to be used as a supplement to the original "SPICE3 Version 3f3 User's Manual" [1]. It is intended for SPICE users who have access to the modified program SPICE-3f3 with the S-CMOS MOS transistor model. It contains the additional features supported by the S-CMOS model and should be used together with the original User's Manual for completeness.
spice/default

```
# Default definitions
# TOP2= /projects/spice3
SYS_DIR= $(DIST_DIR)
OBJ_TOP= $(DIST_DIR)/src
SPICE_DIR= /home/pacific-03/alex/spice
SPICE_LIB_DIR= $(SPICE_DIR)/lib
SPICE_EXEC_DIR= $(SPICE_DIR)/bin
S_SPICE_DIR= $(SPICE_DIR)
S_SPICE_LIB_DIR= $(S_SPICE_DIR)/lib
S_SPICE_EXEC_DIR= $(S_SPICE_DIR)/bin
INSTALL_DIRS= $(SPICE_DIR) $(SPICE_EXEC_DIR) $(SPICE_LIB_DIR)
CC= cc
CC_OPT= -O
LDFLAGS= -lm -ltermlib
GETOPTLIB=
RANLIB= ranlib
ARLOCAL= 1
DEPEND_PROG= cc -M
CLEANASYOUGO= false
X_DIR= /usr
INCX    = -I$(X_DIR)/include -I$(X_DIR)/include/X11     \
 -I$(X_DIR)/include/X11/Xmu     \
 -I$(X_DIR)/include/X11/Xaw
LIBX= -L$(X_DIR)/lib/X11 -lXaw -lXt -lXext -lXmu -lX11
DEVICES= asrc bjt bsim1 S-CMOS bsim2 bsim3 cap cccs ccvs csw isrc \
 ltra mes mos1 mos2 mos3 res sw tra urc vccs vcvs vsrc
ANALYSES= op dc tf ac tran pz noise
INTERFACE_OPTS= -DWANT_MFB -DWANT_X11
BUG_ADDR = alex@pacific.usc.edu
```

```
DEFAULT_EDITOR= vi
ASCII_RAWFILE= 0
OPT_CHAR= -
###The End.  Use the 'build' command in util/ to build spice.
spice/config/solaris
# Sun SPARC systems
#MAKE = /usr/usc/bin/gmake
MAKE = /usr/ccs/bin/make
#MAKE = /bin/make
# In case of a bug (as described in the top-level "readme" file):
# LIBX= -L$(X_DIR)/lib -lXaw -lXt -lXext -Bstatic -lXmu \
#-Bdynamic -lX11
LDFLAGS= -lm -ltermlib -lsocket -lnsl
# HP-UX 7.? or 8.? (HP Unix), defaults for 9000/700
INCX=-I/usr/include/X11R4/Xaw -I/usr/include/X11R4/Xmu \
-I/usr/include/X11R4
LIBX=-L/usr/lib/X11R4/ -lXaw -lXt -lXext -lXmu -lX11
MAKE=/bin/make
CFLAGS=-O
RANLIB=echo
**********************************************************************
*
* S-CMOS Model 1
.model cmosn nmos level = 41
+  Vfb   =   -0.4      Phis   =   1.09    Gamma1  =   0.95
+  Gamma2 =   0.6      Ks     =   0.9     Knz     =   0.2
+  Knb   =   0.04      Etaz   =   0.007   Etal    =   0.001
+  Mu0   =   445       Tox    =   13.0000 Ugsz    =   0.235
+  Ugsl  =   0.06      Ubs    =   0.02    Ecrit   =   10
+  Dl    =   0.1       Dw     =   0.1
+  N1    =   1.5       Kh1    =   1.01    Uds     =   0.05
+  Kgsh  =   1.01      Kh2    =   1.05    Lambdad =   0.12
+  Lambdag =   0.5     Lambdab =   2       Lambdabs =   1
+  Phid  =   0.05      Ksig   =   0.01    Ksub    =   0.1
+  wwid  =   30        wnrw   =   0.3     llng    =   30
+  lsht  =   0.3       cgdo   =   5.98e-10 cgso   =   5.98e-10
+  cgbo  =   5.93e-10  rsh    =   0       cj      =   0.000297
+  cjsw  =   4.54e-10  js     =   1e-08   pb      =   0.8
+  pbsw  =   0.8       mj     =   0.909   mjsw    =   0.163
.model cmosp pmos level=41
+  Vfb   =   -0.4      Phis   =   1.09    Gamma1  =   0.95
+  Gamma2 =   0.6      Ks     =   0.9     Knz     =   0.2
+  Knb   =   0.04      Etaz   =   0.007   Etal    =   0.001
+  Mu0   =   445       Tox    =   13.0000 Ugsz    =   0.235
+  Ugsl  =   0.06      Ubs    =   0.02    Ecrit   =   10
```

```
+ Dl = 0.1 Dw = 0.1
+ N1 = 1.5 Kh1 = 1.01 Uds = 0.05
+ Kgsh = 1.01 Kh2 = 1.05 Lambdad = 0.12
+ Lambdag = 0.5 Lambdab = 2 Lambdabs = 1
+ Phid = 0.05 Ksig = 0.01 Ksub = 0.1
+ wwid = 30 wnrw = 0.3 llng = 30
+ lsht = 0.3 cgdo = 5.98e-10 cgso = 5.98e-10
+ cgbo = 5.93e-10 rsh = 0 cj = 0.000297
+ cjsw = 4.54e-10 js = 1e-08 pb = 0.8
+ pbsw = 0.8 mj = 0.909 mjsw = 0.163
==========================================================
* S-CMOS Model 2
.model cmosn nmos level = 41
+ Vfb = -0.4 Phis = 1.09 Gamma1 = 0.95
+ Gamma2 = 0.6 Ks = 0.9 Knz = 0.2
+ Knb = 0.04 Etaz = 0.007 Etal = 0.001
+ Mu0 = 445 Tox = 13.0000 Ugsz = 0.235
+ Ugsl = 0.06 Ubs = 0.02 Ecrit = 10
+ Dl = 0.1 Dw = 0.1
+ N1 = 1.5 Kh1 = 1.01 Uds = 0.05
+ Kgsh = 1.01 Kh2 = 1.05 Lambdad = 0.12
+ Lambdag = 0.5 Lambdab = 2 Lambdabs = 1
+ Phid = 0.05 Ksig = 0.01 Ksub = 0.1
+ wwid = 30 wnrw = 0.3 llng = 30
+ lsht = 0.3 cgdo = 5.98e-10 cgso = 5.98e-10
+ cgbo = 5.93e-10 rsh = 0 cj = 0.000297
+ cjsw = 4.54e-10 js = 1e-08 pb = 0.8
+ pbsw = 0.8 mj = 0.909 mjsw = 0.163
.model cmosp pmos level=41
+ Vfb = -0.33 Phis = 0.93 Gamma1 = 0.563
+ Gamma2 = 0.309 Ks = 3.4 Knz = 0.217
+ Knb = -3.9E-04 Etaz = 0.005 Etal = 0.038
+ Mu0 = 130.000 Tox = 13.000 Ugsz = 0.1
+ Ugsl = 0.05 Ubs = 0.02 Ecrit = 10
+ Dl = 0.1 Dw = 0.1
+ Uds = 0.01 Lambdad = 1.15 Lambdag = 3.5
+ Lambdab = 2 Lambdabs= 1 Phid = 0.1
+ N1 = 13.5 Kh1 = 1.01 Kh2 = 1.03
+ Kgsh = 1.01 Ksig = 0.01 Ksub = 0.1
+ wwid = 30 wnrw = 0.3 llng = 30
+ lsht = 0.3 cgdo = 2.23e-10 cgso = 2.23e-10
+ cgbo = 6.6e-10 rsh = 0 cj = 4.77e-4
+ cjsw = 1.41e-10 js = 1e-08 pb = 0.85
+ pbsw = 0.85 mj = 0.499 mjsw = 0.198
```

Appenndix C

```
%%%%%%%%%%%%%%%% S-CMOS Parameter Extractor %%%%%%%
%                          1999 : Alex Y. Park, Prof. Bing J. Sheu
% This parameter extraction program extract parameter values
% by usingdc current data only

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%
 path('/home/pacific-03/alex/ascpe/data',path);
 data_clear;
 clear parameter;
 %a1;
 data_clear;
 clear parameter;
 %%%%%%%%%%%%%%%%%%%%%%%   Data acquisition %%%%%%%%%%%%
path('/home/pacific-03/alex/ascpe/data1/10_10',path);
%path('/home/pacific-03/alex/ascpe/data1/1_1',path);
%path('/home/pacific-03/alex/ascpe/data1/1p6_3p6',path);
%path('/home/pacific-03/alex/ascpe/data1/1p6_p4',path);
%path('/home/pacific-03/alex/ascpe/data1/3p4_p4',path);
%path('/home/pacific-03/alex/ascpe/data1/3p6_3p6',path);
%path('/home/pacific-03/alex/ascpe/data1/3p6_1',path);
%path('/home/pacific-03/alex/ascpe/data1/3p6_p6',path);
%path('/home/pacific-03/alex/ascpe/data1/p6_3p6',path);
%path('/home/pacific-03/alex/ascpe/data1/p6_p4',path);
%path('/home/pacific-03/alex/ascpe/data2',path);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
 d96;
%%%%%%%%%%%%%%%%%%%%%% Bias  Condition %%%%%%%%%%%%%%%%
path('/home/pacific-03/alex/ascpe/dgsb',path);
 %%%%%%% VB ==========
vb_0;
%vb_0_to;
%VB_data2;
%vb0_m3p3;
%%%%%%%%% VD  %%%%%%%%%%%%%%%%%
vd0_3p3;
%vd_1p3;
%vd_3;
 %vd_p2_to;
%vd_3
```

```
%%%%%%%% VG %%%%%%%%%%%%%%
%vg0_3p3;
 vgp2_3p3
%%%%%%%%% VS %%%%%%%%%%%%%%
vs0;

 %%%%%%%%%%%%%
x1=0.066:0.066:3.3;
x2=0:0.066:3.3;
x3=0:0.066:3.3;
x4=0:0.066:3.3;
x5=0:0.066:3.3;
x6=0:0.066:3.3;
x=[x1,x2,x3,x4,x5,x6];
x=x';
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%% VD =VD_data;
 VG =VG_data;
 VS =VS_data;
 VB =VB_data;
 IDS_M = ID_m;
 %gm_M=diff(IDS_M)./diff(VG);
gds_M=diff(IDS_M)./diff(VD);
 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%gds_M = gd_m;
 %W = 10e-6;
 %L = 10e-6;
 VDS = VD - VS;
 VGS = VG - VS;
 VBS = VB - VS;
  %gdsl=log(gds_M);
%gdsl=log(gm_M);
plot(x, gds_M, 'b*', x, gds_M, 'r', 'EraseMode', 'Xor');
%plot(x, gdsl, 'b*', x, gdsl, 'r', 'EraseMode', 'Xor');
grid;
xlabel('VDS (V)');
 ylabel('log(gds) ');
 title('log(gds) vs. VDS');
 drawnow;
 path('/home/pacific-03/alex/ascpe/dgsb',path);
 vgp2_3p3;
 vd0_3p3;
 vb_0;
 vs0;
 path('/home/pacific-03/alex/ascpe/data1/10_10',path);
```

```
%path('/home/pacific-03/alex/ascpe/data1/1_1',path);
%path('/home/pacific-03/alex/ascpe/data1/1p6_3p6',path);
%path('/home/pacific-03/alex/ascpe/data1/1p6_p4',path);
%path('/home/pacific-03/alex/ascpe/data1/3p4_p4',path);
%path('/home/pacific-03/alex/ascpe/data1/3p6_3p6',path);
%path('/home/pacific-03/alex/ascpe/data1/3p6_1',path);
%path('/home/pacific-03/alex/ascpe/data1/3p6_p6',path);
%path('/home/pacific-03/alex/ascpe/data1/p6_3p6',path);
%path('/home/pacific-03/alex/ascpe/data1/p6_p4',path);
 %path('/home/pacific-03/alex/ascpe/data2',path);
 d96;
 %data_VDS;
 VD =VD_data;
 VG =VG_data;
 VS =VS_data;
 VB =VB_data;
 IDS_M = ID_m;
  gds_M=diff(IDS_M./VD);
 %gds_M = gd_m;
 W = 10e-6;
 L = 10e-6;
 vd_int;
 parameter = [ECRIT UDS];
 parameter(1) = 10 * 10^6;
 parameter(2) = 0.035;
 %parameter(3) = 1.01;
 disp('initial_ values');
 fprintf('ECRIT=%6.5e, UDS=%6.5e\n\n',parameter(1), parameter(2));
 parameter = fmins('error_eval',parameter);
 disp('final values');
 fprintf('ECRIT=%6.5e, UDS=%6.5e, ERROR=%6.5e\n\n',parameter(1), parameter(2),
ERROR);
 ECRIT=parameter(1);
 UDS=parameter(2);
 % parameter set
format short e;
fid = fopen ('iv.m');
a = fscanf (fid, '%e',[1 inf]);
a=a';
fclose(fid);
k=100;
for m=k:k+20;
figure;
j=1:51;n=51*6*m+1;
for i=1:51*6;
```

```
b(i,1)=a(i+n-1,1);
end;
yk1(j,1)=b(j,1);
yk2(j,1)=b(j+51,1);
yk3(j,1)=b(j+102,1);
yk4(j,1)=b(j+153,1);
yk5(j,1)=b(j+204,1);
yk6(j,1)=b(j+255,1);
x=0:50;
%plot(x*3/51,yk);
plot(x*3.3/51,yk1,'*',x*3.3/51,yk2,'*',x*3.3/51,yk3,'*',x*3.3/51,yk4,'*',x*3.3/
51,yk5,'*',x*3.3/51,yk6,'*');
grid on;
xlabel('V  (V)');
ylabel('I  (A)');
%title(['W/L=  /   , Vdd= , Vd=  (k=',num2str(m),')']);
end;
 %%%    rie.m  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
k=105;
for m=k:k;
figure;
j=1:51;n=51*6*m+1;
for i=1:51*6;
b(i,1)=a(i+n-1,1);
end;
yk1(j,1)=b(j,1);
yk2(j,1)=b(j+51,1);
yk3(j,1)=b(j+102,1);
yk4(j,1)=b(j+153,1);
yk5(j,1)=b(j+204,1);
yk6(j,1)=b(j+255,1);
x=0:50;
yk=[yk1,yk2,yk3,yk4,yk5,yk6];
end;
%id1=fopen('d593.m','w');
%fprintf(id1, '%8.5e \n', yk);
 %yk2=log(yk)
x=0:50;
 %plot(x*3/51,yk,'*');
  %z=diff(yk,x);
plot(x*3.3/51,yk1,'*',x*3.3/51,yk2,'*',x*3.3/51,yk3,'*',x*3.3/51,yk4,'*',x*3.3/
51,yk5,'*',x*3.3/51,yk6,'*');
 grid on;
 xlabel('V (V)');
 ylabel('I (A)');
```

```
%%% extract substrate-bias effects on Vth:  KS GAMMA1 GAMMA2 %%%
path('/home/pacific-03/alex/ascpe',path);
gloval_parm;
data_clear;
clear parameter;
%%% load the data of IDS-VGS %%%
W = 10e-6;
L = 10e-6;
param;
%vto=0.4;
scm_1;
path('/home/pacific-03/alex/ascpe/data',path);
d921;
x=0:50;
x=x*3.3/51;
n=51;
VG=x;
param;
path('/home/pacific-03/alex/ascpe/dgsb',path);
vd_p2_to;
vb_0_to;
VD=VD_data;
 VS=VB_data;
VG=VG';
VB=VB_data;
VGS=VG-VS;
path('/home/pacific-03/alex/ascpe',path);
alex_equ;
parameter=[VFB GAMMA1];
parameter(1)=-0.4;
parameter(2)=0.8;
VDS = VD - VS;
VGS = VG - VS;
VBS = VB - VS;
figure;
%mesh(VG,IDS_S,VD);
plotHandle1=plot(VG,IDS_S, 'b*', VG, IDS_S, 'r', 'EraseMode', 'Xor');
grid
xlabel('VGS (V)');
ylabel('IDS (A)');
 title('extracting VFB, GAMMA1 .....');
drawnow;
%parameter=[vto];
%parameter(1)=0.5;
disp('initial_ values');
```

```
fprintf('VFB = %6.5e, \n',parameter(1) );
error_vto;
parameter = fmins('error_vto',parameter); % extraction VFB and GAMMA1
%vto=parameter(1);
disp('final values');
fprintf('VFB=%6.5e, ERROR=%6.5e\n\n',parameter(1), ERROR);
        clear all;
        clear global;
%%% define global parameters
        gloval_parm;
        Wwid = 10e-6;
        Wnrw = 0.35e-6;
        Llng = 10e-6;
        Lsht = 0.35e-3;
%%% define matlab path
        matlab_path=path;
 %%% load VDSAT-VG data for large device: extract VFB, GAMMA1, PHIS
        data_;
        param;
        par_rult;
        W=10e-6;
        W=10e-6;
        VD = VD_data;
        VG = VG_data;
        VS = VS_data;
        VB = VB_data;
 %%% extract substrate-bias effects on Vth:  KS GAMMA1 GAMMA2 %%%
        data_clear;
        clear parameter;
%%% load the data of IDS-VGS %%%
        data_VGS;
        VD=VD_data;
        VG=VG_data;
        VS=VS_data;
        VB=VB_data;
        IDS_M=ID_m;
        gm_M=gm_m;
          indexbs=4;
        delta_vth=eval_dvt(VG,IDS_M,indexbs);
        Vth_M = vto + delta_vth;
        k=size(VB) ;
        m=k(1)/indexbs;
        for i=1:indexbs
            eval_VBS(i)=VB(2 + (i-1)*m);
        end
```

```
initial_vt1;
    parameter=[KS GAMMA1];
    parameter(1)=0.9;
    parameter(2)=0.8;
disp('initial_ values');
fprintf('KS = %6.5e\n\n',parameter(1));
parameter = fmins('error_dvt',parameter); % extraction VFB and GAMMA1
    KS=parameter(1);
disp('final values');
fprintf('KS=%6.5e, GAMMA1=%6.5e, ERROR=%6.5e\n\n',parameter(1),
        parameter(2),ERROR);
IDS_M = ID_m;
plot_init1;
clear parameter;
        parameter = [mu0 UGSZ UBS];
        parameter(1) = 600e-4;
        parameter(2) = 0.25;
        parameter(3) = 0.02;
disp('initial_ values');
fprintf('mu0=%6.5e, UGSZ=%6.5e, UBS=%6.5e\n\n',parameter(1), parameter(2),
        parameter(3));
parameter = fmins('error_eval1',parameter);
disp('final values');
fprintf('mu0=%6.5e, UGSZ=%6.5e, UBS=%6.5e, ERROR=%6.5e\n\n',parameter(1),
        parameter(2), parameter(3),ERROR);
        mu0=parameter(1);
        UGSZ=parameter(2);
        UBS=parameter(3);
plot_init2;
      clear parameter;
        parameter = [KSUB N];
        parameter(1) = 1;
        parameter(2) = 1;
disp('initial_ values');
fprintf('KSUB=%6.5e, N=%6.5e\n\n',parameter(1), parameter(2));
parameter = fmins('error_eval2',parameter);
disp('final values');
fprintf('KSUB=%6.5e, N=%6.5e, ERROR=%6.5e\n\n',parameter(1), parameter(2),
        ERROR);
KSUB=parameter(1);
N=parameter(2);
data_clear;
clear parameter;
data_VDS;
VD = VD_data;
```

```
VG = VG_data;
VS = VS_data;
VB = VB_data;
IDS_M = ID_m;
gds_M = gd_m;
W=10e-6;
W=10e-6;
plot_initp;
        parameter = [ECRIT UDS];
        parameter(1) = 10 * 10^6;
        parameter(2) = 0.035;
disp('initial_ values');
fprintf('ECRIT=%6.5e, UDS=%6.5e\n\n',parameter(1), parameter(2));
parameter = fmins('error_eval',parameter);
disp('final values');
fprintf('ECRIT=%6.5e, UDS=%6.5e, ERROR=%6.5e\n\n',parameter(1),
        parameter(2), ERROR);
ECRIT=parameter(1);
UDS=parameter(2);
 %%% define matlab path %%%
matlab_path=path;
W = 9e-7;
L = 15e-6;
data_clear;
clear parameter;
data_;
vto=eval_vto(VG_data,VS_data);
   %mode=2;
        eval_VDS = eval_VBS;
data_VGS;
VD=VD_data;
VG=VG_data;
VS=VS_data;
VB=VB_data;
IDS_M=ID_m;
gm_M=gm_m;
indexbs=4;        % 4 different VBS bias conditions
delta_vth=eval_dvt(VG_data,IDS_M,indexbs);
Vth_M = vto + delta_vth;
initial_vt2;
        parameter=[KNB];
        parameter(1)=0;
disp('initial_ values');
fprintf('KNZ=%6.5e, KNB=%6.5e\n\n',KNZ,parameter(1));
parameter = fmins('error_vtw',parameter);   % extraction KNZ, KNB
```

```
        KNB=parameter(1);
disp('final values');
fprintf('KNZ=%6.5e, KNB=%6.5e, ERROR=%6.5e\n\n', KNZ,parameter(1),
        ERROR);
%%% define matlab path %%%
matlab_path=path;
W=10e-6;
L = 5e-7;
data_clear;
clear parameter;
data_;
vto=eval_vto(VG_data,VS_data);
        %mode=3;
        eval_VDS = eval_VBS;
data_VGS;
VD=VD_data;
VG=VG_data;
VS=VS_data;
VB=VB_data;
IDS_M=ID_m;
gm_M=gm_m;
indexbs=4;      % 4 different VBS bias conditions
delta_vth=eval_dvt(VG_data,IDS_M,indexbs);
Vth_M = vto + delta_vth;
initial_vt3;
        parameter=[GAMMA1L];
        parameter(1)=0;
disp('initial_ values');
fprintf('ETA1=%6.5e, GAMMA1L=%6.5e\n\n',ETA1,parameter(1));
parameter = fmins('error_vtl',parameter); % extraction ETA1, GAMMA1L
        GAMMA1L=parameter(1);
disp('final values');
fprintf('ETA1=%6.5e, GAMMA1L=%6.5e, ERROR=%6.5e\n\n', ETA1,
        parameter(1),ERROR);
plot_init3;
clear parameter;
        parameter = [UGSL UGSL2];
        parameter(1) = 1.5e-7;
        parameter(2) = 1e-8;
disp('initial_ values');
fprintf('UGSL=%6.5e,UGSL2=%6.5e\n\n',parameter(1), parameter(2));
parameter = fmins('error_eval3',parameter);
disp('final values');
fprintf('UGSL=%6.5e, UGSL2=%6.5e, ERROR=%6.5e\n\n',parameter(1),
        parameter(2),ERROR);
```

```
UGSL=parameter(1);
UGSL2=parameter(2);
data_clear;
 clear parameter;
data_VDS;
VD = VD_data;
VG = VG_data;
VS = VS_data;
VB = VB_data;
IDS_M = ID_m;
gds_M = gd_m;
plot_init4;
        parameter = [ECRIT ETAZ];
        parameter(1) = 10e6;
        parameter(2) = 2e-8;
disp('initial_ values');
fprintf('ECRIT=%6.5e, ETAZ=%6.5e\n\n',parameter(1), parameter(2));
parameter = fmins('error_eval4',parameter);
disp('final values');
fprintf('ECRIT=%6.5e, ETAZ=%6.5e, ERROR=%6.5e\n\n',parameter(1),
        parameter(2),ERROR);
ECRIT=parameter(1);
ETAZ=parameter(2);
clear parameter;
plot_init5;
        parameter = [LAMBDAD LAMBDAG ECRIT];
        parameter(1) = 1e-7;
        parameter(2) = 1;
        parameter(3) = ECRIT;
disp('initial_ values');
fprintf('LAMBDAD=%6.5e, LAMBDAG=%6.5e, ECRIT=%6.5e\n\n',parame-
ter(1),
        parameter(2),parameter(3));
parameter = fmins('error_eval5',parameter);
disp('final values');
fprintf('LAMBDAD=%6.5e, LAMBDAG=%6.5e, ECRIT=%6.5e,
ERROR=%6.5e\n\n',
        parameter(1), parameter(2),parameter(3),ERROR);
LAMBDAD=parameter(1);
LAMBDAG=parameter(2);
ECRIT = parameter(3);

%=============================================================
==
%       file name: gloval_parm.m
```

```
% global parameters
        %model parameters
 global Tox VFB PHIS mu0 GAMMA1 GAMMA2 KS ETA1 ETA2 ETA3 ETAZ KNZ
KNB
 global UGSL UDS UBS PHID LAMBDAG LAMBDAB LAMBDABS LAMBDAD
KSIG
 global KBSh KDSATh KGFh ECRIT DL DW N KSUB Vt Cox UGSZ
  %controlling
& expression parameters
 global Weff Leff W L Llng Lsht Wwid Wnrw GAMMA1L UGSL2 UBS2 UDSL
 global VDS VGS VBS VD VG VS VB IDS_S gds_S gm_S IDS_M gds_M gm_M
 global VFS VGFh VBST VBSh Vth Vto VGSth ALPHAX VDSAT VDSATh
 global Mr mueff fL fs fc ALPHA BETA F vto
  %global VD_data VG_data VS_data VB_data
 global plotHandle1 plotHandle2 plotHandle3 plotHandle4 plotHandle5
 global plotHandle6 plotHandle7 plotHandle8 plotHandle9 ERROR

global indexbs delta_vth eval_VBS eval_VDS mode Vth_S Vth_M
 %=========================================================
%       function: data_clear.m
 % clear all the setting of I, V
        clear VDS VGS VBS;
        global VDS VGS VBS;
        clear VD VG VS VB;
        global VD VG VS VB;
        clear VD_data VG_data VS_data VB_data;
        global VD_data VG_data VS_data VB_data;
        clear ID_m gd_m gm_m;
        global ID_m gd_m gm_m;
        clear IDS_M IDS_S gds_M gds_S;
        global IDS_M IDS_S gds_M gds_S;
%%=========================================================
%       function: par_val.m
% parameter set
Tox=9e-9;     %gate oxide thickness (m)
VFB=-0.4;      %flat-band voltage (volt)
PHIS=0.85;       %surface inversion potential (volt)
mu0=450e-4;     %intrinsic surface mobility (m^2/volt/sec)
GAMMA1= 0.8;    %zero-bias boly-effect coefficient (volt^0.5)
GAMMA1L=0;
GAMMA2= 0.328;     %high-bias body-effect coefficient (volt^0.5)
KS=2.7e-4;    %depletion charge-sharing coefficient
ETA1=0;       %short-channel effect coefficient (m*volt)
ETA2=0;     %reverse short-channel effect coefficient (m*volt)
ETA3=1e-6;    %exponential reverse short-channel effect coefficient (m)
```

```
ETAZ=0;      %drain-induced barrier lowering coefficient
KNZ=0.244e-6;   %narrow-width threshold voltage coefficient (m*volt)
KNB=5.4e-9;    %narrow-width threshold voltgae substrate coefficient (m)
UGSZ=0.25;     %gate-voltage mobility degradation coefficient (volt^-1)
UGSL=0.06e-6;    %short-channel adjustment of UGSZ (m/volt)
UGSL2= 0;
UDS=0.035;     %drain voltage mobility degradation coefficient (volt^-1)
UDSL= 0;
UBS=0.02; %substrate-voltage mobility degradation coefficient (volt^-0.5)
PHID=0.05; %drain-voltage related channel-length modulation effect potential (volt)
LAMBDAG= 0.5;  %gate-voltgae dependent CLME coefficient (volt^1.5)
LAMBDAB= 2;      %substrate-voltage shifting CLME coefficient
LAMBDABS= 1;     %substrate-voltage dependent CLME coefficient (volt)
LAMBDAD= 0;      %drain-voltage dependent CLME coefficient (volt)
KSIG=0.02;     %sigmoid function coefficient (volt^2)
KBSh=1.01;       %substrate-bias hyperbola function coefficient
KDSATh=1.01;     %strong-inversion hyperbola function coefficient
KGFh=1.01;     %gate to flat-band hyperbola function coefficient
 ECRIT=20e6;       %critical electric field for velocity saturation (volt/m)
DL=0;        %channel-length reduction (m)
DW=0;        %channel-width reduction (m)
N=1.5;       %subthreshold drain current slope
KSUB=0.1;        %subthreshold current shifting coefficient
Vt =0.026;         %thermal voltage (volt)
Cox=3.5e-11 / Tox;        %gate oxide capacitance (farad/m^2)
%%=========================================================
%       function: eval_vto.m
function calc_vto=calc_vto(VG_data,VS_data)
        gloval_parm;
        k=size(VG_data);
        for i=1:(k-1)
                if (VS_data(i)*VS_data(i+1)) <= 0
                    index=i;
                end
        end
        calc_vto = VG_data(index+1) - (VG_data(index+1) - VG_data(index))
              * VS_data(index+1) / (VS_data(index+1) - VS_data(index));
return;
%%=========================================================
%       function: eval_dvt.m
function eval_dvt=eval_dvt(VG, IDS_M, indexbs)
        gloval_parm;
        VG = VG;
        IDS_M = IDS_M;
        k=size(VG);
```

```
        indexbs = indexbs;
        m=k(1)/indexbs;
        for ind1=1:indexbs
          index1=0;
          index2=0;
          for ind2=1:(m-1)
              jj = ind2+(ind1-1)*m;
              if index1==0;
                 if ((VG(jj)) >= (vto+0.3+(ind1-1)*0.1))
                     index1=ind2;
                 end
              end
              if index2==0;
                  if (VG(jj) >= (vto+0.7+(ind1-1)*0.1))
                      index2=ind2;
                 end
              end
            end
         eval_dvt_vth(ind1)=VG(index2+(ind1-1)*m) - (VG(index2+(ind1-1)*m)
             - VG(index1+(ind1-1)*m)) * IDS_M(index2+(ind1-1)*m)
             / (IDS_M(index2+(ind1-1)*m) - IDS_M(index1+(ind1-1)*m));
        end
        for i=1:(indexbs)
                eval_dvt(i)=eval_dvt_vth(i) - eval_dvt_vth(1);
        end
return;
%=============================================================
%      function: Vth_evel.m
    Weff = W - DW;
    Leff = L - DL;
    if mode==1
            Vto = vto;
    end
    if mode == 2
      KNZ = (vto - VFB - PHIS) / ( 1 / Weff - 1/Wwid);
      Vto = VFB + PHIS + KNZ*(1 / Weff - 1/Wwid) + KNB* (1/ Weff - 1/Wwid)
        * eval_VBS - ETAZ * eval_VDS - ETA1*(1 / Leff - 1/Llng) + ETA2
        *(1/ Leff - 1/Llng)* (1 - exp(- Leff / ETA3));
     end
    if mode == 3
      ETA1 = - (vto - VFB - PHIS) / ( 1 / Leff - 1/Llng);
      Vto = VFB + PHIS + KNZ*(1 / Weff - 1/Wwid) + KNB* (1/ Weff - 1/Wwid)
          * eval_VBS - ETAZ * eval_VDS - ETA1*(1 / Leff - 1/Llng)
          + ETA2 *(1/ Leff - 1/Llng) * (1 - exp(- Leff / ETA3));
    end
```

```
 cvth = Vto + (GAMMA1-GAMMA1L*(1/Leff-1/ Llng))*(sqrt(PHIS-eval_VBS)-
sqrt(PHIS))
     + KS * (sqrt(PHIS - eval_VBS) - sqrt(PHIS)).^2 + GAMMA2
     * (sqrt(PHIS - eval_VBS) - sqrt(PHIS - eval_VBS));
 %=============================================================
%       function: alex_equ.m
Weff=W - DW;
Leff=L - DL;
VDS = VD - VS;
VGS = VG - VS;
VBS = VB - VS;
VFS = VFB + VBS;
T_GFh = VGS + KGFh * VFS;
VGFh = 0.5 * (T_GFh + sqrt(T_GFh.^2 - 4 * VGS .* VFS));
VBST = PHIS - ((GAMMA1 - GAMMA2)/KS + sqrt(PHIS))^2;
T_BSh = VBS + KBSh * VBST;
VBSh = 0.5 * ( T_BSh + sqrt(T_BSh.^2 - 4 * VBS .* VBST));
Vto = VFB + PHIS + KNZ *(1 / Weff - 1/ Wwid) + KNB* (1/ Weff - 1/Wwid)* VBS
    - ETAZ * VDS * (1/Leff - 1/Llng) - ETA1 *(1/ Leff - 1/ Llng)+ ETA2
    * (1/ Leff - 1/Llng)*(1 - exp(- Leff / ETA3));
Vth = Vto+(GAMMA1-GAMMA1L*(1/Leff-1/Llng))*(sqrt(PHIS-VBSh)-sqrt(PHIS))
    + KS*(sqrt(PHIS-VBSh)-sqrt(PHIS)).^2+GAMMA2*(sqrt(PHIS-VBS)-sqrt(PHIS-
VBSh));
VGSth = 2 * N * Vt * log(1 + exp((VGS - Vth) / (2 * N * Vt)));
ALPHAX = (1 - GAMMA1 / 2 * (sqrt(VGSth + Vth - VFS + GAMMA1^2 / 4)).^(-1)).^(-
1);
g=1-1/(1.744+0.8364*(PHIS-VBS));
a=1+g*GAMMA1/2*(sqrt(PHIS-VBS)).^(-1);
Vc=VGSth.* a.^(-1)/ECRIT *(1/Leff - 1/Llng);
K=(1+Vc+sqrt(1+2*Vc))/2;
VDSAT=(VGSth).* ALPHAX.^(-1);
KDSATh1 = KDSATh * (1 + 1e-8 / (Leff));
T_DSATh = VDS + KDSATh1 * VDSAT;
VDSATh = 0.5 * (T_DSATh - sqrt(T_DSATh.^2 - 4 * VDS.*VDSAT));
fc = 0.5 * (1 + (VGS - Vth) .* (sqrt((VGS - Vth).^2 + KSIG)).^(-1));
fs = 1 - fc;
Mr=(1+(UGSZ+UGSL*(1/Leff-1/Llng) )*VGSth+UGSL2*(1/Leff-1/Llng)*(VGSth.^2)
   -UBS*(sqrt(PHIS-VBSh)-sqrt(PHIS))+(UDS-UDSL*(1/Leff-1/Llng))*VDSATh)
   .*(1 +VDSATh/ECRIT*(1/Leff-1/Llng));
mueff=mu0*Mr.^(-1);
fL=LAMBDAD*(1/Leff)*(sqrt(PHID+VDS-VDSATh)-sqrt(PHID)).*(1-VBS/LAMBD-
ABS)
   .*((VGSth).^(3/2) +LAMBDAG).^(-1)/LAMBDAB;
BETA = Weff / Leff * Cox * mueff;
ALPHA = ( 1 - fs.* exp(- VDS ./ Vt)).*(1 + fc.*fL + fs .* KSUB);
```

```
F = VGSth.*VDSATh - ALPHAX / 2 .* VDSATh.^2;
IDS_S = ALPHA.*BETA.*F;
%%============================================================
%       function: initial_vp.m
        VDSAT = VS;
       figure;
        plotHandle1=plot(VG,VDSAT, 'b*', VG, VDSAT, 'r--', 'EraseMode', 'Xor');
       %grid on;
       %axis([0,4,-Inf,Inf])
       xlabel('VG (V)');
       ylabel('VDSAT (V)');
       title('extracting VFB GAMMA1 .....');
       drawnow;
 %%============================================================
%       function: error_vsat.m
 function error_vsat=error_vsat(parameter)
       gloval_parm;
       VFB = parameter(1);
       GAMMA1 = parameter(2);
       alphax=(1 - (GAMMA1 / 2)  ./ sqrt(VG - VFB - VB + GAMMA1^2 / 4) ).^(-1);
       vto=eval_vto(VG,VS);
       VDSAT_s=(VG - vto) ./ alphax;

      error_vsat=sum((VS - VDSAT_s).^2);
       ERROR=error_vsat;
       set(plotHandle1(2), 'Ydata', VDSAT_s);
       drawnow;
 return;
 %============================================================
%       function: initial_vt1.m
 %%% initial_ plot %%%%
       figure;
       plotHandle3=plot(eval_VBS,Vth_M,'b',eval_VBS,Vth_M,'r','EraseMode','Xor');
       xlabel('VBS (V)');
       ylabel('Vth (V)');
       title('extracting KS and GAMMA2.....');
       drawnow;
 %%============================================================
%       function: error_dvt.m
 function err=error_dvt(parameter)
       gloval_parm;
       KS = parameter(1);
       GAMMA1 = parameter(2);
       mode=1;
       Vth_evel;
```

```
        Vth_S = cvth;
        err=sum((Vth_M - Vth_S).^2);
        k=size(Vth_M);
        ERROR=sqrt(sum((Vth_M - Vth_S).^2 ./ Vth_M.^2) / k(1));
        set(plotHandle3(2), 'Ydata', Vth_S);
        drawnow;
 return;
 %=============================================================
%       function: plot_init1.m
 % initial_ plot
        VDS = VD - VS;
        VGS = VG - VS;
        VBS = VB - VS;
        figure;
        plotHandle4=plot(VGS, IDS_M, 'b*', VGS, IDS_M, 'r+', 'EraseMode', 'Xor');
        xlabel('VGS (V)');
        ylabel('IDS (A)');
        title('extracting mu0, UGSZ, UBS .....');
        drawnow;
 %%============================================================
%       function: error_eval1.m
 function err=error_eval1(parameter)
        gloval_parm;
       mu0 = parameter(1);
        UGSZ = parameter(2);
        UBS=parameter(3);
        alex_equ;
        err=sum((IDS_M - IDS_S).^2);
        k=size(IDS_M);
        ERROR=sqrt(sum((IDS_M - IDS_S).^2 ./ IDS_M.^2) / k(1));
        set(plotHandle4(2), 'Ydata', IDS_S);
        drawnow;
 return;
%%%============================================================%
%       function: plot_init2.m
% initial_ plot
      VDS = VD - VS;
      VGS = VG - VS;
       VBS = VB - VS;
       figure;
       axis([0 3 10^(-10) 10^(-2)]);
       xlabel('VGS(V)');
       ylabel('IDS (A)');
       title(' extracting KSUB and N .....')
       drawnow;
```

```
%%=============================================================
%       function: error_eval2.m
function err=error_eval2(parameter)
      gloval_parm;
      KSUB = parameter(1);
      N = parameter(2);
      alex_equ;
      k=size(VG);
      m=k(1)/indexbs;
      index=0;
      for i=1:m
        if index==0
           if VG(i) >= (vto + 0.1)
             index = i;
           end
        end
      end
      ii=1;
      for i=1:indexbs
         for j=1:index
           IDS_Ms(ii) = IDS_M(j+(i-1)*m);
           IDS_Ss(ii) = IDS_S(j+(i-1)*m);
           ii = ii + 1;
         end
      end
      err=sum((IDS_Ms - IDS_Ss).^2);
      k = size(IDS_Ms);
      ERROR=sqrt(sum((IDS_Ms - IDS_Ss).^2 ./ IDS_Ms.^2) / k(1));
      set(plotHandle5(2), 'Ydata', IDS_S);
      drawnow;
return;
%%=============================================================
%       function: plot_initp.m
% initial_ plot
      VDS = VD - VS;
      VGS = VG - VS;
      VBS = VB - VS;
      figure;
      plotHandle2=plot(VDS,IDS_M,'b*',VDS,IDS_M,'r+','EraseMode','Xor');
      xlabel('VDS (V)');
      ylabel('IDS (A)');
      title(' extracting UDS .....');
      drawnow;
%%=============================================================
%       function: error_eval.m
```

```
function err=error_eval(parameter)
      gloval_parm;
      if parameter(1) >= 20e6
        param_(1) = 20e6
      end
      ECRIT = parameter(1);
      UDS = parameter(2);
      alex_equ;
      err=sum((IDS_M - IDS_S).^2);
      k=size(IDS_M);
      ERROR=sqrt(sum((IDS_M - IDS_S).^2 ./ IDS_M.^2) / k(1));
      set(plotHandle2(2), 'Ydata', IDS_S);
      drawnow;
return;

%%=============================================================
%       function: initial_vt2.m
% initial_ plot
   figure;
   plotHandle6=plot(eval_VBS,Vth_M,'b',eval_VBS,Vth_M,'r','EraseMode','Xor');
   xlabel('VBS (V)');
   ylabel('Vth (V)');
   title('extracting KNZ, KNB .....');
   drawnow;
%%=============================================================
%       function: error_vtw.m
function err=error_vtw(parameter)
      gloval_parm;
      KNB = parameter(1);
      mode=2;
      Vth_evel;
      Vth_S = cvth;
      err=sum((Vth_M - Vth_S).^2);
       ERROR=err;
      set(plotHandle6(2), 'Ydata', Vth_S);
      drawnow;
return;
%%%=============================================================
%       function: initial_vt3.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% initial_ plot
   figure;
   plotHandle7=plot(eval_VBS,Vth_M,'b',eval_VBS,Vth_M,'r','EraseMode','Xor');
   xlabel('VBS (V)');
```

```
    ylabel('Vth (V)');
    title('extracting GAMMA1L, ETAZ .....');
    drawnow;
%       function: error_vtl.m
function err=error_vtl(parameter)
      gloval_parm;
      GAMMA1L = parameter(1);
      mode=3;
      Vth_evel;
      Vth_S = cvth;
      err=sum((Vth_M - Vth_S).^2);
      ERROR=err;
      set(plotHandle7(2), 'Ydata', Vth_S);
      drawnow;
return;
 %       function: plot_init3.m
% initial_ plot
      VDS = VD - VS;
      VGS = VG - VS;
      VBS = VB - VS;
      figure;
      plotHandle8=plot(VGS,IDS_M,'b*',VGS,IDS_M,'r+','EraseMode','Xor');
      xlabel('VGS (V)');
      ylabel('IDS (A)');
      title('extracting UGSL, UGSL2 .....');
      drawnow;
%       function: error_eval3.m
function err=error_eval3(parameter)
      gloval_parm;
      UGSL = parameter(1);
      UGSL2 = parameter(2);
      alex_equ;
      err=sum((IDS_M - IDS_S).^2 * 10^8);
      k = size(IDS_M);
      ERROR=sum((IDS_M - IDS_S).^2);
      set(plotHandle8(2), 'Ydata', IDS_S);
      drawnow;
return;
 %       function: plot_init4.m
% initial_ plot
      VDS = VD - V
     VGS = VG - VS;
      VBS = VB - VS;
      figure;
      plotHandle9=plot(VDS,IDS_M,'b*',VDS,IDS_M,'r+','EraseMode','Xor');
```

```
      xlabel('VDS (V)');
      ylabel('IDS (A)');
      title(' extracting ECRIT, ETAZ .....');
      drawnow;
%       function: error_eval4.m
function err=error_eval4(parameter)
      gloval_parm;
      ECRIT = parameter(1);
      ETAZ = parameter(2);
      alex_equ;
      k=size(VG);
      ind = 1;
      for i=1:k(1)
        if (VD(i) <=2)
          IDS_Ms(ind) = IDS_M(i);
          IDS_Ss(ind) = IDS_S(i);
          VGset(ind)=VG(i);
          ind = ind + 1;
        end
      end
      err=sum((IDS_Ms - IDS_Ss).^2 );
      ERROR=err;
      set(plotHandle9(2), 'Ydata', IDS_S);
      drawnow;
return;
%       function: plot_init5.m
% initial_ plot
      VDS = VD - VS;
      VGS = VG - VS;
      VBS = VB - VS;
      figure;
      plotHandle9=plot(VDS, IDS_M, 'b*', VDS, IDS_M, 'r+', 'EraseMode', 'Xor');
      xlabel('VDS (V)');
      ylabel('IDS (A)');
      title(' extracting LAMBDAD, LAMBDAG .....');
      drawnow;
%       function: error_eval5.m
function err=error_eval5(parameter)
      gloval_parm;
      LAMBDAD = parameter(1);
      LAMBDAG = parameter(2);
      ECRIT = parameter(3);
      alex_equ;
      k=size(VG);
      ind = 1;
```

```
    for i=1:k(1)
      if (VD(i) > 1.5)
        IDS_Ms(ind) = IDS_M(i);
        IDS_Ss(ind) = IDS_S(i);
        VGset(ind)=VG(i);
        ind = ind + 1;
      end
    end
    err=sum((IDS_M - IDS_S).^2 );
    ERROR=err;
    set(plotHandle9(2), 'Ydata', IDS_S);
    drawnow;
return;
```

Appendix D

SPICE list files

(A) Folded-Cascode Operational Amplifier

```
* OP-amp SPICE netlist file for verification of  the s-CMOS Model
* Refference: CMOS Analog Circuit Design
*.option acct list post measout

mp3 8 8 1 1 cmosp w=6u l=.6u
mp5 10 8 1 1 cmosp w=6u l=.6u
mp4 9 9 1 1 cmosp w=6u l=.6u
mp6 7 9 1 1 cmosp w=6u l=.6u
mn7 4 4 0 0 cmosn w=2u l=.6u
mn8 3 4 0 0 cmosn w=2u l=.6u
mn88 6 vbb 3 3 cmosn w=2u l=.8u
mn9  vbb vbb 0 0 cmosn w=2u l=1u
i1 0 vbb 10u
mp66 6 5 7 7 cmosp w=2u l=.8u
mp55 4 5 10 10 cmosp w=2u l=.8u
mp77 5 5 1 1 cmosp w=2u l=1u
mn99 5 vb1 0 0 cmosn w=2u l=1u
mn100 vb1 vb1 0 0 cmosn w=2u l=1u
i2 0 vb1 10u
mn11 2 vb1 0 0 cmosn w=4u l=1u
mn1 8 v1 2 2 cmosn w=200u l=.8u
mn2 9 v2 2 2 cmosn w=200u l=.8u
vdd 1 0 3.3
***load cap**
cl 6 0 .5p
*.include ~/modelcard/level3.model
*.include ~/modelcard/level2.model
*.include ~/modelcard/BSIM.model
*.include ~/modelcard/BSIM3v3.model
.include ~/modelcard/s-cmod.model
v1 v1 0 1.523 ac 1
v2 v2 0 1.5
*.print v(v1) v(v2) v(6)
.AC DEC 10 100 1000MEG
.PRINT ac VDB(6) VP(6)
.END
```

(B) Analog Comparator
**** Analog Comparator ****

```
M51 7 3 2 2  CMOSN W=10u L=0.35u
M52 8 4 2 2  CMOSN W=10u L=0.35u
M53 7 6 2 2  CMOSN W=20u L=0.35u
M54 8 5 2 2  CMOSN W=20u L=0.35u
M55 5 11 7 7 CMOSN W=20u L=0.35u
M56 6 11 8 8 CMOSN W=20u L=0.35u
M57 5 6 1 1  CMOSP W=50u L=0.35u
M58 6 5 1 1  CMOSP W=50u L=0.35u
M59 5 11 1 1 CMOSP W=20u L=0.35u
M60 6 11 1 1 CMOSP W=20u L=0.35u
M61 9 5 1 1  CMOSP W=25u L=0.35u
M62 10 6 1 1 CMOSP W=25u L=0.35u
M63 9 5 2 2  CMOSN W=10u L=0.35u
M64 10 6 2 2 CMOSN W=10u L=0.35u

VDD 1 0 1.5V
VSS 2 0 -1.5V

Vcomp 11 0 DC 0V pulse(-1.5 1.5 2ns 0ns 0ns 2ns 4ns)
Vinp 3 0 DC 0V pwl(0ns -1.5V 30ns 1V)
Vinn 4 0 DC 0V pwl(0ns 1.5V 30ns -1V)
.tran 0.1ns 30ns

*.include ~/modelcard/level3.model
*.include ~/modelcard/level2.model
*.include ~/modelcard/BSIM.model
*.include ~/modelcard/BSIM3v3.model
.include ~/modelcard/s-cmod.model
.end
```

(C) Wide-Range Gilbert Multiplier

```
* Modified Wide Range Gilbert Multiplier
*.OPTIONS post ACCT OPTS $probe=1 dcon=1
*.print i(vi)
m1  15 16 13 0 cmosn w=0.5u  l=1.75u
m2   8 20 13 0 cmosn w=0.5u  l=1.75u
m3   1 15 15 1 cmosp w=0.5u  l=0.35u
m4   1  8  8 1 cmosp w=0.5u  l=0.35u
m5  13 14  0 0 cmosn w=0.5u  l=0.35u
m6  17 10 12 1 cmosp w=1.25u l=0.35u
m7  17 11  7 1 cmosp w=1.25u l=0.35u
```

```
m8   1 15 17 1 cmosp w=1.25u l=0.35u
m9   9 11 12 1 cmosp w=1.25u l=0.35u
m10  9 10  7 1 cmosp w=1.25u l=0.35u
m11  1  8  9 1 cmosp w=1.25u l=0.35u
m12  7  7  0 0 cmosn w=0.5u  l=0.35u
m13  6  7  0 0 cmosn w=0.5u  l=0.35u
m14 12 12  0 0 cmosn w=0.5u  l=0.35u
m15 18 12  0 0 cmosn w=0.5u  l=0.35u
m16 19  5  6 0 cmosn w=1.5u  l=0.35u
m17  3  5 18 0 cmosn w=1.5u  l=0.35u
m18  4  3  3 1 cmosp w=0.5u  l=0.35u
m19  2  3 19 1 cmosp w=0.5u  l=0.35u
m20  1  2  4 1 cmosp w=0.5u  l=0.35u
m21  1  2  2 1 cmosp w=0.5u  l=0.35u
vdd 1 0 5
v1 16 0 2.5
v2 20 0 2.5
v3 11 0 2.5
v4 10 0 2.5
vbb1 14 0 1.0
vbb2 5 0 2
vi 19 0 2.5
*.include ~/modelcard/level3.model
*.include ~/modelcard/level2.model
*.include ~/modelcard/BSIM.model
*.include ~/modelcard/BSIM3v3.model
.include ~/modelcard/s-cmod.model

.dc v1 1.5 3.5 .01 v3 2.1 3.0 .1
.end
```

(D)Wide Range Gilbert Multiplier *

```
*.OPTIONS post ACCT OPTS
*.option
*.print i(vi)
m1  15 16 13 0 cmosn w=0.5u  l=1.75u
m2   8 20 13 0 cmosn w=0.5u  l=1.75u
m3   1 15 15 1 cmosp w=0.5u  l=0.35u
m4   1  8  8 1 cmosp w=0.5u  l=0.35u
m5  13 14  0 0 cmosn w=0.5u  l=0.35u
m6  17 10 12 1 cmosp w=1.25u l=0.35u
m7  17 11  7 1 cmosp w=1.25u l=0.35u
m8   1 15 17 1 cmosp w=1.25u l=0.35u
m9   9 11 12 1 cmosp w=1.25u l=0.35u
m10  9 10  7 1 cmosp w=1.25u l=0.35u
```

```
m11  1  8  9 1 cmosp w=1.25u l=0.35u
m12  7  7  0 0 cmosn w=0.5u  l=0.35u
m13  6  7  0 0 cmosn w=0.5u  l=0.35u
m14 12 12  0 0 cmosn w=0.5u  l=0.35u
m15 18 12  0 0 cmosn w=0.5u  l=0.35u
m16 19  5  6 0 cmosn w=1.5u  l=0.35u
m17  3  5 18 0 cmosn w=1.5u  l=0.35u
m18  4  3  3 1 cmosp w=0.5u  l=0.35u
m19  2  3 19 1 cmosp w=0.5u  l=0.35u
m20  1  2  4 1 cmosp w=0.5u  l=0.35u
m21  1  2  2 1 cmosp w=0.5u  l=0.35u

vdd 1 0 5
v1 16 0 2.5
v2 20 0 2.5
v3 11 0 2.5
v4 10 0 2.5
vbb1 14 0 1.0
vbb2 5 0 2
vi 19 0 2.5
*.tran 1ns 1us
*.op
*=============================================
.include ~/modelcard/level3
*.include ~/modelcard/level2
*.include ~/modelcard/test.c05
*.include ~/modelcard/bsim.p5
*.include ~/modelcard/bsim11

.dc v1 1.5 3.5 .01 v3 2.1 3.0 .1
*=============================================
*.include ~/modelcard/level3.model
*.include ~/modelcard/level2.model
*.include ~/modelcard/BSIM.model
*.include ~/modelcard/BSIM3v3.model
.include ~/modelcard/s-cmod.model
*.dc v3 3.5 1.5 -.01 sweep v1 2.1 3.0 .1
*.dc v3 3.5 1.5 -.001 v1 2.1 3.0 .1
*.tran 0.1u 10u
.print i(vi)
.end
```

(E)One Bit Comparator.

```
Takes Two Inputs (A and B), and returns Two Ouputs -
*node 8 - (high when two signalsare equal) and node 9 (high when A is Larger Then B).
* Transient Analysis for BSIM3v3.1 test.

*circuit description

M1 Anot A Vdd Vdd  cmosp w=3.6u l=1.2u
M2 Anot A 0 0 cmosn w=1.8u l=1.2u
M3 Bnot B Vdd Vdd  cmosp w=3.6u l=1.2u
M4 Bnot B 0 0 cmosn w=1.8u l=1.2u
M5 AorBnot 0 Vdd Vdd cmosp w=1.8u l=3.6u
M6 AorBnot B 1 0 cmosn w=1.8u l=1.2u
M7 1 Anot 0 0 cmosn w=1.8u l=1.2u
M8 Lnot 0 Vdd Vdd cmosp w=1.8u l=3.6u
M9 Lnot Bnot 2 0 cmosn w=1.8u l=1.2u
M10 2 A 0 0 cmosn w=1.8u l=1.2u
M11 Qnot 0 Vdd Vdd cmosp w=3.6u l=3.6u
M12 Qnot AorBnot 3 0 cmosn w=1.8u l=1.2u
M13 3 Lnot 0 0 cmosn w=1.8u l=1.2u
MQLO 8 Qnot Vdd Vdd  cmosp w=3.6u l=1.2u
MQL1 8 Qnot 0 0 cmosn w=1.8u l=1.2u
MLTO 9 Lnot Vdd Vdd  cmosp w=3.6u l=1.2u
MLT1 9 Lnot 0 0 cmosn w=1.8u l=1.2u
CQ Qnot 0 30f
CL Lnot 0 10f
Vdd Vdd 0 2.5
Va A 0  pulse 0 2.5 1ns .1ns .1ns 10ns 20ns
*Vb B 0 0
Vb B 0  pulse 0 2.5 1ns .1ns .1ns 5ns 20ns
*
*.include ~/modelcard/level3.model
*.include ~/modelcard/level2.model
*.include ~/modelcard/BSIM.model
*.include ~/modelcard/BSIM3v3.model
.include ~/modelcard/s-cmod.model
* transient analysis
.tran 1ns 500ns
.option post
.print tran a b v(9) v(8)
.END
```