USC–SIPI REPORT #352

High-Frequency Mixed-Signal Silicon-On-Insulator Circuit Designs for Optical Interconnections and Communications

by

Liping Zhang

May 2002

Signal and Image Processing Institute
UNIVERSITY OF SOUTHERN CALIFORNIA
Department of Electrical Engineering-Systems
3740 McClintock Avenue, Room 400
Los Angeles, CA 90089-2564 U.S.A.

HIGH-FREQUENCY MIXED-SIGNAL SILICON-ON-INSULATOR CIRCUIT DESIGNS FOR OPTICAL INTERCONNECTIONS AND COMMUNICATIONS

by

Liping Zhang

A Dissertation Presented to the
FACULTY OF THE GRADUATE SCHOOL
UNIVERSITY OF SOUTHERN CALIFORNIA
In Partial Fulfillment of the
Requirements of the Degree
DOCTOR OF PHILOSOPHY
(ELECTRICAL ENGINEERING)

May 2002

Dedication

To my doctor father and parents

Acknowledgments

I hold a deep and constant gratitude for my academic advisor, Prof. Alexander A. Sawchuk, for his insightful technical guidance, invaluable support, and indispensable encouragement throughout the journey of my graduate research study. I enjoyed his classes, meeting minutes, opening remarks, presentations, and research projects that he superbly delegated. I am so grateful for his great guidance on building a translucent pyramid of optoelectronics over the foundation of semiconductor world.

I would also like to sincerely thank my dissertation committee members, Prof. B. Keith Jenkins, Prof. Ulrich Neumann, and two additional qualifying committee members Prof. Alan E. Willner and Prof. Christos Kyriakakis for their technical interest, constructive questions, insightful comments, and constant encouragement on the research work. I am deeply appreciative and would like to give grateful thanks to Prof. John Choma, Jr. for reading, revising my thesis in the final stages, and many insightful technical discussions.

I would like to acknowledge the support of Dr. Ravi Athale and the Consortium for Optics and Optoelectronic Technologies in Computing (COOP) at GMU, the COOP at USC organized by Dr. Alexander A. Sawchuk, Peregrine Semiconductor Corp., MOSIS, and the Integrated Media System Center, a National Science Foundation (NSF) Engineering Research Center (ERC), and other support that made our work possible.

I would also thank for my former colleagues Dr. Charlie B. Kuznia, Dr. Jen Ming Wu, Dr. Chih-Hao Chen, and Dr. Bogdan Hoanca. Their technical merit, perseverance, and patience always encourage me to seek perfection in each part of my work. I enjoyed working with them and other group members - Zahir Y. Alpaslan, Eddie Pansatiankul, Yunsong Huang, Sunkuang Hong, Chanki Min, Nopparit Intharasombat, and Hyukjune Chung for their friendship and share of exciting moments. I would like to thank my other colleagues and supporters: Jeffrey W. Sondeen at USC-ISI, Michael Venditti at the McGill university Photonics Lab, Edward R. Barkley at MIT, Ray Chen at Stanford, Dr. LiLy Cheng at Cadence, Dr. Andreas Andreou at JHU, Dr. Ron Reedy, Jean Richaud, Mike Stuber, John Sung, Chuck Tabbert, at Peregrine Semiconductor for their valuable technical discussions.

I truly appreciate Dr. Allan Weber and Seth Scafani for their valuable prompt help in computers and networks. Their help is indispensable to the success of our projects. I would like to thank Gloria Halfacre, Gerrielyn Ramos, Diane Demetris, Regina Morton, Linda Varilla, Kristi Delgado, and other administrator, staff for their quick last minute help.

I would dearly thank my parents Shuqin Yang and Chuankun Zhang for their generous, forever love and support. Thanks for the love and support from my wonderful brother Lichun, Liqing and sister Lihua. I deeply appreciate my life partner - Benmin Sun for his generous, constant, worry-free support of my research and study, which is indispensable for each of my day to be exciting, wonderful, and efficient.

Table of Contents

List of Acronyms

3G:	Third Generation
AHDL:	Analog Hardware Description Language
ASIC:	Application Specific Integrated Circuit
ATM:	Asynchronous Transfer Mode
AWGN:	Additive White Gaussian Noise
BER:	Bit Error Rate
BiCMOS:	Bipolar Complementary Metal Oxide Semiconductor
BJT:	Bipolar Junction Transistor
BPSK:	Binary Phase Shift Keying
CMOS:	Complementary Metal Oxide Semiconductor
CSMA/CD:	Carrier Sense Multiple Access with Collision Detection
CDF:	Cumulative Distribution Function
CDR:	Clock and Data Recovery
DQPSK:	Differential Quadrature Shift Keying
DSP:	Digital Signal Processing/Processor
EDFA:	Erbium-Doped Fiber Amplifier
EPROM:	Erasable Programmable Read Only Memory
ESD:	Electro-Static Discharge
FC:	Fiber Communication/Channel
FET:	Field Effect Transistor
FIFO:	First-In First-Out
FPGA:	Field Programmable Gate Array
FS:	Frequency Synthesizer
FSDO:	Free Space Digital Optics
FSK:	Frequency Shift Keying
FWHM:	Full Width Half Maximum
GaAs:	Gallium Arsinide
GBE:	Gigabit Ethernet
GBWP:	Gain-Bandwidth Product
HDL:	Hardware Description language
ICO:	Current Controlled Oscillator
IPA:	Intelligent Pixel Array
ISI:	InterSymbol Interference
ICI:	InterCarrier Interference
IF:	Intermediate Frequency
JFET:	Junction Field Effect Transistor
JPEG:	Joint Picture Expert Group
LED:	Light Emitting Diode
LAN:	Local Area Network
LNA:	Low Noise Amplifier
MMIC:	Microwave Monolithic Integrated Circuit
MOSFET:	Metal Oxide Semiconductor Field Effect Transistor
MPEG:	Motion Picture Expert Group
MQW:	Multiple Quantum Well

MSM:	Metal-Semiconductor-Metal
MTR:	Multi-Token-Ring
NF:	Noise Figure
NMOS:	N-type Metal Oxide Semiconductor
NIC:	Network Interface Controller
OEIC:	OptoElectronic Integrated Circuit
OESP:	OptoElectronic Stack Processor
OE-VLSI:	OptoElectronic VLSI
OOK:	On-Off Keying
OPDP:	Optical Parallel Data Packet
QPSK:	Quadrature Phase Shift Keying
PE:	Processing Element
PLL:	Phase Locked Loop
PN:	Pseudorandom Noise
ppm:	Part-Per-Million
PSD:	Power Spectral Density
PSK:	Phase Shift Keying
RF:	Radio Frequency
RMS:	Room Mean Square
RSPA:	Reconfigurable Smart Pixel Array
R-TRANSPAR:	Reconfigurable Translucent Smart Pixel Array
SBWP:	Space Bandwidth Product
SEED:	Self-Electrooptic-Effect Device
SiGe:	Silicon Germanium
SIMD:	Single Instruction Multiple Data
SNR:	Signal-to-Noise Ratio
SIR:	Signal-to-Interference Ratio
SOI:	Silicon-on-Insulator
SOS:	Silicon-on-Sapphire
SPA:	Smart Pixel Array
TDMA:	Time Division Multiple Access
TIA:	Transimpedance Amplifier
TSPC:	True Single Phase Clock
UTSi:	Ultra Thin Silicon
VCO:	Voltage-Controlled Oscillator
VCSEL:	Vertical-Cavity Surface-Emitting Laser
VHDL:	VHSIC Hardware Description Language
VHSIC:	Very High Speed Integrated Circuit
VLSI:	Very Large Scale Integration

List of Figures

List of Tables

ABSTRACT

This research explores architectures and design principles for monolithic optoelectronic integrated circuits (OEICs) through the designs and implementations of a.) a parallel-pipelined media networking and signal processing network; and b.) low-power radio-frequency mixed-signal complementary metal-oxide semiconductor (CMOS) silicon-on-insulator (SOI) circuit and chip designs for wireless and optical communications fabricated in Ultra-Thin Silicon-on-Sapphire (UTSi®-SOS) technology.

A signal processing and networking platform called reconfigurable translucent smart pixel array (R-TRANSPAR) has been implemented. The system uses interlaced 2D arrays of vertical-cavity surface-emitting lasers (VCSELs) and metal-semiconductor-metal (MSM) detectors provided by Honeywell for optical interconnections. The detected optical current was converted into voltage and amplified for further single-instruction multiple data (SIMD) parallel pipeline signal processing and networking. Both free-space and image-fiber chip-to-chip optical communications have been demonstrated based on this platform. A novel 3D optical parallel data packet (OPDP) switching multi-token-ring network has been designed, implemented and demonstrated. Time-division multiplexed (TDM) network node addressing technique is used to enhance channel utilization and throughput.

The ultimate goal of this research is to monolithically integrate silicon CMOS with optical devices for high capacity media processing and communications. High

throughput interconnections demand low noise, high gain-bandwidth product transceivers. We have identified that ultra-thin silicon-on-sapphire as the most promising CMOS SOI technology because of its optically transparent, electrically full-insulating sapphire substrate. The matched thermal expansion coefficients of sapphire with GaAs semiconductor optical devices are desirable for flip-chip bonding.

Four mixed-signal chips have been designed and fabricated in 0.5 μm CMOS SOS technology through MOSIS. Two 2000 CMOS SOS smart-pixel array chips were designed for wire bonding and two 2001 UTSi chips are to be flip-chip bonded with VCSELs and photodetectors arrays. Novel monolithic PIN optical detector arrays have been designed and fabricated in UTSi-SOS technology. Various low power and high frequency techniques including dynamic threshold voltage have been explored. Monolithic multi-GHz $\pi/4$ quadrature phase voltage-controlled oscillators (VCOs), radio frequency (RF) transceivers arrays with built-in self-test (BIST) circuits, full monolithic photoreceivers, differential VCOs, mixers, baluns, and phase-locked loop based clock data recovery circuits have been designed and fabricated in UTSi CMOS SOI technology for wireless, optical interconnections and communications.

Keywords: *SOI, CMOS, OEIC, UTSi, SOS, smart pixel arrays, optoelectronic interconnections, monolithic OEIC integration, optical receiver, VCSEL driver, time division multiple access, LC tank VCO, quadrature phase modulation, phase-locked loop, clock and data recovery, mixer, wireless and optical communication.*

CHAPTER 1 INTRODUCTION

1.1 Motivation and Objective

The steadily increasing demand for high-bandwidth communication channels and high-throughput digital media processing are forces that drive advances in optoelectronic networks and signal processing. Both high performance optoelectronic integrated circuits (OEICs) and intelligent pixel enhanced optical systems play a paramount role in implementing these systems [Decusatis_00]. Multimedia applications are ubiquitous due to recent advances in very large-scale integrated (VLSI) circuits, internet/intranet, broadband (ATM and ISDN) networks, and new compression standards such as JPEG2000, MPEG7, H.261, H.263, etc. [imsc_99]. Sophisticated applications such as multimedia communication, video conferencing, 3D graphics rendering, super high definition (SHD) and high definition TV (HDTV) require the transfer and processing of a large amount of data in real time [Sawchuk_98inv]. Even though the compression standards alleviate the data rates by an order of magnitude, super-computing, massive storage, and high bandwidth networking are still the most demanding technologies for multimedia interactive processing and transmission [Kuznia_oc00]. Hence, it is crucial to design a high-throughput generic processor architecture with high-bandwidth optical interconnects to meet both the real-time computing and communication requirements of various types of media.

The transistor count on a silicon chip has approximately doubled every 18 months for the past two decades, and this trend is continuing [Roadmap 01]. The advent of hardware description languages (such as Verilog, VHDL, AHDL) and

high-density reconfigurable field programmable gate arrays (FPGAs) require efficient processors to satisfy the computing demands of various media processing algorithms. To date, application specific integrated circuits (ASICs) have been applied to implement complicated image/video processing algorithms such as MPEG and JPEG. It is very challenging for ASIC design to keep pace with sophisticated new algorithms. Fortunately, the exponential decrease in the minimum transistor feature size as predicted by Moore's law [Moore_00], had led to powerful, efficient, low-cost, reconfigurable field programmable gate arrays (FPGAs). These reconfigurable digital signal processors distinguish themselves from generic processors by their low cost, reduced design cycle, high flexibility, ability to reprogram in-situ with different algorithms, and high-speed signal processing capability. System-on-chip FPGA technology is used for rapid system prototyping if chip-to-chip interconnection bottlenecks can be resolved.

High throughput computing systems typically also require high-bandwidth networking [Sawchuk_98]. Parallel optical interconnects feature high bandwidth, low loss and crosstalk, low power consumption, and small size. It is essential for optical interconnects to replace the electronics counterpart wherever high interconnection density and high throughput is required [Sawchuk_99].

Optoelectronic smart pixel arrays, with its electronics providing sophisticated signal processing, and its optics offering high-bandwidth interconnections, have become the ultimate choice for long-distance, high-bandwidth information transmission [Goodman_93]. With recent advances in fabricating semiconductor

vertical-cavity surface-emitting lasers (VCSELs) and active pixel devices, dense optoelectronic interconnect arrays have become possible [Sawchuk_97]. Optical interconnections are superior to conventional electronic technology due to its high bandwidth, low-crosstalk, high-density parallel two-dimensional arrays of data links [Goodman_91].

To integrate naturally the high signal processing capability of reconfigurable digital signal processors and the high throughput of optical interconnects, we have designed and implemented a Reconfigurable Translucent Smart Pixel Array named (R-TRANSPAR). R-TRANSPAR is a modular platform demonstration system to explore smart pixel array networking and signal processing architectures. This work includes system architectural issues; the design, fabrication, integration, and test of various VLSI circuits, optoelectronic (OE) devices, the entire OE system, and the development of supporting software and application algorithms [Sawchuk_99].

Optical interconnection systems with terabit throughput demand high I/O density, which requires light sources having low-power dissipation, high efficiency, good temperature stability, and polarization uniformity [Liu_98]. Advances in VCSEL fabrication for improved performance make them a good choice for interconnection light sources. Recent advanced in oxide-confined current VCSELs have lowered the threshold voltage and current, improved the efficiency and modulation speed. The hybrid integration of semiconductor optical devices such VCSEL and MSM detectors with CMOS VLSI is an initial step towards full monolithic integration. The next step is the use of flip-chip bump bonding to attach

GaAs optical source and detectors directly to CMOS chips. This approach is how being explored for optical interconnects. The emergence of oxide-confined 850 nm VCSELs, advances in photodetectors of high responsivity, low-threshold current, and advances in deep sub-micron CMOS SOI semiconductor technologies make optoelectronic intelligent pixel interconnects more attractive than ever.

A monolithic OEIC integration such as CMOS silicon on insulator with source and detectors is the ultimate implementation. There are several successful SOI technologies, such as Peregrine Semiconductor CMOS Ultra-Thin Silicon on Sapphire (UTSi®-SOS) [Peregrine], the new Intel TeraHz CMOS SOI [Intel_01], and IBM SiGe BiCMOS [IBM]. Among other SOI technologies are FIPOS (Full Isolation by POrous Silicon), SIMOX (Separation by IMplanted OXygen), SIMNI (Separation by IMplanted NItrogen), SIMON (Separation by IMplanted Oxygen and Nitrogen), etc [Colinge_97].

Ultra-Thin Silicon-on-Sapphire (UTSi-SOS) is a CMOS SOI process that developed and patented by Peregrine Semiconductor. In this process, 100-nm silicon is first grown on top of a 250-nm insulating and transparent sapphire substrate. There is no well and well contact, transistor is grown directly inside the thin silicon layer and on the sapphire substrate. UTSi is promising for monolithic high performance digital, analog, mixed-signal, and RF circuits and systems for wireless, satellite and optical communications. It has unprecedented flexibility to integrate with optical devices for interconnects and communications due to its electrically insulating and optically transparent substrate - synthetic sapphire (α-Al_2O_3).

This research includes advances in optoelectronic VLSI circuit and chip designs, the system-, network-level integrations of smart pixel arrays, and demonstrations of the steps needed for full monolithic integration of sophisticated optoelectronic system-on-chip VLSI parallel signal processing and networking functions. We have studied various CMOS SOI technologies, and designed various low-power, radio frequency, low noise, high linearity circuit and modules for wireless and optical communications. These modules include dynamic threshold transistor based CMOS standard logic gates, high-speed true-single-phase-clocking and static D-flip-flips, analog macros (such as amplifiers and comparators), and current mode logic (CML) cells, etc. besides shown sides those shown in Table 1-1. Both of the R-TRANSPAR and CMOS-SOI research involves architecture, system, circuit, physical level designs and multi-disciplinary studies as listed in Table 1-2.

	2000 UTSI CHIP#1	2000 UTSI CHIP#2	2001 UTSI CHIP#1	2001 UTSI CHIP#2
CMOS std cells	Dynamic threshold INV, NAND, AND, OR, NOR, XOR, MUX, TSPC DFF, Static DFF, double edge triggered DFF, etc.			
PAD cells	I/O pads, VDD pads, GND pads, bare pads and ESD protected pads, corner pads.			
LVDS std cells	INV, OR, XOR, MUX, DFF, differential amplifier, comparator, output buffer.			
High-Speed Digital circuit	2047-pattern TSPC PRBS	4x4 TDM switch with unicast and broadcast capabilities	Optically clocked TSPC DFF-based PRBS, Double-edge triggered DFF-based PRBS	Frequency divider
Monolithic Mixed-signal, Analog, RF circuits	Two 4x1 LNA transceiver arrays Ring oscillator	4x1 array receiver 4x1 array laser diode driver	4x1 flip-chip bonding optical receivers, 9 monolithic photoreceivers. Quadrature-phase LC-VCO, Mixer, Baluns	4x1 flip-chip boding VCSELs, PLL-based CDR Differential LC-VCO

Table 1-1. Summary of UTSi-SOS chip design work under 2000 COOP-GMU and 2001 COOP-USC Peregrine foundry runs.

ARCHITECTURE LEVEL			
Network Analysis - ATM, SONET, GBE - IP over WDM	Signal Processing - SIMD - MIMD - Multi-Processor	Storage System - CD, DVD - 2-Photon Memory - Holography	Interconnections - I/O, Memory bandwidth - Wireless, Free Space, Fiber
PHYSICAL LEVEL			
Processing System - Microprocessors - Network Processors - Smart Pixel Arrays	Semiconductor Optics - Photodetector Arrays - Laser Diode Arrays	Transmission System - CSMA/CD - Multi-Token-Ring - TDMA, CDMA, WDMA	Packaging System - Hybrid Wire, Flip-chip bonding - Monolithic Integration
SYSTEM LEVEL			
High-Speed VLSI - CMOS, LVDS Logic - CPU, NIC	Analog ASICs & OEICs - Biasing, current source - Optical Transceivers	Mixed-Signal & RF ICs - VCOs, PLLs, CDRs - SER/DES, ADC, DAC	Signaling Techniques - LVDS standard -Transmission Line Theory
PHYSICAL LEVEL			
Bulk CMOS	SOI CMOS	SiGe BiCMOS	GaAs HBT

Table 1-2. Pyramid for wireless, optical media processing, communication, and networking.

1.2 Significance and Contributions of this Research

Figure 1-1 shows the architecture of our proposed media processing and communication network and a research road map. Stage II, III, and IV summarize specific results toward this goal of monolithic OEIC smart pixel array high capacity network as described in this thesis.

At Stage I, we have realized VLSI smart pixel arrays flip-chip bonded to multiple quantum-well (MQW) modulator and detector arrays. At stage II, we designed and constructed a reconfigurable high-performance parallel pipeline signal processing and networking platform, and a novel multi-token-ring network with 3-D optical parallel date packet switching and VCSEL/MSM optical interconnections.

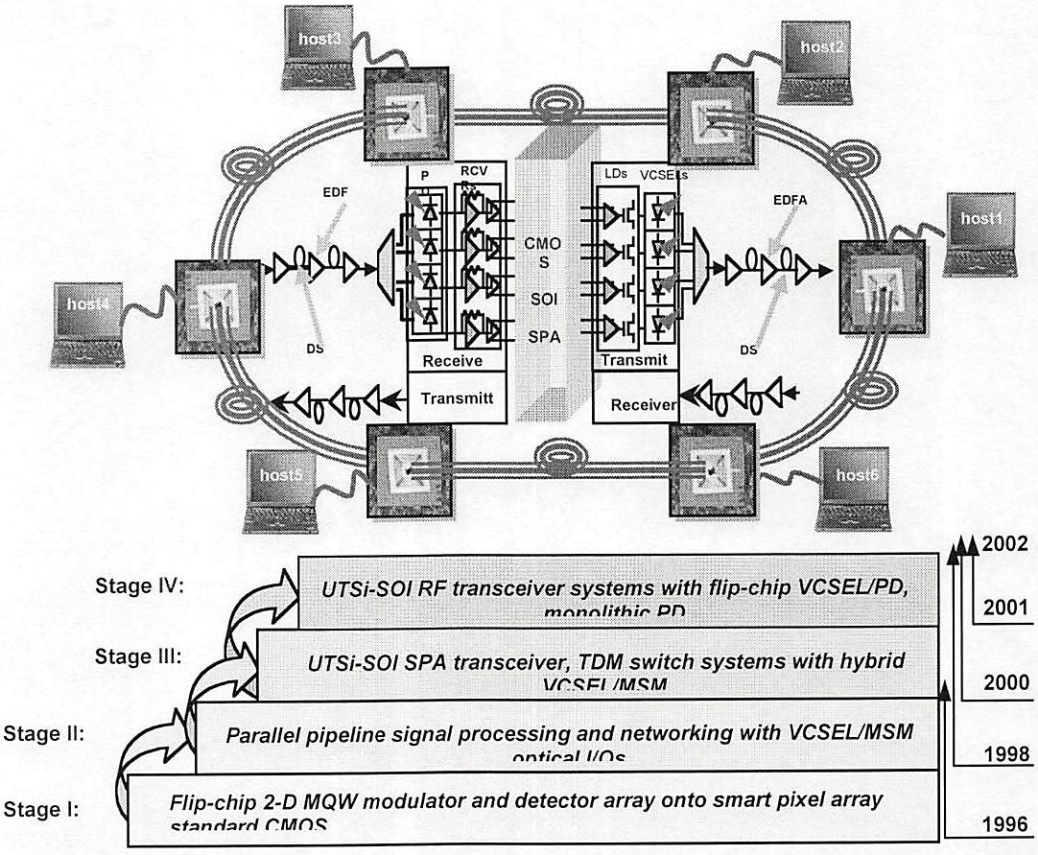


Figure 1-1. Architecture and roadmap of high-capacity monolithic smart pixel array communication networks.

We recently have identified the UTSi-SOS process as one of the most promising technologies for low-power, high-speed digital, analog, mixed-signal, RF and optoelectronic integrated circuits for wireless and optical communications. We have designed and fabricated two chips during the year 2000 and two chips in 2001 as summarized in Table 1-1. Both 2000 chip #1 and chip #2 have been tested under chip in socket or chip-on-PCB environment at 100 MHz, which is the maximum frequency of the functional generator in the Lab. Further high-frequency tests are being conducted.

The 2001 COOP UTSi chip foundry run started with a workshop hosted at USC in June 2001 and was sponsored by the Defense Advanced Research Project Agency (DARPA) through the consortium of optics and optical computing (COOP). The workshop was also supported by Peregrine Semiconductor Corporation during which tutorial and design demonstrations were included. Participants of COOP program could design UTSi CMOS chips with optional flip-chip bonding VCSEL and photodetectors through MOSIS. The COOP-USC workshop had more than 30 people from more than 10 leading research groups.

At stage III of Fig. 1-1, we have successfully designed and fabricated 2000 wire-bonding transceiver arrays, smart pixel time-division multiplexed switch with broadcast capability. At stage IV, we have designed and fabricated 2001 flip-chip bonded VCSEL driver arrays, flip-chip bonded photoreceiver arrays, full monolithic optical receivers, and monolithic RF OEIC optical communication modules such as a phase-locked loop based clock and data recovery (CDR), quadrature phase VCO, etc.

The focus and contributions to this research includes works in stages II, III, and IV. The following is a detailed description of our progress along this roadmap.

(1) Architecture and System Design of Reconfigurable Translucent Smart Pixel Array (R-TRANSPAR) Networking and Signal Processing Platform

- R-TRANSPAR Networking and Parallel Pipeline Signal Processing Architecture

- Network Interface Controller and Signal Processing SIMD Smart Pixel Array
- Designs of Multi-Volt I/O Interfaces, Electrical I/Os, Vertical-Cavity Surface-Emitting Laser (VCSELs) and Metal-Semiconductor-Metal (MSM) Detector Chips Optical Interconnections
- Optical Channel Assignment for 4-*f* Imaging System For Free-Space and Fiber Communications
- High-Speed Multi-Layer PCB Design and Implementation of R-TRANSPAR Platform
- Participated in the Verification of the R-TRANSPAR Networking and Signal Processing Platform

(2) Multi-Token-Ring Network Design, Implementation and Demonstration

- Architecture Design and Protocol Analysis of Multi-Token-Ring Network
- RTL Level and Circuit Level VLSI Design of Multi-Token-Ring Network
- Physical Configurations of Network Nodes on R-Transpar Platform
- Participated in the Verification of Multi-Token-Ring Network

(3) R-TRANSPAR System Test and Demonstration

- Networking R-TRANSPAR Systems With Test Processing Elements By Redesign the Logic, Re-Assign the I/Os, and Reconfigured the FPGA
- Making Test Plans, Participated in Electrical and Optical Channel Tests and Eye-Pattern Measurements

(4) 0.5 μm UTSi-SOS CMOS and LVDS Standard Cell Library Design and Layout

- Peregrine Semiconductor UTSi-SOS Technology and Our Design Methodologies
- 0.5 μm Peregrine UTSi FA Process CMOS Standard Cell Library Design, Layout Simulations, and Characterization with Multi-Threshold Transistors
- 0.5 μm Peregrine UTSi FC Process CML Standard Cell Library Design, Physical Layout, Spectre Simulations and Analog Macro Designs

(5) Architecture, Circuit and Chip Design of Optoelectronic UTSi SOS CMOS Smart-Pixel Transceiver Arrays with Built-In Self-Test (BIST) Circuits

- Networking Mode and Self-Testing Mode Architecture
- Optical Receiver Arrays and VCSEL Driver Arrays LSI Design
- Optical Transceiver Built-In Self-Testing (BIST) LSI Circuit Design

(6) Architecture, Function, and VLSI Chip Design of an SOS CMOS 4x4 Time-Division Multiplexed (TDM) Switch with Broadcasting Capability

- Optical Receiver Arrays and VCSEL Driver Arrays Analog Circuit Design
- Smart Pixel 4x4 Time-Division Multiplexed (TDM) Switch with Address Filter VLSI Circuit and Chip Design

(7) Flip-Chip Architecture and Chip Design for Optoelectronic Smart Pixel Analog CMOS Transceiver Arrays

- Multi-GHz Single-Ended, LVDS Optical Receiver Arrays Analog Circuit Designs
- Multi-GHz LVDS VCSEL Driver Array Design
- I/O Pads and ESD Protection Circuits Designs

(8). Monolithic UTSi-SOI CMOS Photoreceiver Designs

- Transimpedance Amplifier Receiver Array Analog Circuit Designs
- Novel Structures and Designs of UTSi-SOI PIN Photodiodes

(9) Monolithic Single, Quadrature Multi-Phase Differential LC-Tank VCO Chip Design

- Novel Architecture and Circuit Design of 2N-Phase Differential VCOs.
- Chip Designs of a Differential VCO, and $\pi/4$ Differential Quadrature-Phase VCOs for QPSK Modulator
- Designs of Biasing and Self-Startup Circuits

(10) Design and Physical Layout of Monolithic Mixer, Baluns, Clock and Data Recovery (CDR) Circuits based on PLL

- Differential Signal Up-Conversion Mixer Design
- On-Chip 4:1 Balun Design for Single-Ended to Differential Conversion

- Phase-Locked-Loop based Clock and Data Recovery Design

(11) Test-Bed Design, and Tests of UTSi-SOS Chips

- Transmission Line Signaling Analysis
- Testing of UTSi Chip#2 Including High-Speed Multi-Layer PCB Design
- Tests of UTSi-Chip #1

CHAPTER 2 OPTOELECTRONIC INTEGRATED CIRCUIT (OEIC) AND SMART PIXEL ARRAY (SPA) TECHNOLOGIES

2.1 High Performance OEIC Technology

The demanding requirements of optical communication networks have led advances in optoelectronic integrated circuit (OEIC) technology. The use of application specific integrated circuits (ASICs) has greatly expanded during the last decade. These devices are exhibiting higher and higher performance due to the exponential decrease of minimum transistor feature sizes as predicted by Moore's law [Moore_00]. OEIC technology has been improving steadily in recent years and optoelectronic ASICs have great potential for high-bandwidth communication networks. Full custom optoelectronics ASICs (CMOS DVD PICs, BiCMOS DVD PICs, and CMOS fiber receivers have been reported [Zimmermann_98, 99].

2.2 Intelligent Pixel Array (SPA) Technology

The fundamental challenge of future high-performance multiprocessor computing and communication systems is the inherent physical limitations of buses and backplanes [Haney]. The on-chip clock frequency of today's microprocessors is now on the order of GHz. Overall system performance improvement can be obtained only if the off-chip interconnections have high enough bandwidth. The forecast 50 nm process in 2011 leading to on-chip clock rates of about 10 GHz (as shown in Table 2-1) [Semi_01] poses great challenges for GHz off-chip interconnection packaging.

Year	Minimum Feature Size [μm]	Logic Transistor Density [10^6 TX/ CM]	Pin Count		On-Chip Clock		Chip-To-Board Speed	
			ASIC	MPU	Intra-chip [GHz]	Inter-chip [GHz]	bus [GHz]	backplane [GHz]
1999	0.18	6.6	1600	740	1.25	1.20	1.20	0.480
2002	0.13	18	2248	1012	2.10	1.60	1.60	0.885
2005	0.10	44	3158	1384	3.50	2.00	2.00	1.035
2008	0.07	109	4437	1893	6.00	2.50	2.50	1.285
2011	0.05	269	6234	2589	10.00	3.00	3.00	1.540
2014	0.035	664	8758	3541	13.50	3.60	3.60	1.800

Table 2-1. Semiconductor technology forecast (Extract of 2001 ITRS) [Semi_01].

Smart pixel interconnects have been first proposed for use in intelligent processor backplanes [Hinton_96] and are one of the enabling technologies to overcome the interprocessor communication bottleneck. Smart pixels are typically a 2-D array of electrical signal processing elements with enhanced optical I/Os [Sawchuk_98inv]. Smart pixel arrays (SPAs) make the best use of the dense, high processing power of electronics and the low crosstalk and intersymbol interference; spatial, polarization and wavelength parallelism, and the ultra-high communication bandwidth of optics [Sawchuk_92]. A comparison of electronics and optics for interconnections is shown in Table 2-2. With the advance of VLSI technology, SPAs for sophisticated systems have evolved into intelligent pixel arrays (IPAs).

	ELECTRONICS	OPTICS
Electromagnetic interference (EMI)	Emits and is susceptible to EMI	No EMI
Bandwidth-distance product	Skin effect limited bandwidth-distance product	High bandwidth-distance product
Connection and bandwidth	Perimeter I/O, limited bandwidth per pin	Area-I/Os, very high (GHz) bandwidth per channel
Crosstalk	High crosstalk, and intersymbol interference at high frequencies	Low crosstalk, low intersymbol interference
Flexibility	One-signal two-wire, ground loop issues.	Bandwidth reserve by using wavelength division multiplexing (WDM) or dense WDM technology.

Table 2-2. Pros and cons of electronics and optics for interconnections.

The major advantage of an IPA is its ability for sophisticated signal processing, such as an ATM packet switching protocol with thousands of gates. It is the intelligence of the IPAs that distinguishes them from photonic integrated circuits (PICs). PICs do not have any electronic signal processing capability, and typically refer to the monolithic integration of photonic devices such as lasers, detectors, optical waveguides, couplers, gratings, etc. [Hinton96]. The optical signals from the neighbor intelligent pixel arrays communicate through free space or emerging fiber arrays between 2D area-I/Os. Optical input signals are typically detected either through GaAs p-i-n detectors or metal-semiconductor-metal (MSM) photodetectors

and converted to usable voltage levels by the pre-amplifier of a receiver. The receiver post-amplification stages further amplify the signal up to the digital logic level suitable for pixel array to perform signal processing algorithms. The processed electrical signals are then fed into the drivers and converted back into electrical current to drive the emitters.

There are two different categories of optical emitters in SPA or IPA technology. The first is modulator-based technology, where the modulators modulate light from external sources (semiconductor lasers or LEDs) to produce an optical output. Such modulators include multiple quantum well (MQW) p-i-n diodes as demonstrated in a previous USC TRANSPAR-MQW experiment [Chen_99]. In this work CMOS was fabricated with Hewlett-Packard's 14B 0.5 μm process as part of the 1997 Bell Labs/Lucent Technology CMOS-MQW foundry. The MQW modulators in TRANSPAR-MQW are flip-chip bonded to the surface of CMOS die [Sawchuk_98]. The other category of SPA or IPA technology is source-based and utilizes VCSEL or LEDs. Rapidly evolving high performance VCSEL design and fabrication techniques [Bond_98] makes it a very attractive method for high density optical interconnects. There are four major approaches for VCSEL-based intelligent pixel array integration:

1. A hybrid integrated package of VCSEL array, CMOS or GaAs wafer, and optical detector array
2. Thin-film integration of optoelectronic devices on Si or GaAs wafers
3. Flip-chip bonding of VCSELs and detectors onto Si or GaAs wafers

4. Monolithic integration of VCSELs, detectors, and signal processing circuits onto the same substrate

In this work we have used Approach 1 and 3 due to the immaturity of the other choices. We also designed novel fully monolithic optical receiver arrays with on-chip photodiodes. Thin-film integration can be used for both VCSEL- and modulator- based transmitters, but is relatively complicated. Flip-chip bonding is a natural extension of hybrid self-electrooptic-effect device (SEED) technology to bond VCSELs instead of modulators onto wafers. Flip-chip bonding is an optimal choice for prototyping and test with new semiconductor technologies. Monolithic integration of VCSELs, metal-semiconductor field-effect transistors (MESFETs), and MSM detectors was first demonstrated by NTT with 3-dB bandwidth of 220 Mhz [Matsuo_95], where the pixel consists of three transistors and falls into smart pixel category. Monolithically integrated optical devices based on VCSEL/MSM-PD and CMOS optical receivers are still in research stage.

As advanced silicon technology becomes mature, monolithically integrated intelligent CMOS pixel arrays are anticipated as the main technology. The direct applications of monolithic optoeletronic integrated circuits include full duplex optical transceiver modules. They transmit and receive optical signals of different carrier wavelengths. Those transceivers will be key components in high capacity lightwave communications and "intelligent optical networks", where IP transmission occurs directly using dense wavelength division multiplexing (DWDM) [Decusatis_00]. All the features (such as protected switching, packet add/drop, and quality of service) performed by the traditional ATM over SONET-based overlay

networks could be incorporated into intelligent pixel arrays. In recent years, many monolithic OEIC optical receivers have been reported using InGaAs high electron mobility transistors (HEMT)-based photoreceivers [combell] [Fay_98].

Emerging 3D OptoElectronic Stack Processors (3-D OESP) and related technologies integrate stacked silicon IC chips with optoelectronic devices for high performance computing and switching applications [Marchand_00]. Each layer in the stack communicates with its neighbors by electrical perimeter interconnections on the side of the stack [Marchand_00]. 3D chip stacks using VCSEL arrays with the associated drivers, optical receivers, and micro-optics to direct the optical signals might provide an efficient way for short distance communication between the layers. However, the nature of the cube architecture poses inherent thermo-mechanical and thermal issues such as heat sinking and thermal expansion mismatching, which may cause problems with integrating VCSELs or optical detectors.

Integrating p-i-n (positive-intrinsic-negative) photodiodes with analog receiver circuits on the same substrate results in smaller size, better immunity to electromagnetic interference (EMI), high-speed, low cost, and high reliability. In the second phase of this work we use CMOS OE-VLSI circuits based on ultra-thin silicon on sapphire (UTSi) technology. UTSi CMOS consists of a 100-nm silicon layer CMOS circuitry fabricated on top of 250-nm fully insulating, transparent synthetic sapphire substrate. Sapphire is non-conducting and does not absorb, attenuate, distort or combine RF signals [Johnson_95]. Additionally, UTSi CMOS process eliminated the need for transistor isolation wells, which significantly reduced

process complexity. Finally, synthetic sapphire wafers are far more durable than silicon or GaAs wafers.

UTSi technology provides great performance benefits compared to conventional bulk CMOS technology. The most salient features of SOI are elimination of the bulk CMOS latch-up and reduction of junction parasitic capacitance. These features allow ICs to operate at higher speed than the bulk CMOS ICs of equal transistor sizes. SOI technology also alleviates short-channel effect that conventional deep sub-micron CMOS suffers, provides good isolation that allows higher density. Ultra-Thin Silicon (UTSi) CMOS allows true RF integration by combining near ideal passive devices with low-power high performance active devices.

Ultra-thin silicon on sapphire looks promising for monolithic CMOS OEIC integration. Many research groups in optoelectronics, wireless, and satellite communications have been fallen in love with UTSi-SOS because of its monolithic high-performance active and passive devices, small size, radiation hardness and particularly the coexistence of good thermal, themo-mechanical characteristics and optical transparency of the synthetic sapphire.

The intersection of the semiconductor and optical communication world will lead to the monolithic integration of microprocessors, network processors and optical transceiver arrays for high-throughput media processing and communication. Monolithically integrating intelligent pixel array on bulk silicon CMOS is very challenging due to fabrication, parasitics, and packaging issues. Very fast switching

and high-bandwidth optical devices such as VCSEL, MSM photodetectors are fabricated in gallium arsenide semiconductor technology. To integrate these devices monolithically with mainstream silicon CMOS VLSI and OEIC circuits is extremely difficult. GaAs materials cannot be deposited directly on silicon (Si) substrates because the crystal lattices of the two materials do not match. Today's cutting edge research shows that it is very promising to deposite GaAs layer on silicon substrate through an intermediate layer that could reduce the lattice mismatch between GaAs and Si substrate. Such materials include strontium titanate. When a strontium titanate layer is deposited on silicon, it rotates 45 degrees with respect to the silicon substrate, so that the strontium and oxygen atoms line up with silicon atoms, and then GaAs layer having similar lattice structure with strontium titanate layer will be deposited on top. By employing a third layer material in between, monolithic integration of CMOS silicon wafer with GaAs devices may be possible.

CHAPTER 3 A GENERAL-PURPOSED SIGNAL PROCESSING AND NETWORKING PLATFORM WITH VCSEL/MSM INTERCONNECTIONS

3.1 R-TRANSPAR Functions and Implementation

We have designed a research system called Reconfigurable Translucent Intelligent Pixel Array (R-TRANSPAR) [Sawchuk_00inv, Kuznia_00, Zhang_01]. R-TRANSPAR is a networking and signal processing platform that performs parallel signal processing and optical data transfer among network nodes in the form of 3D optical parallel data packets (2D spatial and 1D temporal) as shown in Figs. 3-1 and 3-2. In Fig. 3-1, each packet contains an 8-bit optical clock, an address channel consisting of time-division-multiplexed (TDM) source and destination addresses and 3x4x8 bits of payload. The parallel optical clock is inverted before latch in the packet at the receiving node, so that the time-of-flight penalty can be avoided. The address channel is designed in time-division-multiplexing to enhance channel utilization and throughput.

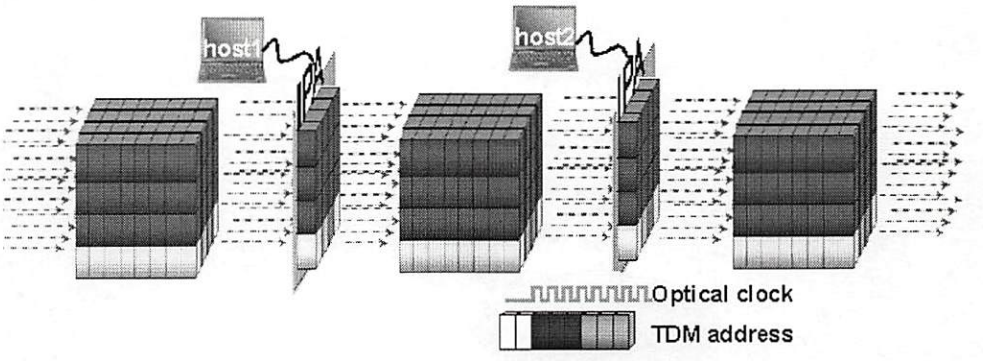


Figure 3-1. 3D optical data packet switching and TDMA addressing in R-TRANSPAR

The specific objective of the optoelectronic R-TRANSPAR system is to implement two different communication and computing-intensive functions: high

capacity networks that transfer packets with spatial parallelism; and parallel pipeline image and video processing applications such as compression and tracking. By utilizing many spatial parallel channels, R-TRANSPAR can achieve high throughput, low latency communication between nodes, even with each channel operating at moderate data rates [Sawchuk_98]. The optical channels are associated with 2D array of smart pixels, each with an optical input and optical output. Each intelligent pixel consists of optical network interface protocol logic and an ALU based processing element with local memory. The network interface is responsible for transmitting and receiving optical data packets under our novel multi-token ring network protocol. Other novel protocol interface will be designed and tested after reconfiguration. The intelligent pixel array is a mesh-networked SIMD array with inherent parallelism that can be fully exploited by images and video algorithms as it allows the convolutions to be performed in parallel on one plane.

Two R-TRANSPAR nodes are shown in detail in Fig. 3-2. Each node contains a system-on-a-chip FPGA array processor, a transimpedance amplifier (TIA) receiver chip [Sawchuk_oc00] fabricated through the MOSIS foundry, and a single chip (fabricated by Honeywell) containing an interlaced 4 x 4 array of VCSEL sources and 4 x 4 array of MSM detectors on a 250 μm x 250 μm grid [Liu_98]. The VCSEL-MSM provides source-based smart pixel photonic input-output rather than the CMOS-SEED modulator-based chips [Wu_99], as used in previous versions of the architecture. The FPGAs are programmed to implement different network logic (such as multi-token-ring protocol, carrier-sense multiple access/collision detection (CSMA/CD) protocol commonly used in Ethernet) and different ALU

configurations. The FPGA is also capable of directly driving the VCSELs. The TIA receiver chip converts and amplifies the detected optical signals into CMOS logic to drive FPGA inputs.

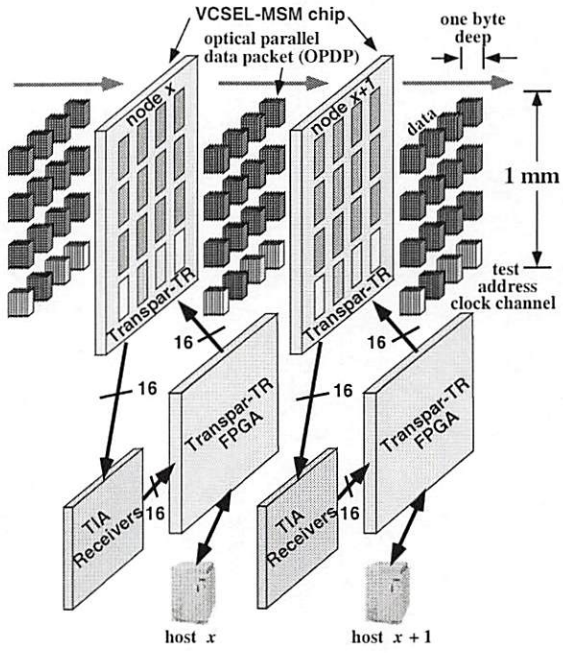


Figure 3-2. Block diagram of R-TRANSPAR node for 3D optical parallel data packet switching.

One general block diagram of R-TRANSPAR internal logic that includes both signal processing SIMD array processors and network processor is shown in Fig. 3-3. For parallel signal processing, each R-TRANSPAR-MTR node can operate as mesh-connected SIMD PE array with electrical I/Os on the edge of the plane or optical I/Os via 2D MSM detector or VCSEL array. The ALU performs add, subtract and Boolean logic operations on bits stored in the local SRAM within the pixel or on bits within neighboring pixels. The prototype system is able to perform very fast

parallel processing of 2D data fields, such as those required in image/video processing or packet header recognition and routing.

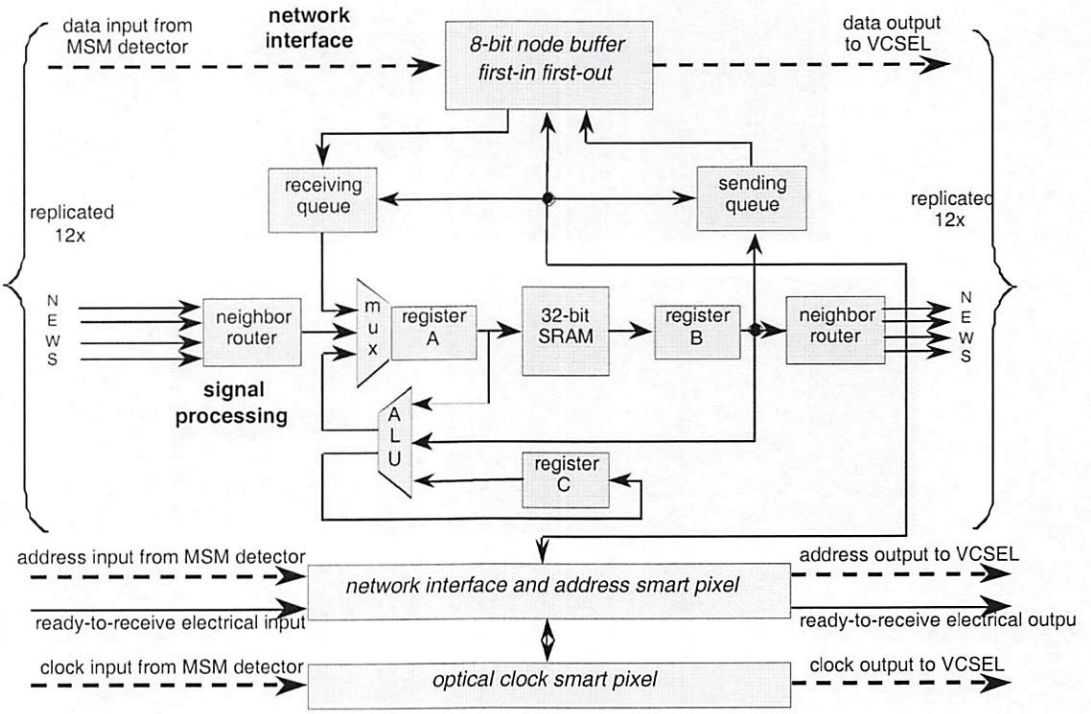


Figure 3-3. A General block diagram of R-TRANSPAR internal logic functions.

The logic design, design compilation, verification, timing analysis, and programming of R-TRANSPAR are performed in Altera MAX+PLUS II EDA tools. The MAX+PLUS II has friend interface with Cadence, Mentor Graphics, Viewlogic and others. It supports VHDL 1987, VHDL 1993 and Verilog HDL design. The Synopsis Express synthesizer is optimized for the VHDL or Verilog HDL code. To be visible, most of the designs, including each of 3x4 signal processing and networking pixel element, time-division multiplex address pixel, multi-token ring network interface controller, optical clock pixel adapting the new protocol, and testing pixels are implemented in transistor switching level logic as graphics design

files (.gds) format. The finite state machine supporting serial ALU operation designed by previous students is revised to interface with multi-token ring protocol and is in VHDL format. The project design is a hierarchy approach and design flow is summarized in Fig. 3-4.

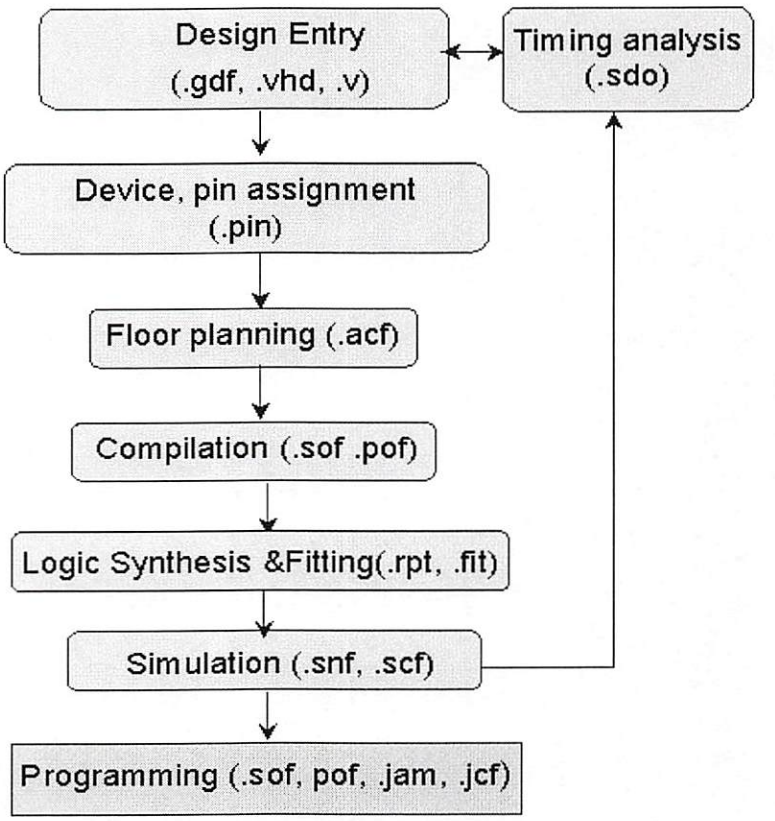


Figure 3-4. Design flow of system-on-chip (SOC) R-TRANSPAR.

Each R-TRANSPAR node is physically implemented as a four-layer printed circuit board (PCB) which has the Altera FPGA, VCSEL-MSM chip, receiver chip, and connects to a host computer through a high-speed digital interface connector. For high-speed considerations, surface mount decoupling capacitors have been attached along all the power lines, a 10 μF cap is attached close to the power

connector and a 1 μF cap is attached to the power line close to the chip. Thus, high frequency noise on the power supply has been minimized. Various test boards has been designed, constructed, and tested. Receiver sensitivity, bandwidth, VCSEL output power efficiency and other device characterization have been measured.

3.2 R-TRANSPAR Electrical and Optical System Designs

3.2.1 System Overview of R-TRANSPAR-FPGA Network Node Design

R-TRANSPAR (Reconfigurable Translucent Smart Pixel Array) is a high throughput photonic ring network architecture that transfers digital data using 3D optical parallel data packets [Sawchuk_oc00]. As a preparing step towards the CMOS monolithic integration of smart pixel array, VCSEL/PD, and transceivers, the R-TRANSPAR is an immediate implementation of intelligent pixel array with optical area-I/Os but in a modular design approach [Chen_oc99]. Associated with a host computer, each R-TRANSPAR node also can serve as a high performance parallel pipeline single-instruction-multiple-data (SIMD) array processor, with an internal arithmetic logic unit (ALU) and internal interprocessor mesh connection.

Figure 3-5 shows the multi-layer printed circuit board of R-TRANSPAR. It is a universal platform to explore advanced optoelectronic parallel pipeline signal processing and networking architectures.

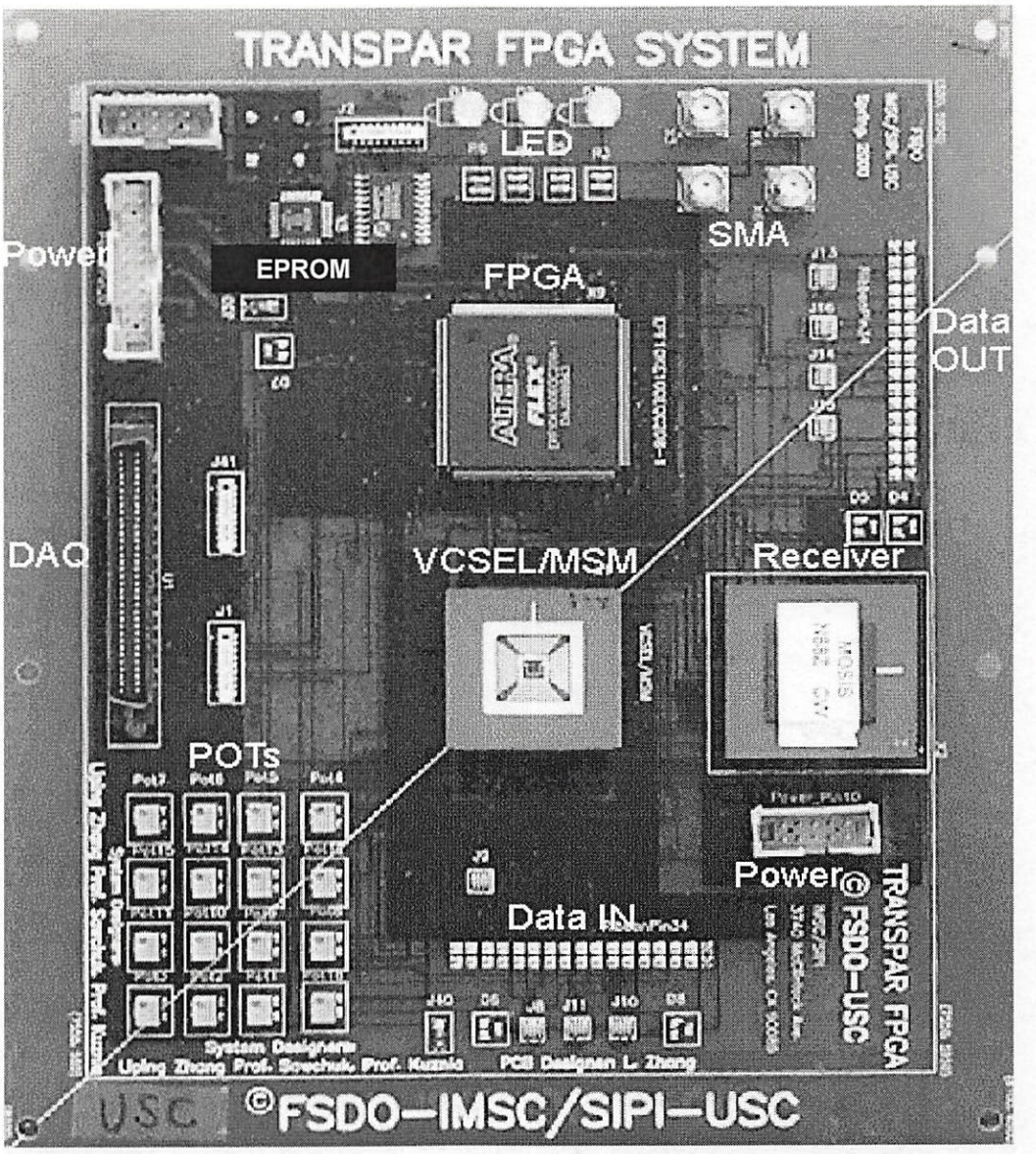


Figure 3-5. Reconfigurable Translucent Smart Pixel Array (R-TRANSPAR) signal processing and networking platform with optical interconnections.

The next sections describe its component - a 200k FPGA, 4x4 interleaved VCSEL/MSM chip, 16x4 optical receiver chip, DAQ high-speed computer interfaces; its smart-pixel array networking function design; its multi-volt I/O interface design; the network level architecture for free-space optical imaging I/O interconnect design; and its implementation as a novel multi-token-ring network.

3.2.2 Components

The optical interconnects of R-TRANSPAR uses a Honeywell VCSEL-MSM chip [Liu_98] supplied by the DARPA-sponsored foundry project operated by the CO-OP program at George Mason University (co-op.gmu.edu/vcsel). Through a series of experiments and investigations of the output-driving curves of different FPGAs, we concluded that the pad drivers of the Altera FPGA chip were capable of directly driving the VCSELs. According to the VCSEL's characteristics, we selected one of the FLEX10K100E devices, whose output driving characteristics is shown in Fig. 3-6. For the Honeywell VCSELs, we found that VCCIO = 2.2 *V* results in a VCSEL drive current of 10 *mA* and optical power of 1mW. The FPGA is able to drive the VCSEL above 100 MHz.

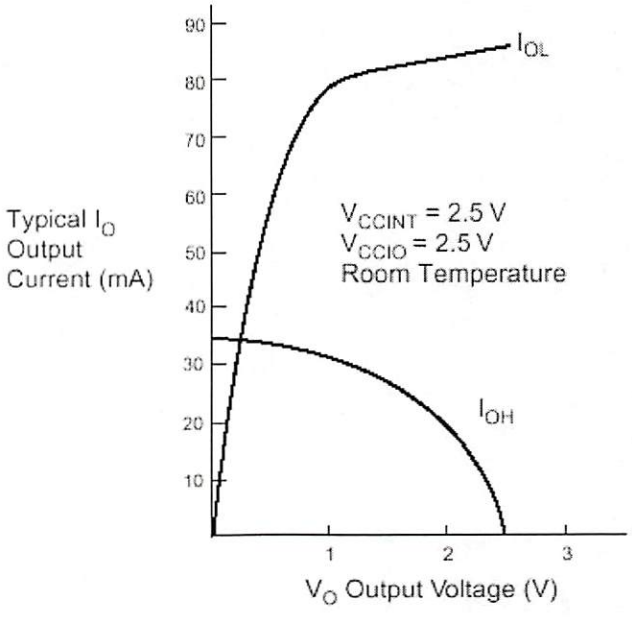


Figure 3-6. I-V curve of the I/O pads acting as VCSEL driver.

A TransImpedance Amplifier Receiver (TIAR) has been designed, fabricated and tested to interface between MSM detector and digital chips. The TIAR receives

sixteen parallel electrical current signals from the MSM photodetectors and converts them into sixteen parallel digital CMOS voltage signals, which drive the FPGA multivolt-I/Os. The specifications of the TIAR include: low crosstalk between small MSM signals (~10 μA); wide dynamic bandwidth (100 Mbps); high transimpedance gain (250 $k\Omega$); and immunity to large parasitic capacitance in a printed circuit board environment.

From the four distinct receivers that had been tested including single-ended and differential-ended designs, one having multistage feedback preamplifier had the best performance for the above specifications. Figure 3-7 shows one design with the best measurement results. The outputs of the receiver preamplifier are followed by another gain stage and XOR gate. Each of the XOR gate output is input to a 4 to 1 multiplexer to share the digital output pads with the other three receiver arrays. Another input to the XOR gate controls whether the receiver array is inverting or non-inverting. The optical signals from the VCSEL transmit to the MSM detector array and then fan out to the TIAR chip.

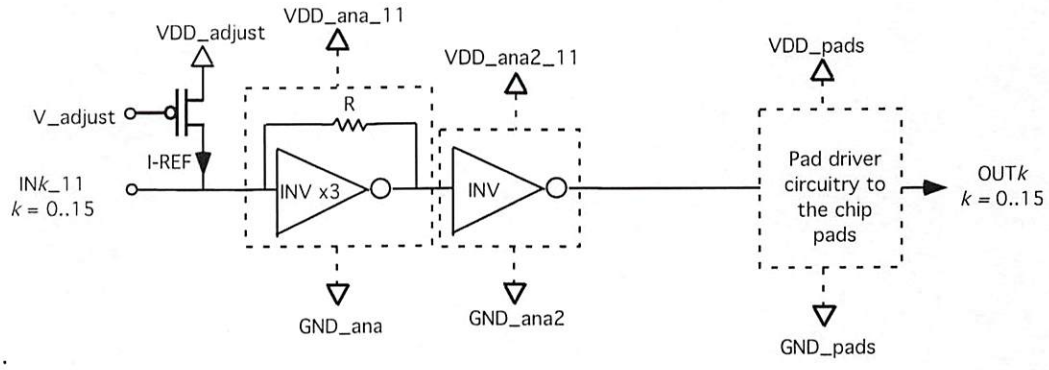


Figure 3-7. A transimpedance amplifier receiver interfacing with MSM chip.

3.2.3 Channel Assignment and VCSEL/MSM Optical Interconnections

VCSEL/MSM optical channel assignment is organized in such a way that the critical optical clock and TDM address channels are located close to the optical axis. Due to the inverting nature of the 4f imaging system and the interlaced orientation of the VCSEL and MSM, one of the two neighbor nodes is rotated by 90 degrees as shown in Fig. 3-8 (circle is VCSEL, square is detector), where the red circle dots represent for VCSEL and squares for MSM detectors. In a 4f imaging system, this orientation of two nodes gives a perfectly matched bi-directional VCSEL-MSM pair of optical interconnections under the conjugated one-to-one mapping. In the fiber image guide communication set-up, this rotation is still necessary due to the relative positions of VCSEL and MSM detector.

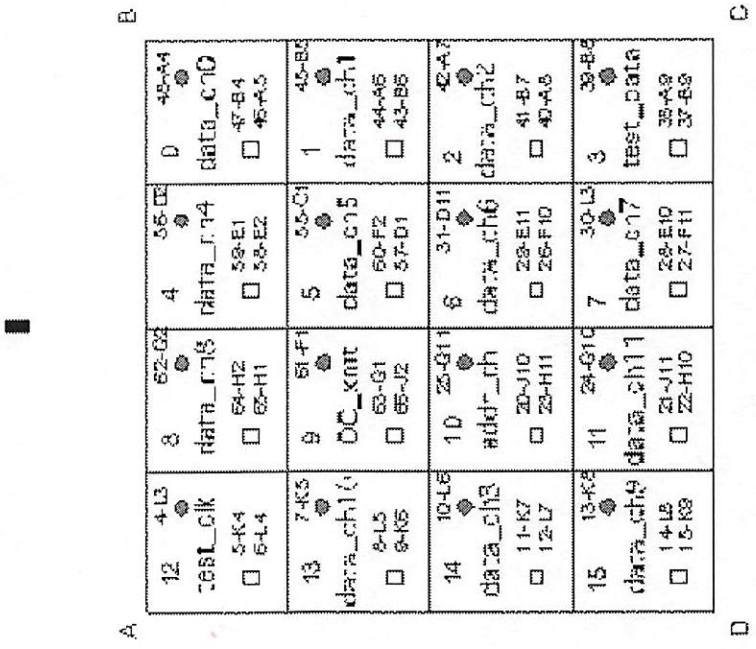


Figure 3-8. Optical interconnect design of VCSEL/MSM orientations and channel assignment with consideration of 4f imaging system in a two-node network.

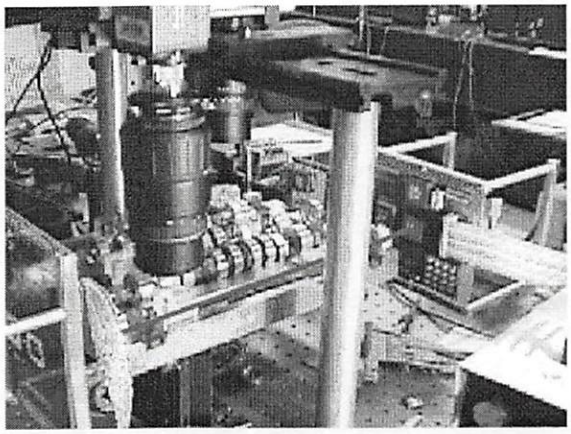
3.2.4 Multi-volt I/O Interface Design

The system-on-a-chip TRANSPAR FPGA is an Altera EPF10K100EQC-1 208-pin enhanced embedded programmable logic device (EPLD). The configuration device is an EPROM (EPC2) running at 3.3-*V*. This Altera FLEX10KE device is a low power high performance 0.22 μm CMOS SRAM process chip. This FPGA family was chosen because of its multivolt-I/O feature and particularly its desirable output driving characteristics. The multi-volt I/O feature allows the device to interface with chips running at different supply voltages. These devices have one set of VCCINT power pins for internal operation and input buffer, another set of VCCIO power pins for I/O output drivers. Our design selects both VCCIO and VCCINT of 2.5-*V*, which is optimal to drive the VCSELs on the Honeywell chip. A 5-*V* TTL high-speed digital I/O board enables the FPGA chip to communicate with a host PC. Since the 2.5-*V* output cannot drives 5-*V* device directly, we have included external pull-up resistors to interface with the 5-*V* TTL device. The TIA receiver chip is in 5*V* AMI 1.2 μm CMOS technology. We use the FPGA's internal clamping diode to limit the 5- *V* receiver output signal to the FPGA 2.5-*V* inputs.

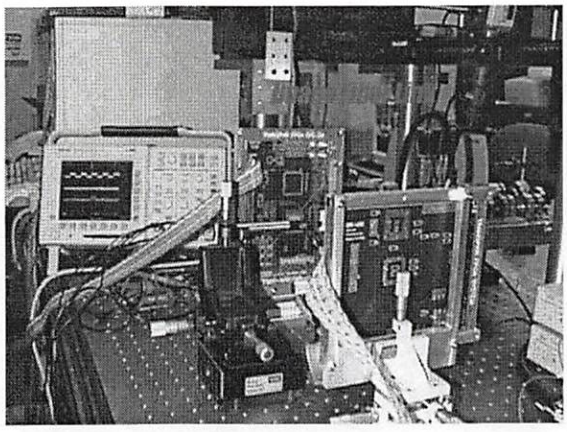
3.3 Demonstration of Translucent Smart Pixel Array Network Optical Interconnections

The optical interconnection interface of R-TRANSPAR has been tested and demonstrated. The conjugate imaging relationship of the interconnection was also demonstrated through free space and fiber image guide.

The free-space system set-up is shown in Fig. 3-9 (a). One of our optical set ups uses two 60 mm focal length glass doublets to form an infinite conjugate ratio imaging system [Sawchuk_00]. This macro-lens system images the 4x4 array of VCSELs on one chip onto MSMs on another chip to create 16 optical parallel channels. The system is bi-directional in that the VCSELs on the second chip are also imaged back onto the MSMs on the first chip, providing additional 16 channels in the reverse direction.



(a)



(b)

Figure 3-9. R-TRANSPAR network system free-space optical link setup (a) and fiber communications between nodes (b).

The R-TRANSPAR network nodes are also connected (by a colleague student) with fiber image guides (FIGs) - bundles of a large number of individual fibers used to transfer 2-D images. A typical FIG has more than ten thousand core fibers with the density on the order of $10^4/mm^2$. Each individual fiber is a step index multi-mode fiber with a 9.2 μm core. The fibers are arranged in a hexagonal array with 13.5 μm pitch. 0.3 m length FIGs is used and more than 50% of the incident optical power is coupled from VCSELs. The diameter of the FIGs is about 1.5 mm and numerical aperture (NA) is 1.0. The distance between each VCSEL and detector and the fiber bundle is controlled carefully using xyz positioners to evaluate various alternatives. The VCSEL beam spots are monitored through a CCD camera connecting to the output of the FIGs. The output size of VCSEL beams is about 50 μm in diameter with a coupling distance in the range of 0 to 50 μm. The image fiber link between the same two nodes (as shown in Fig. 3-9 (b)) has been tested with a clean eye pattern at over 20 Mpbs.

The free-space optical link is tested running at 100 Mbps with a clean open eye-pattern (as shown in Fig. 3-10). The well-defined minima and maxima of the open eye indicate wideband operation, low noise, and low intersymbol interference.

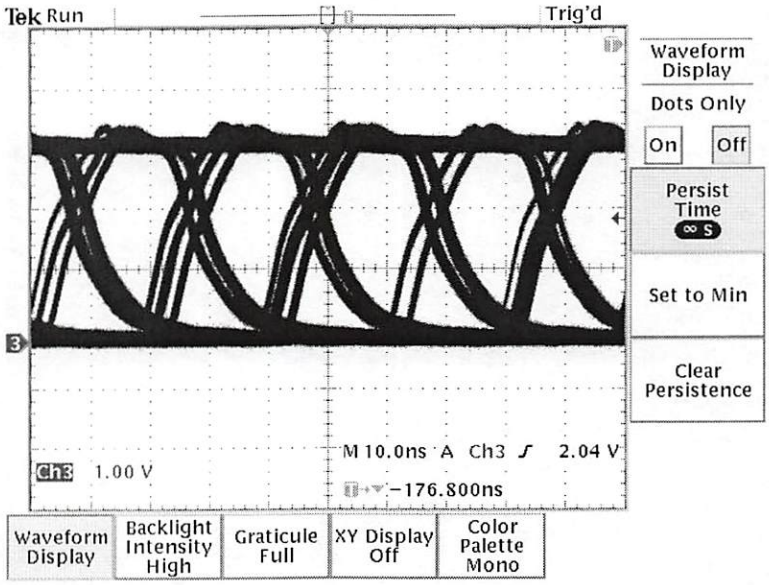


Figure 3-10. Eye pattern of R-TRANSPAR free-space optical link.

CHAPTER 4 ARCHITECTURE, PROTOCOL, AND LOGIC OF 3D OPTICAL PARALLEL DATE PACKET SWITCHING MULTI-TOKEN-RING NETWORKS

4.1 Introduction

Figure 4-1 shows a ring connection of several R-TRANSPAR nodes to form a network that transfers parallel optical data packets. The spatial and temporal parallelism enables very high throughput to be obtained even with moderate data rates on each physical channel.

R-TRANSPAR is flexible so that different protocols for transferring packets among nodes can be tested. A ring version of carrier-sense multiple access, collision detection (CSMA/CD) or a token-ring mechanism is shown in Fig. 4-1.

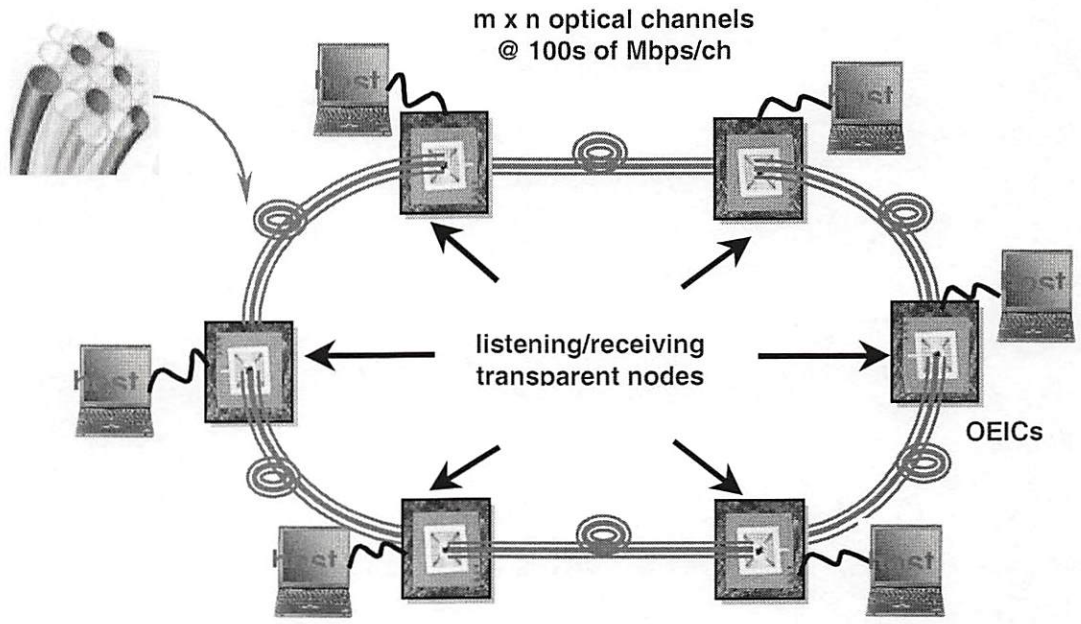


Figure 4-1. R-Transpar optical data packet switching fiber communication network architecture.

The high throughput photonic ring network can transfer 3D optical parallel data packets (OPDPs) in free-space or through fiber. The same network nodes transmiting and receiving 3D OPDPs using carrier sense multiple access with collision detection (CSMA/CD) protocol through fiber.

4.2 3D OPDP Switching Multi-Token Ring Protocol Design and Analysis

In order to avoid possible crosstalk, VCSELs and MSMs on the same node are not allowed to be active simultaneously. A Multi-Token-Ring (MTR) network protocol based on this constraint has been designed. A six-node MTR network is illustrated Fig. 4-2.

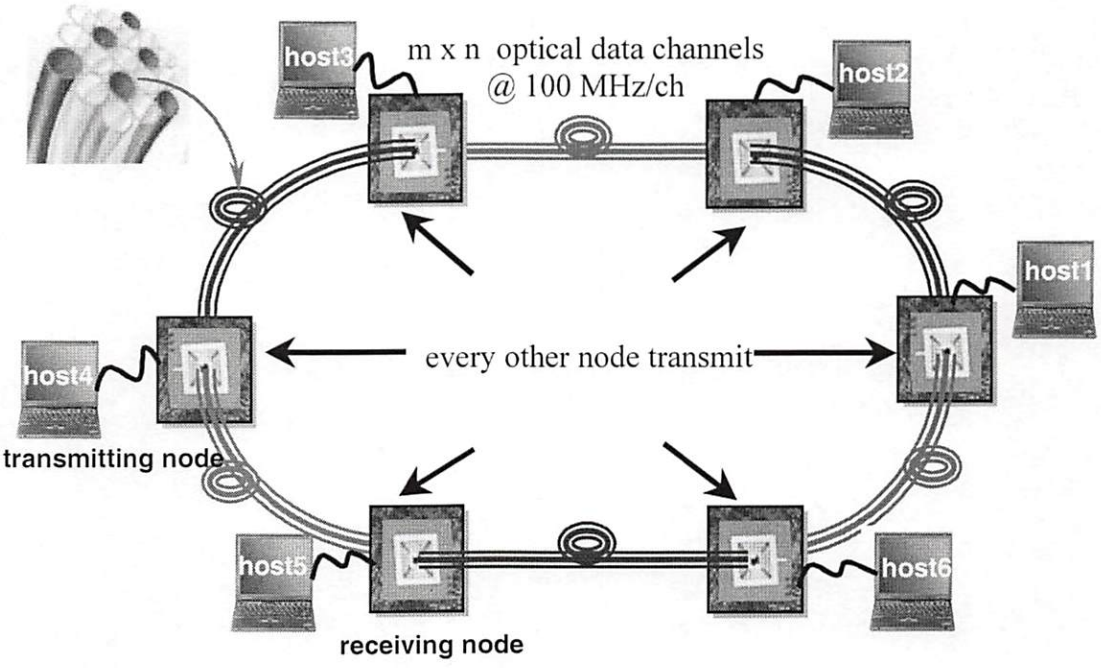


Figure 4-2. A six-node R-Transpar network under multi-token-ring protocol.

In theory, R-Transpar-MTR network can support N nodes, where N is an even number. The OPDPs sent by each node are transmitted counterclockwise and unidirectionally around the ring. In this scheme, $N/2$ nodes transmit optical packets simultaneously under control of a "ready to receive" (Ready2RX) signal from the previous node. Thus, all odd-numbered nodes and all even-numbered nodes transmit at different time slots and packets from alternate network nodes occupy the network concurrently.

As shown in Fig. 4-3, during the transfer of an OPDP, the VCSEL transmitters of a source node are synchronously linked at a fast clock rate to the receivers of the next node using the optical clock channel. This allows each node to perform high-speed data transfers between nodes having independent (and potentially varying) clock rates. The signal transfer rate between nodes operating with a data rate of 100 Mb/s on each of twelve channels is 1.2 Gb/s. Smart pixel devices with hundreds of channels and data rates exceeding 1 Gb/s on each are becoming available, so networks using the basic architecture described here have Tb/s potential throughput. Our focus will be on the demonstration of the high throughput add/drop, and time-division-multiplexing (TDM) organization of source and destination address channel.

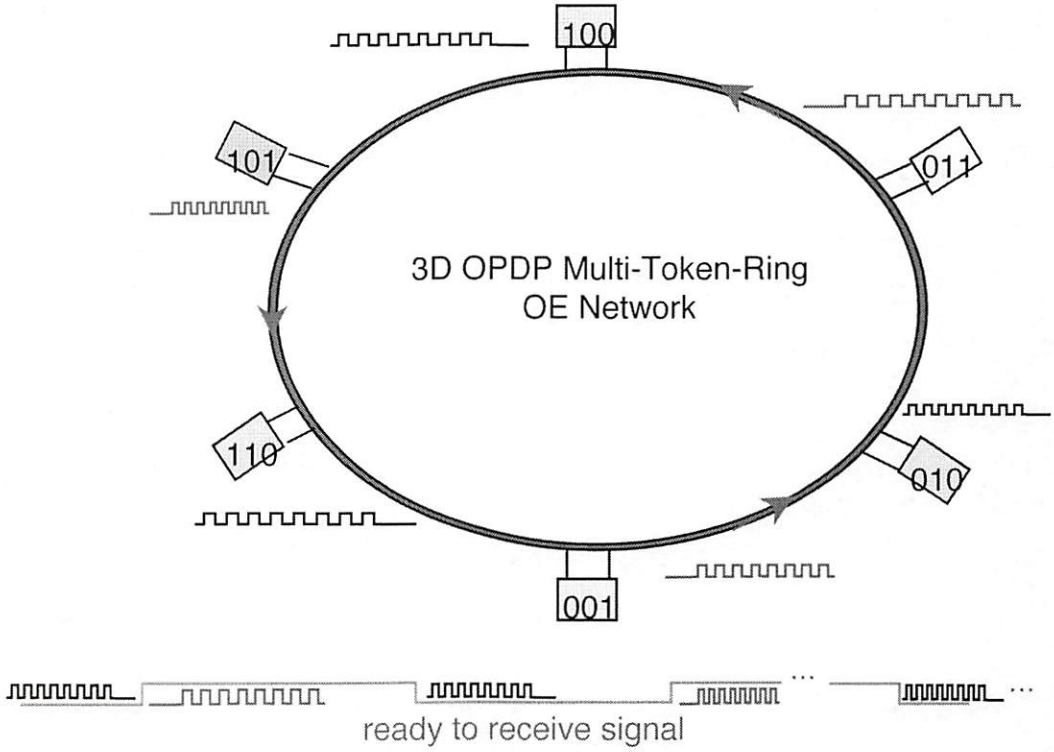


Figure 4-3. Global token control mechanism in multi-token-ring 3D OPDP switching network.

Each packet has 3x4x8-bit payload, 1x8-bit address channel, and an optical clock channel. The source and destination address bits share one channel through TDM scheme. The packet switching protocol is designed such that if the destination address of the incoming packet matches the node address, the packet takes off the network and drops into the receiving queue. The oldest packet in the transmitting queues is added to the network. If no address match occurs, the traffic-on-the-ring has higher priority to continue circulating around the ring toward the next node.

To reduce the crosstalk of the Gaussian beams, we use a global multi-token clock signal to prevent the simultaneous operation of VCSEL and MSM arrays. Data is transmitted in a single direction within the ring. In a N-node multi-token ring

network, there are N/2 tokens in the ring at any given time. Due to the parallel nature of the address and payload channels, unlike a conventional token-ring network IEEE 802.5 protocol, the 3D OPDP switching multi-token-ring network has no overhead.

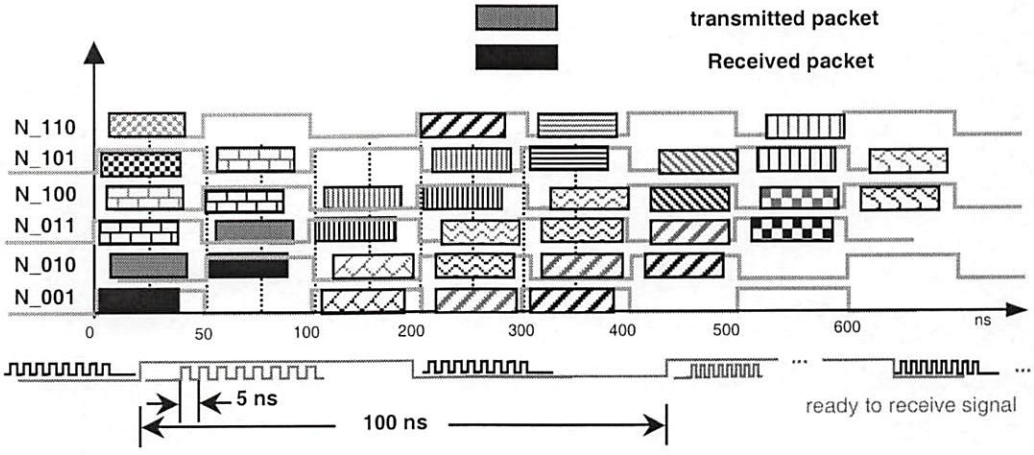


Figure 4-4. Parallel-pipelined packet switching add/drop and retransmission in MTR Network

To minimize packet loss, each node has a transmit queue and a receive queue that serve as a buffer between the very fast optical network transmission rate and the relatively low rate of the electrical smart pixel array processors. The uploading and downloading of data packets between the node and an attached host processor takes place independently and depends on network traffic. Using the R-Transpar-MTR protocol, multiple OPDP transmitted from a source node propagating through intermediate nodes in parallel, and removed by the destination node, or by the source node if its destination address does not match any node address on the ring. Alternative nodes simultaneously detect the incoming OPDP and compares its spatially encoded destination address with each of their own address, downloading on a match, and add a new packet to the ring transmitting during the empty token

time. The 3-D 4x4x8-bit OPDPs propagate over the ring in parallel pipeline as shown in Fig. 4-4.

The comparison and analysis of different protocols confirms that by exploring the third dimension, the number of payload bits is greatly increased and so is the network throughput. There are also a number of advantages of this architecture over others such as bus and star topologies as listed below.

(1) The access to the ring network is deterministic and no collisions are allowed to occur. This is in contrast to CSMA/CD protocol, which is random and contention based. Deterministic procedure is preferable, since for the heavy loads, in unfavorable circumstances, CSMA/CD cannot provide a reasonable throughput.

(2) The MTR mechanism has implemented in distributed form in each node, thus a monitor node is superfluous. The elimination of a central control node from the conventional token-ring network results in low cost and high scalability.

(3) The inherent symmetry of the slotted multi-token ring network naturally guarantees the fairness access mechanism. Furthermore, the fairness is independent with the network expansion. Again, in contrast to the Ethernet bus protocol, which has an inherent head-tail asymmetry.

(4) As the counterpart to an erbium-doped fiber amplifier (EDFA), the buffers in each node reshape the signal and stop the noise accumulating or recirculating over the ring.

A performance analysis has been performed in (network simulator) NS software and matlab program. The comparison of maximum throughput in IEEE 802.3, 802.4 and R-Transpar-MTR protocols is shown in Fig. 4-5. As we can see from the result, multi-token-ring protocol can handle Gigabit per second throughput easily. Assuming the transmitting queues always have packet to transmit and receiving queues are always not full, the network can handle 10 Gbps nicely.

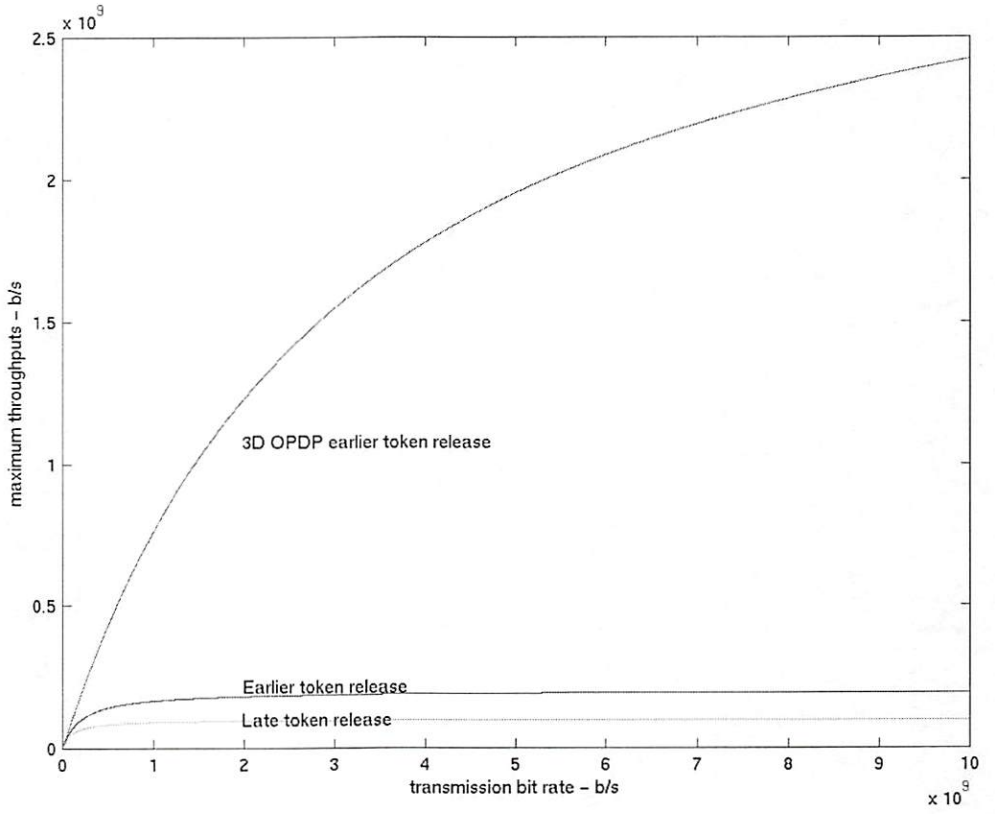


Figure 4-5. Performance comparison of 802.3, 802.4 and R-Transpar-MTR protocols.

Header error control (HEC) channel and hardware will be designed for error detection and correction to be a feasible network system. The multi-token-ring network is a unidirectional ring, and its average latency is half of the round-trip duration. Extra hardware may be needed for self-healing or bypass if a node failure

occurs. Dual-ring multi-token-ring architecture extensions can alleviate or resolve both issues. The network platform we designed to perform networking function is reconfigurable, thus other novel OPDP switching protocols (such as those based on ATM, SONET, or IP over DWDM) can be dynamically reconfigured depending on packet type, traffic level, and other parameters in real-time.

4.3 Design and Implementation of the Multi-Token-Ring Protocol Network with R-TRANSPAR

In Multi-Token-Ring network, VCSEL array in alternative neighboring network nodes (N/2 total) active concurrently, thus, crosstalk between VCSELs and MSM detectors on the same node is eliminated. In this scheme, each node waits for a "ready to receive" signal from the previous node before transmitting an optical packet. In contrast to the CSMA/CD protocol, packets are received, buffered and retransmitted at each node as they traverse the network. A transmitting queue and a receiving queue serve as FIFO buffer between the ultra fast optical networks and relatively low speed of the electrical smart pixel array processors to minimize packet loss. Due to the *parallel* transmission of address and data packets, the processing latency is greatly reduced compared with IEEE802.5 token-ring networks.

Figure 4-6 and 4-7 shows the multi-token-ring network node without and with queuing. The dashed paths are optical paths that show detected signals from the MSM detectors, and transmitted signals to VCSELs. There are 3x4 pixel array with network interface and signal processing functions, one intelligent address pixel for add/drop, and one optical clock for packet synchronization. The pixel element finite state machine is responsible for the SIMD signal processing. The network interface

controller (NIC) implemented the 3D OPDP switching multi-token-ring network protocol, and it allows each node to run at different frequencies that independent to each other.

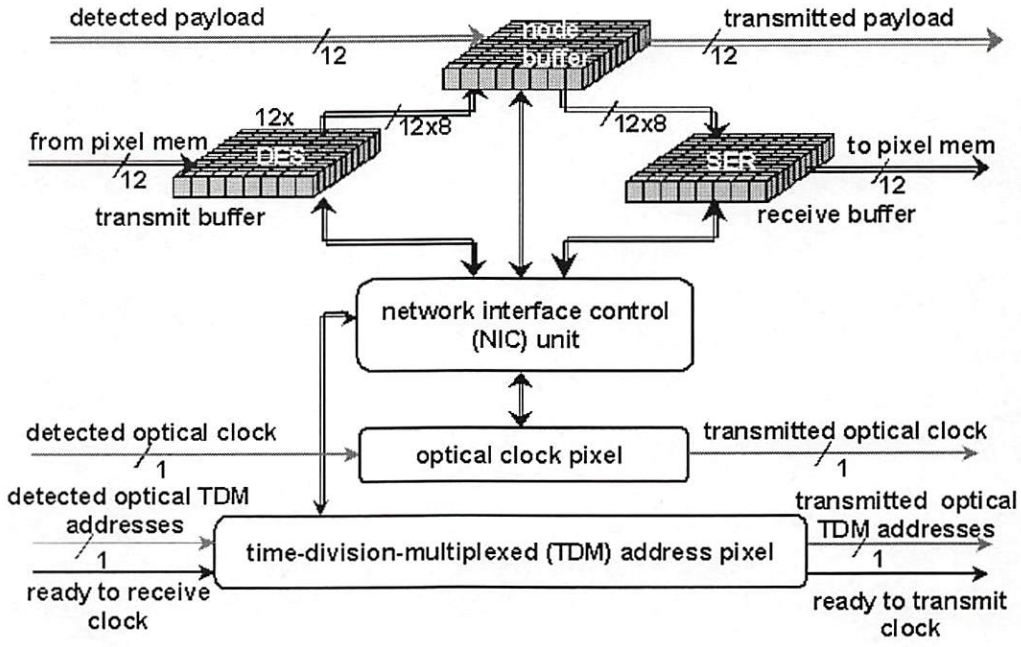


Figure 4-6. Block diagram of R-TRANSPAR-MTR network node without queuing.

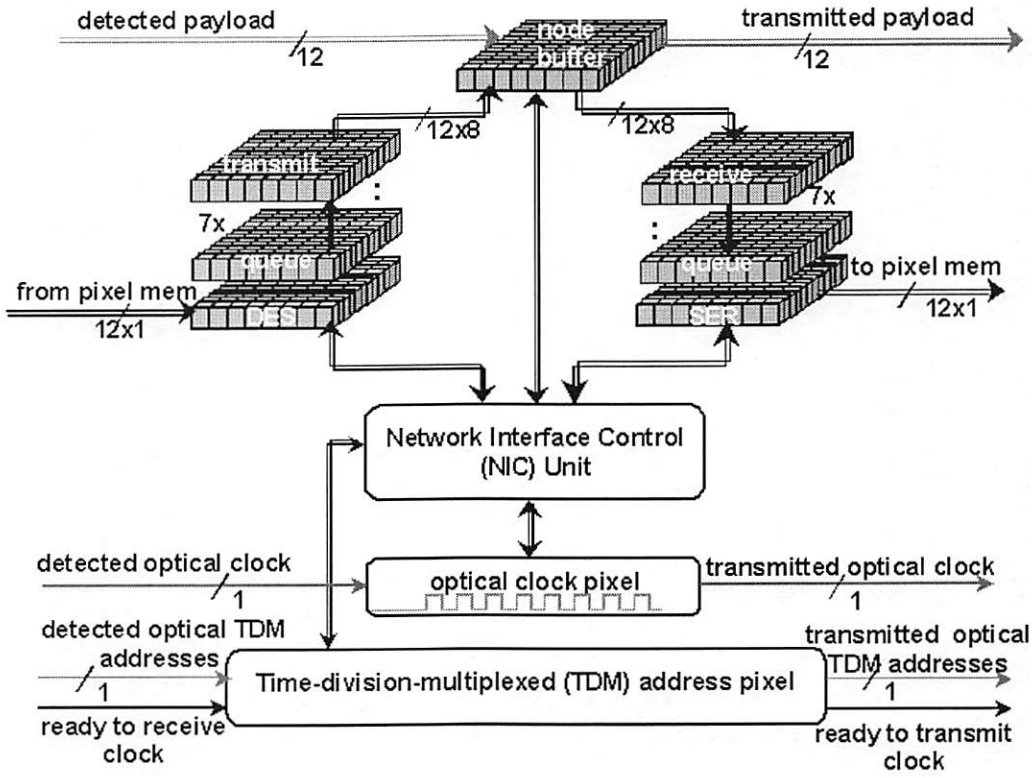


Figure 4-7. Block diagram of R-TRANSPAR-MTR network node with queuing.

Incoming packets are detected at each pixel by the MSM detector and loaded into node buffer during ready to receive signal low. The NIC checks the source and destination address right after the 6^{th} address-bit reach the buffer. Packet drop upon address match, in the mean while, a new packet is uploaded into the node buffer from the transmitting queue. Otherwise, nothing occurs until the ready to receive signal goes high, and the packet in the node buffer transmits to the next node. Attached electronic host processors (not shown) move the packets to the transmitting buffer or from the receiving buffer whenever ALU is idle. Each pixel has an ALU, local memory, registers, and electrical cellular logic mesh connections to the four nearest north-east-west-south (NEWS) neighbor pixels as needed for parallel

pipeline processing applications. The address pixel processes time-division multiplexed (TDM) source/destination addresses formatted to accommodate up to sixteen nodes. Other functional blocks include pad-multiplexing, internal clock generation, a pixel element (PE) finite state machine, and two test PEs with a pseudo-random bit stream generator. The PE finite state machine provides the interface between the low speed host macro-commands and the high-speed on-chip micro-operations. It also monitors the status of the network queues while moving data among those queues and local memory.

4.4 Demonstration of Multi-Token-Ring Network

Each R-TRANSPAR-MTR node is connected to a dedicated personal computer host via the PCI bus using a high-speed digital I/O board. The macro commands of the host computer send or receive signals from the R-TRANSPAR network node. Figure 4-8 shows one of the test results of two R-TRANSPAR nodes network performed by one of my colleagues. Over the top are the Ready to Receive signal for node 1 (Ready2Rx1) and its complement (Ready2Rx2') for node 2. The top set of receive-transmit labels refers to node 1 and the bottom to node 2. Here the time interval for receive and transmit is 400 ns. When the Ready2Rx1 is high, node 1 receives incoming data (Rxd Data 1) and address data (Rxd Address 1) at the clock rate transmitted by the previous node (Rxd Clock 1). In the first 400 ns period shown, there is no address match, so at the next available transmit interval, node 1 retransmits the data and address to node 2 at its own local clock rate. In this example, as before, there is no address match at node 2 so it again retransmits the data and address at its own local clock rate to the next node.

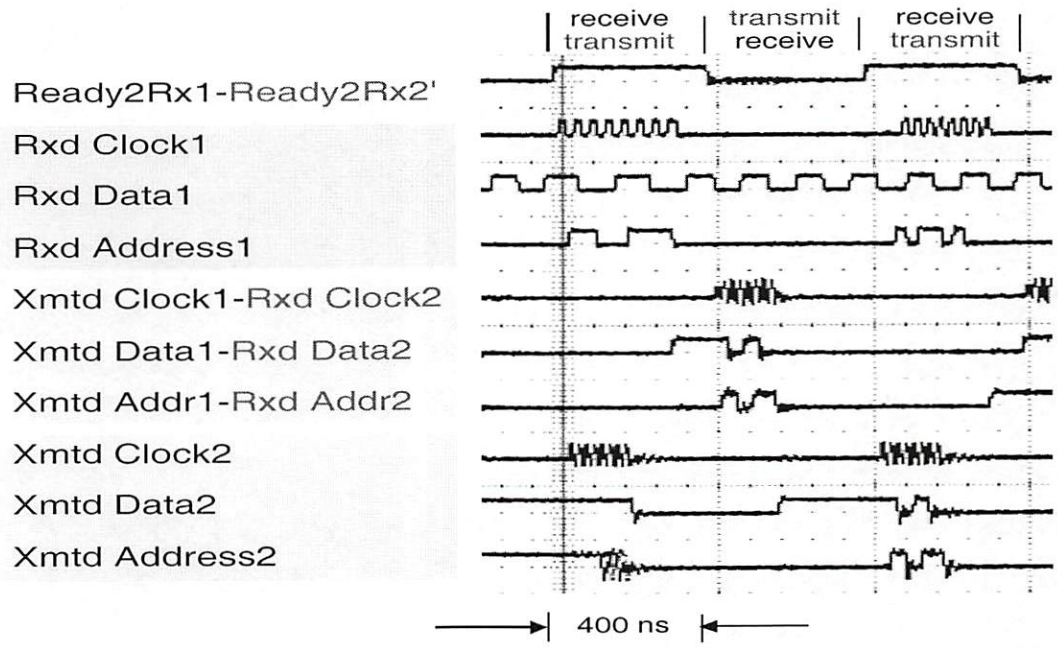


Figure 4-8. Measured results of a two-node R-TRANSPAR multi-token-ring network.

In order to test the multi-token-ring network and parallel pipeline signal processing functions, we have developed software driver interfaces to provide networking functions for the host computer. Algorithms are written using these interface drivers to upload and download packets for various network protocols and parallel pipeline signal processing using several nodes simultaneously for computation.

CHAPTER 5 ULTRA-THIN SILICON-ON-SAPPHIRE (UTSI-SOS) CMOS SILICON ON INSULATOR (SOI) TECHNOLOGY

Next generation computers and servers will have on-chip clock frequencies well in excess of 1 GHz. Maximum overall system performance can only be obtained if the off-chip interconnections have data rates corresponding to the on-chip clock rate. Forecasts for the projected 50 *nm* CMOS process in 2011 predict on-chip clock rates of 10 GHz (as shown in Table 2-1) which poses great challenges for GHz chip inputs and outputs after packaging. Ultra-high speed performance demands low noise, high gain-bandwidth, low-power transceivers and the use of optical interconnections for chip-to-chip communications. The need to integrate these devices monolithically and to operate at these high frequencies has motivated the exploration of new material and semiconductor technologies. Among them, CMOS SOI is one of the most promising technologies in place of conventional silicon CMOS. There has been research on several CMOS SOI technologies including FIPOS (Full Isolation by POrous Silicon); SIMOX (Separation by IMplanted OXygen); SIMNI (Separation by IMplanted NItrogen); SIMON (Separation by IMplanted Oxygen and Nitrogen); etc. However, the successful ones do not exists until recently, including Peregrine Semiconductor CMOS Ultra-Thin Silicon on Sapphire (UTSi-SOS) [Peregrine], Intel TeraHz CMOS SOI invented in 2001[Intel_01], and IBM SiGe BiCMOS [IBM].

Several groups are investigating silicon-on-insulator (SOI) optoelectronic interconnects. We are using this technology to design and fabricate circuits for

wireless and optical communications. Silicon-on-sapphire (SOS) technology is a member of the SOI family in which sapphire (α-Al_2O_3) is the insulator and substrate. A recent advancement in SOS technology has been made by Peregrine Semiconductor Corp. and their SOS is called Ultra-Thin-Silicon on Sapphire (UTSi®). In this CMOS SOI process, 100-nm silicon is grown on top of a full insulating substrate - synthetic sapphire (Al_2O_3). The UTSi process is not only compatible with standard CMOS process but also has three fewer mask steps. Several groups are investigating Ultra-Thin Silicon (UTSi) and other SOI technologies for radio frequency wireless and satellite communications, and photonic interconnects.

UTSi has the unique ability to integrate high-frequency digital, mixed-signal, and RF devices on a single substrate with maximum insulation between them. It also can implement excellent passive components. The synthetic sapphire substrate is optically transparent and a good heat conductor whose thermal coefficient of expansion closely matches that of GaAs optical devices such as VCSELs and photodetectors. These properties make UTSi an excellent candidate for monolithic OEIC integration. UTSi devices also exhibit other high performance characteristics such as radiation hardness, deep-submicron and high-temprature devices. UTSi-SOS is the most mature process among all heteroepitaxial SOI technologies up to date, and one of the most preferred technologies to fabricate high performance wireless, satellite and optical communication ICs.

As shown in Fig. 5-1, SOI CMOS MOSFETs are much less complicated than bulk CMOS, which typically use an epitaxial substrate, n-well, or twin wells. In the thin-film SOI process, there is no need to create diffused wells, deep implants (such as an anti-punchthrough implant for p-channel devices and back-channel leakage suppression implant for n-channel devices) are unnecessary, and the entire impurity profile in the channel is determined by the shallow implant. As a result, the gate consists of polysilicon, where p-type impurities (boron) are used to control the threshold voltage in both the n-channel and the p-channel SOS devices.

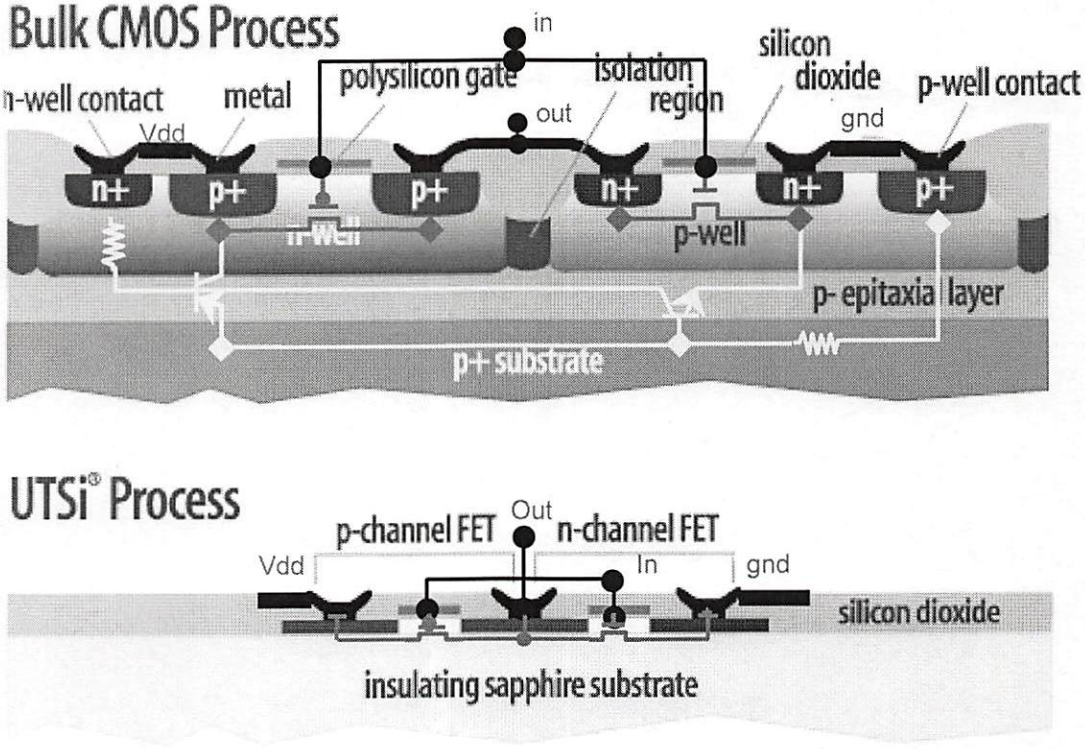


Figure 5-1. Cross-section of bulk silicon CMOS and UTSi-SOS MOSFETs.

The UTSi MOSFET has no wells, well contacts, or pnpn thyristor latchup effects, along with reduced capacitances, resistance and inductance due to the shortened-interconnect distance and full insulation between transistors. All these

factors contribute to the excellent speed performance observed in UTSi-SOS CMOS circuits. In UTSi-SOS process, ultra-thin (100nm) silicon is deposited on an insulating synthetic sapphire wafer, which is the key to many of its advantages. First, the insulating substrate material synthetic sapphire in UTSi-SOS CMOS effectively eliminates the substrate parasitics that exists in standard bulk CMOS. Second, sapphire is electrically non-conducting and does not absorb, attenuate, distort or combine RF signals. Additionally, the UTSi CMOS fabrication process eliminates the need for transistor isolation wells, significantly reducing process complexity. The thin-film SOS technology is ideal for low-noise, high-bandwidth, and low-power device [Johnson_95], which meets the requirements of communication ICs. Below is a complete list of UTSi-SOS advantages [Peregrine]:

- No latch-up due to the isolated substrate
- Low power consumption, compact physical shape, high speed
- Reduced parasitic capacitance and inductance compared with bulk silicon CMOS
- Lower standby leakage current than bulk silicon device (with the same threshold voltage)
- Radiation hardness, high soft-error immunity for space applications
- Multi-threshold transistors
- High-Q inductor and capacitor
- Higher transconductance

- Excellent short-channel behavior
- Quasi-ideal Sharper subthrethold slope
- Lower electric fields
- High temperature circuits
- Fewer mask than bulk CMOS process
- Low-voltage (1V-3V) and low-power consumption
- Smaller parasitic capacitance compared with bulk silicon CMOS
- Lower standby leakage current than bulk silicon device (same threshold voltage)
- Radiation hardness (higher than 300 kRad) for space applications
- Soft error rate lower that 10^{-11} error/bit-day

For standard CMOS logic, the standby power can be negligible, while the dynamic power consumption is given by

$$P = CV^2 f \tag{5-1}$$

where V is the supply voltage, f is the frequency of operation, and C is the logic gate capacitance and wire capacitance. Smaller feature sizes and compact design in UTSi means lower C and lower V, thus higher speed and lower power advantages over conventional bulk CMOS. Low power operation is critical to dense smart pixel optoelectronic interconnections, where heat dissipation is a critical issue.

The sapphire insulator is transparent at 850 nm for VCSEL light to propagate through, and its thermal coefficient of expansion matches that of solder balls, which is ideal for flip-chip bonding VCSEL or MSM photo detectors. p-i-n photodetector array (in GaAs or InGaAs technology) can be connected to the UTSi CMOS receiver arrays through either wire bonding or solder bump flip-chip bonding techniques to form ultra-high throughput multi-channel memory I/O or chip-to-chip interconnections.

This chapter describes the potential benefits and challenges of SOI, and realization of UTSi. We also describe theoretical analysis and design methodologies for UTSi circuits. The eventual goal is to develop flip-chip optical transceiver and monolithic optical receivers by exploring UTSi's capability of monolithic integration of high-speed digital, analog, mixed-signal, RF, and OEIC devices. In the following chapters, we describe UTSi chip designs including smart TDM switch, flip-chip OEICs, and monolithic optical receivers in the 2000 and 2001 COOP-Peregrine UTSi foundry runs, respectively.

5.1 Why Low Power, Low Voltage, and High-Speed?

Power consumption becomes an important figure of merit especially with the performance increase exceeding the limit of power dissipation and the advent of portable wireless communication systems. To reduce the weight and extend the lifetime of the batteries inside systems such as laptops, notebooks and cellphones, low power consumption is absolutely essential. Advances of semiconductor technology and demanding applications have cause a steady increase in speed and

chip size that demands increased overall power consumption and power consumption per unit chip area. This is most prominent in high-bandwidth systems and high performance microprocessors.

Among all low power design techniques, lowing the supply voltage is the most effective approach, especially when combined with other techniques such as multi-threshold logic and current mode logic (CML), etc. Furthermore, device scaling for high-speed and high density requires low voltage operation to avoid breakdown. Whenever the power supply is lowered, V_{gs}-V_{th} also drops. The drain current is a function of I_{dsat} proportional to $(V_{gs}-V_{th})^{\gamma}$, where the value of gamma is between 1 and 2. The propagation delay of the circuit is a function proportional to $C_L*\Delta V/I_{dsat}$, and is inversely proportional to $(V_{gs}-V_{th})^{\gamma}$. When the power supply voltage is lowered, the propagation delay increases. Although the threshold voltage can be scaled down to shrink the propagation delay, an increase in the subthreshold leakage also causes a rise in power dissipation. The voltage bounce $(\Delta V \sim L*dI/dt)$ due to the change in the supply current (dI/dt) on the supply line may further limit stability and performance of low-voltage operation.

CMOS technology has advantages over bipolar, BiCMOS, GaAs technologies in power consumption, noise margins, density, and large-scale integration. The reason why CMOS devices have more compact area is that CMOS devices of the same type can be grown into the same well and thus the distance between devices are very short.

In CMOS logic circuits, power is dissipated whenever the load capacitance is charged or discharged, therefore, power dissipation is proportional to frequency as described in Eq. (5-1). On the other hand, differential bipolar circuits always consume the same amount of power, regardless of the operating speed. CML logic in the CMOS process is very similar to bipolar - its power dissipation is independent of frequency. However, CMOS logic consumes less power for small switching duty factors of 0.1 or less.

5.2 Why Monolithic Integration?

The performance of a system at a particular speed is proportional to the degree of integration. Passive devices such as inductors are the major obstacles to monolithic integration in communication ICs due to the significant process parasitics at RF frequencies. Portable, low-power, and high-speed requirements of handheld or portable devices pose the most challenges for integration. While optical fiber communications have been widely exploited in both long haul and short interconnect systems, one of the key issues in optoelectronics system is the integration and packaging of photodiodes and laser diode with transimpedance amplifiers receiver and transconductance laser driver amplifiers, respectively. Towards the final goal of monolithic integration, there are intermediate steps such as a modular approach; wire-bonding; and flip-chip bonding. The modular system approach has highest parasitics and the lowest bandwidth. In wire bonding, the inductance of the bonding wire and the capacitance plus resistance of the bonding wire and bonding pads degrade the performance. Flip-chip bonding has been widely used, however when the thermal coefficients of the two device materials do not match, the relative stress

between the bonded devices and the substrate may cause the bonds to fail. Monolithic integration provides the ultimate intrinsic integration and thus the best performance.

5.3 Why CMOS SOI?

Although most types of devices (such as bipolar, BiCMOS, etc.) can be fabricated in SOI films, the trend for the SOI technology is undoubtedly in mainstream CMOS. As transistor sizes continue to shrink, it will be difficult for bipolar or BiCMOS to be properly biased due to the low supply voltage required. Bipolar or BiCMOS processes should not be used until clearly there are some good reason and particular significant advantages over CMOS.

SOI technology has existed for 30 years. One of the barriers to the development of SOI is the continuous shrinking of the minimum transistor feature size, and the steady performance increase in bulk CMOS process predicted by Moore's Law. However, as minimum gate lengths approach the nano-meter range, the parasitics and short channel effects becomes dominant and overwhelming. New technologies and processes that can overcome those problems are essential. Figure 5-2 shows the past and predicted relative performance of SOI and bulk CMOS technology over a 25-year period [IBM]. From this figure, SOI exhibits a performance advantages over bulk CMOS. The performance advantage is due to the disappearance of junction capacitance and body effects. In addition, the Peregrine UTSi process has two unique abilities, i.e. monolithic integration of RF devices and

flip-chip bonding of optical devices due to the full insulating optically transparent substrate.

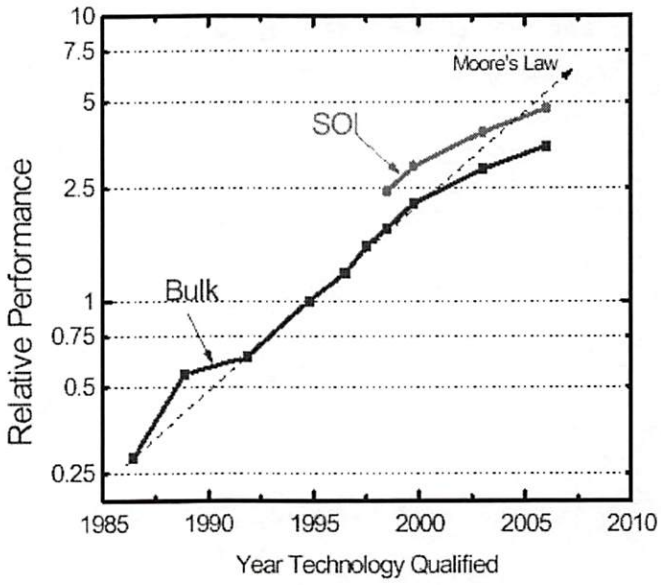


Figure 5-2. Moore's Chart: the relative performance of SOI and Bulk CMOS [IBM].

5.4 Comparison of Thick, Thin -Film SOI Technologies

While SOI has existed for 30 years, there are two major challenges, i.e. to make a defect-free SOI layer and to overcome the single-transistor latch-up phenomenon that we will describe in detail. UTSi has made progress in both areas by finding techniques to grow ultra-thin silicon on an insulating defect-free synthetic sapphire (Al_2O_3) substrate. The use of ultra-thin oxide enables fully depleted devices, and full-depletion contributes to the reduced single-transistor latchup effects which can be further eliminated if the body is grounded.

The cross section of a thick-film SOI MOSFET (shown in Fig. 5-3 (a)) inherently exhibits a parasitic bipolar transistor as shown in Fig. 5-3 (b) and results in an effect known as single-transistor latch up. As they form an N-MOSFET, the

N+ source, drain, and the P-type body also form the emitter, the collector and the base of an NPN bipolar transistor. This NPN transistor is inactive in bulk MOSFET devices since the base (body) is always grounded through well contact. However, as we mentioned before, SOI devices do not have wells or well contacts, and the base of the bipolar transistor is typically left floating with some accumulation potential. The active bipolar transistor introduces side effects. In some cases, it can amplify the base current (the minority current generated by impact ionization near the drain) by β, as a positive feedback to the drain current, and cause anomalous subthreshold slope [Colinge_97]. The other undesirable effect is the reduced drain breakdown voltage, unless the base is grounded according to bipolar transistor theory.

Figure 5-3. (a) Cross-section of a thick-film SOI N-MOSFET, (b) equivalent circuit of a thick-film SOI CMOS MOSFET.

In thin-film SOI devices, such as UTSi-SOS MOSFETs, the oxide layer is thin and the device can be fully depleted as shown in Fig. 5-4 (a). If there is no back accumulation, the parasitic bipolar transistor is inactive as shown in Fig. 5-4 (b).

(a) (b)

Figure 5-4. (a) Cross-section of a thin-film SOI N-MOSFET and (b) equivalent circuit of a thin-film SOI CMOS MOSFET.

One thing to notice is that when the MOSFET is turned off, there is no channel current and thus no parasitic bipolar effects. For both thick- and thin-film devices, the single-transistor latchup phenomenon only occurs when the transistor is turned on, and the weak inversion current can induce impact ionization near the drain.

5.5 Fabrication Process of SOI and Doping Profile

UTSi-SOS is compatible with the standard bulk CMOS process, and has three fewer mask steps. The process comparison of a typical SOI with bulk CMOS is summarized in table 5-1 [1.2].

Like standard CMOS circuits, SOI circuits are also fabricated on a silicon layer except the layer is very thin. For example, UTSi silicon layer is about 100 nm. The silicon layer is doped with either donor atoms (such as 5-valence electron phosphorus for an n-type wafer) or acceptor atoms (such as 3-valence electron boron for a p-type wafer). In the UTSi-SOS process, a p-type silicon layer is used on top of the insulating sapphire wafer.

CONVENTIONAL BULK CMOS	UTSI SOS PROCCESSING
1. Oxidation	1. Oxidation
2. Well lithography, well doping and drive-in	
3. Nitride deposition, active area lithography. Field implant lithography, Field implant, Field oxide growth, Nitride strip	2. Nitride deposition, active area lithography
4. P-channel lithography, anti-punchthrough implant	
5. Gate oxide growth, p-channel Vth implant, n-channel Vth lithography.	3. Gate oxide growth, p-channel Vth implant, n-channel Vth lithography and n-channel Vth implant.
6. Anti-punchthrough implant, n-channel Vth implant.	
7. Poly deposition and doping, gate lithography and etching, p+ S&D lithography, p+ S&D implant, N+ S&D lithography, N+ S&D implant, S&D reoxidation, dielectric deposition.	4. Poly deposition and doping, gate lithography and etching, p+ S&D lithography, p+ S&D implant, N+ S&D lithography, N+ S&D implant, S&D reoxidation, dielectric deposition.
8. Contact hole lithography, contact hole opening.	5. Contact hole lithography, contact hole opening.
9. Metallization, metal lithogrphy, metal patterning, sintering.	6. Metallization, metal lithogrphy, metal patterning, sintering.

Table 5-1. Comparison of the standard bulk CMOS and UTSi-SOS process.

5.6 Delay and Power Consumption of SOI Devices

A key advantage of SOI is the high-speed possible due to the reduced source and drain capacitance and compact intra-cell connections. The SOI process also results in increased transconductance in the case of fully depleted devices (such as IN-IP). In later sections, we show how an optimized 3-stage ring oscillator in the 0.5 μm CMOS UTSi SOS process has a speed improvement by a factor of two over its

bulk CMOS counterpart. In the same process, a well-designed high-speed dynamic true-single-phase-clock DFF can directly interface with the 2.5 GHz output of the VCO.

Aside from the increased speed, SOI technology can reduce standby and switching power dissipation. The lower standby power dissipation is due to the reduced area of the reach-through SOI source and drain junctions, and the reduced switching power consumption is due to reduced threshold voltage, low source/drain capacitance, and low voltage operations. In both SOI and bulk CMOS, it is well known that the power consumption of a complementary MOS circuit is proportional to its operating frequency. For circuits operating at multi-GHz, current mode logic is a better choice because its power consumption is independent of operating frequency.

The most effective way to reduce power dissipation is to operate at a lower voltage, and in fact, low voltage is required as the minimum transistor feature sizes continue shrinking. Low power dissipation is particularly important at high frequency for CMOS logic, where dynamic power dissipation is dominant and is proportional to the square of supply voltage, stray capacitance and frequency. However, reducing the power supply voltage not only poses great challenges in analog circuit design but also causes speed performance drops. In CMOS circuits, the output drivability of MOSFET will be weaker, the voltage or current swing will be smaller, threshold voltage variations will be more prominent, and the gate delay

will be more serious. When the threshold voltage approaches Vdd/2, gate delays will increase rapidly.

One solution to lowering the power supply voltage while overcoming the above problems is to lower the threshold voltage. Multi-threshold voltage transistors in UTSi technology have been developed under these considerations. Dynamic threshold voltages are accomplished by controlling the amount of boron doped into the gate oxide. A low-threshold voltage is desired to compensate for the performance drop due to lower power supply voltage, and to shorten the gate delay significantly. However, on the other hand, it increases the cutoff current, decreases the on/off ratio, and increases the transient switching current, hence increases switching power dissipation. Thus a better trade-off, and optimized Vth/Vdd value is significant for both low power and high-speed operation in UTSi-SOI circuit design.

5.7 ESD Protection

The electrostatic discharge (ESD) phenomenon occurs whenever a charged body or object discharges into integrated circuits. ESD has resulted the discovery of electricity, as described in Benjamin Franklin's kite experiment [Gale_94] and the development of wireless communications, where Hertz used two ESD gaps as the transmitter and the receiver, respectively [Lee_96]. However, for semiconductor devices, ESD protection is extremely important because it exists everywhere and can destroy a poorly protected circuit. As the continuing decrease of channel length, ESD protection circuit designs become more challenging [Luh_00].

The trend of VLSI chip size is to double every 18 months. As the chip size increases, the number of I/O pins increase exponentially. The required number of I/Os can be estimated based on the number of gates in the chip using Rent's rule, which is empirically derived as

$$N_p = k \cdot N_{gates}^{\beta} \tag{5-2}$$

where N_p is the number of I/O pins, k is a constant based on the type of circuit (logic, memory, etc.), N_{gates} is the number of gates, and β is an exponential factor depends on the circuit. Equation (5-2) states that the I/O and power pin counts on chip will increase dramatically as the chip size increases. ESD protection is crucial especially when the chip has larger pin count for I/O and power [Dabral_98].

The I/O pads, particularly the input pads of MOS circuits, have to be well protected against ESD. The reason is that the input impedance of a MOSFET is capacitive, and small amounts of external charge placed on a bonding pad connecting to a gate could cause the gate oxide of the MOSFET to break down. ESD pulses as high as 2000 volts can be generated by the resistance and capacitance of the human body [HBM_93]. The ESD stress is not only able to destroy the I/O peripheral devices but also the delicate internal logic circuits [Duvvury_88]. N-MOSFETs, inverters, clock buffers are prone to be damaged mainly caused by NPN and PNPN snapbacks, and PNPN latchup, respectively. These can be solved by increasing source and drain spacing and increasing clock buffer sizes, etc. Oxide layers in decoupling capacitors based on active devices are easily damaged. In SOI circuits,

metal-insulator-metal (MIM) or (metal-metal-metal) MMM capacitors are preferred to avoid ESD stress.

The snapback characteristic of an NMOS device in which the gate is grounded and the drain is connected to the input pad is shown in Fig. 5-5 (b). During snapback, the channel resistance has a positive temperature coefficient. The current increase causes the corresponding region to heat up as resistance increasing even further, which allows current to flow elsewhere. Right after the first snapback, the drain current instantly flows into the device and drain voltage drops to a hold value. If the drain voltage is further increased, a second snapback will occur. With the onset of the second snapback, the resistance of the current path has a negative temperature coefficient. The snapback Ids-Vds characteristics of an N-MOSFET can be utilized to clamp ESD pulses, therefore the diode connected N-MOSFET in Fig. 5-6 (b) can be used as ESD protection.

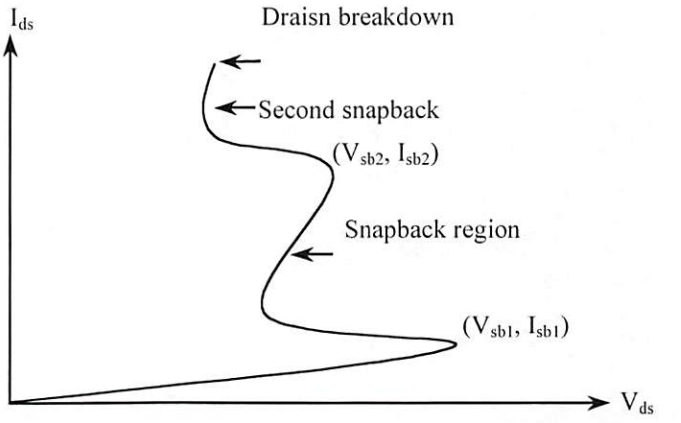


Figure 5-5. A typical NMOS snapback characteristics.

Because the snapback current is linearly proportional to the device width, ESD MOSFETs or diodes are usually very large. A double diode ESD protection

configuration is shown in Fig. 5-6 (a). These schemes rely on a diode becoming forward biased and providing a low-impedance path to pull the excessive charge away from the gate either to the power or the ground. The N-MOSFET scheme uses the n+ as a resistor to limit the current through the pad and the NG diode to protect against negative transients and the breakdown voltage of the diode to protect against positive transients. The double diode scheme uses a PG/NG diode pair connected to VDD/GND to protect against positive/negative transients. To effectively prevent ESD from occurring, either a double diode strategy as shown in Fig. 5-6 (a) or an NMOSFET as shown in Fig. 5-6 (b), or the combination of both can be used. Preferably, a combination of both schemes is used together with good power and ground buses to provide a low-impedance path to discharge the unwanted electrostatic charge.

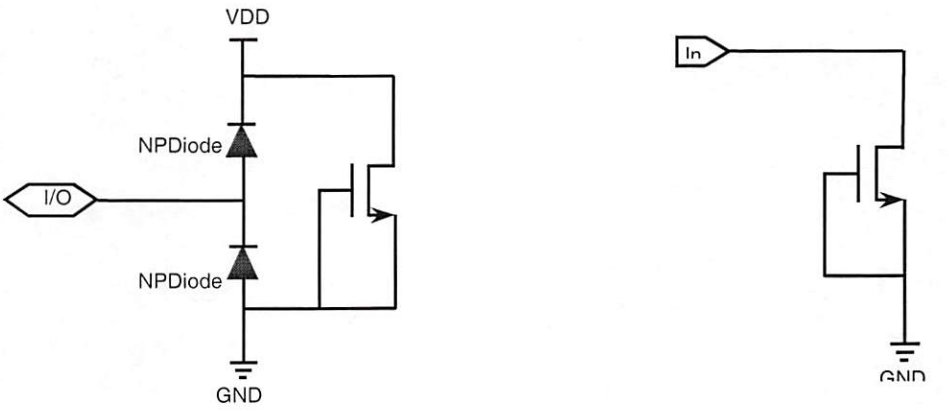


Figure 5-6. (a) Double ESD diode protection, (b) N-MOSFET ESD protection.

CHAPTER 6 RADIO FREQUENCY SOI ACTIVE, PASSIVE, AND OPTOELECTRONIC DEVICES

This chapter presents the modeling of CMOS SOI active devices, passive devices, and optoelectronic devices. Comparisons of active and passive devices with their counterparts in bulk CMOS process are also given. As these devices continuous to shrink observing Moore's law, accurate modeling and performance prediction is essential for optimized designs of ASICs, VLSI, ULSI, RFICs, and OEICs. Precise models are critical to designing fabricatable high-performance CMOS SOI circuits that are competitive to other processes such as GaAs bipolar or SiGe BiCMOS.

6.1 SOI Active Devices - MOSFETs

0.5 μm UTSi MOSFET has cut-off frequency f_T > 50 GHz and offer potentially high frequency operation due to the greatly reduced parasitics and very short interconnects over the fully insulating sapphire substrate. The UTSi process also allows low (0.3-V) or even zero threshold voltages [UTSi_1.8] thus enable low voltage and low power consumption circuits if properly designed.

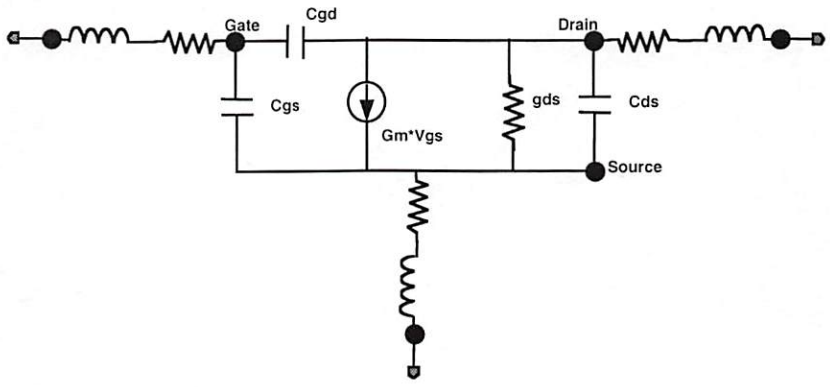


Figure 6-1. RF small signal model for an SOI MOSFET.

Figure 6-1 shows the small signal RF model of an SOI MOSFET with no source-bulk capacitance, drain-bulk capacitance, or body effects.

6.1.1 Threshold Voltage

The threshold voltage of a MOSFET is defined as the gate-source voltage at which the surface potential Φ_s is equal to $2|\Phi_f|$. For enhancement-type transistors, the threshold voltage of the NMOS is positive and the threshold for PMOS is negative. The polarity of the threshold voltage is reversed in case of depletion-type transistors.

The threshold voltage of an enhancement bulk N-MOSFET is classically given by:

$$V_{th} = V_{FB} + 2\Phi_F + \frac{qN_a X_{d\max}}{C_{ox}} \tag{6-1}$$

where V_{FB} is the flatband voltage, equal to Φ_{MS} - Q_{ox}/C_{ox} (ignoring the fast surface states, N_{it}), Φ_F is the Fermi potential, equal to $kT/q*ln(N_a/n_i)$, and X_{dmax} is the maximum depletion width,

$$X_{d\max} = \sqrt{\frac{4\varepsilon_{si} \cdot \Phi_F}{q \cdot N_a}} \tag{6-2}$$

In case of a thick-film SOI MOSFET, ($t_{si} > 2\ X_{dmax}$), there is no interaction between the front and back depletion zones and the threshold voltage equation is the same as for bulk CMOS.

The threshold of a fully depleted, thin-film enhancement n-channel SOI transistor, can be obtained by solving the Poisson equation,

$$d^2\Phi/dx^2 = qN_a/\varepsilon_{si}, \tag{6-3}$$

This is the case when the thickness of the accumulation or inversion layers is small relative to the silicon film thickness. However, in ultra-thin (t_{ox} = 10.5 nm) silicon where the device is fully depleted, complicated interactions occur between the front inversion channel and the body accumulation layer, and all these effects have to be taken into consideration. Furthermore, the amount of depletion implant varies the threshold voltage.

6.1.2 Short-Channel Effects

The short channel effect refers to the roll-off of threshold voltage caused by the reduction of depletion charge due to source and drain encroachment. This is very significant in bulk CMOS transistors. In a short channel device, the lower base of the trapezoid cross section as in Fig 5-3 (a) is significantly shorter and can even disappear.

In a thin-film SOI device, the silicon film is much thinner, and the trapezoid cross section can be retained rather than growing into a triangle shape as in bulk silicon MOSFET. Thus short channel effects in SOI device occur at much smaller minimum gate lengths. By inspection, we can predict that short channel effects can be effectively minimized by exploiting double-gate four terminal devices, where one gate sits above the silicon film, while the other sits below it.

6.1.3 Gm and Gm-I Characteristics

By definition, the transconductance is the ratio of drain current to the gate voltage and represents the controllability of the gate voltage over drain current. The g_m of a bulk NMOS in saturation ($V_{DS}>V_{dsat}$) can be given by:

$$g_m = dI_{Dsat}/dV_G = \frac{W}{L}\mu_n C_{ox}(V_G - V_{th}) + 4\Phi_F\left(\frac{C_D}{C_{ox}}\right)^2\left(1-\sqrt{1+\left(\frac{C_{ox}}{C_{dep}}\right)^2\frac{V_G - V_{FB}}{2\Phi_F}}\right) \tag{6-4}$$

where $C_D = \varepsilon_{si}/X_{dmax}$ [Grove_67] and I_{dsat} can be approximated by

$$I_{dsat} \approx \frac{W\mu_n C_{ox1}}{2L(1+\alpha)}(V_{G1} - V_{th})^2, \quad where, \alpha = \frac{\varepsilon_{si}}{X_{d\max} C_{ox}} \tag{6-5}$$

The transconductance g_m of a thin-film, fully depleted SOI MOSFET can be written as

$$g_m = dI_{dsat}/dV_{G1} = \frac{W\mu_n C_{ox1}}{L(1+\alpha)}(V_{G1} - V_{th}) \tag{6-6}$$

Whenever there is back accumulation, $\alpha = \frac{C_{si}}{C_{ox1}}$, and when the back is fully depleted, $\alpha = \frac{C_{si}\cdot C_{ox2}}{C_{ox1}(C_{si}+C_{ox2})}$, where C_{ox1} and C_{ox2} are the gate and back oxide capacitance, respectively. Typically the values of α are in the following sequence,

$$\alpha_{\text{fully\_depleted\_SOI}} < \alpha_{\text{back\_accumulation\_SOI}} < \alpha_{\text{bulk}}$$

Thus the transconductance is lowest in bulk MOSFETs, higher in SOI with back accumulation and highest in fully depleted SOI MOSFETs.

The voltage gain of a MOSFET is given by

$$\frac{\Delta Vo}{\Delta Vi} = \frac{\Delta I_d}{g_d}\frac{1}{\Delta V_i} = \frac{\Delta Vi \cdot g_m}{g_D}\frac{1}{\Delta V_i} = \frac{g_m}{g_D} = \frac{g_m}{I_D}V_A \tag{6-7}$$

where, V_A is earlier voltage same as in bulk MOSFETs, g_D is output drain conductance, and g_m is the transconductance. The peak voltage gain occurs when gm/ID reaches maximum. In subthreshold region,

$$\frac{g_m}{I_d} = \frac{dI_D}{I_D \cdot dV_G} = \frac{q}{(1+\alpha)\cdot k \cdot T} = \frac{q}{n \cdot k \cdot T} \tag{6-8}$$

where n is the body factor. In strong inversion,

$$\frac{g_m}{I_d} = \sqrt{\frac{2\mu C_{ox} \cdot W/L}{(1+\alpha)I_D}} = \sqrt{\frac{2\mu C_{ox} \cdot W/L}{n \cdot I_D}} \tag{6-9}$$

Since α is much lower in fully depleted ultra-thin film SOI MOSFETs than in its bulk or back accumulation SOI counterpart, much higher g_m/I_d can be obtained.

6.1.4 Kink Effect

In a thick-film SOI device, the thickness of the silicon film is larger than twice the value of $X_{d\max}$ as defined by

$$X_{d\max} = \sqrt{\frac{4\varepsilon_{si} \cdot \Phi_F}{q \cdot N_a}}, \tag{6-10}$$

where Φ_F is the Fermi potential given by

$$\Phi_F = \frac{kT}{q}\ln(\frac{N_a}{n_i}), \tag{6-11}$$

and N_a is the doping concentration of P-type substrate region. There is neutral silicon layer (called body) beneath the front depletion zone, thus the device is partially depleted. If the body is connected to ground, it acts as a bulk device, otherwise if it is floating, it gives two parasitic effects - the kink effect and parasitic floating-base NPN bipolar single transistor latch up effect.

In a thin-film SOI device, the silicon film thickness is less than $X_{d\max}$ and the silicon film is fully depleted at threshold, except the back gate presents thin accumulation. Fully depleted devices do not exhibit any kink effect, unless the back gate is in accumulation or a negative bias is used [Colinge_97].

6.1.5 Floating Body Effects

One of the distinctive issues in SOI technology is the floating body effect. In bulk silicon CMOS, the body of the transistor is always tied to either VDD or GND depending on their type to eliminate the body effects. In SOI process, the body is usually floating. Thick-film SOI MOSFET exhibits single-transistor latch-up phenomenon as described in Chapter 5. This phenomenon leads to some undesirable effects, among which are extremely steep subthreshold slope and lower drain breakdown voltage. However, the single transistor latch-up effect is reduced in ultra-thin fully depleted devices, or totally eliminated if the body's accumulation (if any) is discharged.

The charge and discharge of the floating body due to the current flowing between source and drain results in a capacitive coupling between the gate and body and other transient effects:

1. Transient leakage current in pass transistor logic such as SRAM, DRAM

2. Overshoot or undershoot in response to a square wave input at the gate

3. Degradation of logic state in dynamic circuits

To mitigate these problems, partially depleted devices should have body ties, however, fully depleted devices usually have weakly or no floating body effects.

6.2 SOI Passive Devices

One of the obstacles in RFIC/OEIC designs has been the difficulty to design fabricatable high-performance integrated passive elements. However, novel technology such as UTSi-SOS can produce high quality passive devices with increased quality factors due to the fully insulating lossless substrate - synthetic sapphire.

Each passive device at radio frequency cannot be modeled as pure element such as inductance, resistance, and capacitance. Usually lumped models made of a combination of the three pure elements are used in RF design. Furthermore, when the size of the device is larger than 0.1 wavelengths of the circuit media, transmission line effects should be included in the models.

6.2.1 Inductors

High Q inductors are crucial building blocks for RF front-end, wireless, optical communications such as homodyne, heterodyne receivers in communication links. Local oscillator is one of the essential elements for optical communications,

especially above 10 GHz, and monolithic high-Q inductor is critical to ensure low phase-noise to minimize interference between channels. Radio frequency inductors require special attention due to the limitations posed by various parasitics.

For RFICs and OEICs, inductors that have equivalent inductance values in the range of several nH, self-resonant frequencies in the range of Multi-GHz, and high-Qs are necessary. Unfortunately, standard bulk silicon CMOS technology suffers from losses in substrate and metallization, and high-Q, high-resonant frequency monolithic inductors in the nH range are difficult to realize in this process. At least some kinds of shielding or lift-off techniques are necessary. The series resistance of the inductor itself is one source of loss, which is due to conduction current (Ohmic losses) and magnetically induced currents (Eddy currents). Two factors account for the Ohmic loss - the resistance of the microstrip formed by multiple metal layers and the geometry of the inductor. Another way to make good inductors is through printed circuit board techniques such as microstrip, which provide inductance in the range of a nano Henry. A third method is to use off-chip bonding wires. To achieve inductance with a Q factor of around 100, off-chip bonding wires have to be employed. The length of these wires is typically several mils. Bond wire inductance, however, is sensitive to bonding geometry and the existence of neighboring bond wires, making accurate prediction of the inductance values difficult. A tightly wound coil not only provides self inductance but also exhibits heat loss due to wire resistance, skin effect loss, eddy current loss, and hysteresis loss when magnetic material is used. Common bond wire metals include gold and aluminum. Gold is preferred because of its higher conductivity and

flexibility. This allows higher Q bond wires with shorter physical lengths to be bonded for a given die height.

Lumped monolithic inductors are critical elements in RF circuit design. They are used as tuned loads, inductor peaking for bandwidth broadening, filters to filter out noise and gain enhancement by tuning out parasitic capacitance at center frequency. Spiral inductors with middle terminals are also used to make on-chip baluns.

An on-chip inductor can be realized by stitching multiple low loss metal layers, particular those that are thicker with lower resistivity. The on-chip UTSi SOI inductor is preferred because it meets the size requirement of highly integrated RFICs and OEICs for wireless and optical communication systems. Unfortunately, bulk CMOS on-chip inductors fabricated on the lossy substrate have low Q. At least some types of shield or lift-off techniques are necessary. In contrast, UTSi CMOS inductors have much higher Q, and higher resonant frequencies due to the full insulating substrate. A typical UTSi on-chip inductor can easily have quality factor of 10 to 20, with resonant frequency of 10s of GHz. A great advantage of SOI is that monolithic high-Q inductor can be made without any post processing such as substrate removal or lifting techniques due to the full insulating substrate. Because the UTSi SOI substrate is lossless and fully insulating, there is no series resistor to the substrate.

A variety of symmetric spiral inductors in square, octagonal, circular shapes have been designed assuming a microstrip structure on 10-mil thick sapphire.

Experiments [Chaki_95] found that the octagonal or circular shape has 10% less resistance than the square shape. Furthermore, increase line spacing is more effective than increase line width to achieve high-Q. A more effective way of increasing Q is to gradually increase line spacing and line width from center out. For RF circuits, a symmetric inductor layout such as shown in Fig. 6-2 (a) is critical. Figure 6-2 (b) and (c) show inductor small signal models in bulk CMOS and SOI, respectively. Fig. 6-3 shows a more accurate T-type small signal model for the symmetric UTSi inductor [Zhang_iscas].

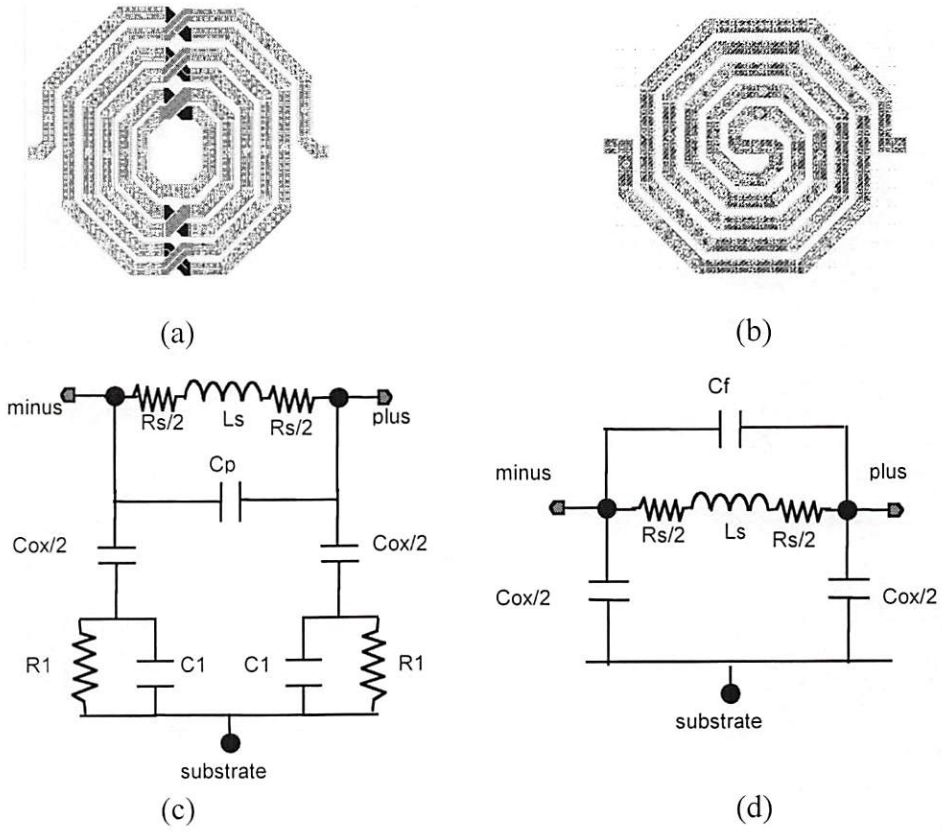


Figure 6-2. (a), (b) Symmetric inductors in UTSi-SOS technology (c) SSM of bulk CMOS inductor , and (d) SSM of SOI inductor.

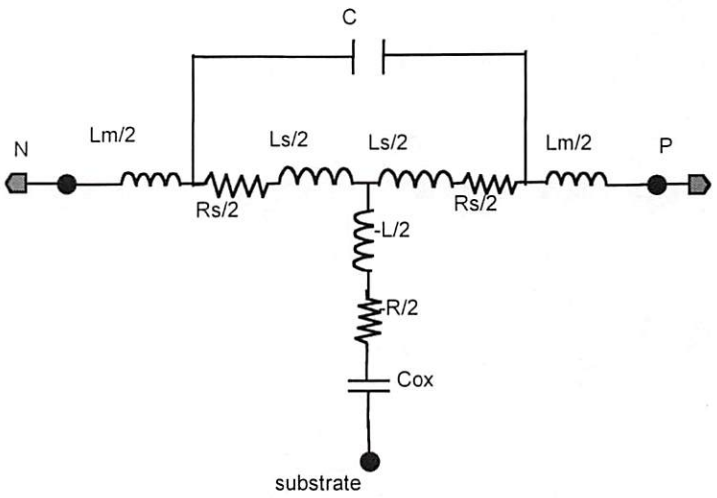


Figure 6-3. T-type UTSi-inductor small signal model

6.2.2 Capacitors

Because monolithic capacitors typically require large chip areas, they are generally avoided in circuit design. However, they are required in some applications. In UTSi-SOS technology, four types of monolithic capacitors can be achieved: (1) gate-to-drain capacitors, (2) double poly capacitor, (3) metal-insulator-metal (MIM) capacitor, and (4) metal-metal-metal (MMM) capacitor.

High-Q capacitance can be accomplished using MIM capacitors. Large values (2-200 *pF*) of capacitance can be achieved using a MOS gate capacitor, where source and drain are tied together as the bottom plate and the gate as the top plate. UTSi has very thin gate oxide (10.5 nm) which allows larger capacitance per unit area compared with bulk device. It should be noted that when the MOS gate capacitor is used, it should be reverse-biased. Furthermore, the potential across the

gate to drain/source should be at least twice the threshold of the device. Otherwise, as the voltage drops, the capacitance reduces and become noisy and non-linear. Large capacitance can be obtained by tiling small capacitors in 2-D arrays to have an accurate value.

Most one-poly-three-metal (1P3M) CMOS processes can produce the MMM type capacitor. It consists of three metal layers in parallel. Metal1 and Metal3 are connected as one terminal and Metal2 is the other terminal. In a 2P3M process, a double-poly capacitor can be realized. Again, a large capacitor can be accomplished by arraying primitive cells. The equivalent circuit is a series RC with values of

$$R = Rcell \ / \ (MW * ML) \tag{6-12}$$

$$C = Ccell * MW * ML. \tag{6-13}$$

6.2.3 Resistors

There are two types of active resistors: deposited semiconductor film and metal film. Deposit semiconductor films can be fabricated by diffusion into a host semi-insulating substrate or by depositing a polysilicon layer or by implanting impurities in a predefined area. Metal films are made by evaporation of metal on substrate with a lithographic pattern. Metal films are generally superior to the semiconductor films because metal films are less sensitive to changes in temperature and voltage.

In UTSi SOI technology, two popular types of resistors are diffused silicon resistor and silicided poly resistor. The diffused silicon can be realized by doping

N+, P+, and SN. The total resistance is calculated as the sum of the sheet resistance and the contact resistance is

$$R = Rsheet * L / (W-\Delta W) + 2 * Rcontact, \quad (6\text{-}14)$$

where, *Rsheet* is the sheet resistivity in Ω/square, *L* is the length of the resistor, from center to center of the contacts, *W* is the width of the resistor, and square is unit sheet area.

Typically, n-channel FETs and NPN bipolar transistors are preferred as resistors because their electron mobility is about two to three times the hole mobility.

6.2.4 Microstrip and Balun

Fully differential circuits are the choices in many RF integrated circuit designs due to their common-mode rejection of power supply noise. However, most test equipment such as oscilloscope, spectrum and network analyzers can only handle single-ended inputs and outputs, which requires differential to single-ended probes, and some probes cannot tolerate a DC offset. In this case, a balun is highly desired.

A balun is a transformer connected between a balanced source or load and an unbalanced source or load. A balanced line has two conductors, with equal currents in opposite directions. A balun can convert a single-ended signal to differential signals or vice versa. Edge-coupled milcrostrip lines and discrete tuning capacitors can be used. Baluns are very desirable in RF circuits to convert single-ended signals

into differential signals or vice versa for better common mode noise suppression with differential inputs and outputs. A balun can also be used as an impedance transformer depending on the inductance ratios of its primary and secondary windings. This function is very useful between a high impedance local oscillator (LO) driver output to low impedance differential mixer inputs.

Baluns can be classified into two types, active and passive ones. In monolithic microwave integrated circuits (MMICs), active baluns often exhibit magnitude and phase imbalance over moderate bandwidth [Dearn_98]. On-chip passive devices have been widely used in RFIC for higher performance. Typically, passive baluns consists of inductors, capacitors, resistors, which pose a disadvantage of consuming large amount of silicon area particularly at low frequencies because of the large spiral inductor [Liang_01].

There are several methods of realizing an on-chip balun with 4:1 impedance ratio. One way is to use two identical baluns by connecting their primary windings in series, and secondary windings in parallel. Compact baluns in square and octave spiral shape are designed in 0.5 μm UTSi-SOS technology using three metal layers.

6.3 SOI Optical Detectors and Modulators

For monolithic optical receivers, an on-chip photodetector is required. In the bulk CMOS process, a vertical diode can be easily formed by the well and substrate. For example, in an n-well process, the diode uses n-well and p-substrate, where a lower voltage is applied to prevent the diode from forward biasing. Unlike standard

bulk CMOS, UTSi-SOS process does not have well, and the substrate is fully insulating. Furthermore, the optical transparent substrate synthetic sapphire, plus the ultra-thin silicon give very low absorbtion coefficients, and low responsivity. These make it extremely challenge to make photodiodes in UTSi technology.

6.3.1 Photodiodes

Light beams impinging on a semiconductor material produce an electrical current by releasing electron-hole pairs. Those individual carriers released within the depletion region accelerate toward the diode terminals as part of conducting current, and those released outside get diffused or simply recombined. The depth and extent of the junction determines the location of the depletion region and the light wavelengths with highest responsivity. Applying reverse bias to the junction expends the depletion region as long as it is not exceed the junction breakdown voltage. The relation of photocurrent and optical power can be expressed as

$$i = R * P \tag{6-15}$$

where R is the responsivity and P is the radiant flux energy in watts. The response of i exhibits dual time constants. Those photons generated inside depletion region being accelerated rapidly to the terminals and generate the fast or drift component of the total current. The carriers produced outside the depletion region either recombine or drift slowly towards the depletion region. Those reach the depletion region get accelerated and proceed rapidly. The interim diffusion time produces a slow component of the total current.

To design high bandwidth optical receiver circuits, an accurate small-signal model of the photodiode is a prerequisite. A photodiode can be modeled and analyzed as a discrete semiconductor device as shown in Fig. 6-4, consisting of an ideal diode, a current source, parallel parasitic capacitor *Cj* and dark resistor *Rj* (the resistance of zero-biased junction), and a series resistance of the semiconductor material *Rs*.

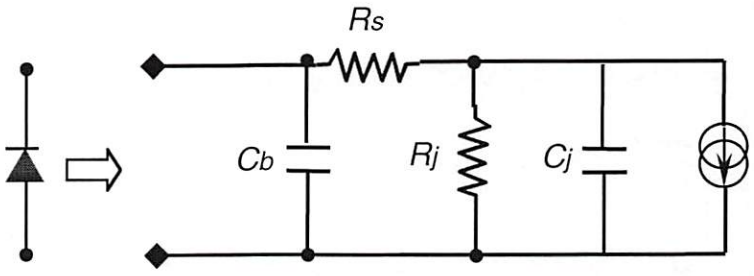


Figure 6-4. Small Signal Model (SSM) of a photodiode.

Parasitic capacitance is critical to the photodiode's stability, bandwidth and noise. It varies with the diode's area and voltage and can be expressed as

$$C_D = C_{D0} \Big/ \sqrt{1 + V_R / \Phi_B} \tag{6-16}$$

where C_{D0} is the zero-biased photodiode capacitance, Φ_B is the junction build-in voltage, and V_R is the reverse bias voltage.

PIN and avalanche diodes are two variations of the basic photodiode that improve its responsivity. PIN photodiodes increase the spectral bandwidth or frequency range by widening the depletion regions using an intrinsic layer. Avalanche photodiodes increase the magnitude of the output current and the

response speed by biasing the diode at the verge of breakdown, thus introduce avalanche multiplication to amplify the fundamental photodiode current. However, biasing a photodiode near its breakdown voltage poses significant practical difficulties. Since photons generate carriers at a range of depths with a given range proportional to the photon wavelength, longer wavelengths require wider depletion regions for efficient conversion. PIN photodiodes increase its responsivity at higher spectral bandwidth or light frequencies by increasing the thickness of the depletion region.

6.3.2 Quantum Effect Devices

Vertical-Cavity Surface-Emitting Lasers (VCSELs) have rapidly advanced in recent years and become one of the best candidates for short distance high bandwidth 2D dense optical interconnections. VCSELs have been fabricated in GaAs or InGaAs technology. Figure 6-5 shows its physical structure and small signal model.

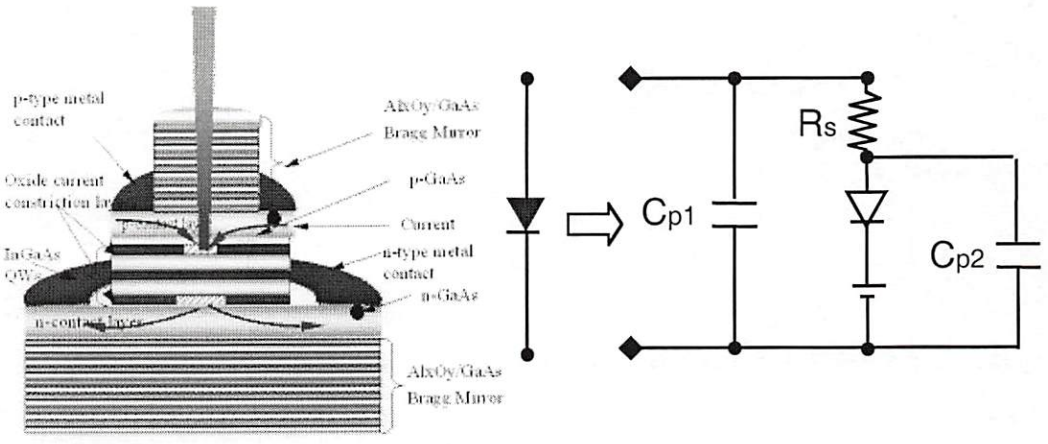


Figure 6-5. VCSEL physical structure and its small signal model.

Fabricating integrated quantum devices directly in SOI CMOS technology is very challenging due to the small band gap of silicon. This is probably the most significant limitation to complete integration of optical input and output with SOI circuits. For the immediate future, flip-chip bonding of GaAs VCSELs and photodetectors to SOI CMOS is the most promising approach.

The state-of-the-art of the integration of GaAs material with silicon is to use an intermediate layer. The property of such a layer must be similar to both GaAs and silicon materials and thus reduce the lattice mismatch between the two. If the GaAs can grow over silicon on top of an intermediate layer, then monolithic integration of VCSEL and photodetector optical I/Os with CMOS SOI circuits can be realized.

CHAPTER 7 HIGH-FREQUENCY CMOS SOI CMOS/CML STANDARD CELL LIBRARY, AND ANALOG MACRO DESIGNS

7.1 Introduction

ICs operating at speeds greater than 10 Gb/s in GaAs, MESFETs, GaAs HBTs, Si bipolar, and SiGe techonology have been reported. However, the power consumption of these ICs is relatively high. Standard CMOS circuits have the advantage of low power but generally operate at relative lower speed (slightly > 1 Gb/s). Optical communication systems operating at gigabits per second and above demand OEICs to handle high-frequency signals of at least half the data rate. Fast switching logic beyond conventional CMOS logic is crucial for better noise suppression and low power consumption. Multi-Gb/s Pseudorandom Bit Stream (PRBS) generators are essential for performance measurements of a high-bandwidth optical transceiver link, whenever expensive high-bandwidth equipment is not available. Recently, several CMOS communication OEICs such as transceiver, mux/demux, clock and data recovery, and PLL circuits operating at greater than 1 Gb/s have been reported. The maximum data rates of these circuits are limited by the frequency of CMOS logic. For example, the maximum clock frequency of a 0.18-μm CMOS chip is 3.1 GHz, and that of a 0.15-μm CMOS chip is 3.0 GHz. Emerging CMOS SOI technology exhibits greater advantages in low-power and higher frequency, but still has limitations, the maximum clock frequency of a 0.5 μm CMOS UTSi chip is 2.5 GHz.

This chapter presents some theoretical analysis and design methodologies for novel UTSi SOI circuits for high-speed, low voltage and low power VLSI systems. Section 7.2 presents the design flow of SOI CMOS in Cadence EDA environment. In section 7.3, we present the UTSi-SOS CMOS standard cell library design and two types of high-speed dynamic PRBS. One of these is true-single-phase-clock (TSPC) dynamic D-flip-flop based, the other is double-edge-triggered D-flip-flop based. Section 7.4 describes current mode logic (CML) and low-voltage differential-signal (LVDS) logic standard cell macros in UTSi SOI technologies. Section 7.5 identifies the pros and cons of CMOS and CML logic family for wireless and optical communication. Section 7.5 describes the design of amplifiers.

7.2 Design Flow of SOI CMOS In Cadence EDA Environment

The Peregrine UTSi-SOS CMOS SOI process is commercially available and has been evolving from internally named DA to FA, and FA to FC process over the last two years. These processes are similar but vary in feature sizes, model parameters, etc. Our ASIC standard cell library design flow is a standard bottom-up methodology. The steps we used to design all our digital standard cells or analog macros are listed here and a more detailed design flow diagram is shown in Fig. 7-1.

- Design transistor-level schematic and create symbol
- Pre-layout transistor level simulation
- Pre-layout timing analysis
- Design transistor-level layout view of equal height
- Layout standard cell design rule check (DRC)

- Electrical rule check (ERC)
- Layout versus schematic (LVS) check
- Post-layout simulations and timing analysis

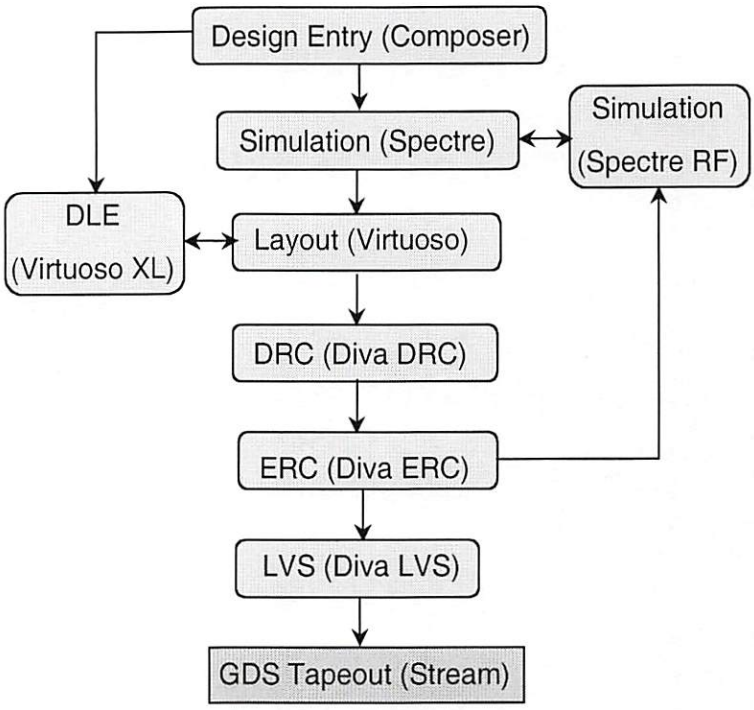


Figure 7-1. Design flow for digital standard cells, analog micros, mixed-signal, and RF circuits in Cadence EDA environment.

7.3 0.5 μm UTSi CMOS SOI Standard Cell Library Design

The Peregrine UTSi-SOS is a patented process that belongs to CMOS SOI family. It has multi-threshold voltage transistors, and for maximum noise margin, low delay, low-power dissipation, and high-speed operation, different design strategies are used. We have developed our own standard logic cell libraries for both 0.5-μm UTSi FA and FC process. In each library, approximately 20 standard cells

containing CMOS gates, multiplexers, various latches, flip-flops, Schmitt triggers, and other miscellaneous circuits.

Each cell layout has several versions using transistors with different threshold voltages optimized for speed and power dissipation. All the cells were designed to use the first metal layer only and keep the second and third layers free for power supply distribution and cell interconnects. The height of each standard cell is 23.40 microns as specified in standard cell diva-DRC rules. Most digital cells use the minimum transistor size for multi-GHz frequency switching and low-power consumption.

As noted in Chapter 5, in comparison to conventional CMOS, UTSi SOI circuit layout can be more compact because it allows NLOCOS (N diffusion in bulk CMOS) and PLOCOS (P diffusion in bulk CMOS) to lie next to each other. Figure 7-2 illustrates the physical layout of a bulk CMOS inverter and a UTSi inverter.

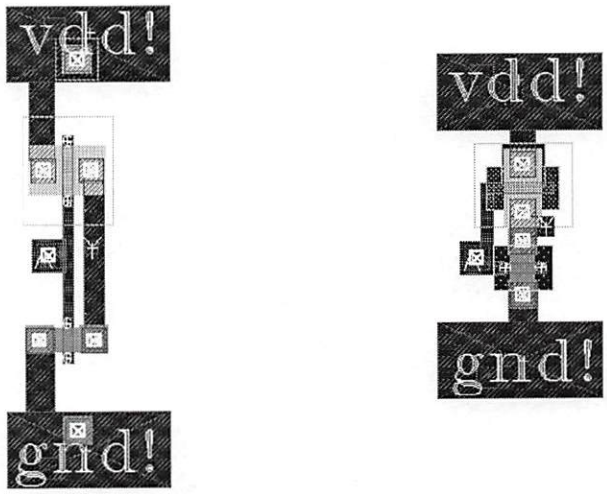


Figure 7-2. Comparison of bulk CMOS inverter layout (left) and UTSi SOI inverter layout (right).

7.4 0.5 μm UTSi LVDS Standard Cells

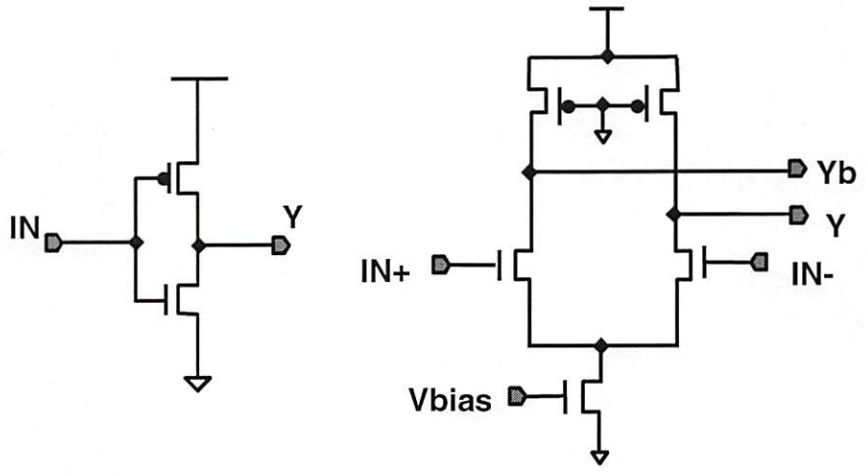
Compared to CMOS logic, low voltage differential signal (LVDS) logic such as differential current mode logic (DCML) is capable of much faster operation, better noise suppression, and lower power consumption independent of frequency. Therefore, LVDS signaling is very desirable for 10 Gb/s communication systems where speed and power dissipation is critical. One of the challenges in circuit design is to meet the LVDS standard at the input interface. The standard requires a wide input signal range: differential amplitude can vary from 100mV to 400mV, and the common mode can vary from 50mV to 2.35V. The maximum operation frequency however is degraded by the fluctuation of the threshold voltage of the differential pair, and the fluctuation increases as the minimum gate length decreases. A feedback MOS current mode logic (CML) circuit immune to the threshold fluctuation has been adopted for 10Gb/s optical communication systems.

For better noise suppression both internally and externally, we designed a number of low-voltage differential signal standard cells. These cells include the basic logic gates such as differential inverter, NAND, NOR, XOR gates and multiplexers. Each cell has differential inputs and 400-mV voltage swing differential outputs.

7.5 CML Logic vs. CMOS Logic

Current mode logic (CML) is a member of the LVDS family. Having differential inputs and outputs. CML logic is preferred in RF communications because of its better noise suppression capability for both internal and external noise sources. The advantages of the CML family are high-speed operation and low power consumption that is independent of operating frequency. While CMOS logic consumes less power at speeds (< 2GHz), the power-consumption of CML circuits is independent to frequency.

Figure 7-3 shows inverters in CMOS logic and conventional DCM logic. The CMOS logic has the advantage of low power consumption at lower frequency, and its maximum speed is relatively slow. For example, the maximum toggle frequency of a conventional 0.18- μm CMOS inverter is only about 3.5 GHz. The CML can operate much faster than the CMOS due to its smaller input capacitance and smaller signal amplitude.



(a) (b)

Figure 7-3. Inverter circuit diagram in (a) CMOS logic and (b) Differential current mode logic (DCML).

The power required by CMOS logic results from charging the subsequent load capacitance whenever switching to '1' occurs, and therefore, it increases linearly with operating frequency. If leakage current is ignored in high frequency operation, the power consumption of CMOS logic can be expressed as

$$P_{CMOS} = C\,V^2 f, \tag{7-1}$$

which is proportional to the operating frequency. On the other hand, however, the power consumption of CML logic is the sum of the penetration currents of the input differential pair transistors, which is the same as the drain current of the tail current source transistor. Since the current source transistor operates in the saturation regime, and is mainly determined by its gate bias voltage, thus the contribution of the common source node of the differential input pair can be ignored. Therefore, the

power consumption of the CML logic is nearly independent of its operating frequency.

As shown in Fig. 7-4, the power consumption of CMOS is equivalent to CML at around 2 GHz. Above that frequency, CMOS power consumption continues to increase linearly with frequency while CML is constant. One drawback of CML logic is its area, which is about 2-4 times larger that its CMOS counterpart. However, for ultra-high frequency operation CML logic is the choice due to its low power consumption advantages.

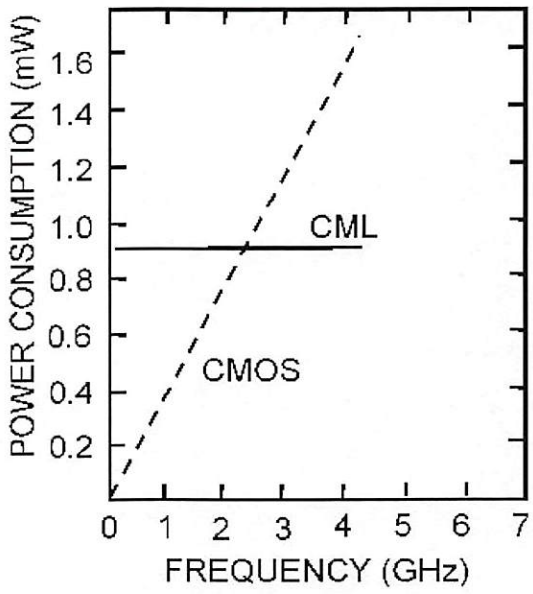


Figure 7-4. Power consumption of CMOS and CML circuits as a function of frequency.

Although many high-speed logic circuits such as those based on flip-flops are digital circuits, most designs are bipolar for high-speed operation. For low power consumption, digital circuits can be realized using CML-logic in bipolar or CMOS process. A CML logic flip-flop has high-speed and low power consumption. However it has a higher transistor count and larger area. The high-performance

UTSi SOI process makes it possible to use dynamic CMOS flip-flops to implement the typical mobile communications frequency circuits ranging from 900MHz up to 2.4 GHz with low power operations. A typical structure of such a high-speed dynamic D-flip-flop is true-single-phase-clock (TSPC) D-flip-flop by Yuan and Svensson [Yuan_89] as shown in Fig. 7-5. For the UTSi SOS technology, it has been optimally sized for low power consumption and high-speed.

7.6 Design and Layout of Canon Analog Micros in Silicon-on-Sapphire

A primarily trade-off in digital circuit design is between speed and power dissipation. However, besides power dissipation and bandwidth, analog circuits also have the trade-offs among gain, linearity, noise, input/output impedance, and voltage swing. To avoid transistor breakdown, the continuing scaling of CMOS process requires low voltage operation which poses challenges in analog circuit design. Reducing the biasing voltage leaves less room for linearity. Innovative circuits have to be created in place of the conventional cascode structures to comply the voltage scaling. Analog circuits such as Opamps, filters, comparators, data converters, oscillators, phase-locked loops, frequency synthesizers and RF transceivers contain many functions but rely on device models. Accurate device models are important especially to new technologies. The properties of interests for circuit simulations include dc, ac behavior, linearity, matching, noise, and temperature dependence.

CHAPTER 8 MULTI-GHZ RADIO FREQUENCY MIXED-SIGNAL MONOLITHIC UTSI CIRCUITS FOR WIRELESS AND OPTICAL COMMUNICATIONS

8.1 Introduction

Chapters 8 and 9, we describe circuit and system designs, physical layout, simulations, fabrications and tests of four chips in 0.5 μm UTSi-SOS CMOS SOI technology for wireless and optical communications. On the four distinct chips there are high-frequency digital, analog, mixed-signal and monolithic RF circuits and modules. The chips contain a wide variety of circuits and sub-systems needed for wireless and optical transceiver, signal processing, communications and networking.

In the 2000 COOP-GMU UTSi CMOS foundry chips, we have designed and fabricated two chips including 4x1 optical transceiver (receiver + VCSEL driver) arrays, optical transceiver BIST (built-in self-testing circuits consists of VCO and two types of pseudo-random bit stream generators and multiplexers), 4x4 electrical time-division multiplexed switch with option of optical transmission, and one 40 μm x 40 μm active pixel detector with voltage amplifier. These OEICs are integrated with VCSEL and detector arrays for optical communications. In the 2001 COOP USC UTSi-SOS foundry run, we have designed two chips containing single-ended and differential ended receivers, current mode differential VCSEL drivers, monolithic photoreceivers, mixer, baluns, double-edge triggered DFF-based PRBS, a fully differential LC-Tank VCO, $\pi/4$ differential quadrature-phase VCO, and a clock and data recovery circuits based on phase-locked loop.

Table 8-1 is a summary description of these chip designs. The columns list the four different chips, and the rows classify these circuits into different categories, i.e. digital, analog, mixed-signal, and RF circuits.

	2000 UTSI CHIP#1	2000 UTSI CHIP#2	2001 UTSI CHIP#1	2001 UTSI CHIP#2
CMOS std cells	Dynamic threshold INV, NAND, AND, OR, NOR, XOR, MUX, TSPC DFF, Static DFF, double edge triggered DFF, etc.			
PAD cells	I/O pads, VDD pads, GND pads, bare pads and ESD protected pads, corner pads.			
LVDS std cells	INV, OR, XOR, MUX, DFF, differential amplifier, comparator, output buffer.			
High-Speed Digital circuit	2047-pattern TSPC PRBS	4x4 TDM ADD/DROP switch	Optically clocked TSPC PRBS, Double-edge triggered PRBS	Frequency divider
Monolithic Mixed-signal, Analog, RF circuits	Two 4x1 LNA transceiver arrays Ring oscillator	4x1 array receiver 4x1 array laser diode driver	4x1 flip-chip bonding optical receivers Quadrature-phase LC-VCO, Mixer, Baluns	4x1 flip-chip boding VCSELs, PLL Differential LC-VCO

Table 8-1. Summary of UTSi-SOS chip design work under 2000 COOP-GMU and 2001 COOP-USC peregrine foundry runs.

This work was made possible with the support of the Consortium for Optical and Optoelectronic Technologies in Computing (COOP) at George Mason University and at the University of Southern California, and was sponsored by the Defense Advanced Research Project Agency (DARPA). Among the four chips we designed, two of them designed in 2000 UTSi-SOS FA process had been fabricated and the other two designed in 2001 UTSi-SOS FC process are currently being fabricated. To the best of our knowledge, some of them are among the most

complicated UTSi circuits and subsystems designed to date. These circuits are innovative and important elements for optoelectronics and communications.

8.2 Multi-Ghz CMOS Optical Transceiver LSI Chip and 4 x 4 Time Division Multiplexing Smart Switch Chip In Silicon-On-Sapphire

In the remainder of this chapter, we describe the design, fabrication and functionality of two different 0.5 micron CMOS optoelectronic integrated circuit (OEIC) chips based on the Peregrine Semiconductor Ultra-Thin Silicon (UTSi®) on insulator technology. Among the two 2000-UTSi chips, the chip#1 contains transceiver and network components, including four channel high-speed CMOS transceiver modules, pseudo-random bit stream (PRBS) generators, a voltage controlled oscillator (VCO) and other test circuits. The transceiver chips can operate in both self-testing mode and networking mode. An on-chip clock and multi-GHz true-single-phase-clock (TSPC) D-flip-flop have been designed to generate a PRBS at over 2.5 Gb/s for the high-speed transceiver arrays to operate in self-testing mode. In the networking mode, an even number of transceiver chips forms a ring network through free-space or fiber ribbon interconnections.

The 2000-UTSi chip#2 contains four channel optical time-division multiplex (TDM) switches, optical transceiver arrays, an active pixel detector and additional test devices. These chips have been designed for use with external 850 nm vertical cavity surface emitting lasers (VCSELs), and metal-semiconductor-metal (MSM) or GaAs p-i-n detector die arrays to achieve high-speed optical interconnections. The package methods could be either wire bonding or flip-chip bonding of the CMOS

SOS smart-pixel arrays with arrays of VCSELs and photodetectors onto an optoelectronic chip carrier as a multi-chip module (MCM).

8.3 Figured of Merit for Optical Receivers

Optical receivers are one of the key components in optical fiber communication systems [Zhou_96]. Low cost, high-performance monolithic OEIC receivers are essential for high-speed optical data links. In many mixed-signal circuits and systems, the performance is strongly determined by the front end of the system. This is especially true in an optical receiver where both the performance of the photodetector and the low-noise preamplifier, the electrical and physical interface, play key roles in the receiver and system's performance. A higher degree of integration enables higher performance. A monolithically integrated receiver typically consists of an MSM or a PD detector, a transimpedance preamplifier, a limiting postamplifier, an output buffer, and perhaps clock and data recovery circuitry if necessary.

One of the design challenges is that the front-end receiver preamplifier needs to operate at GHz rates with very low noise while the post-amplification stage and signal processing pixels demand high-frequency operation, which produce large switching noise. Fortunately, unlike optical signal, there is no signal reflection due to the good isolation characteristic of MOSFETs if the interconnection transmission lines have impedance match and are properly terminated. Among the performance specifications such as bit error rate (BER), jitter, and eye pattern parameters, BER is the ultimate system performance test. The sensitivity is defined as the average

minimum incident power for the optical receiver to maintain a minimum bit error rate (BER).

There are two types of front-end receiver topologies - differential-ended and single-ended. The single-end configuration was adopted due to its compact design for dense area I/O interconnections. The specific design also meets the requirement of high sensitivity, which is one of the most important performance specifications of an optical receiver. Optical sensitivity, P_s can be expressed by

$$P_s = Q \cdot i_{rms} / R \tag{8-1}$$

where, i_{rms} is the input referred room-mean-square noise current of the optical receiver, R is the PD responsivity, Q has a theoretical relationship to error rate. High signal-to-noise-ratio (SNR) contributes to high optical sensitivity. Low input current noise and high responsivity are the keys to high optical sensitivity.

Increased receiver sensitivity is accomplished by increasing the gain and decreasing the noise figure of the receiver's low noise amplifier (LNA), the stage that has the most effect on the receiver's sensitivity. The equation describing the overall system noise figure consisting of two or more stages can be calculated using the recurrence relation [Gonzales_84]

$$F_n = F_{n-1} + \frac{F_n - 1}{G_{n-1}} \qquad (with\ F_0 = 1) \tag{8-2}$$

Where F_n is the noise figure seen after the nth stage, F_{n-1} is the noise figure seen after the $(n-1)^{th}$ stage, and G_{n-1} is the gain of the $(n-1)^{th}$ stage. From Eq. (8-2),

we can see that the frontier transistors in the chain have more effect on the overall noise figure of the receiver modules. The low-noise pre-amplifier must therefore have a high gain and a low noise figure to reduce the noise figure of the succeeding stages in order to obtain high sensitivity.

The front-end of the photodetector and optical receiver converts the optical power, P_o into electrical power V_e

$$V_e = P_o \cdot R \cdot H , \tag{8-3}$$

where R is the responsivity of the photodiode (PD), H is the closed loop transfer function of the TIA. The bandwidth of the optical receiver can be derived and approximated by,

$$F_c = A_v /(2 \cdot \pi \cdot R_f (C_d + C_{in})) \tag{8-4}$$

where, A_v is the open-loop voltage gain of the TIA, R_f is the feedback resistance, C_{in} is the input capacitance of the TIA plus parasitic capacitance, and C_d is the capacitance of the PD.

From Eqs. (8-3) and (8-4), high PD responsivity gives maximum photocurrent, high SNR, and reduced component and parasitic capacitance at high bandwidth operating point. In addition to these constraints, it is desirable that the optical power be limited to $1mW$ for eye safety reasons. In recent years, interest has been growing in MSM detectors due to their low capacitance, high speed, and ease of integration with semiconductor process.

8.4 Architecture of the Optical Transceiver Chip

The optical communication transceiver chip (2000-UTSi Chip#1) was designed and fabricated in the 0.5-μm CMOS UTSi-SOS Peregrine FA process. The block diagram (not including pads and ESD protection) is shown in Fig. 8-1. At the top are two 4x1 transceiver arrays and self-testing circuits. The chip is designed to operate with external detector and VCSEL arrays as shown. Each array consists of 4 channels, and each channel incorporates a preamplifier, a postamplifier, a level restoring circuit, and a decision/decoder circuit. The pre-amplifier is a transimpedance amplifier (TIA) receiver to convert the detected photocurrent into a usable voltage for the post-amplifier stages and to further amplify, reshape the signal to digital logic voltages. On the bottom of Fig. 8-1, are VCO and PRBS generators shared by all the transceiver arrays above. The chip also has a frequency divided clock and PRBS electrical output for monitoring and the test of some additional standard cells designed in this foundry run [Zhang_oc].

The chips can work in both self-testing mode and networking mode. In networking mode, optical signals propagate either through free space or fiber ribbon, and are detected by the externally connected MSM or positive-intrinsic-negative (PIN) photodetector array with output photocurrent ranging from 1 μA to 10s of μA.

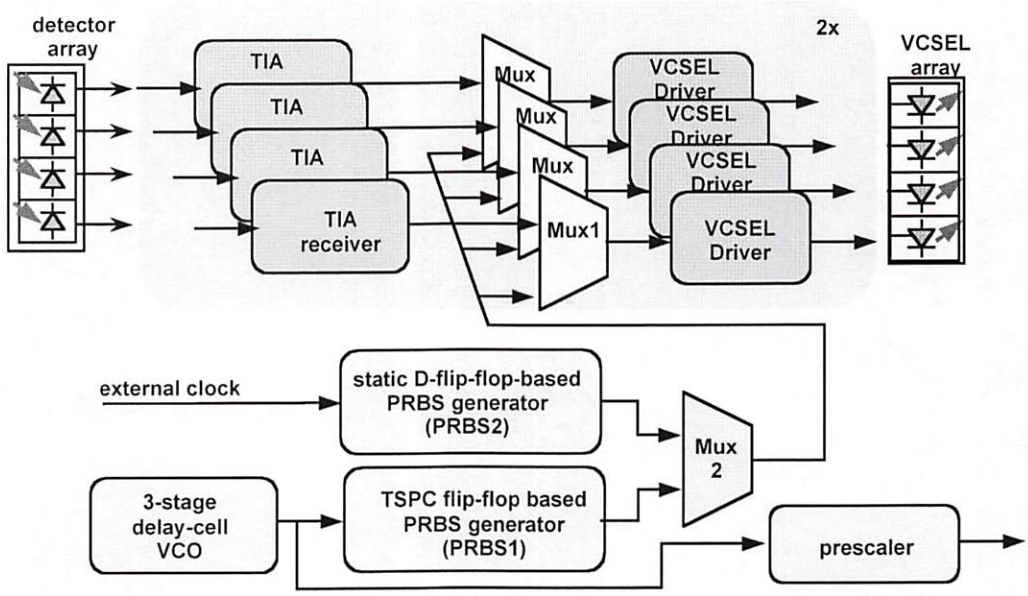


Figure 8-1. Block diagram of 2000 UTSi-SOS chip #1: optical transceiver arrays with BIST circuits.

Each multiplexer (Mux1) in the multiplexer array selects either the optical receiver output, or the BIST circuit output, feed into the corresponding VCSEL drivers and drive the externally connected VCSELs to emit optical beams which propagate to the next node, again either through free space or fiber ribbon. In self-testing mode, another multiplexer (Mux2) selects one of the two PRBS outputs as input to the VCSEL driver and then to the VCSELs. One PRBS is a static logic D-flip-flop based and is clocked by an external clock and has 2047 patterns. The other one is based on a true-single-phase clock (TSPC) D-flip-flop, which directly interfaces with the GHz frequency clock output from the voltage-controlled oscillator. Each of the 2.5-volt CMOS outputs of the Mux1 array feeds into the corresponding VCSEL driver input to drive the VCSELs to emit digital optical signals. The chip is designed to incorporate VCSEL and InP-based PIN photodetector or MSM detector arrays through wire or flip-chip bonding.

8.5 Circuit Designs of Optical Receiver and Receiver Arrays

The 2000 UTSi Chip # 1 transceiver chip contains two optical transceiver arrays. Two distinct low-noise transimpedance amplifier (LNTA) receiver arrays are designed and fabricated in 0.5-μm ultra-thin silicon on sapphire 0.5-μm CMOS technology. Each array has 4x1 optical receivers with simulated power dissipation of 1.2 mW at 1 GHz and the maximum bandwidth of 2.5 GHz. These unique receiver designs have wide dynamic range, high bandwidth, low noise figure, high sensitivity and low-power consumption.

There are major three types of pre-amplifiers, i.e. high impedance, low impedance 50 Ω, and transimpedance amplifiers. The pre-amplifier of our optical receiver is a transimpedance amplifier (TIA) due to its optimum trade-off between noise, bandwidth, and dynamic range. The receiver design uses intensity modulation and direct detection (IM/DD) scheme.

Figure 8-2 shows the unique design of one of the transimpedance amplifier (TIA) receivers. It consists of three stages and uses multi-threshold transistors RP (Vth = -0.7 V) and IN (Vth = 0.05 V). The first stage is a three inverter-based high gain transimpedance stage, with a tuning voltage applied to the gate of the RP FET to control the gate of an IN FET and thus the transimpedance (75 KΩ). Inside the transimpedance stage feed forward path, a diode-connected RP FET and an IN FET is added for current limiting, increasing the bandwidth, broadening and stabilizing the gain of this stage. The stage next to the transimpedance stage is an inverter

operating in its linear region as a postamplifier with a very small gain of 1.4, and the last stage is an inverter as asynchronous decision circuit. The first transimpedance stage with feedback tunable resistance and the switching offset between the TIA stage and the decision circuits are critical, particularly for single-input DC coupled operations. The transistor are sized to have large noise margin and good linearity.

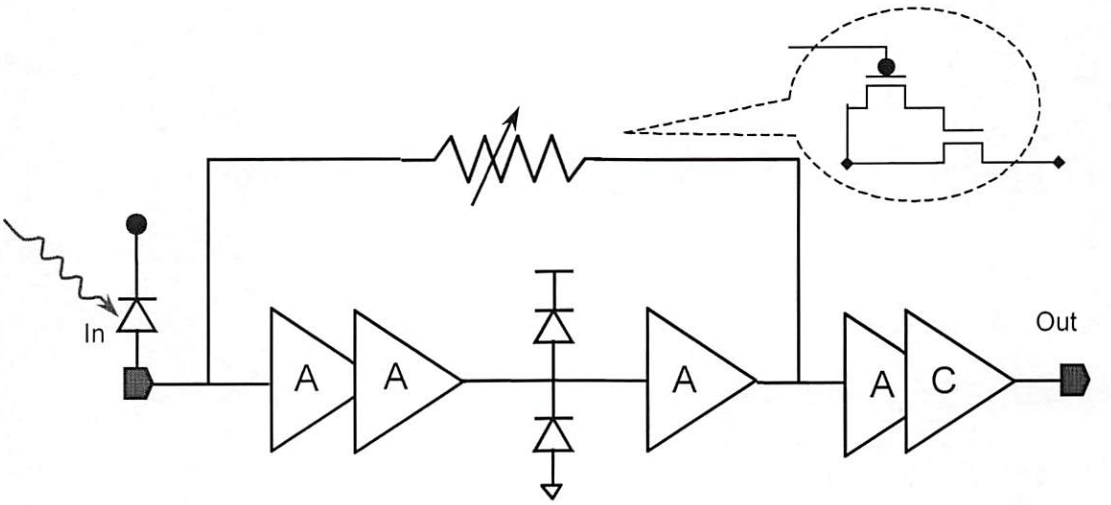


Figure 8-2. One of the single-ended transimpedance amplifier receiver.

It is clear that the threshold voltage is one of the most important parameters for device and circuit design. In this unique receiver design, besides the current limiting and feedback active resistance network, multi-threshold devices are used to accomplish high performance and lower leakage power dissipation. In active mode, a low threshold (0.05 V, IN transistor) is desired to obtain higher performance. However, in standby mode, a high threshold (-0.7 V, RP transistor) is preferred to reduce leakage current and thus power dissipation.

The ultra low power dissipation (480 μA with 2.5-V power supply) and compact dimension allow very high density optical interconnections, which is essential for THz throughput parallel transceivers or page-oriented memory readouts. A 4x1 optical receiver array was formed by duplicate the single receiver circuit with a shared receiver tune voltage. Figure 8-3 shows one of the Spectre simulation results with the worst case input testing vectors, where a '1' pulse followed a long string of '0', or vice versa.

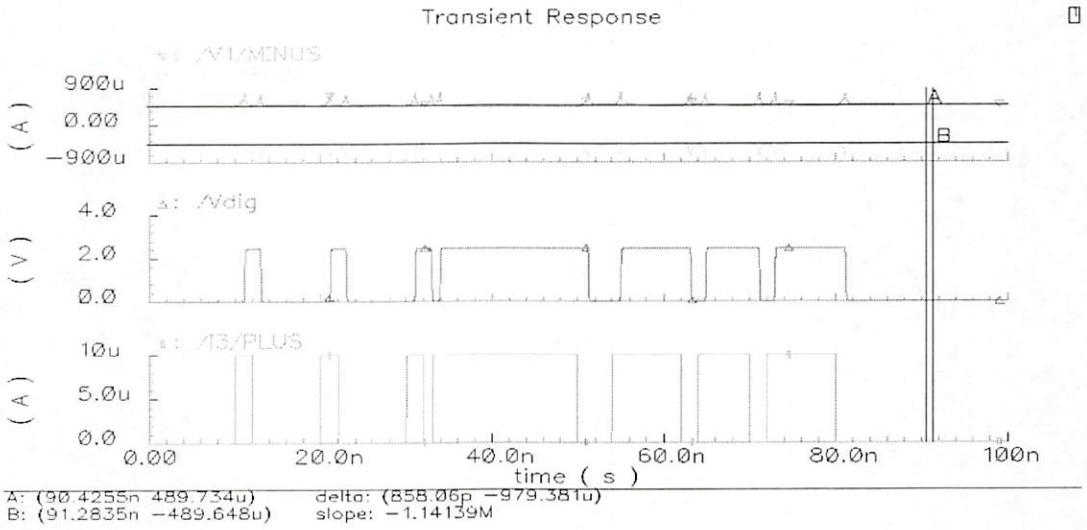


Figure 8-3. One of the Spectre results with the worst-case current inputs to the TIAR array.

In summary, the receiver designs have current limiting, and slew rate control circuit to obtain high-bandwidth and good sensitivity. Three inverter voltage amplifiers having similar gain were cascaded to obtain wide bandwidth. The global active resistance feedback provides high tranimpedance gain.

8.6 VCSEL Driver and VCSEL Driver Array Circuit Designs

With the standardization of 10 Gbps Ethernet, the most desirable light sources for such data-communications links have been investigated. Optical interconnects based on low threshold current vertical-cavity surface-emitting laser (VCSEL) diodes bring high-density area I/O arrays into reality [Yang_95]. Optical transmitters based on VCSEL offer low power consumption, low bit error rate, and multi-Gbps data transfer rate. VCSELs with bandwidth exceeding 10 GHz will play the major role in next generation high-capacity network [Krishnamoorthy_99], where the intimate integration VCSEL with silicon circuits are the key for high bandwidth communications. In the last decade, many high-speed optical receivers but few laser diode drivers have been reported for the bandwidth demanding optical interconnects and optical fiber communication systems. As in the same optical communication link with the receivers, laser diode driver is of paramount importance. The performance of laser diode driver circuits is crucial for high quality light transmission. Its design, though concept is simple, is challenging due to stringent specifications such as high output current (in the range of mAs), nearly zero bit error rate at full bit-rate speed, and compensation for the temperature dependent characteristics of the I-V curve of a laser diode. Some of the requirements of laser driver include tens or hundreds of pico-second equal rise and fall times, no significant timing jitter (phase noise), and impedance match to minimize reflections in multi-gigabit per second bit rate.

We have designed and fabricated two distinct 4-channel Multi-GHz VCSEL driver circuits in 2000 UTSi Chip #1 and Chip #2. One configuration has 9-15 *mA*

peak-to-peak dynamic tuning range with 2.5-*V* low supply voltage. The other design is current mirror VCSEL Driver (CMVD) followed by ratioed inverter amplifier boosting stages which has peak-to-peak ac signal outputs of 12 *mA*. The simulation results show the arrays operate at more than 5Gb/s data rate per channel. These laser driver arrays have the following features:

(1) Current switching is used instead of current steering.

(2) *Low voltage (2.5 V) and low power consumption due to very few transistors.*

(3) *IP-IN transistor pairs with stronger driving capability (than RP-RN) has been used.*

In experimental measurements of the circuit performance, off-chip 30-Ω resistors replace the anticipated VCSELs or VCSEL array made by Truelight or EMCORE.

8.7 Optical Transceiver Self-Testing Circuitry Design

2000 UTSi-Chip #1 also contains built-in self-test (BIST) non-return-to-zero (NRZ) pseudorandom bit stream (PRBS) and on-chip clock generators that we have designed and fabricated. The transceiver self-testing circuitry eliminates the needs for expensive high bandwidth function generators while testing the transceiver circuits at high frequencies. The self-test circuit includes a tunable frequency clock generator, two types of PRBS generators, and a prescaler for off-chip measurement. The clock generator consists of a current mirror circuit with frequency tuning

voltage, a delay cell using inverter chains, a NAND gate for reset and clock buffer. The 5-stage ratioed-delay cell VCO is simulated having a dynamic range of 400 MHz ~ 1.5 GHz, and the 3-stage delay cell VCO has a frequency range of 1.25 GHz to more than 2.5 GHz. The frequency tunable GHz VCO clock output signal directly feeds into the 11-bit length maximum pattern PRBS generator, which consists of eleven 8-transistor True-Single-Phase-Clock (TSPC) D-flip-flops and a 6-transistor exclusive NOR gate. The TSPC flip-flop is a dynamic circuit designed in place of the static D-flip-flop to be able to directly interface with the high-frequency clock from the VCO.

In the self-testing mode, two on-chip pseudo-random bit streams (PRBS1 and PRBS2) are selected by a multiplexer (Mux 2), whose output shares one VCSEL driver and VCSEL channel with the output of the receiver through another 2-to-1 MUX (Mux 1 array). PRBS2 runs at an external off-chip clock rate, while high frequency PRBS1 runs at the on-chip frequency adjustable oscillator VCO clock rate.

Figure 8-4 shows one of the Spectre simulations for the BIST circuits including the VCO, PRBS, and MUX running at 2.5 GHz, one is output of the VCO, the other is the 11-bit PRBS output signal. Optimizing the multiplexer design is very critical to avoid limiting the data throughput. The on-chip high-speed PRBS generators can test high-speed operations of the VCSEL driver arrays without the need for high-speed function generators, which offers an efficient method for system test and integration. We have simulated the eye diagram of the VCSEL driver

running with the built-in VCO and 2047-pattern PRBS at about 2.5 Gbps. The eye pattern was obtained by driving the VCSEL from the PRBS and drawing the output waveform of each VCSEL driver on one window. The VCSEL output has a value of 10 mA peak-to-peak current, corresponding to Vbias = 1 volt. The bit width is 0.409 ns, i.e. 2.445 Gbps. Correspondingly, the VCO running at 2.445 GHz clocks the dynamic PRBS generator. The VCSEL driver itself runs at much higher speed, and ultra-fast data rates can be achieved if a high-bandwidth NRZ bit stream source is available.

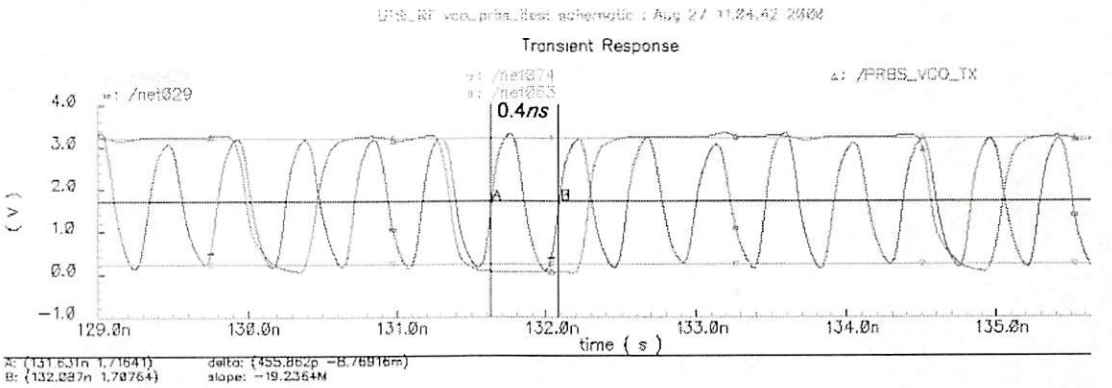
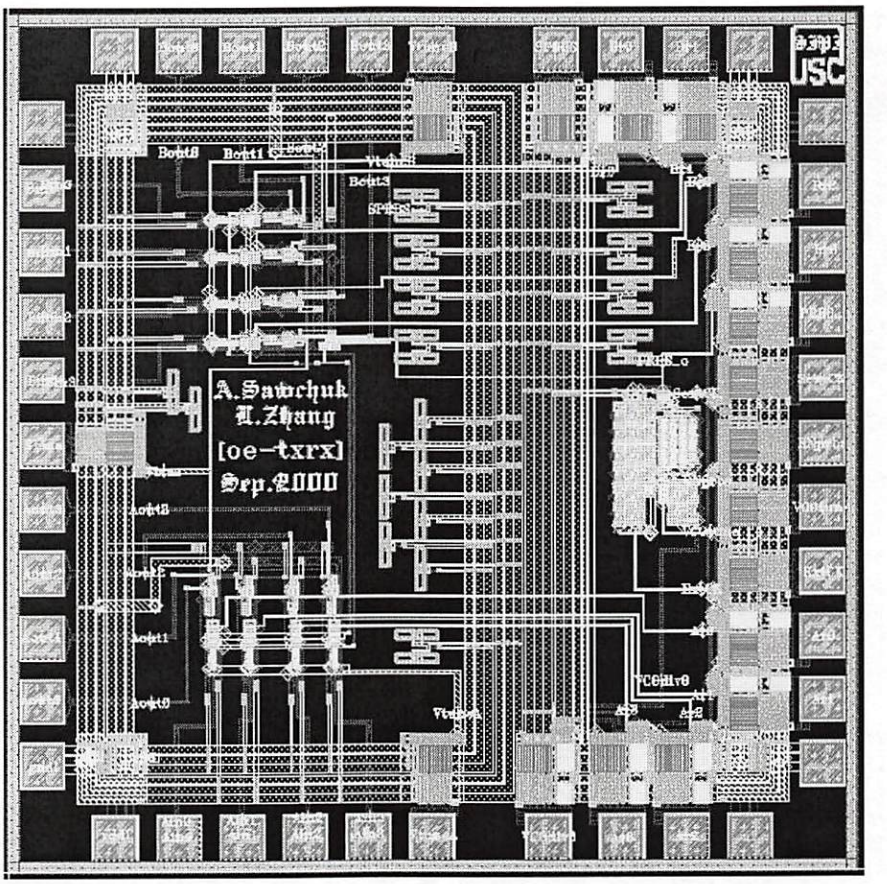


Figure 8-4. One of the 2.5 GHz Spectre results for the BIST circuits.

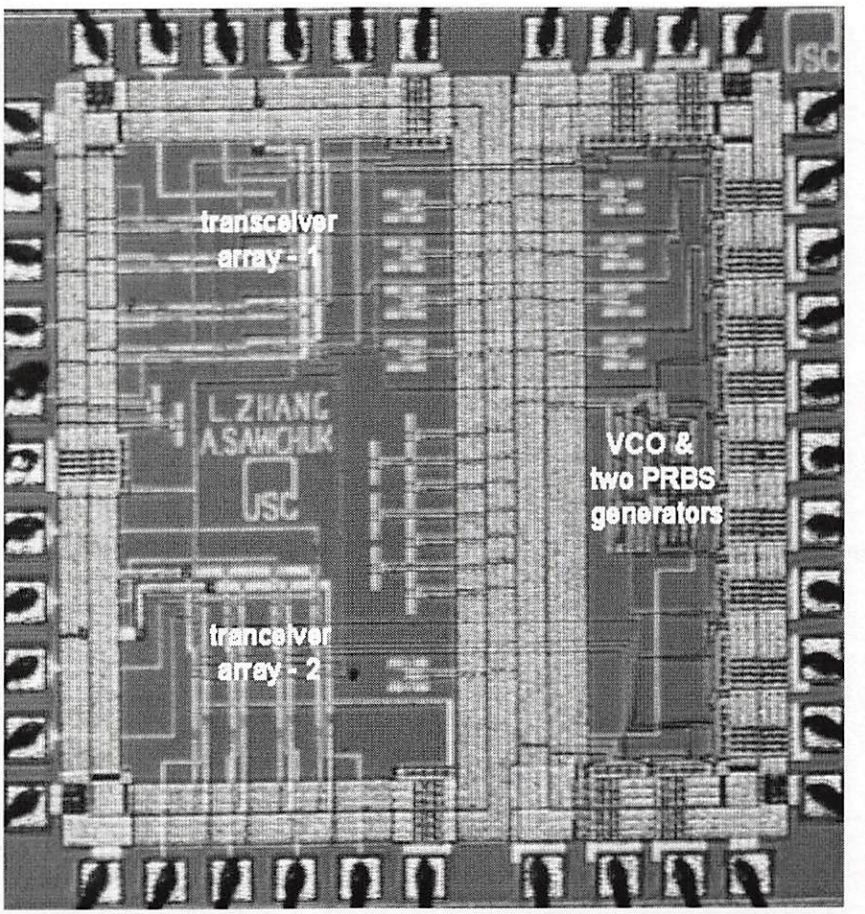
8.8 Chip Layout, Spectre Simulations and Photograph for 2000 UTSi Chip #1: Optical Transceiver Array with Built-In Self-Testing (BIST) LSI Circuits

The physical layout of the chip is shown in Fig. 8-5 (a), and Fig. 8-5 (b) is a photograph of the chip fabricated in 0.5-μm UTSi-SOS CMOS technology. The size of the full custom chip is 2x2 mm^2. The chip has two Electro-Static Discharge (ESD) rings - analog (left) and digital (right) ESD rings, two 4x1 optical transceiver and self-testing circuits. Full-custom physical layout of a chip is always a

combination of science and art. Special care had been taken in the physical layout, low parasitics in the receiver front-end has been obtained, and low crosstalk between neighboring receiver channels has been accomplished. Spectre transient simulation data-rate is over 4 Gbps.



(a)



(b)

Figure 8-5. (a) Chip layout of the 2000 UTSi-SOS optical transceiver arrays with BIST Circuits,(b) chip photograph of transceiver arrays with BIST circuits.

The circuit design, full custom physical layout, pre-layout and post-layout simulations were carried out in Cadence EDA tools. Figure 8-6 shows the transient response of the 2000 UTSi-SOS CMOS transceiver with BIST circuits. Up to 80 ns, the output signal of the receiver was fed into the VCSEL driver. After 80ns, the PRBS signal drives the VCSEL. In the meanwhile, the bias voltage of the VCSEL driver reduced to have a 0~9 *mA* current output. Due to the pad driver, the electrical output curve of the receiver circuit has larger rise and fall delays compared with the output signal measured before the output pad.

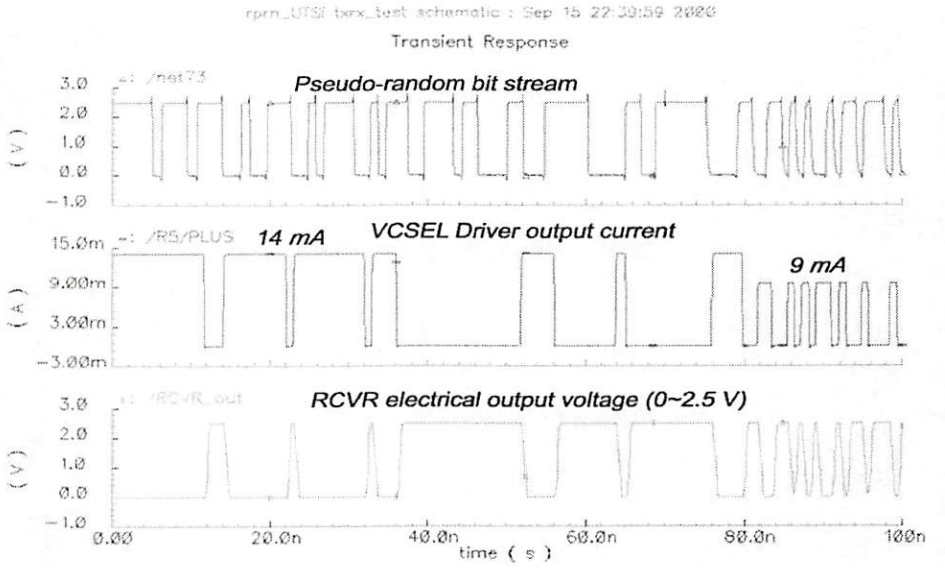


Figure 8-6. The Spectre transient response of a transceiver channel in 2000 SOS optical transceiver chip.

The VCSEL small signal model used in the simulation can be found in Chapter 6. A simple resistor array can replace VCSEL in electrical measurement. The simulated loop performance of single channel is over 4Gbps, which are promising for high-speed optical transmission system. Spectre simulation results of all the four channels showed 5 Gbps data rate considering the capacitance of the detector, capacitance of the bonding pad, and the inductance of the bonding wire.

8.9 Architecture and Design of 2000 UTSi Chip #2: the High-Speed 4x4 TDM Electrical Switching Optical Signal (ESOS) Chip

A critical component that is required for many photonic switching applications is smart switches with broadcast capability [Dias_88]. The counterpart of the optical switching fabric is the electrical switching optical signal (ESOS) fabric. The potential advantages of all-optical switching fabric include performance rate-independent and the elimination of OE and EO conversions. However, there are

challenges of scaling and immature technology in the all-optical approach. The pros of an ESOS fabric include more mature switching technology, and capability of managing traffic at lower level. The cons of ESOS are the cost and power dissipation, however these have become less significant with the latest advances in VLSI, smart pixel array technologies, and high-performance VCSEL/PD arrays.

We have designed 4x4 TDM switches incorporating the optical receiver and VCSEL arrays as optical I/Os. The functional block diagram is shown in Fig. 8-7. The on-chip four non-overlapping low frequency clocks enable the sequential transmission of the packets from input channels. For simplicity, each input packet has 8 bits, in which the least significant 2 bits represent destination address, the 3rd LSB bit is for broadcast, and the remaining bits are payload.

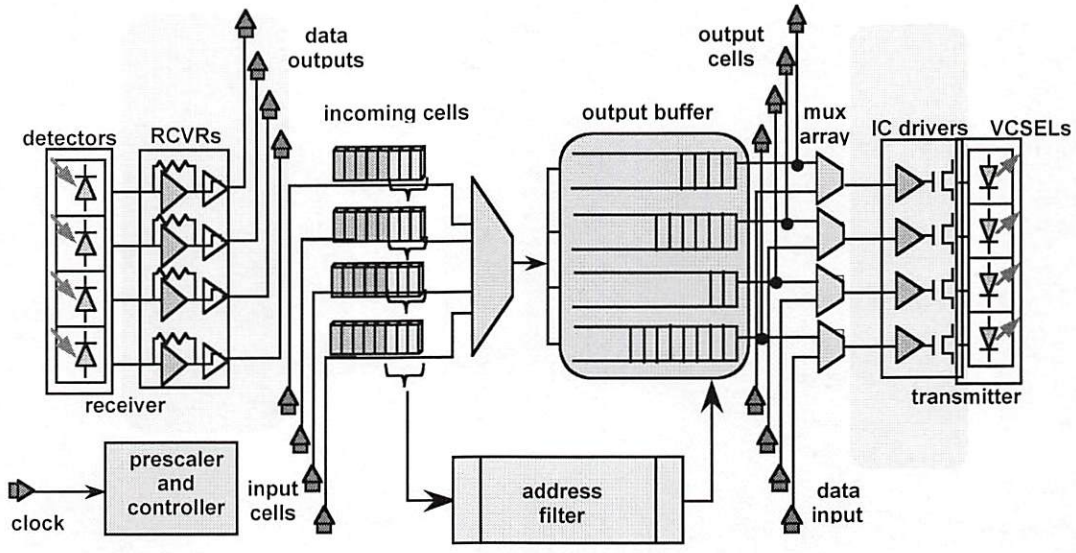
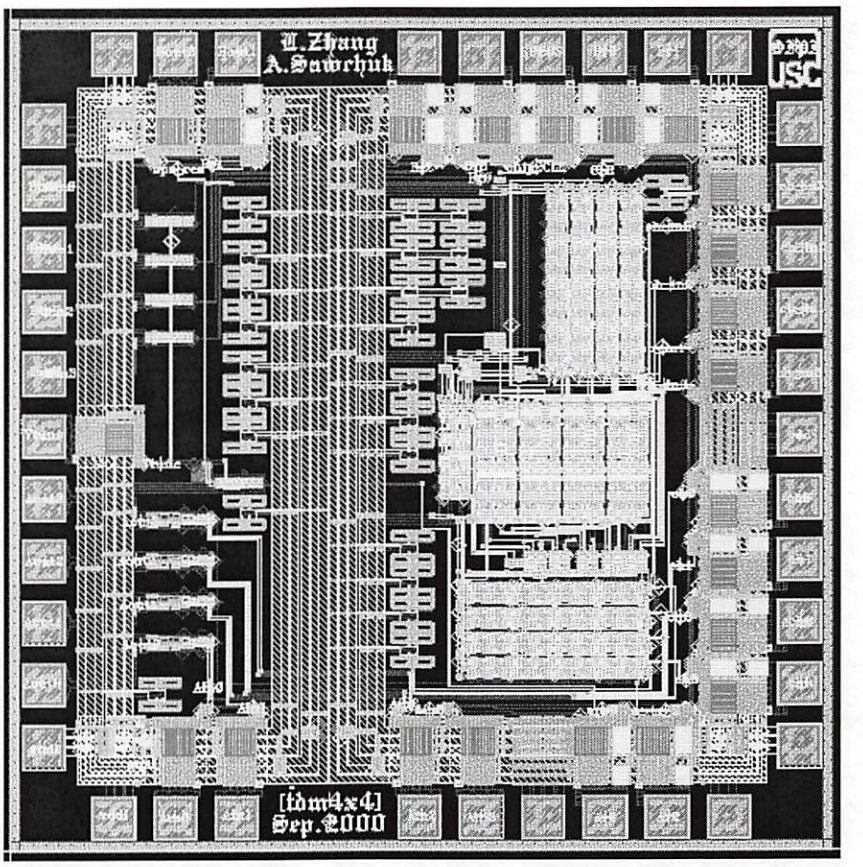


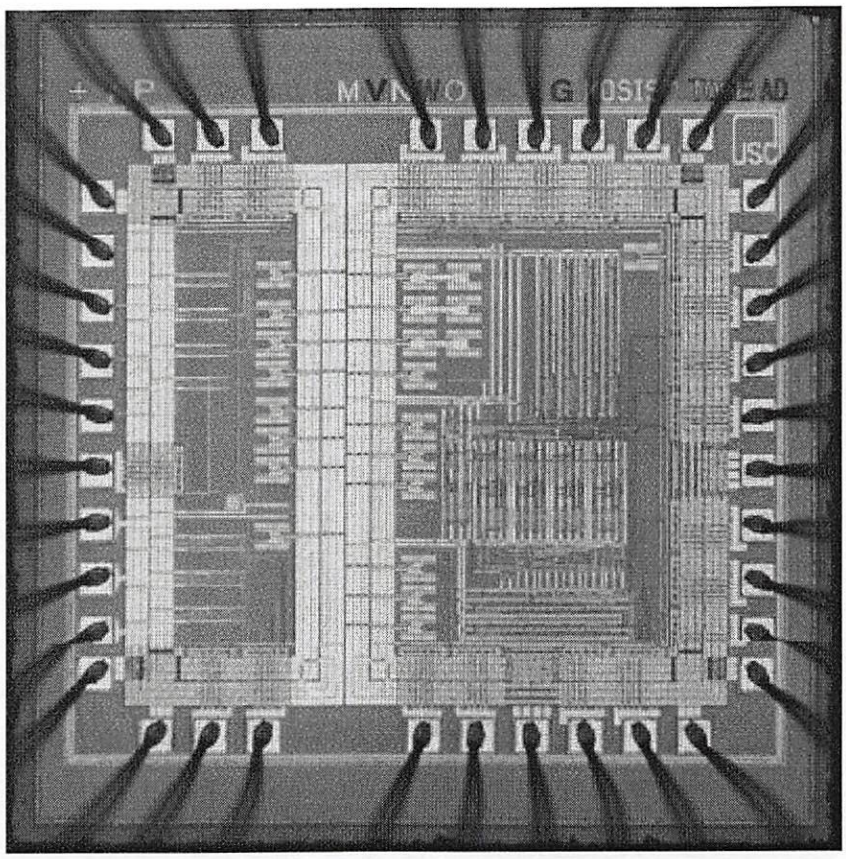
Figure 8-7. The functional block diagram of 2000 UTSi Chip #2: the 4x4 TDM ESOS smart switch with broadcast capability.

The incoming data packets for each input channel are sequentially streamed into a single data channel via a 4-to-1 multiplexer. The headers of the packets drop into the address filter to be decoded. The multiplexed data packets then transmit to the targeted output channel, or broadcast to all the channels, depending on its header. The output packets have an option to transmit electrically through the pads or optically through VCSEL driver and VCSEL arrays. On the same chip, we also designed a 4x1 receiver array with its corresponding electrical output pads. By connecting the receiver array output pads with the inputs of the TDM switch, without having off-chip high-speed signals, we obtain a 4x4 electrical switching optical signal chip module (optical input and optical output).

Figure 8-8 shows the chip layout and photograph of the 4x4 electrical switching optical signal TDMA switch. Besides the optical input and output, the chip also has electrical outputs form the TIA receivers, and electrical inputs to the VCSEL drivers. The multiplexed output of the TDMA switch output and the electrical input fan out to the VCSEL driver and thus has an option of optical transmission.



(a)



(b)

Figure 8-8. Chip layout of the 2000 UTSi-SOS 4x4 smart switch, (b) chip photograph of the TDMA ESOS 4x4 smart switch chip.

As shown in Fig. 8-8, the bare pads on the left side are electrically connections to the optical I/Os. Connecting to the four VCSEL bonding pads is the transmitter array, and receiver array associates with the bare pads of the photodiode array. The receiver and transmitter arrays share one ESD ring, and the 4x4 TDM switch is confined inside the other ESD ring to the right. This scheme allows the receiver and VCSEL driver array to have a cleaner power supply with less interference due to the high switching noise of the digital TDM switch. In addition, the decoupling capacitors attached to both rings also help to reduce the switching noise effectively.

8.10 ESD Protection for SOS UTSi chips

Electro Static Discharge (ESD) stresses the I/Os of a semiconductor VLSI chip with high-voltage and high-current [Bernstein_98]. High frequency and highly miniaturized active components are especially prone to damage by ESD. GaAs Multi-chip module integrated circuits (MMICs) also can be damaged by ESD and precautions must be taken. One significant source of ESD damage related to test environment is when statically charged components are inserted into the printed circuit board (PCB) after the static sensitive device. This static charge dumps into the PCB and can affect or damage any semiconductor in its path since most semiconductors on a PCB are connected to ground and are susceptible, because during the assembly the ground may be floating. Typically, electronic devices can be damaged when stressing as little as 20 Volts. However, a person walking across a carpet in a dry environment can generate (and discharge) as much as 35,000 Volts!

Electrostatic discharge is a critical issue in SOI technology due to the insulator. The significance of effective ESD prevention for SOI chip cannot be overemphasized. For the ESD protection, two ESD rings are designed. One is designed for the analog circuit and the other is for digital use.

8.11 2000 UTSi Chip #2 Test-Bed Design and Measurement

The test setup for the packaged chip is a four-layer high-speed PCB, consisting of power and ground layers, RF edge SMA connectors, microstrip transmission line impedance control and terminating resistors as shown in Fig. 8-9.

To interconnect several of them, VCSEL and photodetector arrays lie on opposite sides to facilitate free-space or fiber optics communication links.

Our initial tests of this chip have confirmed that the VCSEL driver and receiver worked at data rate of 100 Mbps. Figure 8-10 shows the measured results of the receiver array operated at 100 MHz in the test under the harsh environment of packaged chip-on-PCB, which was band-limited by the inputs from the test function generator. The eye diagrams of VCSEL driver array are shown in Fig. 8-11. We are planning to do die-on-PCB tests, which should operate at least 2.5 GHz as predicted by the SpectreRF simulations.

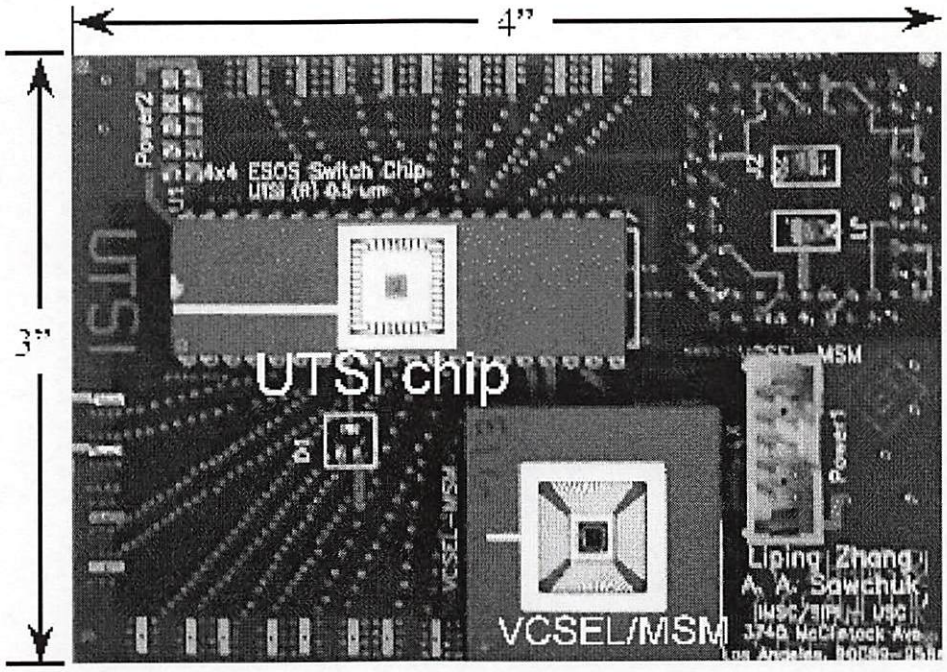


Figure 8-9. Four-layer high-speed test-bed for 2000 UTSi chip#2.

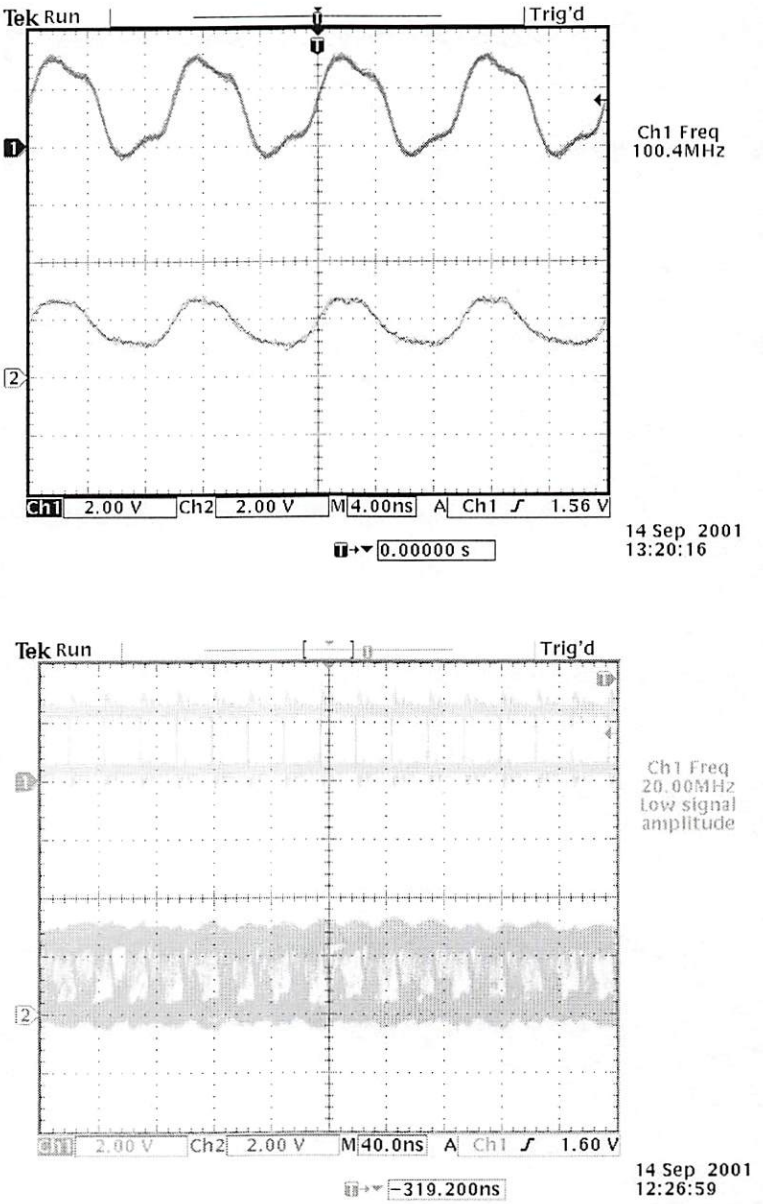


Figure 8-10. Measured results of 2000 UTSi Chip #2 receiver array (top) and VCSEL driver array (down) under packaged-chip-on-PCB environment.

The 2000 UTSi Chip #1 tests were performed under chip-inside-socket environment and the eye diagram at 100 MHz is shown in Fig. 8-11. These results were obtained by applying the maximum frequency signal from out functional generator, which is 100 MHz. Further multi-GHz high-frequency bare die test will be performed once multi-GHz test equipment is available.

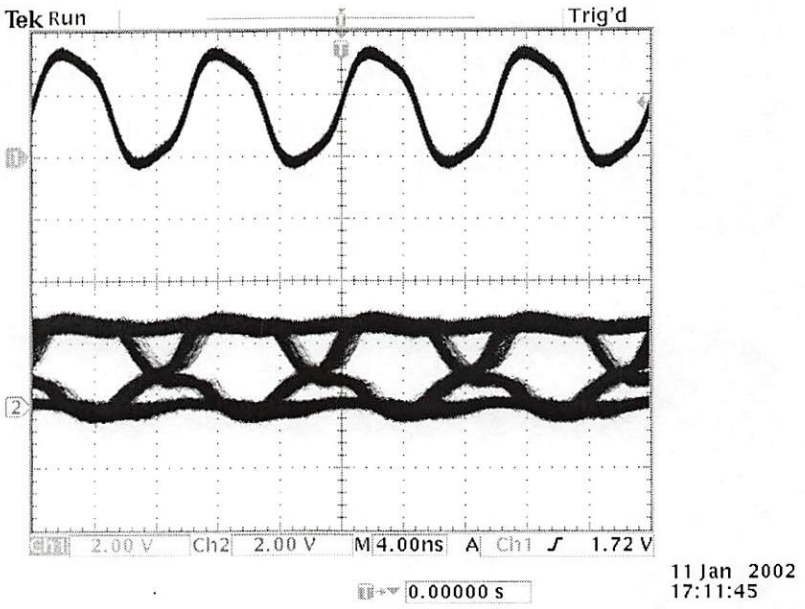


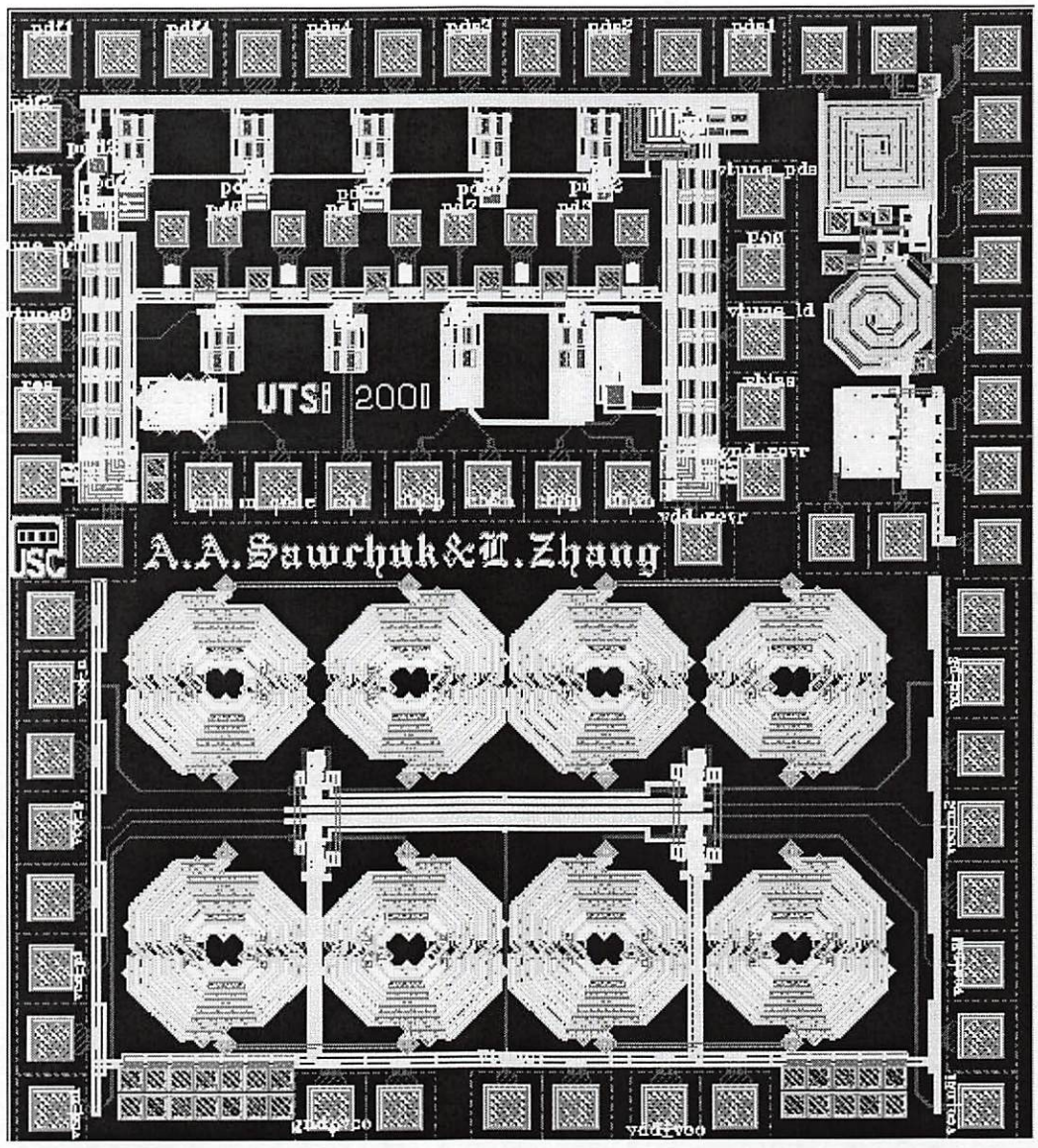
Figure 8-11. Measurement results of 2000 UTSi Chip #1 under chip-in-socket environment.

CHAPTER 9 UTSI-SOS ANALOG CIRCUIT DESIGNS FOR FLIP-CHIP TRANSCEIVER AND MONOLITHIC OPTICAL RECEIVER ARRAYS

9.1 The Block Diagram and Physical Layout of 2001 UTSi Chip #1 and Chip #2

In chapters 9 and 10, we discuss techniques for advanced integration of photodetectors and VCSELs with UTSi-SOS CMOS circuits. We present the design of two chips (2001 UTSi Chip #1 and 2001 UTSi Chip #2) on wireless and optical communications [Zhang_cleo]. This chapter describes the designs and layouts of flip-chip optical transceivers and full monolithic optical receivers with on-chip photodetectors. In the next chapter, other mixed-signal and RF circuits are described.

Figure 9-1 (a) and (b) shows the block diagram and physical layout of 2001 UTSi Chip #1 (the Flip-Chip Optical Transceiver, Monolithic Optical Receiver Array, and VCO SOS-Chip) respectively. It contains three different optical receiver designs intended for flip-chip bonding to 4 x 1 EMCORE positive-intrinsic-negative (pin) detector arrays. One is a single-ended transimpedance amplifier with a second order resistance feedback network for high gain and bandwidth. Another design has low voltage differential multi-GHz outputs. An optically clocked 2047-pattern pseudo-random bit-stream (PRBS) generator based on true-single phase clock (TSPC) D-flip-flops are included for built-in high frequency self-testing. Eight optical receivers have inputs from novel p-i-n UTSi-SOS photodiodes to test fully monolithic optical receiver designs.



(a)

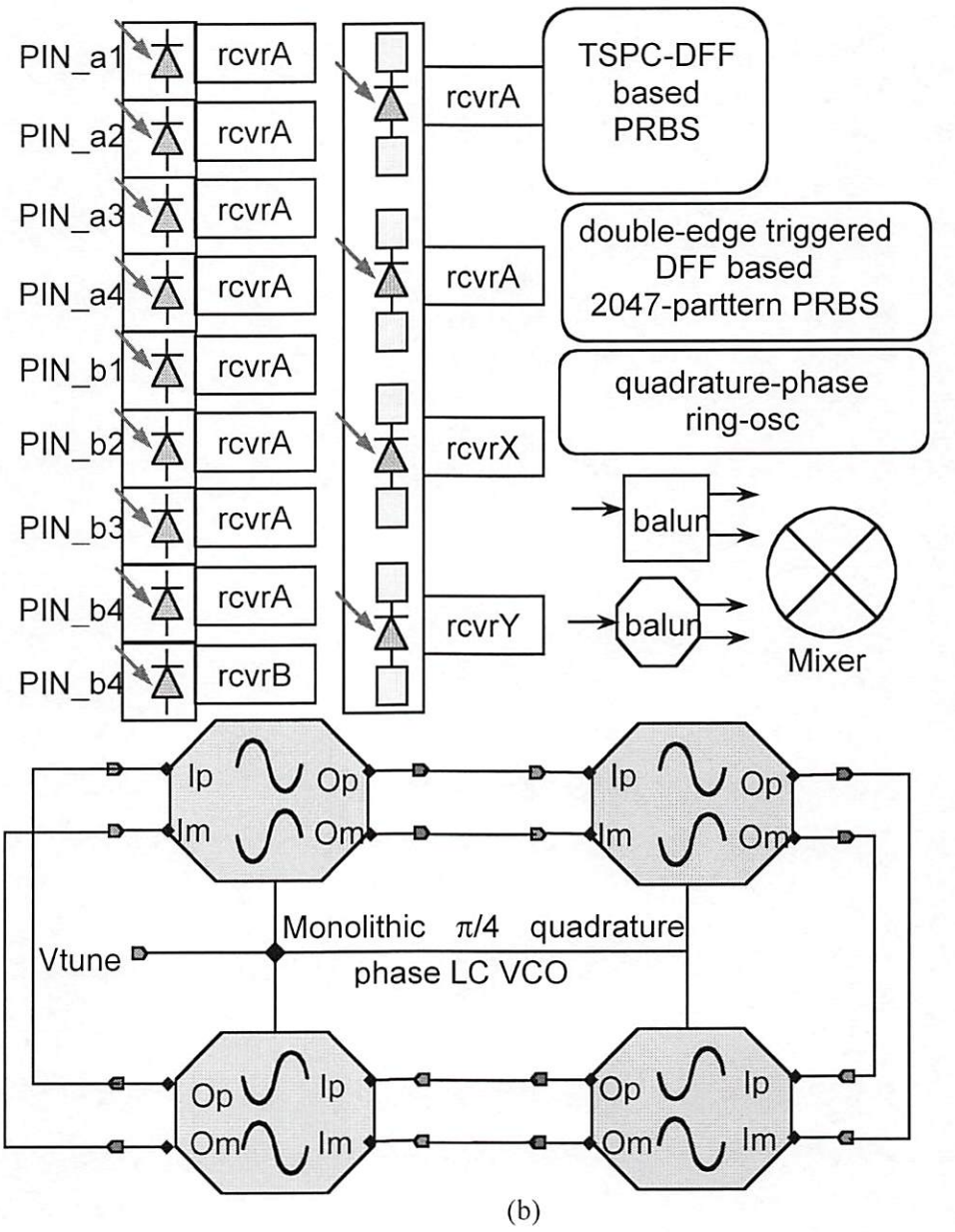


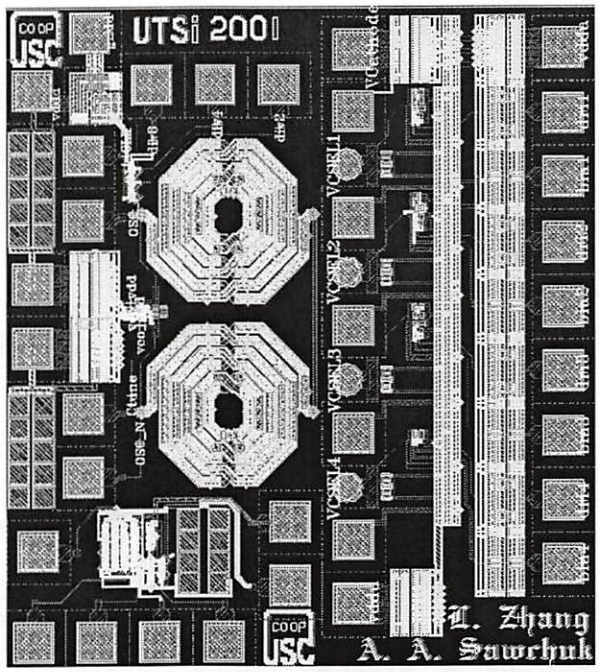
Figure 9-1. (a) Physical layout and (b) block diagram of the 2001 UTSi Chip #1: flip-chip, monolithic optical receiver arrays, quadrature-phase VCO, mixer and baluns.

On the top row are 9 monolithic UTSi SOI p-i-n photodiodes with integrated receivers. Over the corner is a mixer with two baluns, as single-ended to differential converter for better noise suppression. A double-edge triggered D-flip-flop based

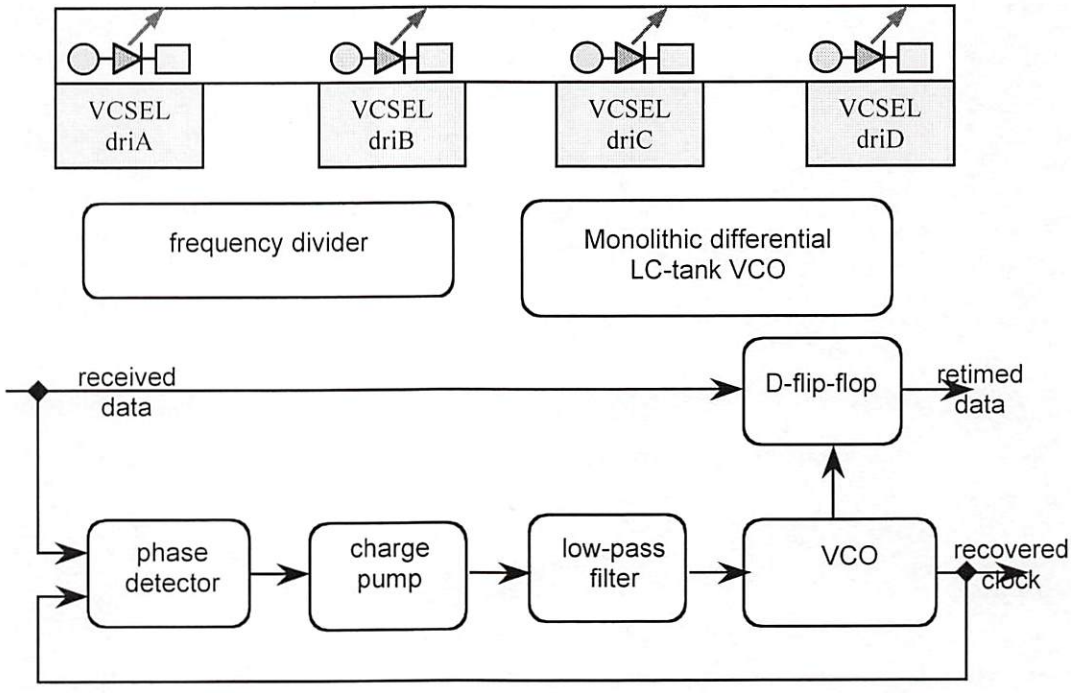
2047-pattern PRBS generator is next to it. The bottom half of the chip is the $\pi/4$ full differential LC-Tank VCO which gives eight phase outputs.

Physical layout and floor-planning is very significant to the performance of the transceiver arrays. To reduce the parasitic capacitance, receiver front ends have good proximity to the detector bonding pads. Between photodetector and receiver is very thin metal line. Each transceiver cell uses individual power line and on-chip power decoupling capacitors had been attached as many as allowed. For high frequency operation, ground-signal-ground structure is deployed and estimated minimal ESD protection is provided.

Figure 9-2 shows the layout of the 2001 UTSi CMOS flip-chip VCSEL driver array and differential LC-VCO chip. It includes a negative resistance-based, balanced differential LC-tank VCO with center frequency at 5 GHz, a multi-GHz frequency divider, a compact PLL-based CDR, and four distinct VCSEL drivers with 250 μm-pitch circular bonding pads for EMCORE VCSEL array, which has a common cathode but individual input and bias. The green squares are MIM power decoupling and low-pass filtering capacitors.



(a)



(b)

Figure 9-2. (a) Chip physical layout and (b) block diagram and of flip-chip VCSEL driver array and LC-tank VCO 2001 UTSi chip.

In summary, the two 2000 UTSi-SOS chips contain analog optoelectronic integrated circuit (OEIC) transceiver arrays, high-speed static and dynamic LSI circuits. The two 2001 UTSi-SOS chips contain high-speed digital, mixed-signal, analog, RF and OEIC circuits for wireless and optical communications. It has monolithic optical receivers and flip-chip optical transceiver arrays. We are among few of the first research groups to incorporate ultra-thin silicon-on-sapphire CMOS technology for optical transceiver modules, as a milestone towards full monolithic integrated VCSEL/MSM CMOS SPA systems.

9.2 Flip-Chip VCSEL and PD with UTSi-SOS CMOS ICs

Ultra-thin silicon-on-sapphire CMOS technology can produce high performance optical communication integrated circuits and systems on a transparent sapphire substrate, which allows flip-chip bonding of both surface emitting or bottom emitting lasers in a 3-D stack optoelectronic interconnection configuration. This unprecedented optically transparent characteristic is unique among any other semiconductor technologies to date. Flip-chip bonding can effectively eliminate bonding wire inductance, the major band-limiting factor in wire-bonding integration. The fully insulating substrate in UTSi technology enables high degree of isolation between the μA current of an optical detector and the mA current needed for VCSEL driver arrays.

Flip-chip bonding is a reliable, mature, and preferred technique for hybrid device integration. This flip-chip bonding structure is also reliable and easy to package. It works as follows: solder balls of precise dimensions are laid on the wettable metal pads of chips to be bonded. When the solder balls are melted, surface

tension forces bring the structure into alignment, and bond one chip to another. Figure 9-3 illustrates the structure of wafer level flip-chip bonding optical devices onto UTSi-SOS CMOS smart pixel arrays circuits.

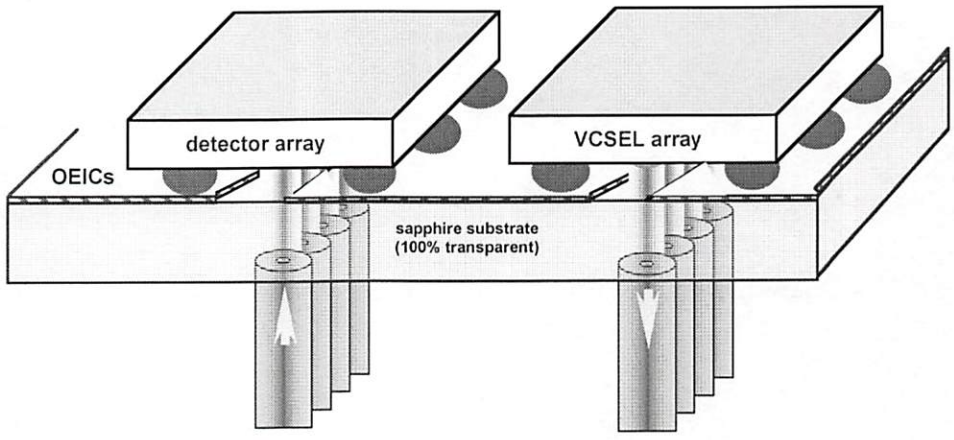


Figure 9-3. Wafer level flip-chip bonding optical devices to UTSi OEICs.

VCSEL or photodetector arrays are flip-chip bump-bonded onto a SOS wafer, and fiber arrays (or fiber image guide) are aligned with the optical windows of the optical devices, which direct the optical beams in and out through the transparent sapphire substrate. There are several advantages of the flip-chip architecture. First, the fiber array can be attached to the substrate to direct optical beams into the detector or pick up optical signals from the VCSEL cavity. Secondly, microlens arrays can be directly etched into the sapphire where the fiber arrays are attached. Finally, the top and bottom of the sapphire substrate can have an antireflective coating to increase optical power efficiency. With the availability of ultra-high bandwidth VCSEL and detector arrays, the bandwidth of such a system is largely dependent on its OE interfaces, particularly optical transceivers.

In our dedicated 2001 COOP-USC-Peregrine foundry run, we have designed and fabricated two chips containing digital, analog, mixed-signal and RF circuits. One chip (2001 UTSi Chip #1) contains a flip-chip 4 x 1 receiver array, 9 monolithic optical receivers, a quadrature phase VCO, single and double edge triggered dynamic D-flip-flop based pseudo-random bit streams, mixer and baluns. The other (2001 UTSi Chip #2) contains a flip-chip VCSEL driver array, a full differential LC-tank VCO, and a clock date recovery (CDR) circuit based on a phase-locked loop (PLL). Almost all these circuit designs are unique and novel. In this and the next chapter, we describe the design and simulation of the flip-chip optical transceiver and monolithic optical receiver arrays that are being fabricated in 0.5-μm CMOS UTSi SOS technology.

9.3 Flip-Chip Single-Ended and Low-Voltage Differential Signaling Transimpedance Receiver Array Designs

We have designed and fabricated several novel optical receivers intended for flip-chip bonding to 4 x 1 EMCORE p-i-n detector arrays. One of them (design A) is a single-ended transimpedance amplifier with a second-order negative resistance feedback network for better stability, high gain and bandwidth. Another design B has low voltage differential signal (LVDS) outputs. The circuit diagrams of the receiver designs are shown in Figs. 9-4 and 9-5. The second-order global feedback loop poses a stability challenge in the circuit design. The sizes of the resistors are optimized and first-order feedback is added to ensure the second pole is far away from the first pole.

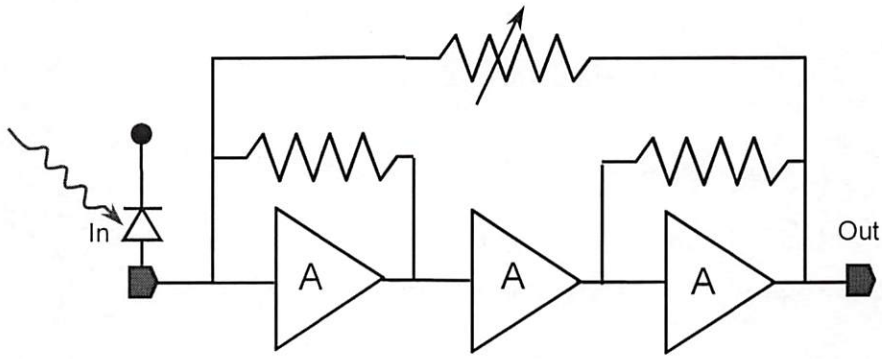


Figure 9-4. Receiver design A: a novel single-ended optical receiver design with 2nd-order tunable resistance feedback.

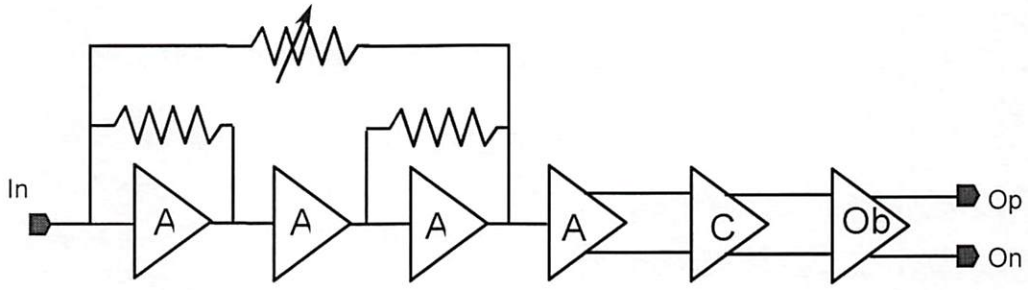


Figure 9-5. An optical receiver design with differential LVDS outputs.

A novel 2047-pattern pseudo-random bit-stream (PRBS) generator based on true-single phase clock (TSPC) D-flip-flops are designed and the output of one of the designs as its clock input thus form an optical clocked PRBS generator for built-in high frequency self-testing. Figure 9-3 shows the circuit diagram of the design with LVDS differential outputs. The differential stage contains comparator and output driver stages.

9.4 Monolithic PIN Photoreceiver Array Design

As shown in Fig. 9-2, eight novel positive-intrinsic-negative (PIN) photodiodes were developed in ultra-thin silicon-on-sapphire technology and eight single-ended optical transimpedance amplifier receivers described earlier have been connected to the UTSi PIN photodiode. The eight photodiodes are of a variety of different shapes and structures. Mainly two geometric types were selected, one is spiral, the other is finger-shaped. The direction of optical beam can be either normal to the surface or the substrate of the SOS wafer. The combinations of the optical beam direction and shape produce eight different photodiode designs.

Figure 9-6 shows a third design - the differential LVDS outputs stage for one of the monolithic optical receiver.

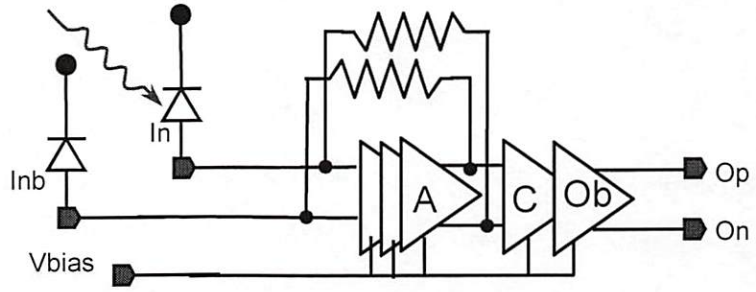


Figure 9-6. Differential LVDS outputs stage for monolithic optical receiver.

The optical receivers for the photodiodes include the multi-GHz single-ended transimpedance amplifier receiver with second-order negative resistance feedback network.

9.5 Optical-Clocked PRBS Generator and PRBS Generator Based on Double-Edge Triggered D-Flip-Flop

A very fast novel dynamic double-edge triggered D-flip-flop cell was designed and post layout simulated. The physical layout is 600 μm x 800 μm in 0.5 μm CMOS SOS technology. A 2047-pattern PRBS functional generator based on this cell has been designed on chip for testing the optical receiver circuitry at several GHz frequencies. The circuit diagram of the optically clocked PRBS generator is shown in Fig. 9-7, where the detected optical clock trigger the PRBS circuits and output NRZ pseudo-random bit streams.

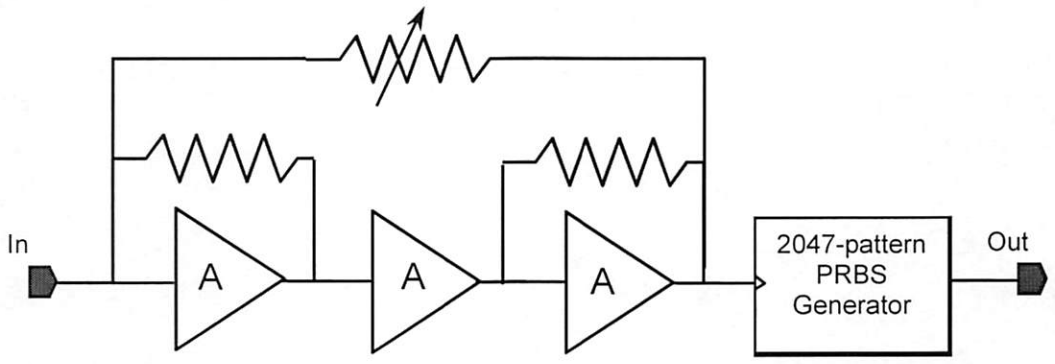


Figure 9-7. The circuit diagram of the optically clocked PRBS generator.

9.6 CMOS SOS Flip-Chip VCSEL Driver Array Designs

Wafer-level flip chips provide an innovative solution in establishing flip-chip as a standard surface-mount process [Lu_01]. Two-dimensional (2-D) parallel optical interconnects (POIs) which utilize either free-space or guided-wave enable high-density, high-bandwidth communications between very large scale OEIC chips [Goodman_84], [Tooley_96]. 2-D-POI technologies have experienced significant progress in recent years, primarily due to the advances made in optoelectronic-VLSI

(OE-VLSI) and optical semiconductor device technologies. Large 2-D arrays of surface-normal devices (such as vertical cavity surface-emitting lasers and electroabsorption modulators) are now routinely flip-chipped to foundry CMOS chips [Krishnamoorthy_99] [Ayliffe_01][Krishnamoorthy_98].

One VCSEL driver on 2001 UTSi Chip #2 is a transimpedance amplifier followed by a PMOS differential pair amplifier, one of the differential inputs connects to the bias and the other connects to the low-voltage output from the preamplifier, which modulates the gate of one of the p-transistor. The bias voltage on the other P-MOSFET provides a bias dc current. The tail current of the differential pair drives the VCSEL.

Four distinct VCSEL drivers formed a 4 x 1 array, with each output connected to a VCSEL anode bond pad. Each element of the array has individual input and bias control, and shares a common cathode and power supplies.

9.7 Spectre Simulation Results of the UTSI-SOS Flip-Chip Optical Receiver and VCSEL Driver Array Designs

A 3 GHz operation has been obtained in the post-layout Spectre simulations for the receiver designs after parasitics extractions. Figure 9-8 and 9-9 show the SpectreRF transient response for differential receiver X and receiver Y.

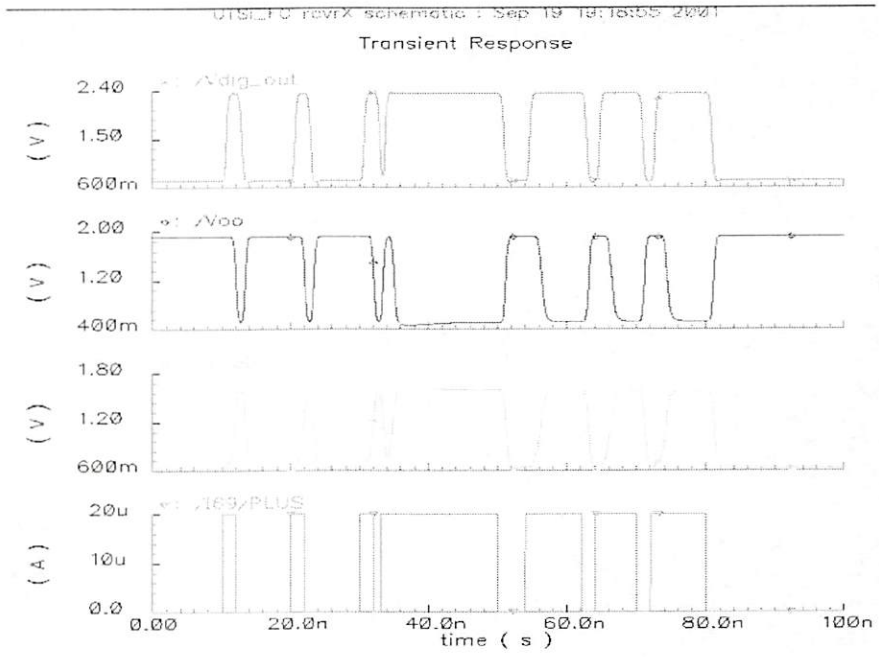


Figure 9-8. Spectre simulations for the single-ended receiver designs with extracted parasitics.

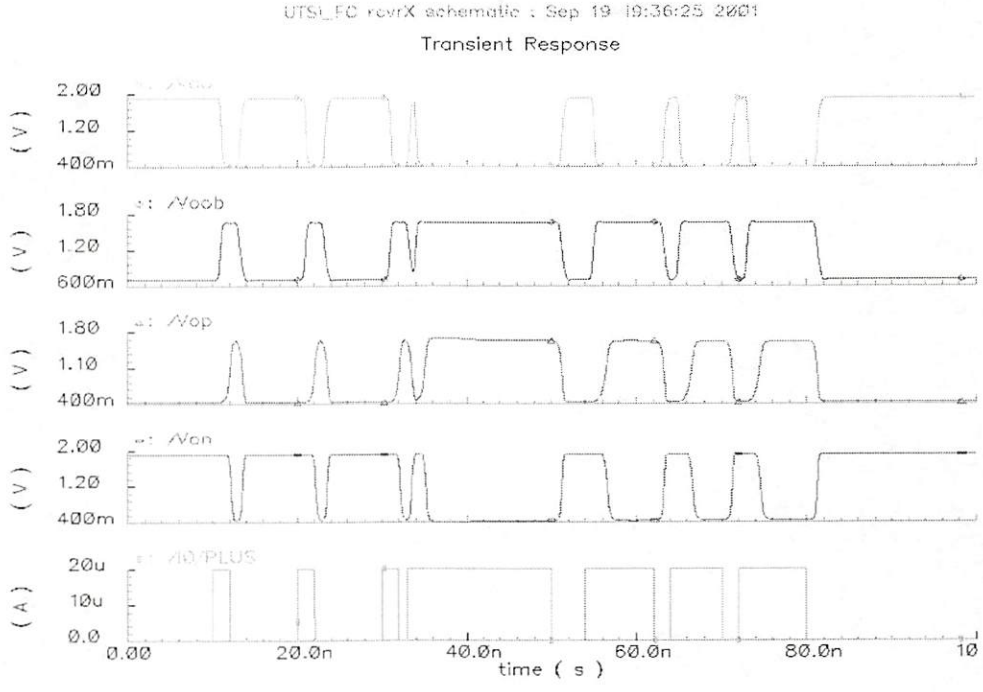


Figure 9-9. Spectre simulations for the LVDS receiver designs with extracted parasitics.

CHAPTER 10 MONOLITHIC RF π/4 DIFFERENTIAL, QUADRATURE PHASE, MULTI-PHASE VCOS, AND PLL-BASED CDR CIRCUIT DESIGNS IN SILICON ON SAPPHIRE

10.1 Introduction

Besides the optical receiver, VCSEL driver arrays, RF mixer baluns, and PLL based clock and data recovery circuits, 2001 UTSi Chip #1 also contain the π/4 quadrature phase VCO, and 2001 UTSi Chip #2 also contain a fully balanced differential LC-tank VCO. This chapter presents the theoretical design, modeling and fabrication of novel full-balanced, differential, π/4 quadratic-, and multi-phase LC-tank voltage-controlled oscillators (VCOs) for microwave phase-locked loop (PLL) frequency synthesizers, wireless, and optical communications. We present a generalized differential VCO design methodology based-on traveling wave theory. The monolithic VCOs are designed and fabricated in 0.5-μm Peregrine Semiconductor Ultra-Thin Silicon (UTSi®) on sapphire CMOS technology.

The varactor-based quadrature VCO has a simulated phase-noise of less than -110 dB at 1 *MHz* offset frequency from a ~5 GHz carrier, with less than 5 mW power consumption at nominal 3-V voltage supply. The outputs are peak-to-peak signals of 3-V which are enough for mixer circuits operating in the linear region or being accepted by current mode differential logic and other low voltage differential logic.

As wireless and optical communications systems grow rapidly, there are increasing demands for highly integrated, low-power, ultra-high bandwidth communication RFICs or OEICs (optoelectronic integrated circuits). Examples include 5 GHz band multimedia wireless systems based on the IEEE 802.11 standard. Among them, high frequency-band monolithic VCOs are necessary to minimize the size of PLL frequency synthesizers, which are intrinsic to modern microwave and optical communication systems in frequencies above 10 GHz. VCOs are one of the most challenging circuits for monolithic CMOS integration. Low phase-noise is essential for low interference with neighbor channels having compact channel spacing. High spectral purity VCOs are well known to be the crucial components in RF transceivers and clock and data recovery (CDR) circuits. Many monolithic VCOs based-on SiGe bipolar or AlGaAs/GaAs HBTs have been reported [Kyranas_00]. However, it is more desirable to implement them in mainstream CMOS technology, so that channel coding, modulation and other data processing can be processed on the same chip monolithically.

Ultra-Thin Silicon-on-Sapphire (UTSi-SOS) CMOS technology is capable of monolithically integrating high-speed digital, analogy, mixed-signal and RF devices on the same substrate. The fully insulating lossless synthetic sapphire substrate allows monolithic higher-Q inductors to be produced. Thus low noise and precise quadrature phase outputs required by many other systems, especially single-sideband communication systems, can be accomplished.

10.2 Monolithic CMOS SOS LC-Tank VCO Design

The local oscillator is one of the essential elements for optical communications at frequency exceeding 10 GHz, where additive white Gaussian noise (AWGN) is one of the key factors to the bandwidth and bit error rate of the entire system. Monolithic high-Q Inductors are critical for having enough low phase-noise to ensure low interference between channels. Bulk CMOS on-chip inductors fabricated on a standard CMOS lossy substrate have a relatively low Q, and may require some shielding and lift-off design and fabrication techniques.

10.2.1 Phase Noise of LC-Tank VCO

A LC-VCO consists of a resonance LC-tank circuit and an active element canceling the losses in the tank to maintain oscillation. The desirable properties of a VCO include: low-phase and output noise, high-linearity, low-temperature-drift, high-degree of spectral purity with sinusoidal output. Furthermore, stable oscillation and high-frequency wideband performance are required for VCOs. Phase noise and power consumption in VCOs are important parameters as can be seen from the Figure of Merit (F_oM) equation defined by [Kinget_99]

$$F_oM = 10 \cdot \log((\frac{f_0}{\Delta f})^2 \cdot \frac{1}{L(\Delta f) \cdot P}) \tag{10-1}$$

where, Δf is the offset frequency, f_0 is the carrier frequency, $L(\Delta f)$is the phase noise, and P is the power consumption. Equation (9-1) shows that low phase noise and low power dissipation are critical to the overall performance. The most effective parameter to improve phase-noise is to increase the quality factor Q of the LC-tank.

At constant phase-noise, a higher Q allows less signal power and lower power consumption. Varactor-based LC-tank VCOs have high Q and low phase-noise.

10.2.2 Design of a Differential LC-Tank VCO

Figure 10-1 shows the schematic of a differential LC-tank VCO that we have designed. To achieve low phase noise at high frequency, two pairs of MOS varactors D1, D2 are coupled to the oscillator nodes and the oscillator is tuned through the backgate of the two MOS varactors. The circuit is a monolithic MOSFET LC oscillator consisting of two cross-coupled pair of FETs with current tail source. Thus, the varactor capacitance is averaged over the oscillator swing and the VCO tuning is linearized effectively. The series resistance of the varactor is negligible and the only varactor parameters of interest are the maximum and minimum tunable capacitance. In simulations using SpectreRF, the phase-noise of the VCO is less than -120 dBc/Hz at 1 MHz offset frequency from its carrier, and the power consumption is less than 5 mW as shown in Fig. 10-2.

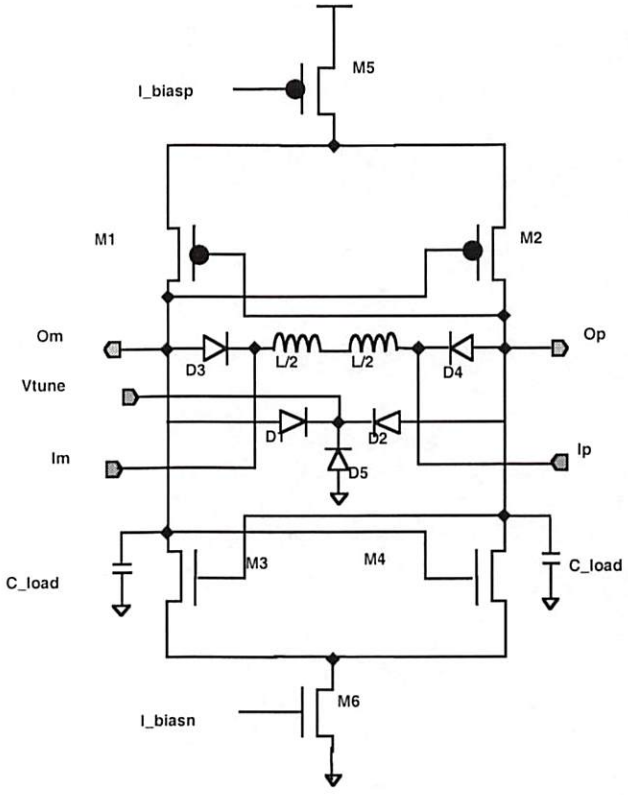


Figure 10-1. VCO cell schematic.

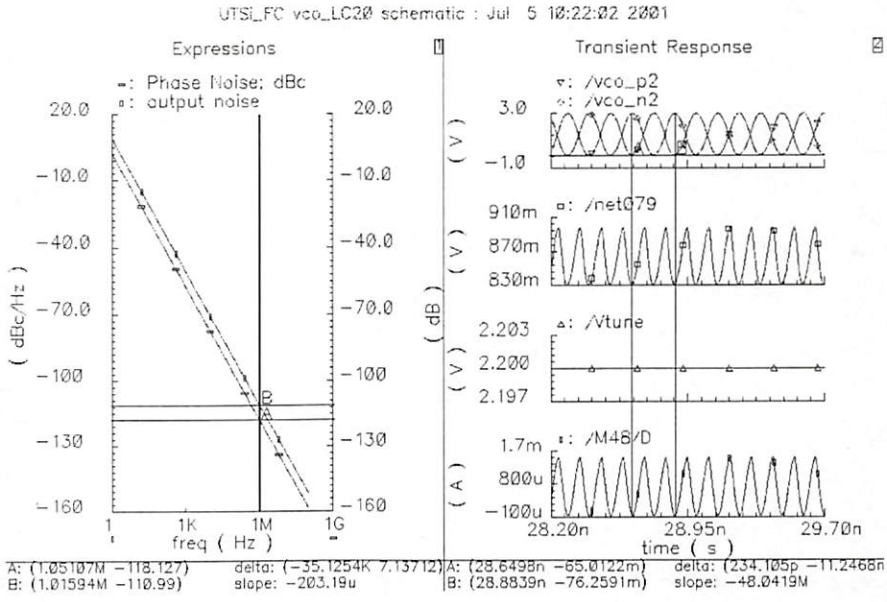


Figure 10-2. SpectreRF results of differential VCO Phase-noise, output-noise (left) and transient response (right).

10.3 Precise π/4 Differential Quadrature-Phase VCO

A novel quadrature-phase LC-tank VCO was designed for quadrature phase modulator in single-sideband communication systems or multi-phase clocks in microprocessor. This VCO design uses balanced symmetric inductors and was developed using traveling wave superposition and circuit theorems. It cascades an even number of differential oscillator cells as a daisy chain and cross-connects one of them to form a ring. The coupling of direct-connected pair of cells make the next stage in-phase, while the coupling of cross-connected pairs of cells makes the next stage anti-phase.

Unlike conventional differential quadrature phase shift keying (DQPSK) that has four possible phase states, π/4-DPSK has eight possible phase states [Farag_99]. Compared with quadrature VCO design based on CMOS inverter or differential current model logic (CML) inverter delay cells, this design has precise quadrature phase, equal rising and falling clock edge, and exactly 50 % duty cycle.

The schematic of the π/4 Differential Quadrature-Phase (DQP) VCO is shown in Fig. 10-3. By connecting four single differential VCO cells, terminals Im, Ip as differential inputs (floating in case of a single-phase VCO) from previous stages, and terminals Om, Op as the outputs to the next stage, a precise π/4 differential quadrature-phase VCO can be obtained. This varactor-based π/4 quadrature VCO has simulated phase-noise of less than -110 dBc/Hz at 1 MHz offset frequency from a ~5 GHz carrier, with less than 3 mW power consumption at

nominal 3-V voltage supply. The outputs are 3 V peak-to-peak signals which are enough for mixers to operate in linear region or to drive current mode or low voltage differential logic.

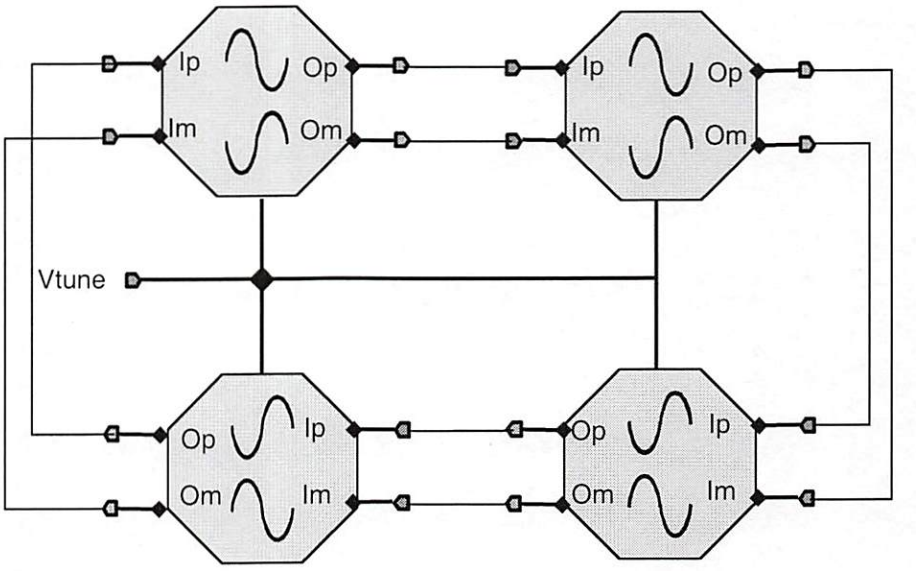


Figure 10-3. Schematic of the π/4 differential quadrature-phase VCO.

10.4 Multi-Phase VCO Design

By cascading 2n (where n is an integer) differential LC oscillators as a daisy chain, and cross coupling any one of them to make a loop, we can precisely obtain 4n phase outputs. The circuits are shown in Fig. 10-4. This design was developed using traveling wave superposition and circuit theorems, where in-phase waves enhance each other, and antiphase waves compromise one another [Zhang_iscas].

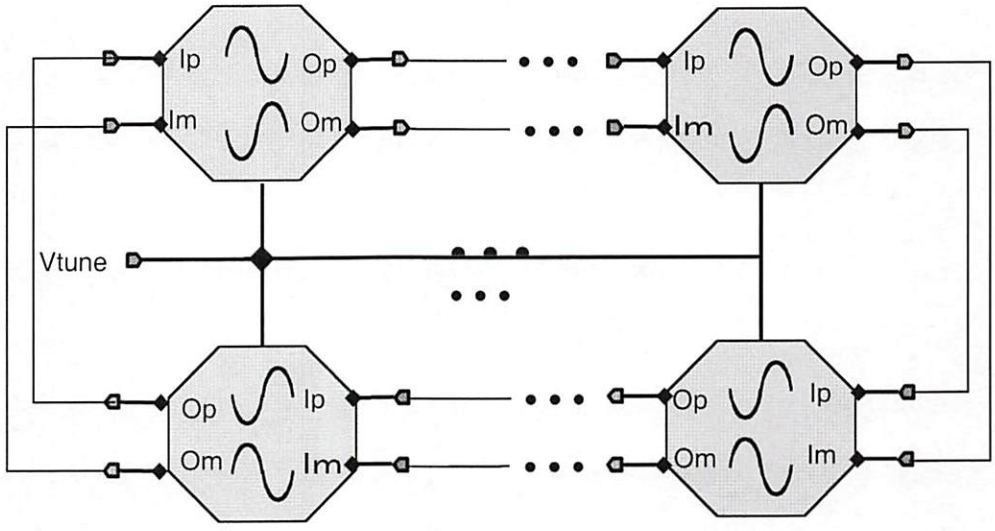


Figure 10-4. Schematic of differential multiphase 2n-phase VCO.

The coupling of the direct-connected pairs of waves leads the next stage in-phase, while the coupling of the cross-connected pairs of waves leads the next stage to be anti-phase. The balanced even number daisy-chain cascade connected oscillator distributes the anti-phase from the only cross coupling evenly over the ring.

10.5 Spectre RF Simulations on AC Transient, Phase and Output Noise

The Spectre RF simulations of the transient response, periodic small signal (PSS) simulations for phase and output noise results are shown in Fig. 10-5. The phase and output noise is shown at the left and the transient response on the right half of the figures. The tune voltage is set to be 2.2 V to keep the diode inverse biasing as varactor. The voltage supply is 3 V and the average current drawn from the power supply is about 800 μA. π/4-differential quadrature phase outputs have many advantages over differential quadrature phase outputs and can be utilized in a differential phase shift keying modulator.

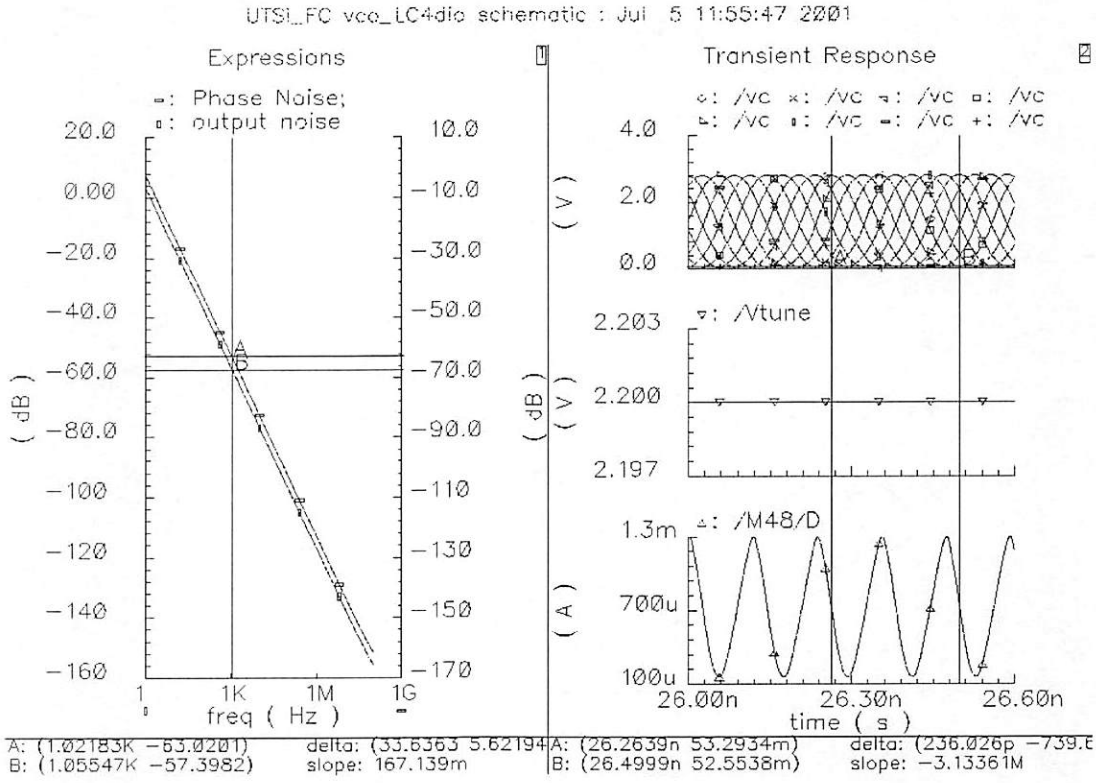


Figure 10-5. SpectreRF of the output noise, phase noise and transient response for the π/4 differential quadrature-phase VCO.

The physical layout of the fully symmetric quadrature-phase output VCO is located at the bottom half of 2001 UTSi Chip # 1. As measured from the layout, the quadrature phase VCO chip area is about 1 mm x 600 um with bonding pads. The prototype device and the test board will be assembled using a die-on-PCB technique, in which the bare die is flip-chip bonded directly onto the printed circuit board.

10.6 Phase-Locked Loop (PLL) Based Clock Data Recovery (CDR)

A PLL (phase-locked loop) is used to synchronize the output signal of the oscillator with a reference or input signal both in frequency and in phase. After being synchronized, or locked state, the phase error is reduced to a minimum. The

classical analog or digital PLL consists of three basic functional blocks - phase detector, loop filter, and current/voltage-controlled oscillator (ICO/VCO).

The VCO oscillates at an angular frequency of ω_2, determined by the output signal u_f of the loop filter. The angular frequency is given by

$$\omega_2 (t) = \omega_0 + K_0 * u_f(t) \qquad (10\text{-}2)$$

where ω_0 is the center frequency of the VCO and K_0 is the gain of the VCO in $s^{-1}V^{-1}$ [Best_99].

The phase detector compares the phase of the VCO output signal with that of the referenced input signal and output a signal $u_d(t)$ which is approximately proportional to the phase error θ_e as long as it is inside the limit.

$$u_d(t) = K_d * \theta_e \qquad (10\text{-}3)$$

where K_d represents the gain of the phase detector in $Vrad^{-1}$. $u_d(t)$ consists of a DC component and a undesired superimposed AC component, which will be cancelled by the loop filter.

The entire PLL system works as follows, we assume that the angular frequency of the input signal is equal to the center frequency ω_0. Then the VCO operates at its center frequency, and the phase error will be eventually zero, which is the prerequisite for the VCO to operate at its center frequency. If the phase error is not zero initially, the PD outputs a nonzero signal u_d, after a while, the loop filter

would also produce a finite signal u_f to tune the VCO and change its operating frequency correspondingly until the phase error vanishes. Now assume the frequency of the input signal changed by + $\Delta\omega$. The phase of the referenced input signal will then starts to lead the phase of the VCO output signal and the phase error appears and increases. Then the output signal of the PD starts to rise as well, so does the output of the loop filter, which cause the frequency of the VCO to increase. Thus the phase error decrease, after the settling time, the VCO will operate at exactly the frequency of the input signal. Depending on the design of the loop filter, the phase error in looked-state should be either zero or a constant value.

One of the most intriguing capabilities of the PLL is the input noise suppression [Lee_01]. Suppose the input signal of the PLL is buried in noises, which cause the zero crossing of the input signal to lead or lag stochastically. This causes the output of the PD to jitter around an average value. If the corner frequency of the PD is low enough, no noise will be noticeable in the output of the loop filter, and the phase of the VCO output will be equal to the average of the phase of the input signal.

The Clock Data Recovery (CDR) circuit contains a phase-frequency detector, charge pump, VCO to extract the clock from the incoming data channel, and a TSPC-D-flip-flop for data retiming. The block diagram of the CDR is shown in Fig. 10-6.

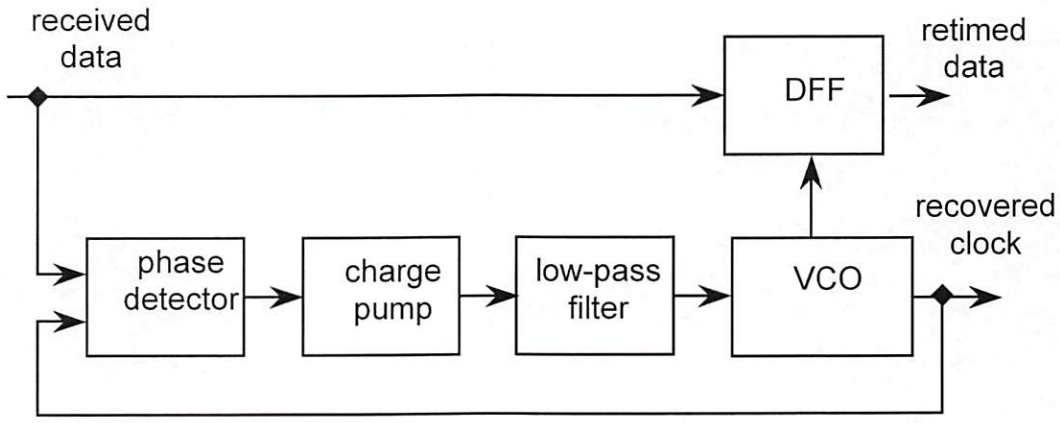


Figure 10-6. Block diagram of the PLL-based clock date recovery (CDR) circuit.

10.7 UTSi-SOS Chip Packaging

There are mainly three packaging methods, namely, wire bonding, flip-chip bonding, and multi-chip module. Wire bonding (typical 2nH parasitic inductance) method welds tiny bonding wires between the chip pads on two unsealed dies. It is mechanically simple with tolerance of the locations of the pads but introduce larger parasitics. Flip-chip bonding technology first places solder balls on each chip attachment pad. The chip is then placed face down onto the other chip, and solder is directly reflowed in place. Flip-chip bonding is electrically ideal because of the low parasitics (typically 0.05 pF and 0.05 nH) due to the very short bonding length. Figure 10-9 shows a multi-chip-module (MCM) die-on-PCB packaging of UTSi transceiver array chip with VCSEL/PDs. We anticipate that the Die-On-PCB (DOP) multi-chip module approach would have lowest parasitic capacitance and inductance. Our die-on-PCB MCM consists of the following dies: detector array, optical receiver array, 4x4 electrical switching optical module, and VCSEL array. These dies will be flip-chip bonded onto the SOS wafer.

Another optional packaging method is to use an optoelectronic chip carrier (OCC) with optical waveguides. The optical waveguides will route light from an input fiber ribbon to the detectors and from VCSELs to an output fiber ribbon. On the other end of those waveguides, there are tuning mirrors, which reflect light out of the plane to the detector or reflect the light from VCSEL to the guide. This method will be adopted as we see whenever is necessary.

10.8 Summary of UTSi Mixed-Signal and RF Circuit Designs

This chapter presents precise single-, $\pi/4$ quadrature- phase output differential UTSi-SOS LC-tank monolithic VCO designs of very low phase-noise, low power consumption, and multi-GHz operation. The design theory can be extended to design LC high frequency VCOs with any even number of phase outputs. Beside the precise quadrature–phase, the simulation results show that the balanced, cross-coupled ring architecture can further suppress the phase noise (through filtering, attenuation) and enhance spectral purity. The novel $\pi/4$ differential quadrature-phase LC-VCO with center frequency at 5 GHz can be used in a DQPSK modulator and achieve optical communication link of 20 GHz.

CHAPTER 11 SUMMARY AND FUTURE WORK

11.1 Summary of R-TRANSPAR Network Platform and High Throughput Multi-Token-Ring Network

We have designed, implemented, and tested a reconfigurable translucent smart pixel array (R-TRANSPAR) universal signal processing and networking platform. We have also designed a novel optoelectronic multi-token-ring (OE-MTR) network, where each node is implemented by the R-TRANSPAR platform. The optoelectronic multi-token-ring network has been verified and demonstrated for 3D optical parallel data packet add/drop, retransmission and other signal processing, networking functions. The R-TRANPAR is designed as an array of 2-D reconfigurable signal processing and networking elements, each with parallel optical data packet input/output. This research demonstrates steps towards monolithically integrated smart pixel arrays with active sources. The R-TRANSPAR system is a universal test-bed for networking and signal processing. It is the intermediate system before the monolithic integration of silicon CMOS VLSI with gallium-arsenide (GaAs) based semiconductor lasers and detectors.

The features of R-TRANSPAR networking and signal processing platform include:

- Subword and data packet level parallelism
- Computational intensive operations
- High-throughput smart pixel input/output (I/O) and local memory access
- Parallel pipeline processing and networking

The features of OE-MTR network include:

- High-throughput 3D optical parallel data packet switching
- Novel Collision-free multi-token-ring network protocol
- Time-division-multiplexed source and destination address channel
- Queuing and buffering

The R-TRANSPAR platform has demonstrated the high throughput and fast switching capabilities of optoelectronics in networks and multimedia signal processing. Our work also includes the development of network protocols for the transmission of heterogeneous media data over high data rate optoelectronic networks, and prediction of performance in terms of end-to-end data rate, latency, robustness, synchronization and quality of service. We will continue to explore the use of R-TRANSPAR digital optic systems for the encoding, decoding, transmission and switching of digital audio and video streams on very high-speed networks, and for advanced hardware interfaces for electronic processors. We were able to use a fast prototyped digital-signal-processing platform without optical interconnections to do communication channel coding and in the future, we will perform more sophisticated communication channel coding, signal, images, and video processing, 3D graphics algorithms using R-TRANSPAR platform.

11.2 Summary of 2000- and 2001 UTSi SOS Wire, Flip-Chip Bonding and Monolithic Integrated OEIC Chips

We were among the first 5 groups incorporating ultra-thin silicon-on-sapphire CMOS technology for optical transceiver modules in year 2000, and the organizer of COOP-USC-Peregrine 2001 workshop and foundry run hosting more than 10 groups.

We are the only group who have designed well-functioning optical transceiver arrays in our first debut of UTSi-SOS CMOS technology. We have made progress in optoelectronic smart pixel integration, monolithic optical receivers and wireless communication circuit modules. These are the milestones towards full monolithic integrated VCSEL/MSM CMOS SPA systems.

11.2.1 2000 UTSi-SOS Chip#1: Optical Transceiver Array with Built-In Self-Testing (BIST) LSI Circuits

The physical layout and photograph of the Optical Transceiver Array chip is shown in Fig. 11-1 (a), and Fig. 11-1 (b) respectively. It was fabricated in Peregrine Semiconductor 0.5-μm radiation-hard CMOS UTSi-SOS FA technology. The size of the full-custom chip is 2x2 mm^2. The chip has two Electro-Static Discharge (ESD) rings - analog (left) and digital (right) ESD rings, two 4x1 optical transceiver and self-testing circuits. Spectre transient simulation data-rate is over 4 Gbps. For Vdd = 2.5 volts, with zero BER.

11.2.2 2000 UTSi-SOS Chip #2: Time-Division-Multiplexing Smart Switch Chip

The 2000 UTSi-SOS chip#2 fabricated under COOP-GMU contain two 4 x 1 optical receiver array, 4 x 1 laser diode driver array, and ESO smart TDM switch with broadcast capability. This chip has switching intensive digital part and low noise high bandwidth analog front-end for optical communicaitons.

11.2.3 2001 UTSi Chip#1: Flip-Chip Optical Receivers, Monolithic PIN Receivers, Optically Clocked PRBS, Mixer With Baluns, CMOS VCO, $\pi/4$ Diferential Quadratic-, Multiphase Phase Voltage-Controlled Oscillators in Silicon-On-Sapphire

The 2001 UTSi Chip #1 was mainly designed for flip-chip bonding VCSEL and photodetector arrays, it also has monolithic optical receiver array, and VCO. It contains three different optical receiver array designs intended for flip-chip bonding to 4 x 1 Emcore positive-intrinsic-negative (p-i-n) detector arrays. Both multi-GHz single-ended transimpedance amplifier and low voltage differential signal receivers have been designed in this chip. In addition, it has an optically clocked 2047-pattern pseudo-random bit-stream (PRBS) generator based on true-single phase clock (TSPC) D-flip-flops are included for built-in high frequency self-testing. Eight optical amplifiers have inputs from novel p-i-n UTSi-SOS photodiodes to test monolithic optical receiver designs.

On the top row are 9 monolithic UTSi SOI p-i-n photodiodes with integrated receivers, over the corner space is a mixer with two baluns, as single-ended to differential converter for better noise suppression. The bottom half of the chip is the $\pi/4$ full differential LC-Tank VCO which gives eight phase outputs.

11.2.4 2001 UTSi Chip#2: Flip-Chip Laser Diode Drivers, Monolithic Differential LC-Tank Voltage-Controlled Oscillator, PLL-Based CDR In Silicon-On-Sapphire

The 2001 UTSi CMOS Chip #2, i.e. flip-chip VCSEL driver array and differential LC-VCO chip includes a negative resistance-based, balanced differential LC-tank VCO with center frequency at 5 GHz, a multi-GHz frequency divider, a

compact PLL-based CDR, and four distinct VCSEL drivers with 250 μm-pitch circular bonding pads for Emcore VCSEL array, which has a common cathode but individual input and bias. The green squares are MIM power decoupling and low pass filtering capacitors.

11.3 Future Work

There are two parallel tasks in our future work towards monolithic OEIC integration and smart pixel array technology. For smart pixel array image and video processing, we will continue to develop novel image, audio, video processing, 3-D computer graphics, and computer vision algorithms. We will implement the algorithms in parallel pipeline smart pixel arrays and use our R-Transpar signal processing and networking platform to demonstrate as real systems. 2-D channel coding, modulation, error detection and correction algorithm for wireless and optical communications will also be implemented in the universal R-TRANSPAR platform. Other novel network protocols excluding Ethernet and multi-token-ring protocols will be designed for high-throughput interconnections.

The other work is to test the 2001 UTSi-SOS OEIC transceiver and RF optical communication chip modules after receiving the fabricated dies from the MOSIS. The test approach will be direct probe testing or die-on-PCB, in which the bare die is flip-chip bonded directly onto the printed circuit board as described earlier.

REFERENCES

[Akatsu_95] Y. Akatsu, "High-speed monolithically integrated pin-HEMT photoreceivers," *Flat Panel Display Technology, Technologies for a Global Information Infrastructure, ICs for New Age Lightwave Communications, RF Optoelectronics, 1995 Digest of the LEOS Summer Topical Meetings*, pp. 33-34, 1995.

[Ayliffe_01] M. H. Ayliffe, D. R. Rolston, A. E. L. Chuah, Eric Bernier, F. S. J. Michael, D. Kabal, Andrew G. Kirk, and David V. Plant, "Design and testing of a kinematic package supporting a 32 x 32 array of GaAs MQW modulators flip-chip bonded to a CMOS chip," *Journal of Lightwave Technology*, vol. 19, no. 10, October 2001.

[Bernstein_98] K. Bernstein, K. M. Carrig, C. M. Durham, P. R. Hansen, D. Hogenmiller, E. J. Nowak, N. J. Rohrer, *High Speed CMOS Design Style*, Kluwer Academic Publishers, ISBN, 0-7923-8220-X, 1998.

[Best_99] Roland E. Best, *Phase-Locked Loops Design, simulation, and applications*, 4th edition, McGraw-Hill, 1999.

[Bond_98] A. E. Bond, P. D. Dapkus, "Monolithically integrated surface and substrate emitting vertical cavity surface emitting lasers for smart pixels," *Broadband Optical Networks and Technologies: An Emerging Reality/Optical MEMS/Smart Pixels/Organic Optics and Optoelectronics, 1998 IEEE/LEOS Summer Topical Meetings*, pp. IV/7-IV/8, 1998.

[Brenner_98] M. K. Hibbs-Brenner, Y. Liu, R. Morgan and J. Lehman, "VCSEL/MSM detector smart pixel arrays," *Proc. IEEE Summer Topical Meeting on Smart Pixels*, Monterey, CA, pp. 3-4, July, 1998.

[Chaki_95] S. Chaki, S. Andoh, Y. Sasaki, N. Tanino, and O. Ishihara, "Expenrimental study on spiral inductors," *1995 IEEE MTT-S Digest,* pp. 753-756, 1995.

[Chan_95] M. Chan, S. S. Yuen, Z-J Ma, K. Y Hui, P. K. Ko, C. Hu "ESD reliability and protection schemes in SOI CMOS output buffers," *IEEE Transactions on Electron Devices*, vol. 4210, pp. 1816 –1821, Oct. 1995.

[Chen_99] C.-H. Chen, B. Hoanca, C.B. Kuznia, A. A. Sawchuk, J.-M., Wu, "Translucent smart pixel array (TRANSPAR) chips for high throughput networks and SIMD signal processing," *IEEE Journal on Selected Topics in Quantum Electronics*, vol. 52, pp. 316-329. March-April 1999.

[Chen_oc99] C.-H. Chen, B. Hoanca, C. B. Kuznia, D. Pansatiankul, L. Zhang and A. A. Sawchuk, "Modulator and VCSEL-MSM smart pixels for parallel pipeline networking and signal processing," in *18th Congress of the International Commission for Optics: Optics for the Next Millennium*, *Proc. SPIE*, vol. 3749, pp. 241-242, 1999.

[Clymer_86] B. Clymer and J. W. Goodman, "Optical clock distribution to silicon chips", *Proc. SPIE*, vol. 625, pp. 134-142, 1986.

[Colinge_97] Jean-Pierre Colinge, *Silicon-on-Insulator Technology: material to VLSI*, 2nd edition, Kluwer Academic Publishers, Boston/Dordresht/London, 1997.

[Dabral_98] S. Dabral and T. J. Maloney, *Basic ESD and I/O Design*, John Wiley & Sons, Inc. 1998.

[Dearn_98] Andrew Dearn, "The design of monolithic differential VCOs," *IEE*, London, 1998.

[Decusatis_00] Casimer Decusatis, "Optoelectronics for multi-terabit intelligent wavelength division multiplexing networks," *2000 Digest of the LEOS Summer Topical Meetings*, FL, pp. 41-42, July 2000.

[Dias_88] A. R. Dias, R. F. Kalman, J. W. Goodman, A. A. Sawchuk, "Fiber optic crossbar switch with broadcast capability," *Optical Engineering,* vol. 27, Page(s): 955-960, 1988.

[Duvvury_88] C. Duvvury, R. N. Rountree, and O. Adams, "Internal chip ESD phenomenon beyond the protection circuits," *Proc. IEEE International Reliability Physics Symposium*, pp. 19-25, 1988.

[Farag_99] E. N. Farag, M. I. Elmasry, *Mixed Signal VLSI Wireless Design Circuits and Systems*, Kluwer Academic Publishers, Boston/Dordrecht/London, 1999.

[Fay_98] P. Fay, I. Adesida, C. Caneau, S Chandrasekhar, "High sensitivity 12 Gb/s monolithically integrated pin-HEMT photoreceivers," *1998 International Conference on Indium Phosphide and Related Materials,* pp. 439 –442, 1998.

[Fujimoto_93] N. Fujimoto, et al., "Gigabit-per-second optical parallel transmitter/receiver modules with fully integrated GaAs MESFET LSI chips," *OFC/IOOC '93 Technical Digest,* pp. 165-167, 1993.

[Fukasbiro_95]. Y. Fukasbiro, et al., "A high-speed 10-channel-integrated compact transmitter for optical subsystem interconnections," *IEICE Japan Technical Report*, OSC 95, vol. 4, 1995.

[Gale_94] *World of Scientific Discovery*, Gale Research Inc., p. 215, Detriot, 1994.

[Gonzales_84] Gonzales, Guillermo, *Microwave Transistor Amplifiers,* New Jersey Prentice Hall, 1984.

[Goodman_84] J. W. Goodman, F. J. Leonberger, S.-Y. Kumg, and R. A. Athale, "Optical interconnections for VLSI systems," *Proc. IEE*E, vol. 72, pp. 850–866, 1984.

[Goodman_91] J. W. Goodman, "Optical interconnections in computing", in *Computation & Cognition*, C.W. Gear, Editor, NEC/SIAM, Philadelphia, pp. 22-31, 1991.

[Goodman_93] J. W. Goodman, H. M. Ozaktas, "Constraints in the construction of computers with ever-larger numbers of processors," *Optical Computing, Proceedings of the SPIE*, vol. 1806, pp. 82-88, 1993. (Invited Paper)

[Grove_67] A. S. Grove, *Physics and Technology of Semiconductor Devices*, J. Willey & Sons, pp. 326, 1967.

[Haney_00] M. W. Haney, M. P. Christensen, P. Milojkovic, G. J. fokken, M. Vickberg, B. K. Gilbert, J. Rieve, J. Ekman, P. Chandramani, F. Kiamilev, "Description and evaluation of the FAST-Net smart pixel-based optical interconnection prototype," *Proceedings of the IEEE*, June 2000.

[HBM_93] *ESD Sensitivity Testing: Human Boday Model (HBM) Component Level*, ESD Association Standard, 1993.

[Hinton_96] H. S. Hinton, "Progress in the smart pixel technologies," *IEEE Journal on Selected Topics in Quantum Electronics*, vol. 21, pp.14 –23, April 1996.

[Huang_94] K.-S. Huang, C. B. Kuznia, B. K. Jenkins, A. A. Sawchuk, "Parallel architectures for digital optical cellular image processing," *Proceedings of the IEEE*, vol. 8211, pp. 1711–1723, Nov. 1994 .

[IBM] IBM corporation http://www.ibm.com

[IMSC_99] D. McLeod, U. Neumann, C. L. Nikias, A. A. Sawchuk, "Integrated media systems," *IEEE Signal Processing Magazine,* vol. 161, pp. 33-43, Jan. 1999.

[Intel_01] Intel Corporation http://www.intel.com.

[Johnson_95] R. A. Johnson, C. E. Chang, P. R. de la Houssaye, G.A. Garcia, I. Lagnado, P.M.. Asbeck, "Microwave characteristics of high f/sub max/ low noise thin film silicon-on-sapphire MOSFETs," *Proceedings of The IEEE International SOI Conference*, pp. 18-19, 1995.

[Joo_00] Y. Joo, M. A. Brooke, "Compact current input oversampling modulator design for a scalable high frame rate focal plane arrays," *ISCAS 2000* Conf., Geneva, Switzerland, May 2000.

[Kinget_99] P. Kinget, "Integrated GHz voltage controlled oscillators," in W. Sansen, J. H. Huijsing, and R.Van De Plassche,(Eds), *Analog Circuit Design*, pp.353-381, Kluwer Academic publishers, 1999.

[Krishnamoorthy] A. V. Krishnamoorthy and K. W. Goossen, "Progress in Optoelectronic-VLSI Smart Pixel Technology Based On GaAs/AlGaAs MQW Modulators," *International Journal of Optoelectronics*, vol. 11, pp. 181-198, 1997.

[Krishnamoorthy_98] A. V. Krishnamoorthy and K. W. Goossen, "Optoelectronic VLSI: Photonics integrated with VLSI circuits," *IEEE J. Selected Topics Quantum Electron*, vol. 4, pp. 899–912, Nov./Dec. 1998.

[Krishnamoorthy_99] A. V. Krishnamoorthy, L. M. F. Chirovsky, W. S. Hobson, R. E. Leibengath, S. P. Hui, G. J. Zydzik, K. W. Goossen, J. D. Wynn, B. J. Tseng, J. Lopata, J. A. Walker, J. E. Cunningham, and L. A. D'Asaro, "Vertical-cavity surface-emitting lasers flip-chip bonded to gigabit-per-second CMOS circuits," *IEEE Photon. Technol. Lett.*, vol. 11, pp. 128-130, Jan. 1999.

[Kuznia_00] C. B. Kuznia, A. A. Sawchuk, L. Zhang, B. Hoanca, S. Hong, C. Min, D. Pansatiankul, and Z. Y. Alpaslan, "A modular test system for smart pixel optical interconnections and pipeline processing using field programmable gate arrays (FPGAs)," *OSA Annual Meeting*, Providence RI, October 22-26, 2000.

[Kuznia_99] C. B. Kuznia, C.-H. Chen, B. Hoanca, L. Zhang, D. Pansatiankul, J.-M. Wu, and A. A. Sawchuk, "Modular system demonstrator for hybrid VCSEL/MSM smart pixel networking," *Optics in Computing*, *OSA Technical Digest*, pp. 156-158, Optical Society of America, Washington, DC, 1999.

[Kuznia_99] C. B. Kuznia, J.-M. Wu, C.-H. Chen, B. Hoanca, L. Cheng, A.G. Weber and A. A. Sawchuk, "Two-dimensional parallel pipeline smart pixel array cellular logic (SPARCL) processors-chip design and system implementation," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 5, pp. 376-386, 1999.

[Kuznia_oc00] C. B. Kuznia, A. A. Sawchuk, L. Zhang, B. Hoanca, S. Hong, C. Min, D. Pansatiankul, and Z. Y. Alpaslan, "Parallel pipeline networking and signal processing with field programmable gate arrays (FPGAs) and VCSEL-MSM Smart Pixels," *Optics in Computing 2000 Conference*, Quebec, Canada, June 2000.

[Kyranas_00] A. Kyranas, Y. Papananos, "A 5 GHz fully integrated VCO in a SiGe bipolar technology," *The 2000 IEEE International Symposium on Circuits and Systems*, vol. 5, pp. 193-196, Geneva, ISCAS 2000.

[Lee_01] C.-H. Lee, K. McClellan, J. Choma, Jr., "A supply-noise insensitive CMOS PLL with a voltage regulator using DC-DC capacitive converter," *IEEE Journal of Solid-State Circuits*, vol. 36, Issue: 10, pp. 1453–1463, Oct. 2001,

[Lee_96] T. H. Lee, "CMOS RF IC Design," *Hot Interconnects Tutorial*, 1996.

[Liang_01] T. Liang, J. Gillis, D. Wang, P. Cooper, "Design and modeling of compact on-chip transformer/balun using multi-level metal windings for RF integrated circuits," *2001 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, May 2001.

[Lin_95] C.-K. Lin, P. D. Dapkus, "High performance wafer-bonded bottom emitting 850 nm VCSELs on Transparent substrates," Nanostructures and Quantum Dots/WDM Components/VCSELs and Microcavaties/RF Photonics for CATV and HFC Systems, *Digest of the LEOS Summer Topical Meetings*, pp. 63-64, 1999.

[Liu_98] Y. Liu, "Smart pixel module development for free space optical interconnect," *Proc. Int. Topical Meeting Optical Computing*, pp. 528-531, June 1998.

[Lu_01] J. Lu, S. C. Busch, and D. F. Baldwin, "Solder wetting in a wafer-level flip chip assembly," *IEEE Transactions On Electronics Packaging Manufacturing*, vol. 24, no. 3, July 2001.

[Luh_00] L. Luh, J. Choma, Jr., J. Draper, "A Zener-diode-activated ESD protection circuit for sub-micron CMOS processes," *Proceedings of The 2000 IEEE International Symposium on Circuits and Systems*, Geneva, vol. 5, pp. 65-68, 2000.

[Marchand_00] P. Marchand, S. Esener, "Free-space optics for 3D multi-chip environment," *2000 Southwest Symposium on Mixed-Signal Design*, pp. 7-8, San Diego, CA, SSMSD 2000.

[Matsuo_95] S. Matsuo, T. Nakahara, Y. Kohama, Y. Ohiso, S. Fukushima, T. Kurokawa, "Monolithically integrated photonic switching device using an MSM PD, MESFETs, and a VCSEL," *IEEE Photonics Technology Letters*, vol. 710, pp. 1165–1167, Oct. 1995.

[Miller_00] David A. B. Miller, "Rationale and challenges for optical interconnects to electronic chips," *Proceedings of the IEEE, Optical Interconnections for Digital System*, pp. 728-749, June 2000.

[Miller_95] D. A. B. Miller, "Dense optical interconnection for silicon electronics," Published in *"Trends in Optics 1995", International Commission for Optics, Academic Press,* pp. 207-222, 1995.

[Miller_97] D. A. B. Miller and H. Ozaktas, "Limit to the bit-rate capacity of electrical interconnects from the aspect ratio of the system architecture," *Special Issue on Optical Interconnects, J. Parallel and Distributed Computing*, vol. 41, pp. 42-52, 1997.

[Moore_00] *The National Technology Roadmap For Semiconductors-Technology Needs*, Semiconductor Industry Association, 2000.

[Peregrine] Peregrine semiconductor http://www.peregrin-semi.com

[Riishoj_94] J. Riishoj, "5 Gbit/s laser-driver GaAs IC," *Electronics Letters*, vol.30 no. 10, 1994.

[Roadmap_01] *International Technology Roadmap for Semiconductors*, 1999 Edition and 2000 Update, 2001. Semiconductor Industry association, San Jose, CA, USA.

[Runge_92] K. Runge, et al., "AlGaAs/GaAs HBT IC's for high-speed lightwave transmission systems," *IEEE J. of Solid State Circuits*, vol. 10, pp. 1332-1339, 1992.

[Sawchuk_00inv] A. A. Sawchuk; C. B. Kuznia, "Optoelectronic interconnections for high throughput networks and pipeline signal processing," Electronic-Enhanced Optics, Optical Sensing in Semiconductor Manufacturing, Electro-Optics in Space, Broadband Optical Networks, 2000. *Digest of the IEEE LEOS Summer Topical Meetings*, pp. I35-I36, 2000.

[Sawchuk_92] A. A. Sawchuk, "Applications of smart pixel devices in optical computing and interconnection networks," *LEOS '92, Conference Proceedings. IEEE Lasers and Electro-Optics Society, 1992 Annual Meeting*, pp. 369-370, 1992.

[Sawchuk_97] A. A. Sawchuk, "Optoelectronic memory applications for VCSEL based smart pixels," *Lasers and Electro-Optics Society Annual Meeting,* 1997. *IEEE LEOS '97,10th Annual Meeting. Conference Proceedings*, vol. 2, pp. 149-150, 1996.

[Sawchuk_98inv] A. A. Sawchuk, "Optical signal and image processing: from analog systems to digital pipeline smart pixels," *Proc. IEEE International Conference on Image Processing 1998 (ICIP98)*, Chicago, IL, Oct. 5-7, 1998, (invited paper).

[Sawchuk_99] A. A. Sawchuk, "Photonic networks, switches, computer interfaces and parallel signal processing for multimedia," *Integrated Media Center (IMSC) annual report*, 1999.

[Schneider_96] R. P. Schneider, M. R. T. Tan, S. W. Corzine, and S. Y. Wang, "Oxide confined 850nm vertical-cavity lasers for multimode-fibre data communications", *Electron. Lett.*, vol. 32, pp. 1300-1302, 1996.

[Schow_99] C. L. Schow, J.D. Schaub, R. Li, J. Qi, J. C. Campbell, "A monolithically integrated 1-Gb/s silicon photoreceiver," *IEEE Photonics Technology Letters*, vol. 111, pp. 120 –121, Jan. 1999.

[Semi_01] *International Technology Roadmap for Semiconductors*, 2000 Edition, 2001. Semiconductor Industry Association, San Jose, CA, USA.

[Szymanski_96] T. H. Szymanski and S. H. Hinton, "Reconfigurable intelligent optical backplane for parallel computing and communications," *Applied Optics*, no. 35, pp. 1253-1268, 1996.

[Tanabe_01] A. Tanabe, M. Umetani, I. Fujiwara, T. Ogura, K. Kataoka, M. Okihara, H. Sakuraba, T. Endoh, F. Masuoka, "0.18-m CMOS 10-Gb/s multiplexer/demultiplexer ICs using current mode logic with tolerance to threshold voltage fluctuation," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 988-996, June 2001.

[Tooley_96] F. A. P. Tooley, "Challenges in optically interconnecting electronics," *IEEE J. Select. Topics Quantum Electron*, vol. 2, pp. 3–13, Apr. 1996.

[UTSi_1.8] Ultra-Thin Silicon (UTSi) *Design Manual 1.8*, Chapter 1.

[Wu_99] J.-M. Wu, C. B. Kuznia, B, Hoanca, C.-H. Chen and A. A. Sawchuk, "Demonstration and architectural analysis of CMOS/MQW smart pixel array cellular logic (SPARCL) processors for SIMD parallel pipeline processing," *Applied Optics*, vol. 38, pp. 2270-2281, 1999.

[Yang_95] G. M. Yang, M. H. Macdougal and P. D. Dapkus. "Ultralow threshold vertical cavity surface emitting lasers obtained with selective oxidation", *Electron. Lett.*, vol. 31, pp. 886-888, 1995.

[Yuan_89] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 1, pp. 62-70, Feb. 1989.

[Zhang_01] L. Zhang, S. Hong, C. Min, Z.Y. Alpaslan and A.A. Sawchuk, "Optical multi-token-ring networking using smart pixels with field programmable gate arrays (FPGAs)," *Proc. Photonic Devices and Algorithms for Computing III Symposium*, San Diego, CA, *Proc. SPIE*, vol. 4470, 2001.

[Zhang_cleo] Liping Zhang, Alexander A. Sawchuk, et al., "Flip-chip optical transceivers, monolithic pin receivers and quadratic-phase voltage-controlled oscillators in ultra-thin silicon-on-sapphire," *Conference on Lasers and ElectroOptics (CLEO), IEEE-LEOS*, Long Beach, CA, May 2002.

[Zhang_iscas] L. Zhang and A. A. Sawchuk, "Monolithic multi-phase LC-VCO in ultra-thin silicon-on-insulator (UTSi-SOI) CMOS Technology," *International Symposium of Circuits and Systems, ISCAS 2002*, Phenix, Arizona, May 26-29, 2002,

[Zhang_oc] L. Zhang, S. Hong and A. A. Sawchuk,"Design and testing of ultra thin silicon (UTSi) chips with optical transceivers and voltage-controlled oscillators," *Optical Computing*, April 2002.

[Zhou_96] Z. Zhou, B. Pain, R. Panicacci, B. Mansoorian, J. Nakamura, E. R. Fossum, "On-focal-plane ADC: recent progress at JPL," *Proceedings of SPIE – The International Society for Optical Engineering*, vol. 2745, pp. 111-122, 1996.

[Ziegler_96] J. F. Ziegler, et al., "'IBM experiments in soft fails in computer electronics," *IBM Journal of Research and Development*, vol. 40, no. 1, pp.3-18, Jan. 1996.

[Zimmermann_98] H. Zimmermann, "Full custom CMOS and BiCMOS OPTO ASICs," *1998 5th International Conference on Solid-State and Integrated Circuit Technology. IEEE Proceedings*, pp. 344–347, 1998.

[Zimmermann_99] H. Zimmermann, A. Ghazi, T. Heide, R. Popp, R. Buchner, "Advanced photo integrated circuits in CMOS technology," *IEEE Proceedings of 49th Electronic Components and Technology Conference*, pp. 1030-1035, 1999.